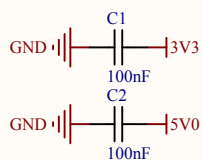


# DECOUPLING

The diagram illustrates two decoupling capacitors, C1 and C2, connected between GND and power rails (3V3 and 5V0). Both capacitors are labeled 100nF.



## USER BREAKOUT

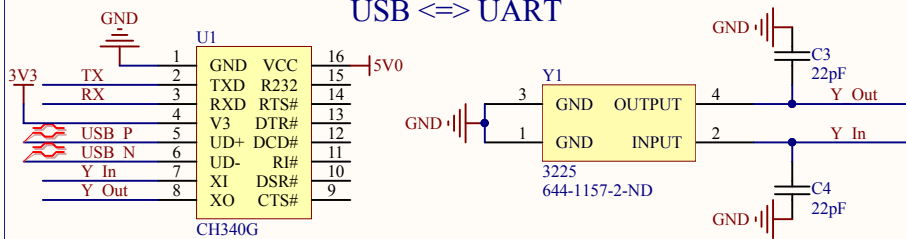
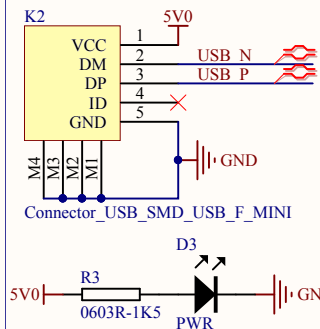
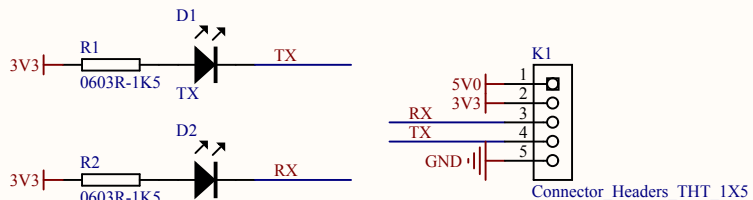
3V3 — R1 (0603R-1K5) — TX (D1) — TX


3V3 — R2 (0603R-1K5) — RX (D2) — RX

5V0  
3V3  
RX  
TX  
GND

K1

Connector\_Headers\_THT\_1X5



Title: <b>CH340G breakout</b>			* <i>Robbe's Workshop</i> 
Size: <b>A4</b>	Number:	Revision: <b>A</b>	
Date: <b>2/06/2015</b>	Time: <b>22:36:00</b>	Sheet <b>2</b> of <b>2</b>	
File: <b>D:\Github\DP_UART\DP_UART_RVA.SchDoc</b>			

K2

D3

330

U1

K1

C4

Y1

R2D2

R1D1

C3

C1

