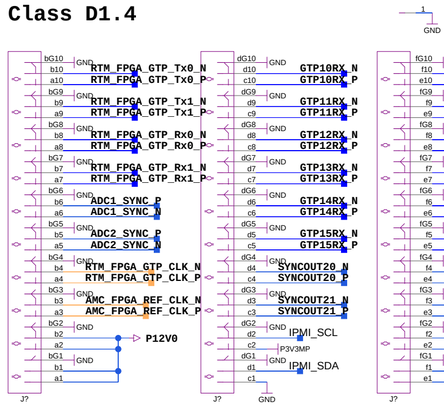
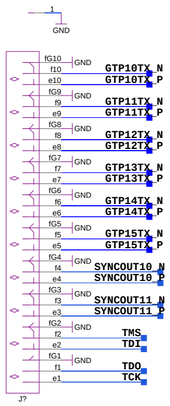
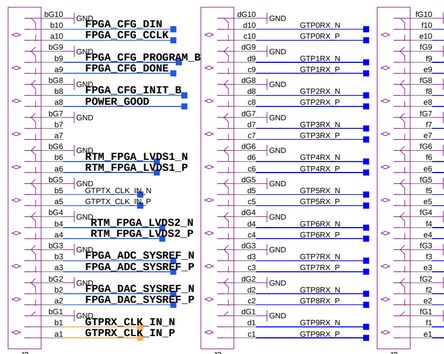
# Class D1.4





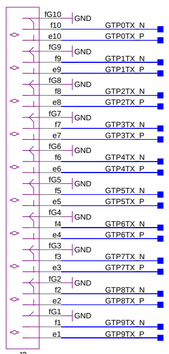


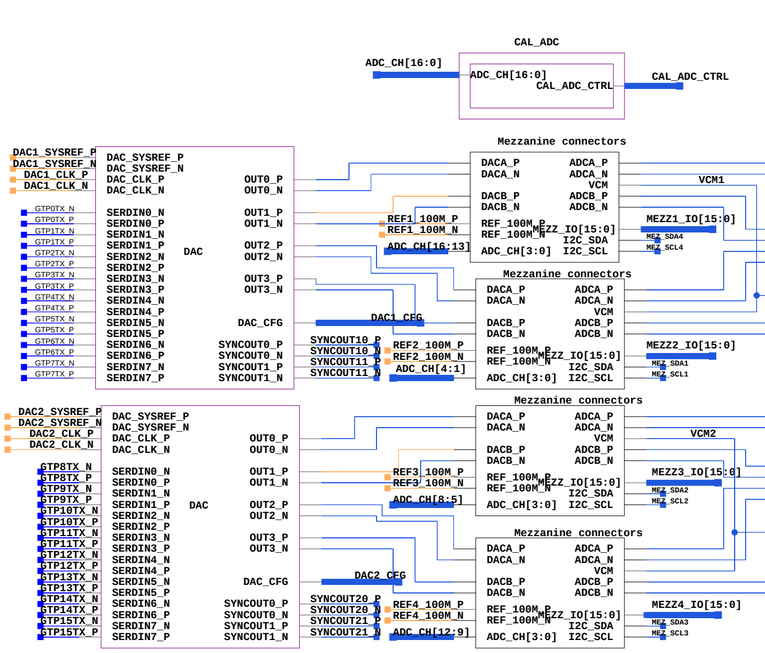


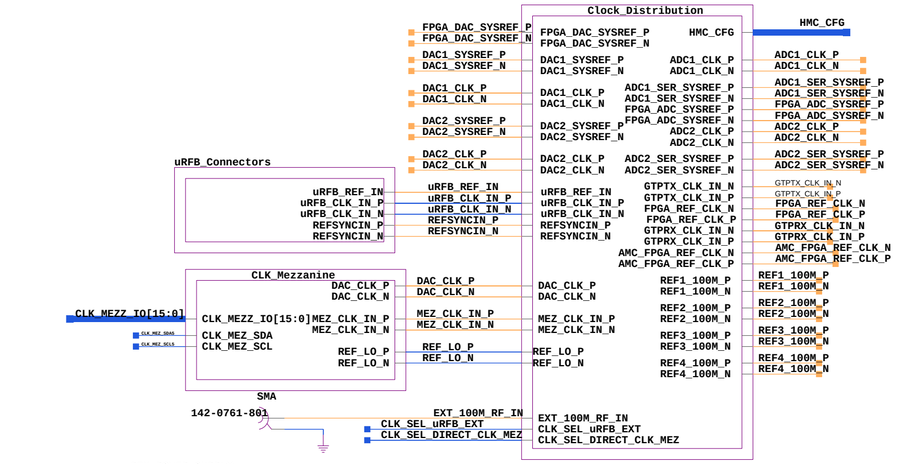



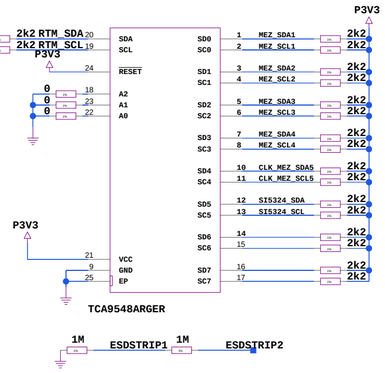


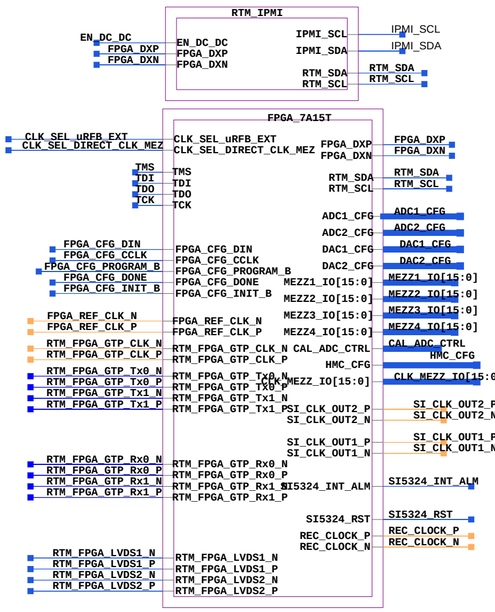




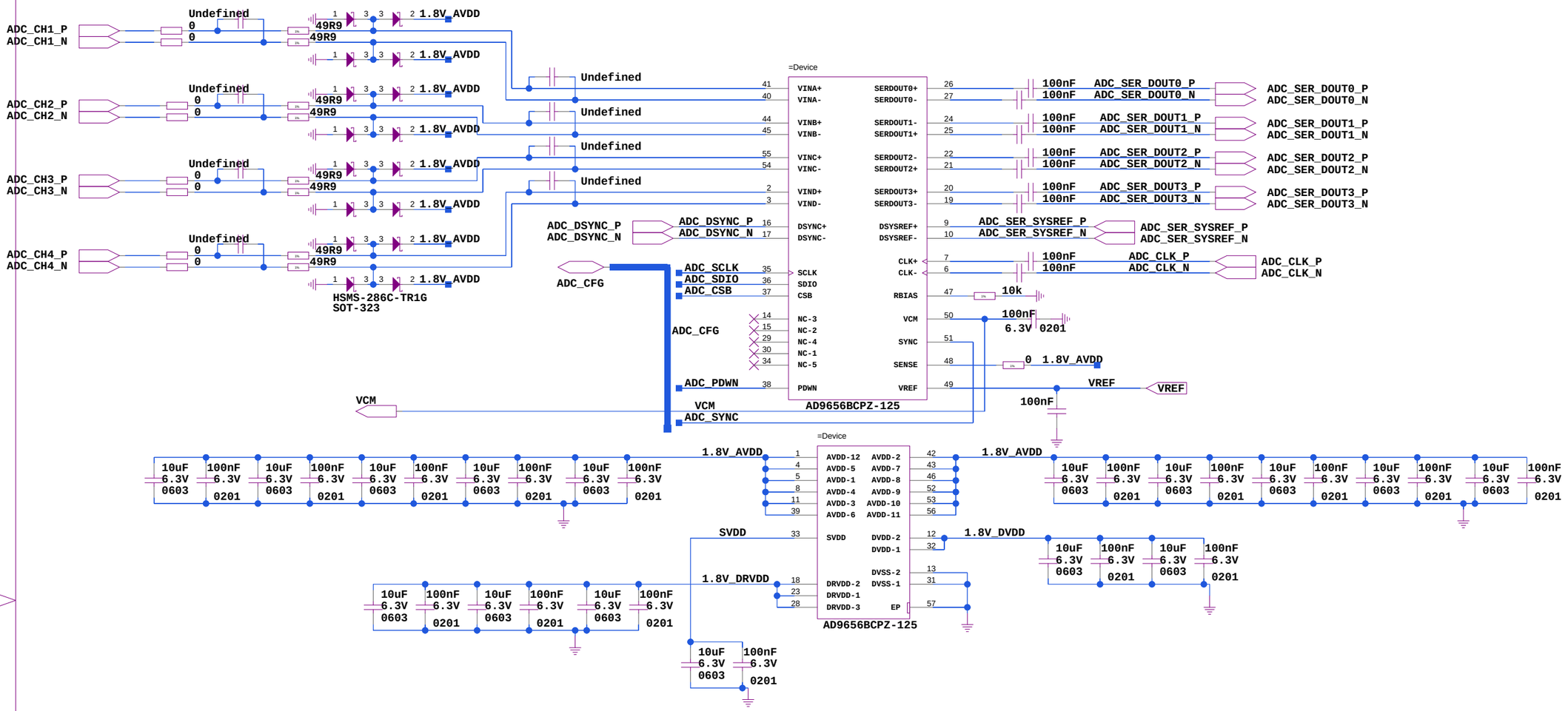



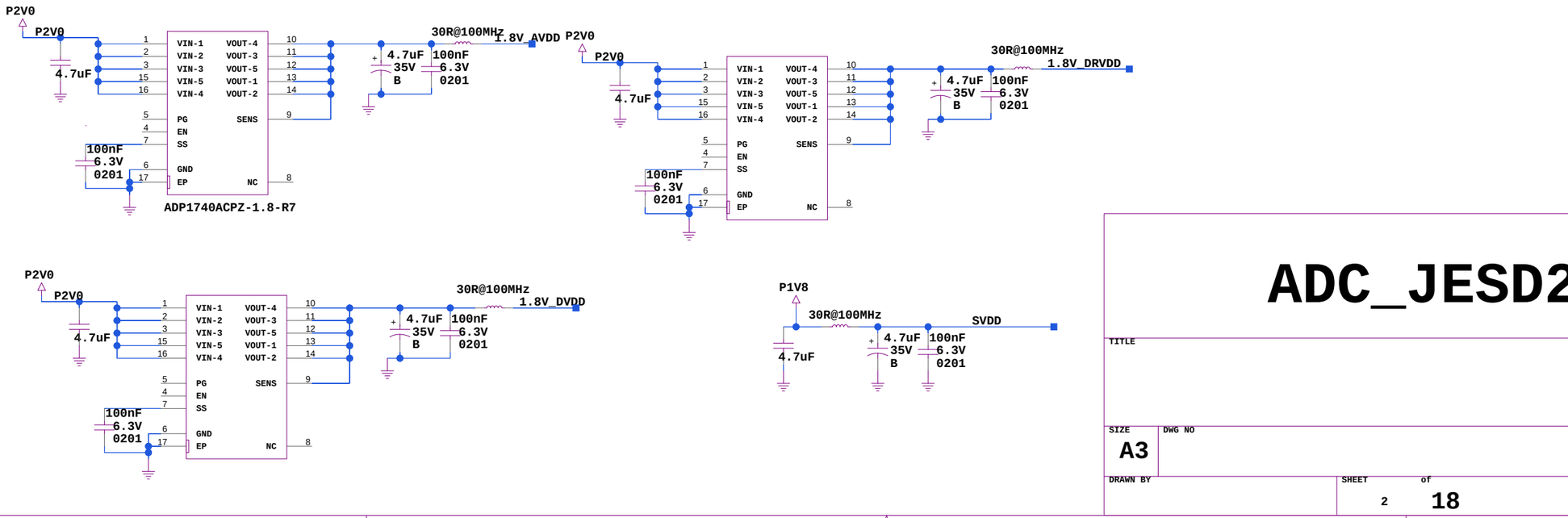



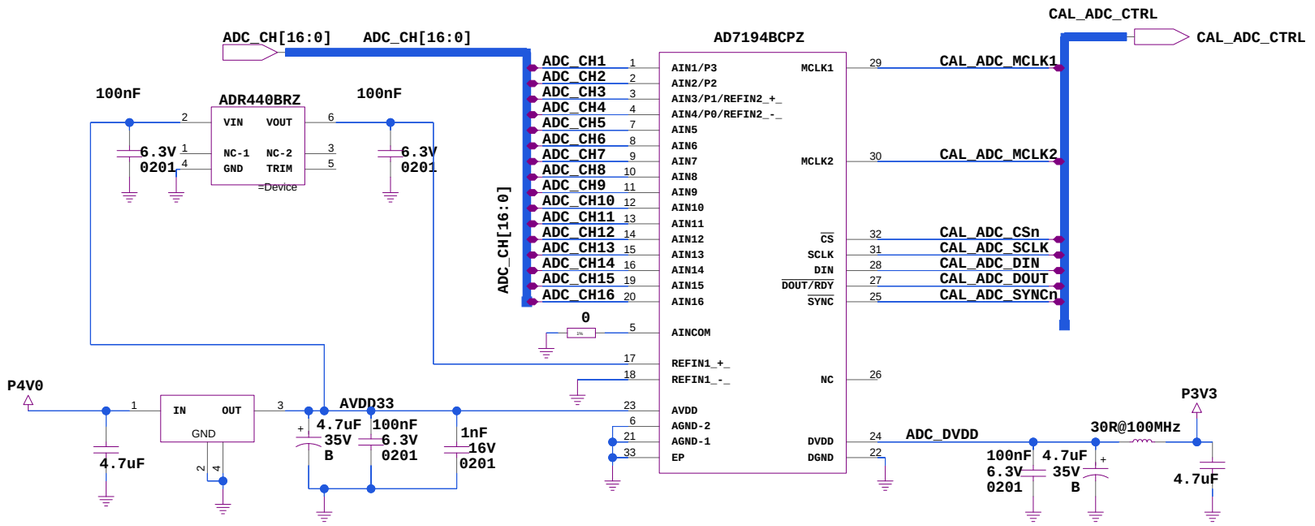

| | | | |
|---|---|---|---|
| TITLE | Sayma_RTM | | |
| SIZE A2 | DWG NO 1 | | REV |
| DRAWN BY | SHEET 1 of 18 | | 02/11/2016:00:40 |




# ADC_JESD204B

| | | | |
|---|---|---|---|
| TITLE | | | |
| SIZE A3 | DWG NO | | REV |
| DRAWN BY | SHEET 2 of 18 | | 02/11/2016:00:40 |




# CAL_ADC

| | | | |
|---|---|---|---|
| TITLE | | | |
| SIZE A3 | DWG NO | | REV 1 |
| DRAWN BY | SHEET 3 of 18 | | 02/11/2016:00:40 |

# Clock_Distribution

| | | |
|---|---|---|
| TITLE | | |
| SIZE A3 | DWG NO 1 | REV |
| DRAWN BY | SHEET 5 of 18 | 02/11/2016:00:40 |

CLK_SEL_DIRECT_CLK_MEZ
uRFB_CLK_IN_P DNP
uRFB_CLK_IN_N DNP
uRFB_REF_IN 100nF
49R9 100nF
input BW setting
P3V3_CLK 120R@100MHz 1uF 16V 0402 100nF
LTC6957IDD-1#PBF
Si53307
CLK_SEL_uRFB_EXT
L=CLK0, H-CLK1
10k
BSS138LT1G
To additionally isolate inactive CLK
Shutdown inputs are used
LVPECL mode -> SFOUT[1:0] = open
EXT_100M_RF_IN
ADCLK948BCPZ
clock module
MEZ_CLK_IN_N REF_LO_P
MEZ_CLK_IN_P REF_LO_N
REFSYNCIN_P
REFSYNCIN_N
DAC_CLK_P
DAC_CLK_N
HMC_CFG
HMC_SPI_SYNC
HMC_SPI_SDATA
HMC_SPI_SLEN
HMC_SPI_SCLK
HMC_RESET
HMC_SPI_GPIO
Oscillator place holder
RC place holder
VCC1_VCO
VCC5_PLL1
VCC6_OSCOUT
VCC_PLL
VCC7_PLL2
VCC2_OUT
VCC_CLOCKOUT1
VCC9_OUT
VCC_CLOCKOUT2
VCC3_SYSREF
VCC_CLOCKOUT3
VCC4_OUT
VCC8_OUT
P4V0
LT1963AEST-3.3#PBF
4.7uF
22uF 6.3V 0805
100nF 6.3V 0201
120R@100MHz
1uF 16V 0402
100nF 6.3V 0201
1nF 16V 0201
HMC7044LP10BE
REF1_100M_P
REF1_100M_N
REF2_100M_P
REF2_100M_N
REF3_100M_P
REF3_100M_N
REF4_100M_P
REF4_100M_N
DAC1_CLK_P
DAC1_CLK_N
DAC1_SYSREF_P
DAC1_SYSREF_N
DAC2_CLK_P
DAC2_CLK_N
DAC2_SYSREF_P
DAC2_SYSREF_N
ADC1_CLK_P
ADC1_CLK_N
FPGA_DAC_SYSREF_P
FPGA_DAC_SYSREF_N
ADC2_CLK_P
ADC2_CLK_N
ADC1_SER_SYSREF_P
ADC1_SER_SYSREF_N
FPGA_REF_CLK_N
FPGA_REF_CLK_P
ADC2_SER_SYSREF_P
ADC2_SER_SYSREF_N
GTPTX_CLK_IN_P
GTPTX_CLK_IN_N
FPGA_ADC_SYSREF_P
FPGA_ADC_SYSREF_N
GTPRX_CLK_IN_P
GTPRX_CLK_IN_N
AMC_FPGA_REF_CLK_N
AMC_FPGA_REF_CLK_P

# IOVDD=3.3

SERDIN0_P SERDIN0_N SERDIN1_P SERDIN1_N SERDIN2_P SERDIN2_N SERDIN3_P SERDIN3_N SERDIN4_P SERDIN4_N SERDIN5_P SERDIN5_N SERDIN6_P SERDIN6_N SERDIN7_P SERDIN7_N — 6.3V 100nF

DAC_TXEN0 DAC_TXEN1

DAC_CLK_P DAC_CLK_N

DAC_SPI_SDO DAC_SPI_SDIO DAC_SPI_SCLK DAC_SPI_CSn

SIOVDD33 IOVDD

VTT: 1uF 16V 0402; 100nF 6.3V 0201 ×4

AVDD33: 4.7nF 10V 0201 ×4; 100nF 6.3V 0201 ×2; 1nF 16V 0201 ×2; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C

CVDD12: 4.7nF 10V 0201 ×4; 100nF 6.3V 0201 ×2; 1nF 16V 0201 ×2; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C

DVDD12: 4.7nF 10V 0201 ×4; 100nF 6.3V 0201 ×2; 1nF 16V 0201 ×2; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C

Replace with W2L16C473MAT1S

AD9154BCPZ

DAC_CFG

DAC_IRQn DAC_RESETn DAC_SPI_CSn DAC_SPI_SCLK DAC_SPI_SDO DAC_SPI_SDIO DAC_TXEN0 DAC_TXEN1

OUT0_P OUT0_N OUT1_P OUT1_N OUT2_P OUT2_N OUT3_P OUT3_N

SYNCOUT0_P SYNCOUT0_N SYNCOUT1_P SYNCOUT1_N

PDP_OUT0 PDP_OUT1

DAC_SYSREF_P DAC_SYSREF_N

LDO_BYP1 LDO_BYP2: 1 1uF 16V 0402; 1uF 16V 0402

IRQ DAC_IRQn; RESET DAC_RESETn

I120: 4k02

DNC-1 DNC-2

PVDD12: 4.7nF 10V 0201 ×4; 100nF 6.3V 0201 ×2; 1nF 16V 0201 ×2; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C; 100nF 6.3V 0201 ×3; 1nF 16V 0201; 1nF 16V 0201

SVDD12: 4.7nF 10V 0201 ×4; 1nF 16V 0201 ×2; 1nF 16V 0201 ×2; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C; 100nF 6.3V 0201 ×3; 1nF 16V 0201; 1nF 16V 0201

SDVDD12: 4.7nF 10V 0201 ×4; 100nF 6.3V 0201 ×2; 1nF 16V 0201 ×2; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C

XVDD33: 4.7uF 35V B; 47uF 16V C

SIOVDD33: 1nF 16V 0201; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C

PLLVDD12: 1nF 16V 0201; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C

IOVDD: 100nF 6.3V 0201; 1nF 16V 0201; 100nF 6.3V 0201; 1nF 16V 0201; 4.7uF 35V B; 47uF 16V C

Replace with W2L16C473MAT1S

P2V0 — 4.7uF; VIN-1 VIN-2 VIN-3 VIN-5 VIN-4 VOUT-4 VOUT-3 VOUT-5 VOUT-1 VOUT-2 PG EN SS GND EP SENS NC; 100nF 6.3V 0201

PVDD12: 4.7uF 35V B; 100nF 6.3V 0201

SVDD12: 4.7uF 35V B; 100nF 6.3V 0201

DVDD12: 4.7uF 35V B; 100nF 6.3V 0201

PLLVDD12: 4.7uF 35V B; 100nF 6.3V 0201

CVDD12: 4.7uF 35V B; 100nF 6.3V 0201

P1V8 — 120R@100MHz — IOVDD: 1uF 16V 0402; 100nF 6.3V 0201; 1nF 16V 0201

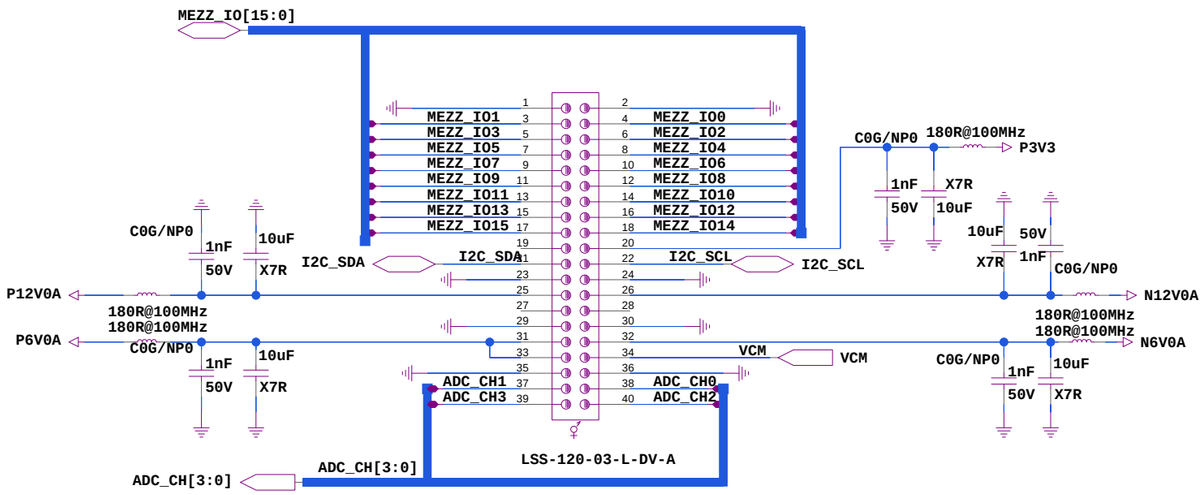
P4V0 — LT1963AEST-3.3#PBF (IN OUT GND) — 4.7uF

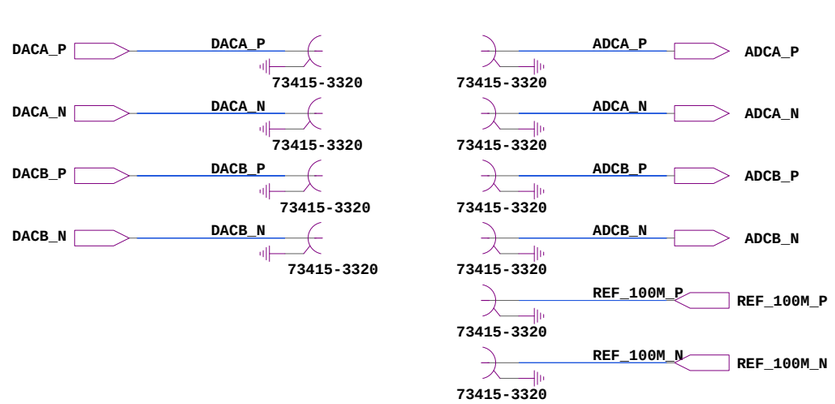
AVDD33: 4.7uF 35V B; 100nF 6.3V 0201

SIOVDD33: 4.7uF 35V B; 100nF 6.3V 0201

# DAC_JESD204B

| | | | |
|---|---|---|---|
| TITLE | | | |
| SIZE A3 | DWG NO | | REV 1 |
| DRAWN BY | SHEET 6 | of 18 | 02/11/2016:00:40 |



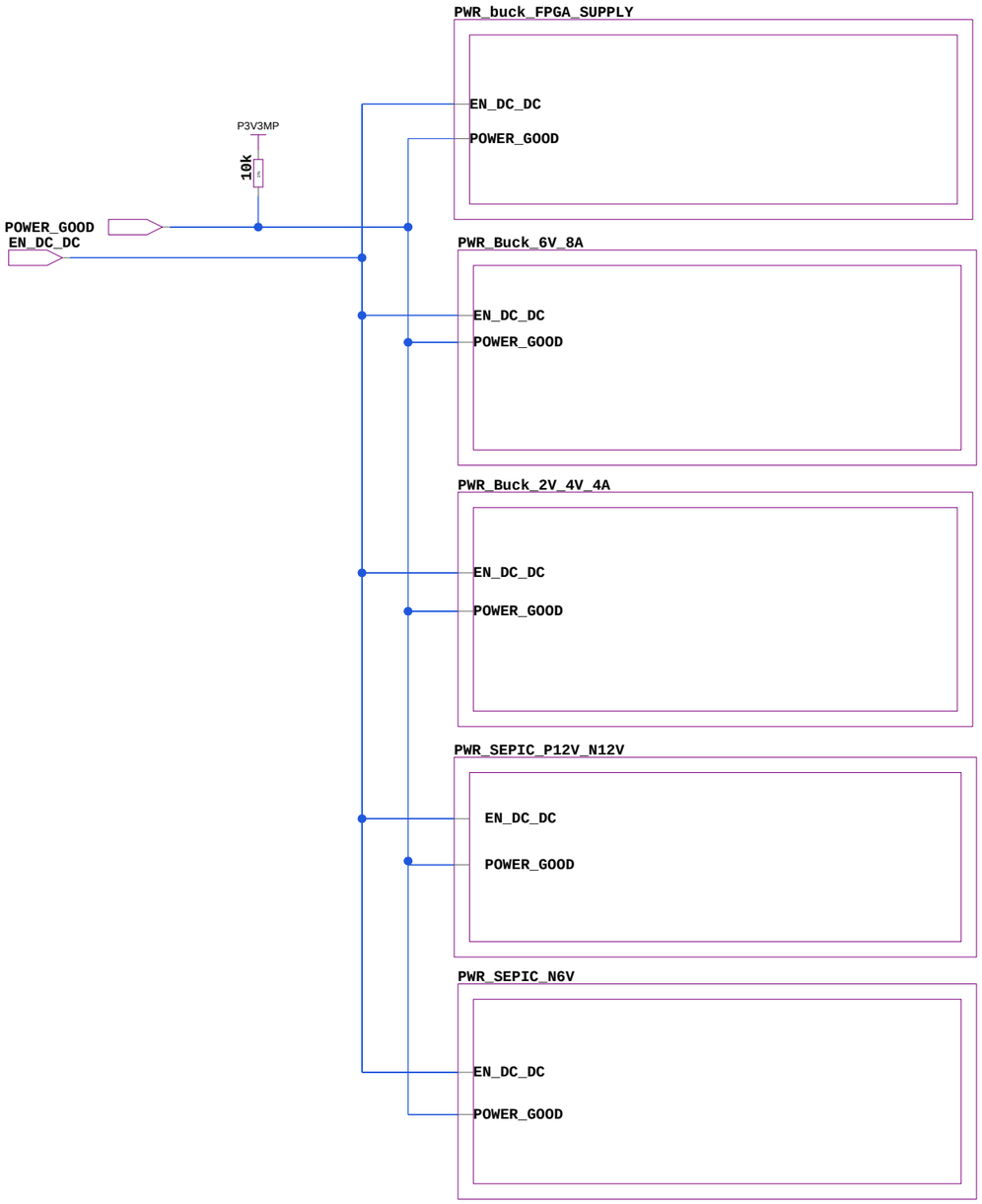

+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

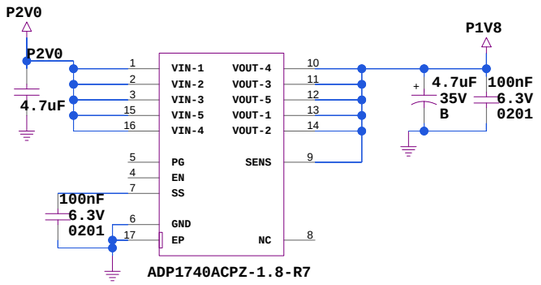
# ADC_DAC_AFE_Mezzanine

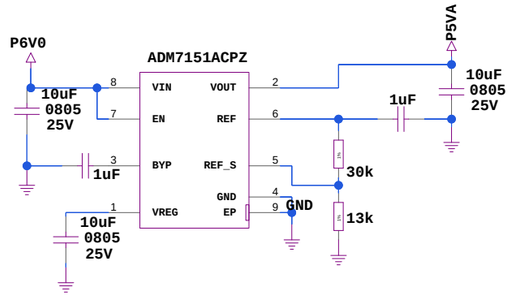
TITLE

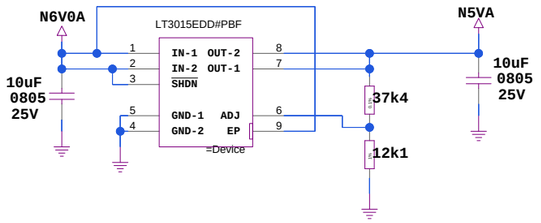
| SIZE | DWG NO | REV |
|---|---|---|
| A3 | 1 | |

| DRAWN BY | SHEET | of | |
|---|---|---|---|
| | 9 | 18 | 02/11/2016:00:40 |




RTM modules power requirements

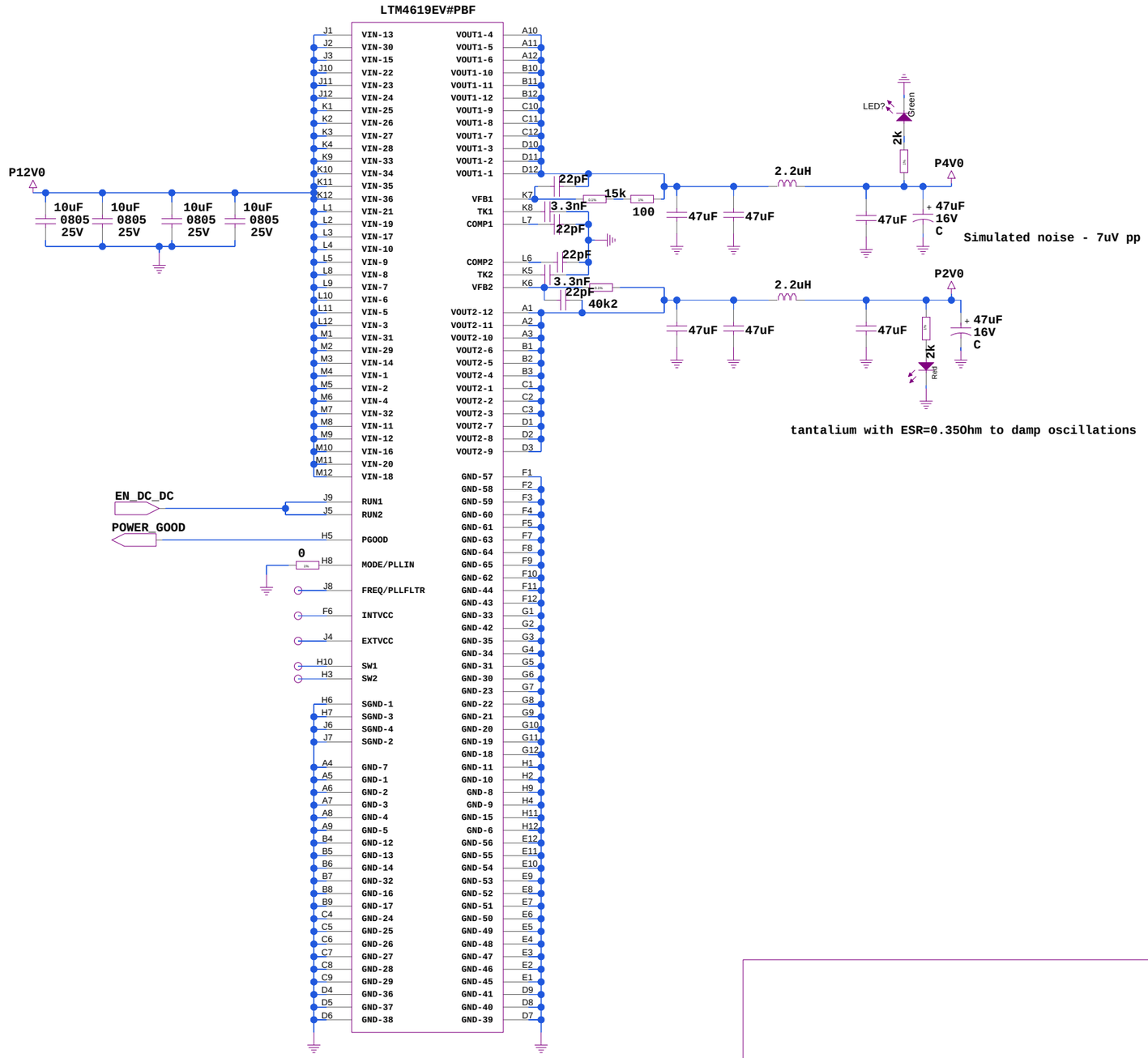
+12VDC @ 1A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 250 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 8 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 750 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

RTM power requirements

+4VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz
+2VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

# RTM_POWER_SUPPLY

| | | |
|---|---|---|
| TITLE | | |
| SIZE A3 | DWG NO 1 | REV |
| DRAWN BY | SHEET 11 of 18 | 02/11/2016:00:40 |

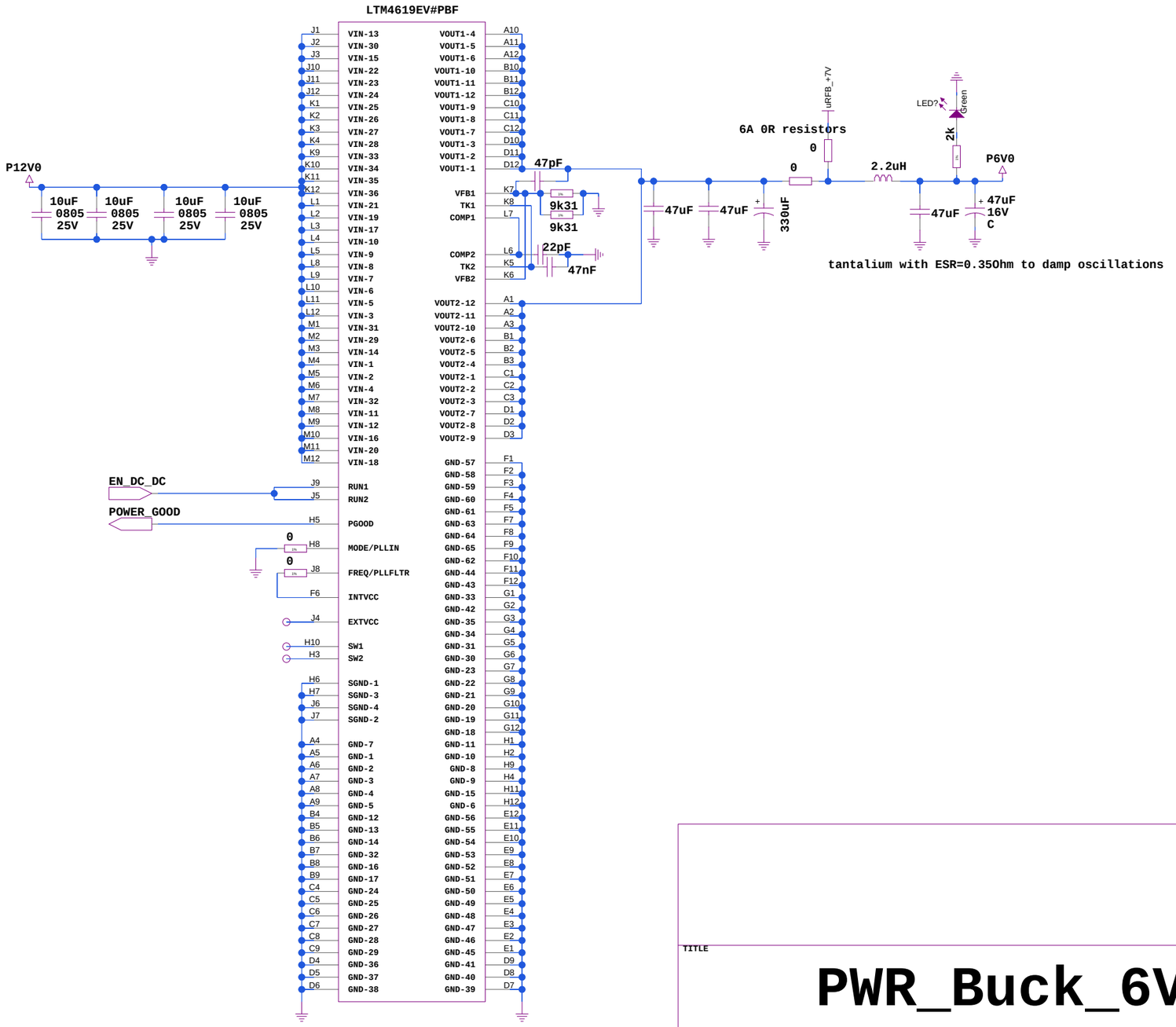



TITLE

# PWR_Buck_2V_4V_4A

| SIZE | DWG NO | REV |
|---|---|---|
| A3 | 1 | |

| DRAWN BY | SHEET | | |
|---|---|---|---|
| | 12 | of 18 | 02/11/2016:00:40 |

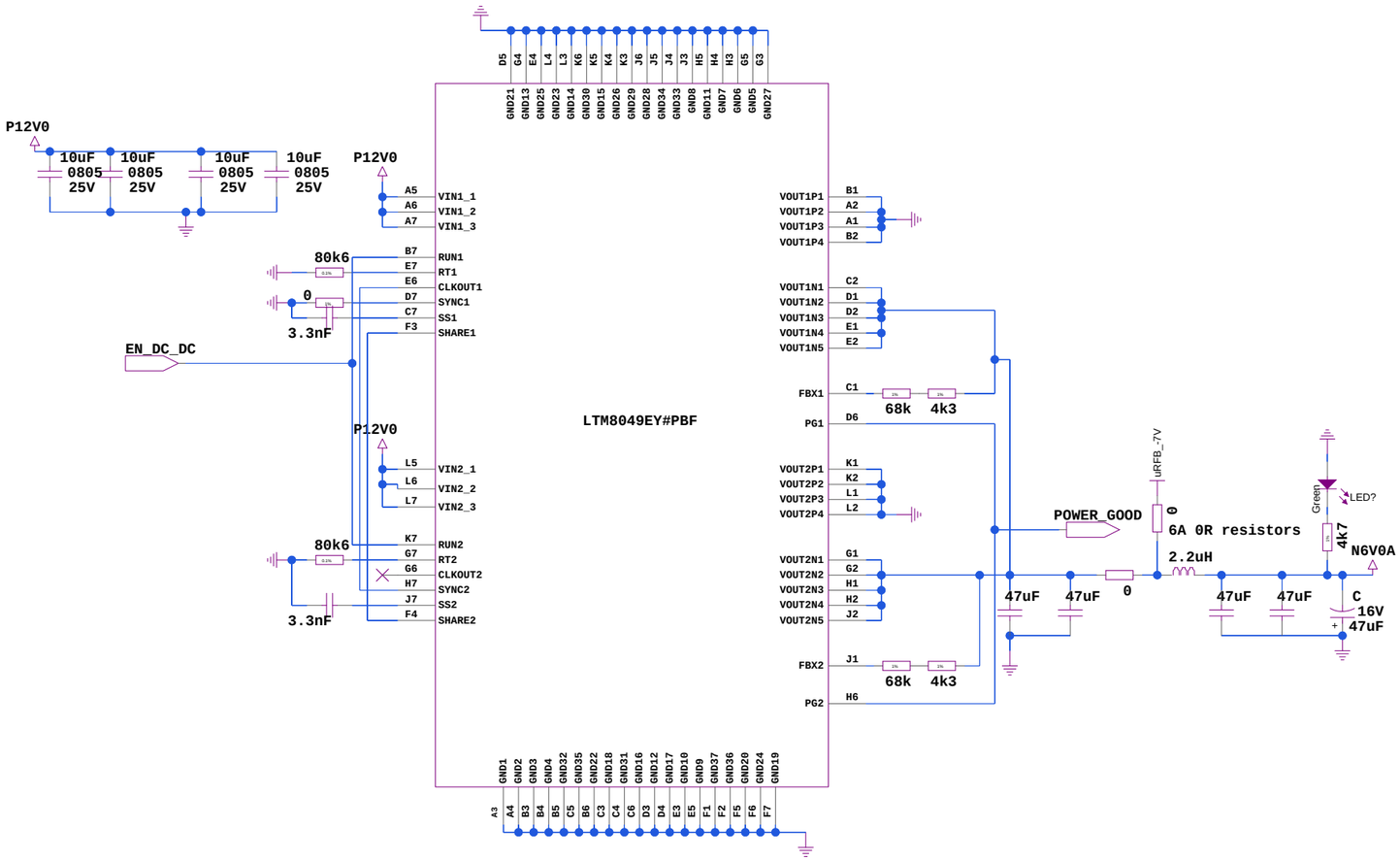



TITLE

# PWR_Buck_6V_8A

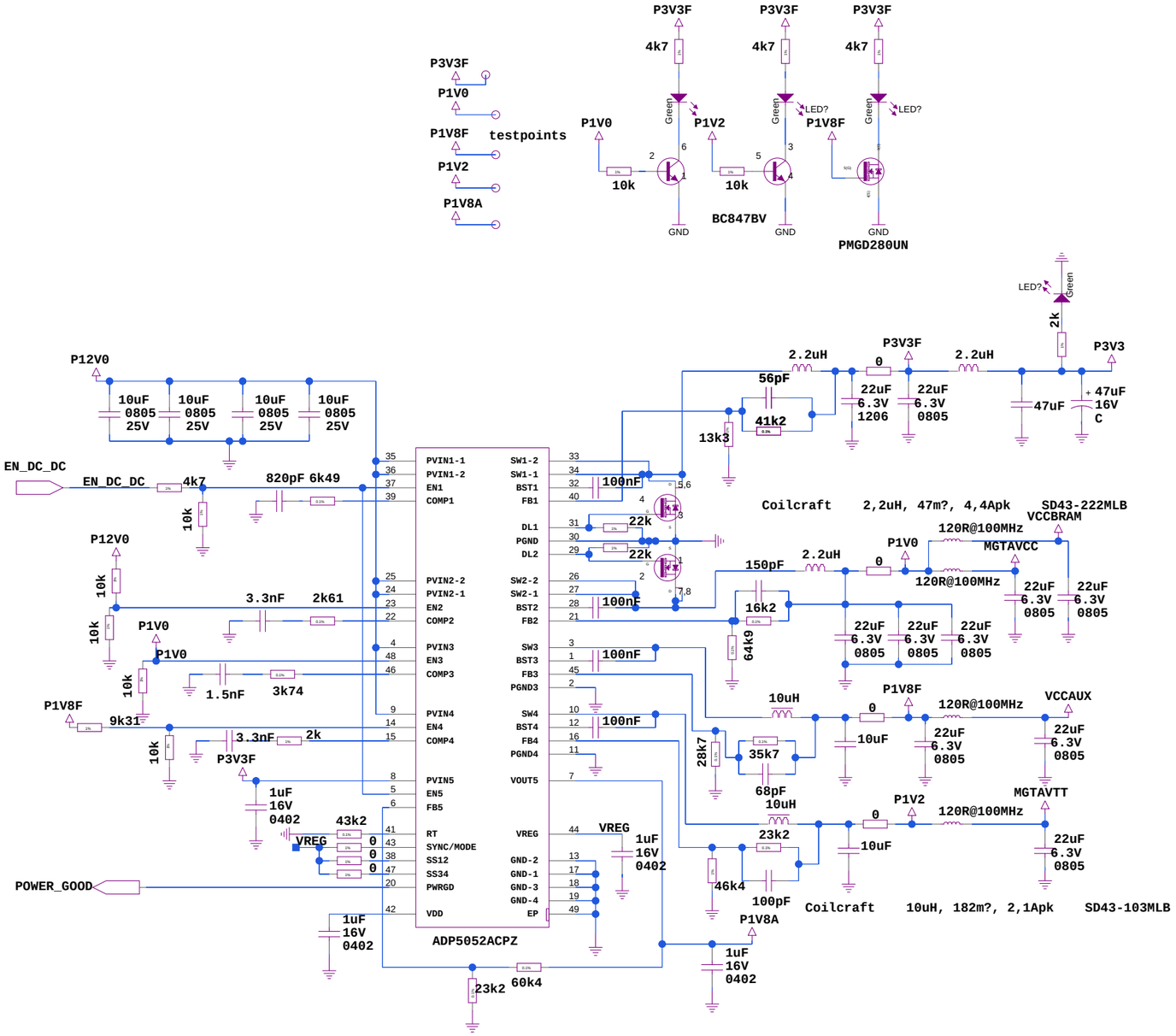
| SIZE | DWG NO | REV |
|---|---|---|
| A3 | 1 | |

| DRAWN BY | SHEET | of | |
|---|---|---|---|
| | 13 | 18 | 02/11/2016:00:40 |




# PWR_SEPIC_N6V

| | | |
|---|---|---|
| TITLE | | |
| SIZE A3 | DWG NO 1 | REV |
| DRAWN BY | SHEET 14 of 18 | 02/11/2016:00:40 |




TITLE

# PWR_buck_FPGA_SUPPLY

| SIZE | DWG NO | REV |
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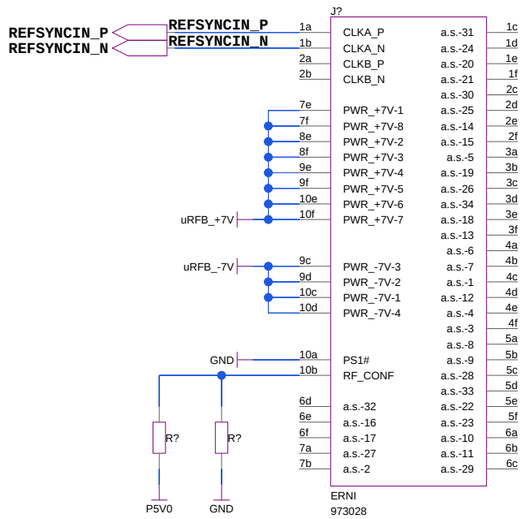
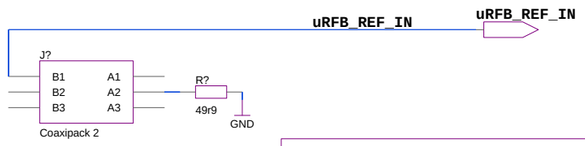
| A3 | 1 | |

| DRAWN BY | SHEET | of | |
|---|---|---|---|
| | 16 | 18 | 02/11/2016:00:40 |

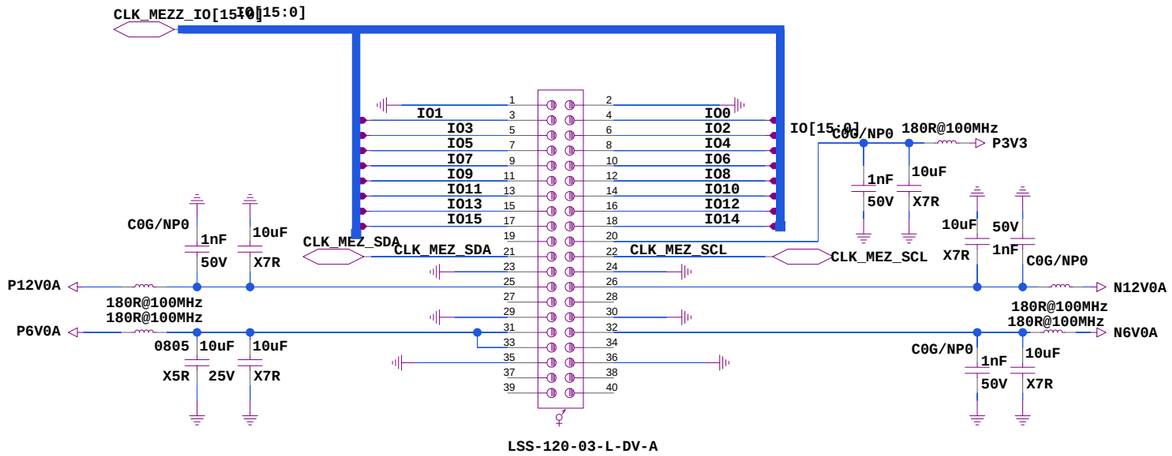


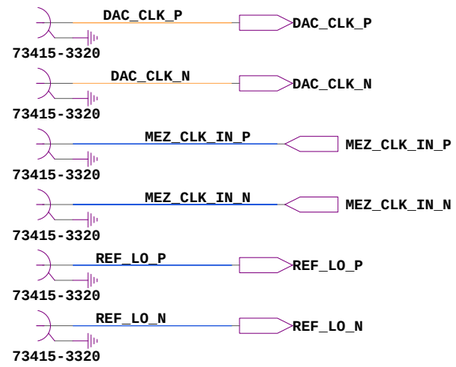





# uRFB_Connectors

| | | |
|---|---|---|
| TITLE | | |
| SIZE A3 | DWG NO 1 | REV |
| DRAWN BY | SHEET 18 of 18 | 02/11/2016:00:40 |

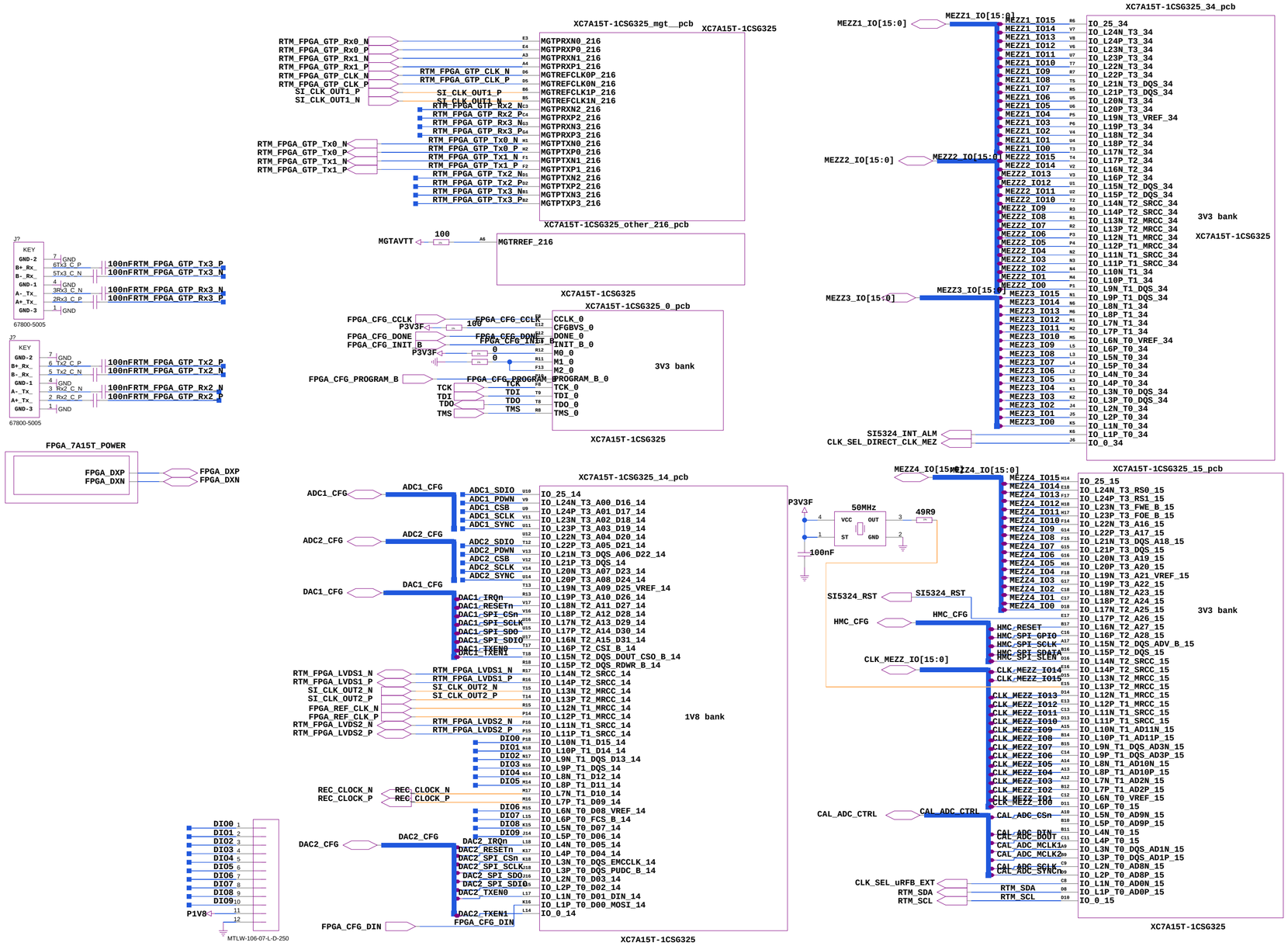



+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth

+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth

+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

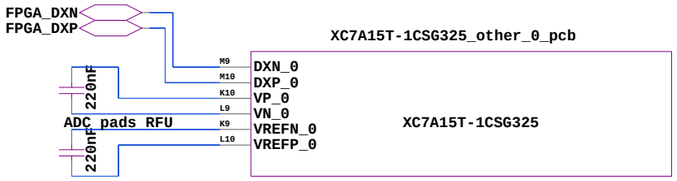


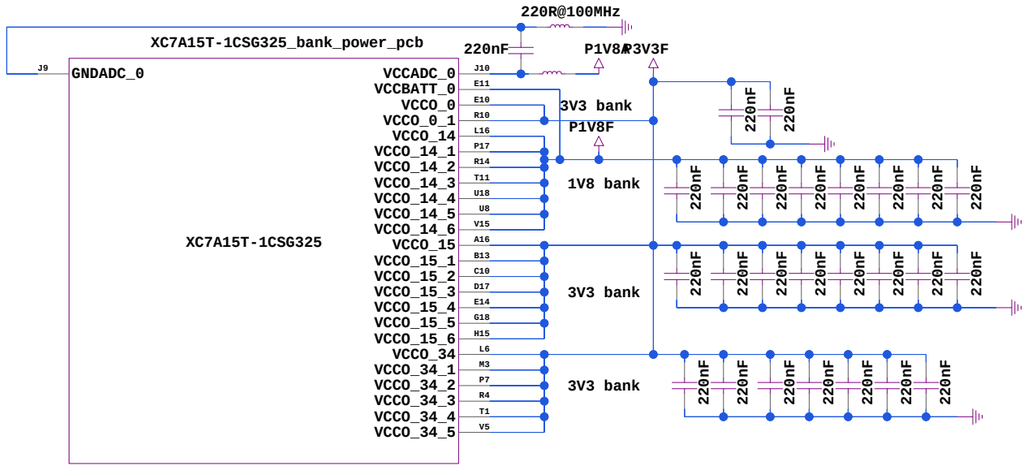

TITLE

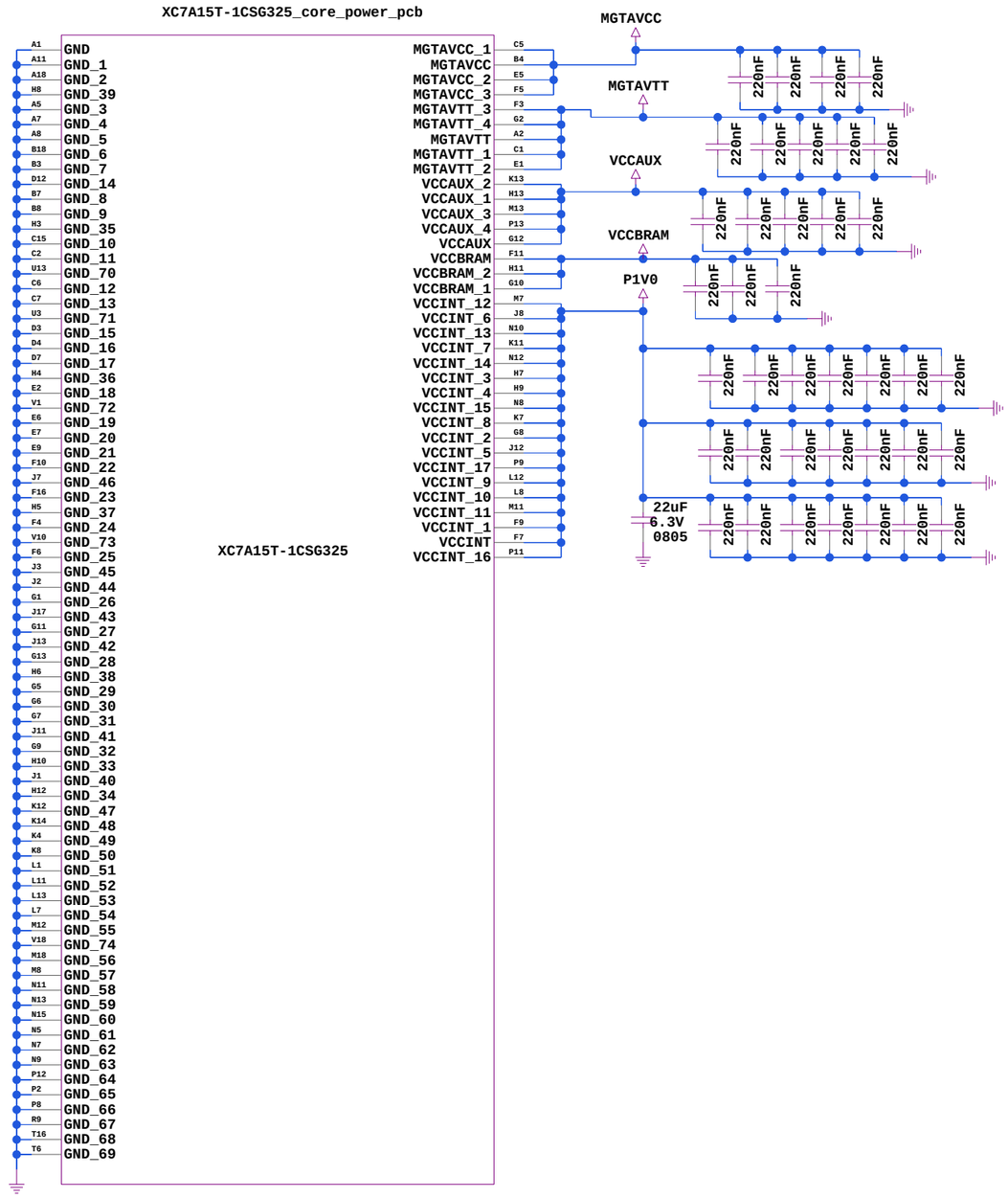
# FPGA_7A15T

| SIZE | DWG NO | REV |
|---|---|---|
| A2 | 1 | |

| DRAWN BY | SHEET | of | |
|---|---|---|---|
| | 18 | | 02/11/2016:00:45 |




TITLE

# FPGA_7A15T_POWER

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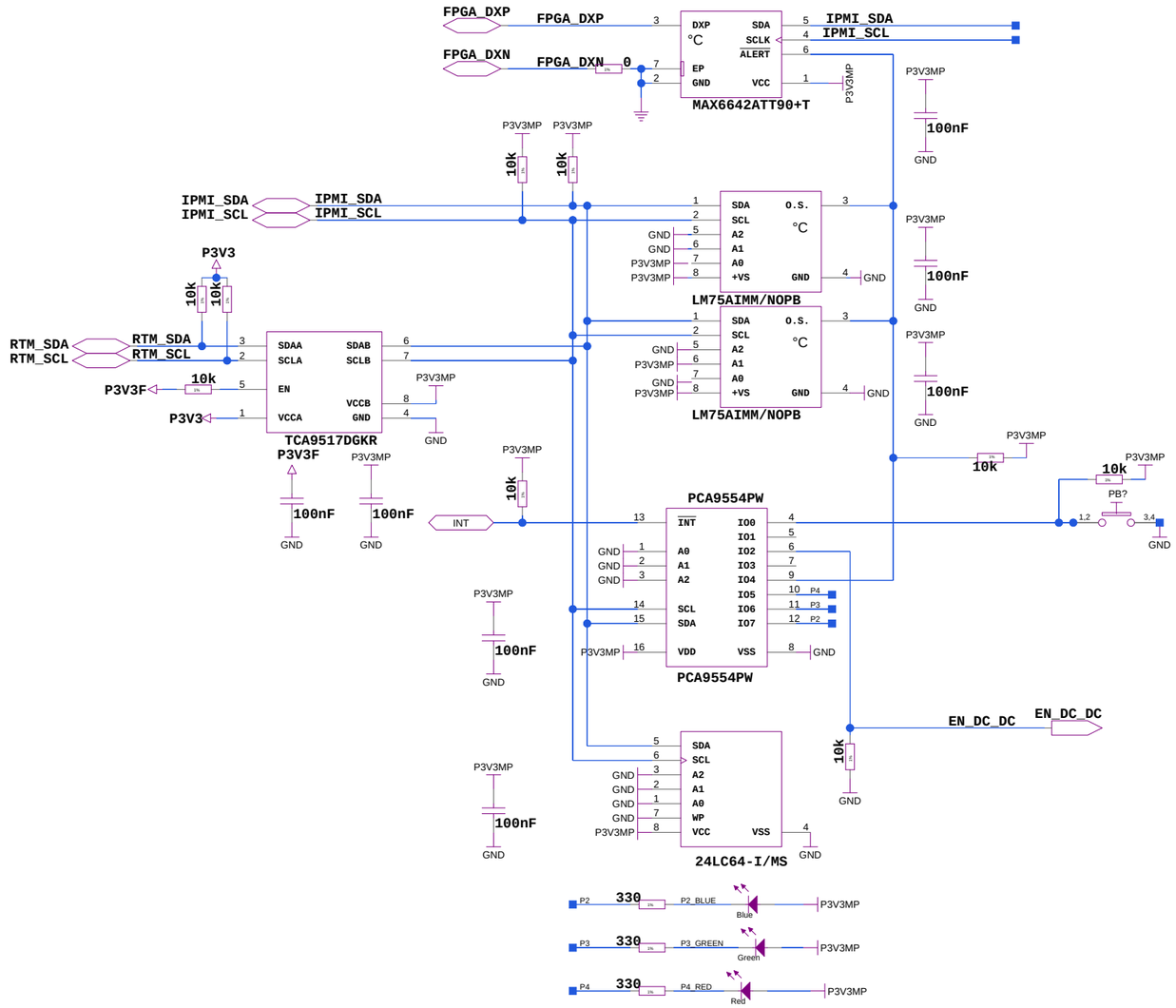
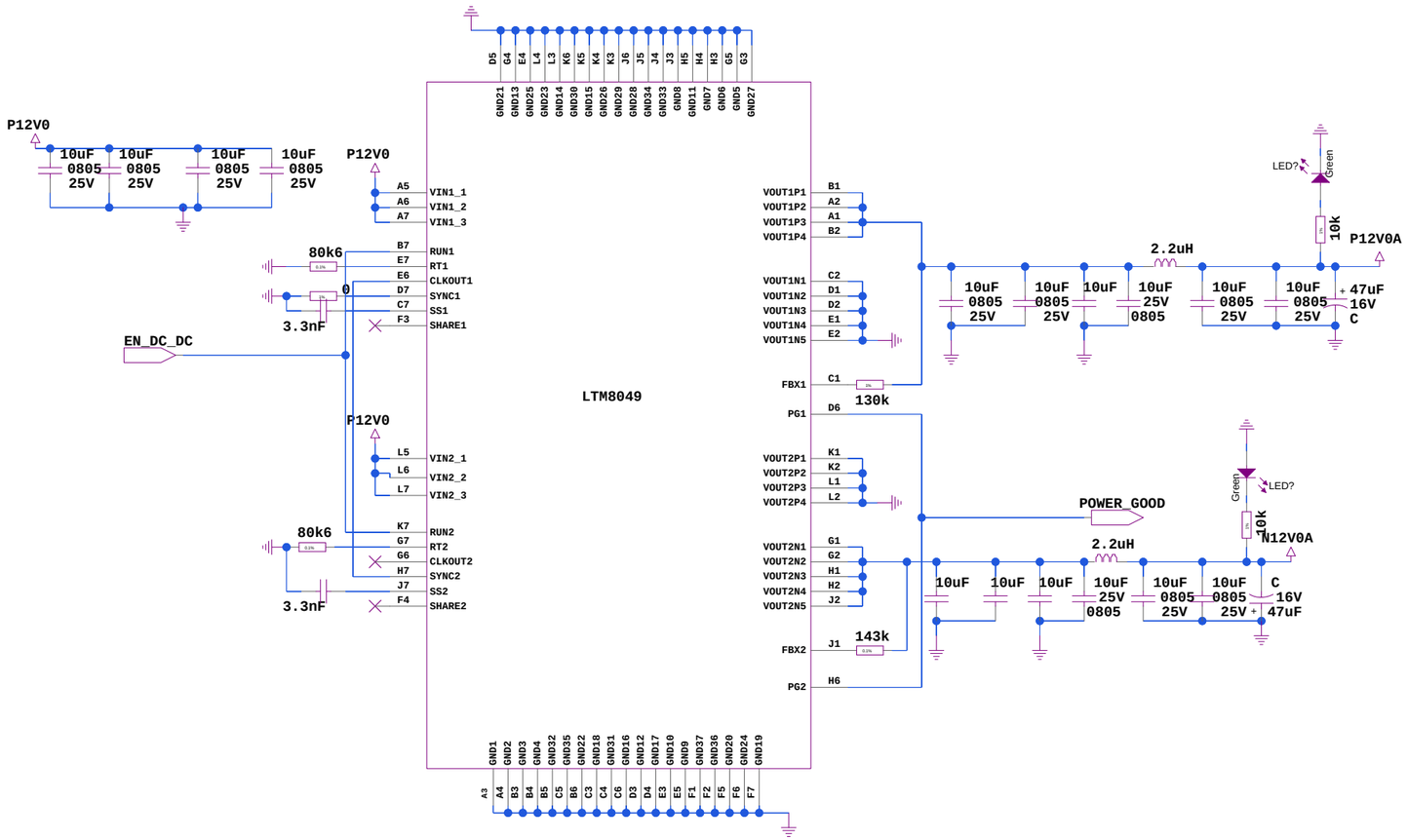
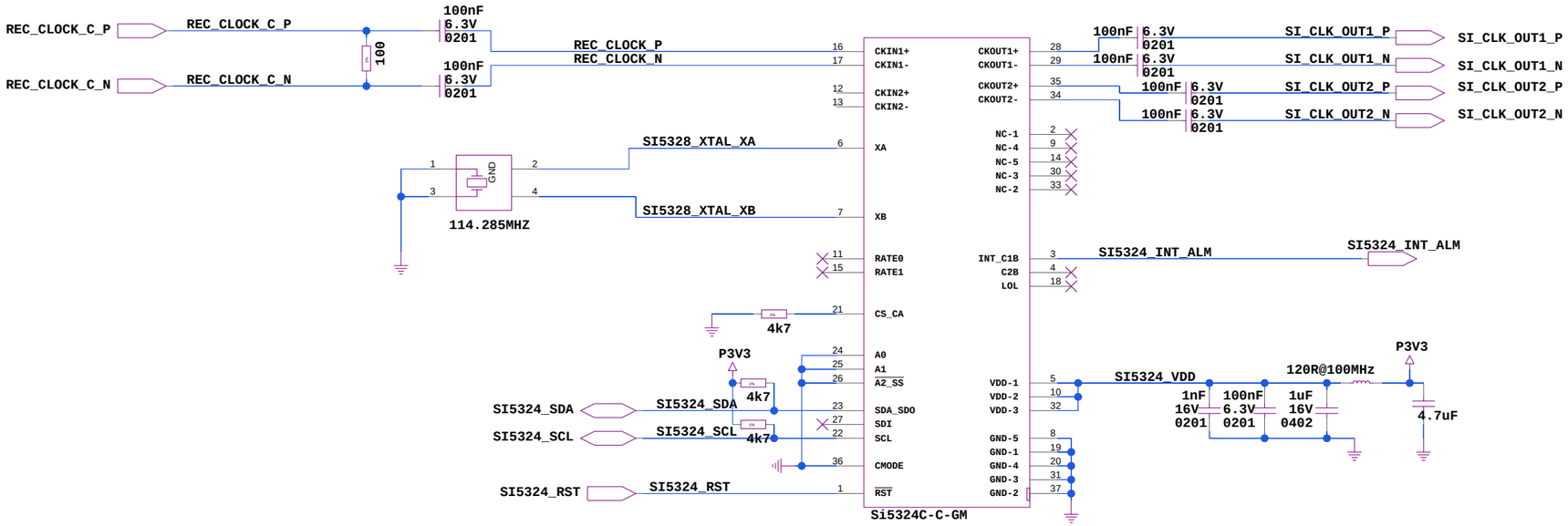
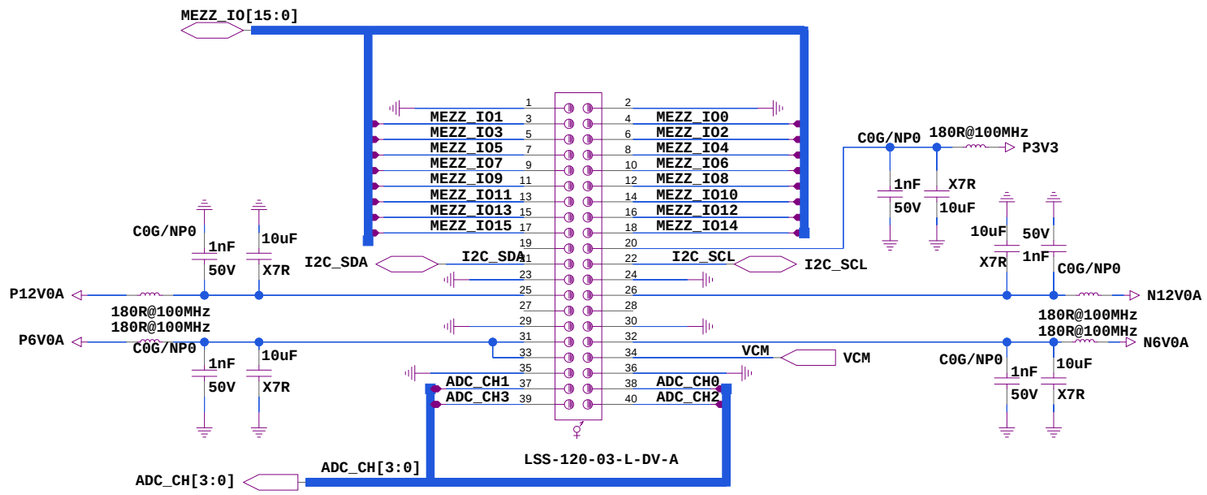
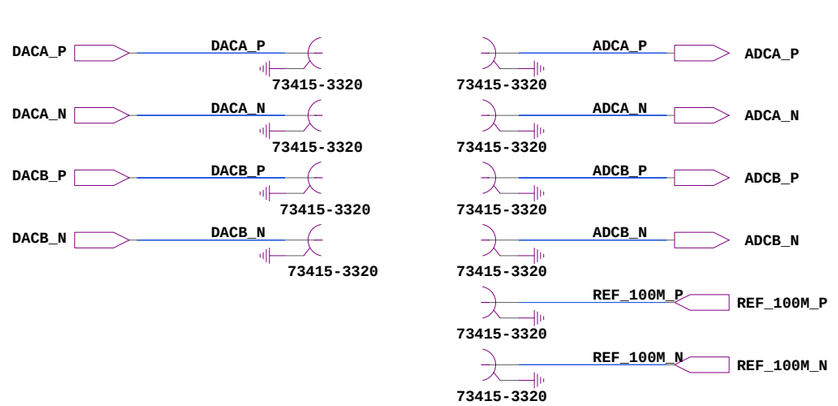
| | 18 | | 02/11/2016:00:47 |


FPGA_DXP
FPGA_DXP
FPGA_DXN
FPGA_DXN
0
DXP
°C
EP
GND
SDA
SCLK
ALERT
VCC
MAX6642ATT90+T
IPMI_SDA
IPMI_SCL
P3V3MP
100nF
GND
10k
P3V3
P3V3F
RTM_SDA
RTM_SCL
SDAA
SCLA
EN
VCCA
SDAB
SCLB
VCCB
TCA9517DGKR
SDA
SCL
A2
A1
A0
+VS
O.S.
LM75AIMM/NOPB
INT
PCA9554PW
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
VDD
VSS
PB?
EN_DC_DC
WP
VCC
24LC64-I/MS
P2
P3
P4
330
P2_BLUE
P3_GREEN
P4_RED
Blue
Green
Red


LTM8049
P12V0
10uF 0805 25V
10uF 0805 25V
10uF 0805 25V
10uF 0805 25V
80k6
0
3.3nF
EN_DC_DC
VIN1_1
VIN1_2
VIN1_3
RUN1
RT1
CLKOUT1
SYNC1
SS1
SHARE1
VIN2_1
VIN2_2
VIN2_3
RUN2
RT2
CLKOUT2
SYNC2
SS2
SHARE2
VOUT1P1
VOUT1P2
VOUT1P3
VOUT1P4
VOUT1N1
VOUT1N2
VOUT1N3
VOUT1N4
VOUT1N5
FBX1
130k
PG1
VOUT2P1
VOUT2P2
VOUT2P3
VOUT2P4
VOUT2N1
VOUT2N2
VOUT2N3
VOUT2N4
VOUT2N5
FBX2
143k
PG2
2.2uH
10uF 0805 25V
10uF 25V 0805
47uF 16V C
P12V0A
LED?
Green
10k
POWER_GOOD
N12V0A
GND21 GND13 GND25 GND23 GND14 GND30 GND15 GND26 GND29 GND28 GND34 GND33 GND8 GND11 GND7 GND6 GND5 GND27
GND1 GND2 GND3 GND4 GND32 GND35 GND22 GND18 GND31 GND16 GND12 GND17 GND10 GND9 GND37 GND36 GND20 GND24 GND19


REC_CLOCK_C_P
REC_CLOCK_C_P
REC_CLOCK_C_N
REC_CLOCK_C_N
100
100nF
6.3V
0201
100nF
6.3V
0201
REC_CLOCK_P
REC_CLOCK_N
CKIN1+
CKIN1-
CKIN2+
CKIN2-
XA
XB
RATE0
RATE1
CS_CA
A0
A1
A2_SS
SDA_SDO
SDI
SCL
CMODE
RST
SI5328_XTAL_XA
SI5328_XTAL_XB
GND
114.285MHZ
4k7
P3V3
4k7
4k7
SI5324_SDA
SI5324_SDA
SI5324_SCL
SI5324_SCL
SI5324_RST
SI5324_RST
CKOUT1+
CKOUT1-
CKOUT2+
CKOUT2-
NC-1
NC-4
NC-5
NC-3
NC-2
INT_C1B
C2B
LOL
VDD-1
VDD-2
VDD-3
GND-5
GND-1
GND-4
GND-3
GND-2
Si5324C-C-GM
100nF
6.3V
0201
100nF
6.3V
0201
100nF
6.3V
0201
100nF
6.3V
0201
SI_CLK_OUT1_P
SI_CLK_OUT1_N
SI_CLK_OUT2_P
SI_CLK_OUT2_N
SI_CLK_OUT1_P
SI_CLK_OUT1_N
SI_CLK_OUT2_P
SI_CLK_OUT2_N
SI5324_INT_ALM
SI5324_INT_ALM
SI5324_VDD
120R@100MHz
P3V3
1nF
16V
0201
100nF
6.3V
0201
1uF
16V
0402
4.7uF




+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

# ADC_DAC_AFE_Mezzanine

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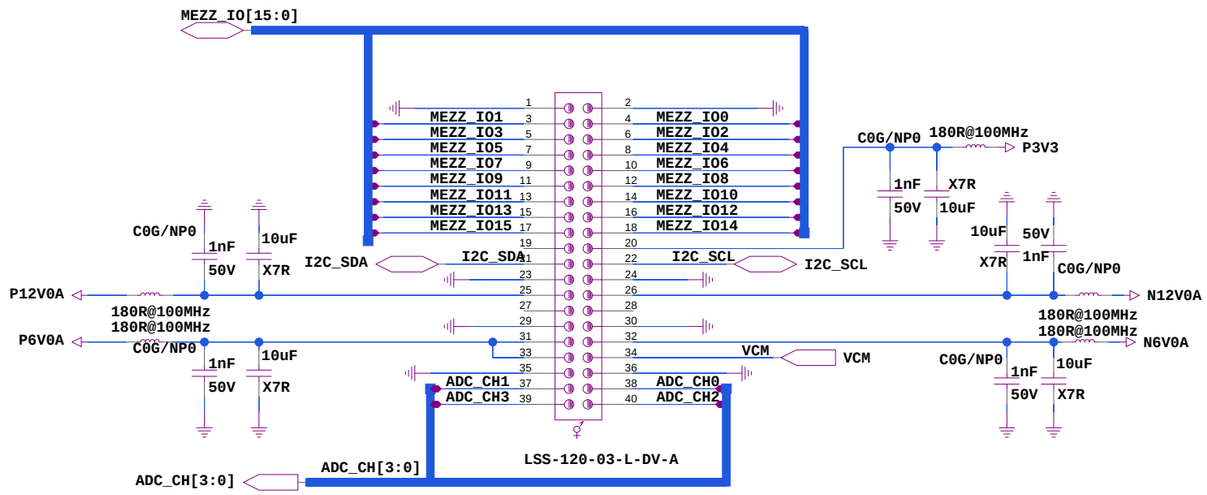


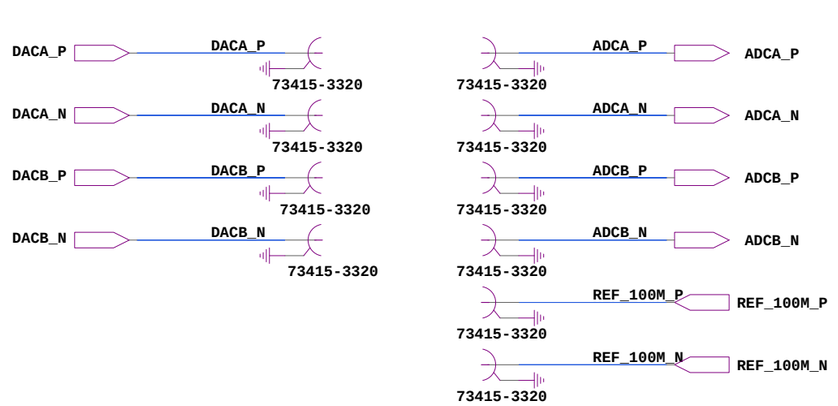


+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

# ADC_DAC_AFE_Mezzanine

| | | |
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| TITLE | | |
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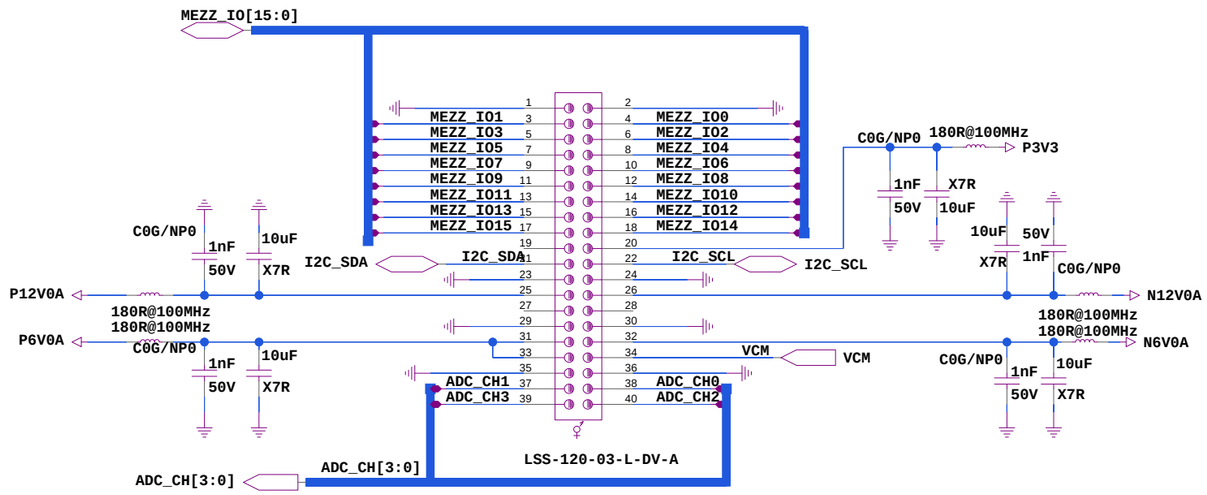


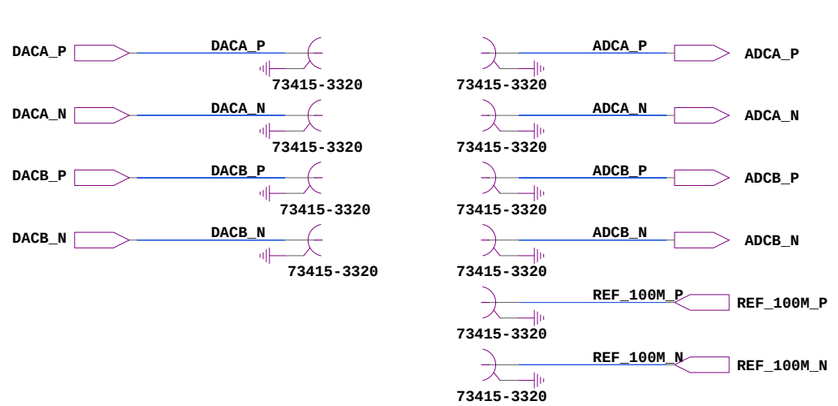


+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

# ADC_DAC_AFE_Mezzanine

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|---|---|---|
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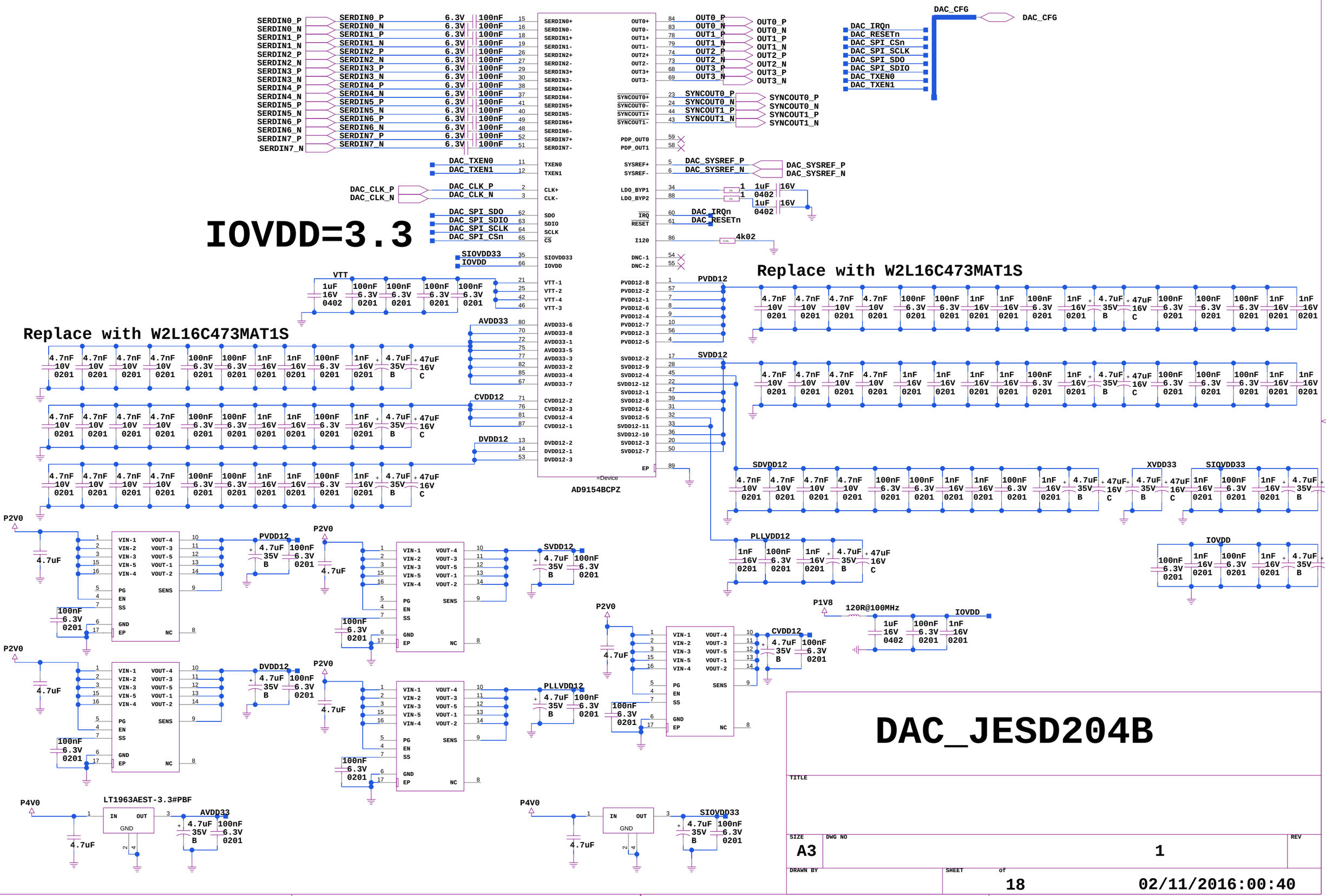


# DAC_JESD204B

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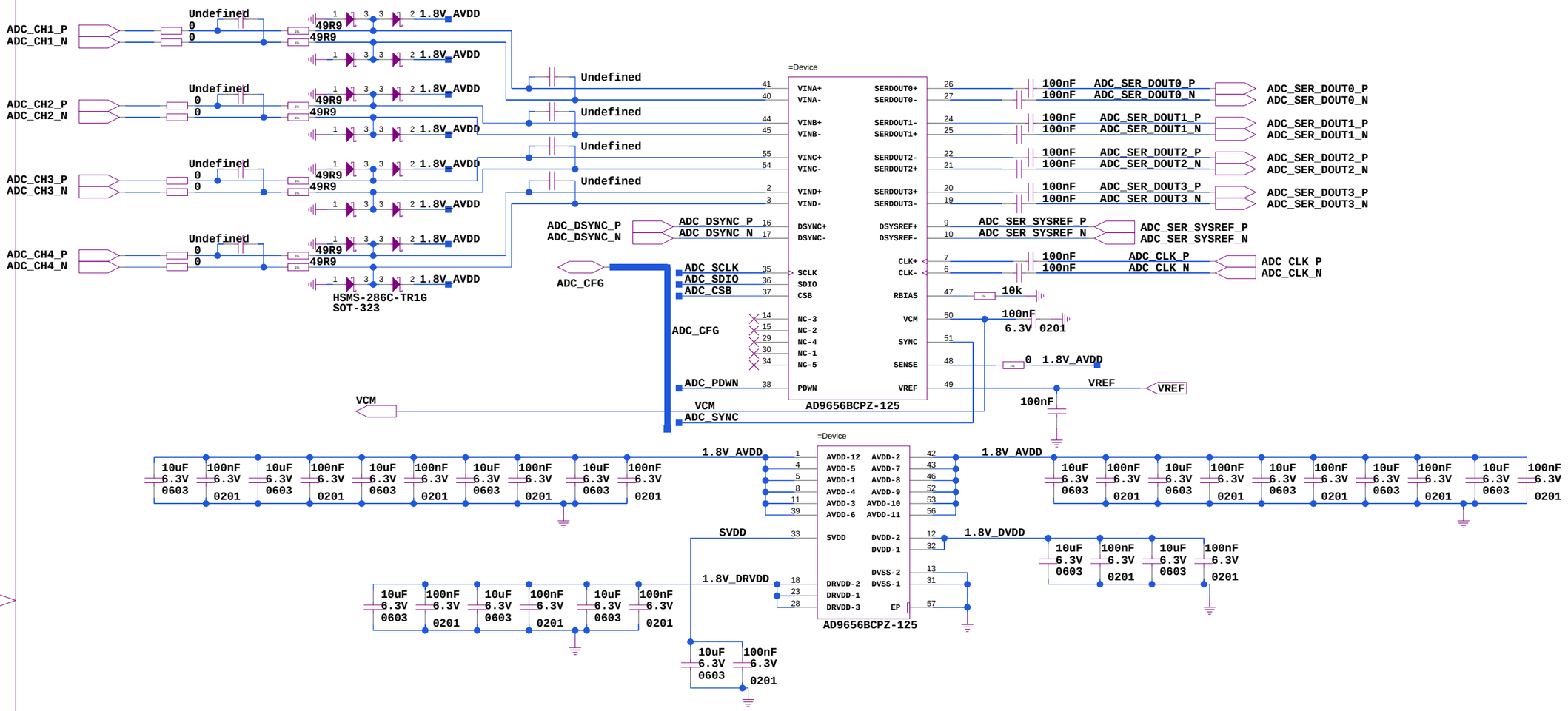


# ADC_JESD204B

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