Class D1.4

J2 — RTM_FPGA_GTP_Tx0_N/P, Tx1_N/P, Rx0_N/P, Rx1_N/P; ADC1_SYNC_P/N; ADC2_SYNC_P/N; RTM_FPGA_USR_IO_N/P; AMC_MASTER_AUX_CLK_N/P; P12V0

J2 — GTP10RX_N/P, GTP11RX_N/P, GTP12RX_N/P, GTP13RX_N/P, GTP14RX_N/P, GTP15RX_N/P; SYNCOUT20_N/P, SYNCOUT21_N/P; IPMI_SCL, IPMI_SDA (P3V3MP)

J2 — GTP10TX_N/P, GTP11TX_N/P, GTP12TX_N/P, GTP13TX_N/P, GTP14TX_N/P, GTP15TX_N/P; SYNCOUT10_N/P, SYNCOUT11_N/P; TMS, TDI, TDO, TCK

J3 — GND

J1 — FPGA_CFG_DIN, FPGA_CFG_CCLK, FPGA_CFG_PROGRAM_B, FPGA_CFG_DONE, FPGA_CFG_INIT_B; USR_UART_N/P; RTM_FPGA_LVDS1_N/P; GTP_CLK2_IN_N/P; RTM_FPGA_LVDS2_N/P; FPGA_ADC_SYSREF_N/P; FPGA_DAC_SYSREF_N/P; GTP_CLK1_IN_N/P

J1 — GTP0RX_N/P, GTP1RX_N/P, GTP2RX_N/P, GTP3RX_N/P, GTP4RX_N/P, GTP5RX_N/P, GTP6RX_N/P, GTP7RX_N/P, GTP8RX_N/P, GTP9RX_N/P

J1 — GTP0TX_N/P, GTP1TX_N/P, GTP2TX_N/P, GTP3TX_N/P, GTP4TX_N/P, GTP5TX_N/P, GTP6TX_N/P, GTP7TX_N/P, GTP8TX_N/P, GTP9TX_N/P

P3V3 — R21 2k2 RTM_SDA; R20 2k2 RTM_SCL; P3V3

IC1 TCA9548ARGER — SDA, SCL, RESET, A2, A1, A0, VCC, GND, EP; SD0/SC0 … SD7/SC7

MEZ_SDA1, MEZ_SCL1, MEZ_SDA2, MEZ_SCL2, MEZ_SDA3, MEZ_SCL3, MEZ_SDA4, MEZ_SCL4, CLK_MEZ_SDA5, CLK_MEZ_SCL5, SI5324_SDA, SI5324_SCL

R17 0, R18 0, R19 0; R16 2k2, R15 2k2, R14 2k2, R13 2k2, R12 2k2, R11 2k2, R10 2k2, R9 2k2, R8 2k2, R7 2k2, R6 2k2, R5 2k2, R4 2k2, R3 2k2, R2 2k2, R1 2k2

P3V3 — R186 1M ESDSTRIP1; R187 1M ESDSTRIP2

CAL_ADC — ADC_CH[16:0] → ADC_CH[16:0] CAL_ADC_CTRL → CAL_ADC_CTRL

P1V8 — 30R@100MHz L1; C2 4.7uF 35V B; 100nF 6.3V 0201; C48; LM4140ACM-1.2/NOPB IC2 (VIN, VREF, EN, GND-1, NC, GND-4, GND-2, GND-3); C1 4.7uF 35V B

DAC1_SYSREF_P/N, DAC1_CLK_P/N → DAC_SYSREF_P/N, DAC_CLK_P/N; SERDIN0_N/P … SERDIN7_N/P; OUT0_P/N … OUT3_P/N; DAC1; DAC_CFG; SYNCOUT0_P/N

DAC1_CFG; SYNCOUT10_P/N; REF2_LO_P/N; ADC_CH[4:1]

Mezzanine_connectors1 — DACA_P/N, DACB_P/N, VCM, REF_LO_P/N, ADC_CH[3:0], MEZZ_IO[15:0], I2C_SDA, I2C_SCL; ADCA_P/N, ADCB_P/N; MEZZ1_IO[15:0]; MEZ_SDA4, MEZ_SCL4

REF1_LO_P/N; ADC_CH[16:13]; VCM1

Mezzanine_connectors2 — MEZZ2_IO[15:0]; MEZ_SDA1, MEZ_SCL1

ADC1_SYNC_P/N; ADC1_CLK_P/N; ADC1_SER_SYSREF_P/N

ADC1 — ADC_CH1_P/N … ADC_CH4_P/N, VCM, ADC_DSYNC_P/N, ADC_CLK_P/N, ADC_SER_SYSREF_N/P; ADC_SER_DOUT0_N/P … ADC_SER_DOUT3_N/P; ADC_CFG, VREF

ADC1_CFG → GTP0RX_N/P … GTP3RX_N/P

DAC2_SYSREF_P/N, DAC2_CLK_P/N → DAC_SYSREF_P/N, DAC_CLK_P/N; SERDIN0_N/P … SERDIN7_N/P; OUT0_P/N … OUT3_P/N; DAC2; DAC_CFG; SYNCOUT0_P/N

DAC2_CFG; SYNCOUT20_P/N; REF4_LO_P/N; ADC_CH[12:9]

Mezzanine_connectors3 — DACA_P/N, DACB_P/N, VCM, REF_LO_P/N, ADC_CH[3:0], MEZZ_IO[15:0], I2C_SDA, I2C_SCL; ADCA_P/N, ADCB_P/N; MEZZ3_IO[15:0]; MEZ_SDA2, MEZ_SCL2

REF3_LO_P/N; ADC_CH[8:5]; VCM2

Mezzanine_connectors4 — MEZZ4_IO[15:0]; MEZ_SDA3, MEZ_SCL3

ADC2_SYNC_P/N; ADC2_CLK_P/N; ADC2_SER_SYSREF_P/N

ADC2 — ADC_CH1_P/N … ADC_CH4_P/N, VCM, ADC_DSYNC_P/N, ADC_CLK_P/N, ADC_SER_SYSREF_N/P; ADC_SER_DOUT0_N/P … ADC_SER_DOUT3_N/P; ADC_CFG, VREF

ADC2_CFG → GTP4RX_N/P … GTP7RX_N/P

CLK_MEZZ_IO[15:0] → CLK_MEZZ_SDA, CLK_MEZZ_SCL; MEZ_CLK_IN_P/N; REF_LO_P/N; CDR_CLK_CLEAN3_P/N

uRFB_Connectors — uRFB_REF_IN, uRFB_REF_CLK_IN_P/N, REFSYNCIN_P/N, uRFB_DAC_CLK_IN, uRFB_REF_LO

CLK_Mezzanine — DAC_CLK_P/N, MEZ_CLK_IN_P/N, REF_LO_P/N

142-0761-801 SMA J4 — SMA ground loop isolation; C347 10pF; EXT_100M_RF_IN, EXT_100M_RF_IN_GND

FPGA_DAC_SYSREF_P/N, DAC1_SYSREF_P/N, DAC1_CLK_P/N, DAC2_SYSREF_P/N, DAC2_CLK_P/N, uRFB_REF_IN, uRFB_REF_CLK_IN_P/N, REFSYNCIN_P/N, uRFB_DAC_CLK_IN, uRFB_REF_LO, CLK_MEZZ_IO[15:0], DAC_CLK_P/N, MEZ_CLK_IN_P/N, REF_LO_P/N, CDR_CLK_CLEAN3_P/N, EXT_100M_RF_IN, EXT_100M_RF_IN_GND → CLK_DIST_CFG

CLK_DIST_CFG → ADC1_CLK_P/N, ADC1_SER_SYSREF_P/N, FPGA_ADC_SYSREF_P/N, ADC2_CLK_P/N, ADC2_SER_SYSREF_P/N, GTP_CLK1_IN_N/P, RTM_MASTER_AUX_CLK_N/P, GTP_CLK2_IN_N/P, AMC_MASTER_AUX_CLK_N/P, REF1_LO_P/N, REF2_LO_P/N, REF3_LO_P/N, REF4_LO_P/N

RTM_POWER_SUPPLY — POWER_GOOD, EN_DC_DC

SI5324_INT_ALM, SI5324_SDA, SI5324_SCL, SI5324_RST → SI5324_INT_ALM, SI5324_SDA, SI5324_SCL, SI5324_RST; Si5324 Clock recovery

REC_CLOCK_P/N, CDR_CLK_CLEAN2_P/N, CDR_CLK_CLEAN1_P/N, AUX_CLOCK_C2_P/N → REC_CLOCK_C_P/N, CDR_CLK_CLEAN3_P/N

CDR_CLK_CLEAN3_P/N

J62 U.FL; optional CLK input; J63

RTM_IPMI — EN_DC_DC, FPGA_DXP, FPGA_DXN; POWER_GOOD, IPMI_SCL, IPMI_SDA, RESETn, RTM_SDA, RTM_SCL

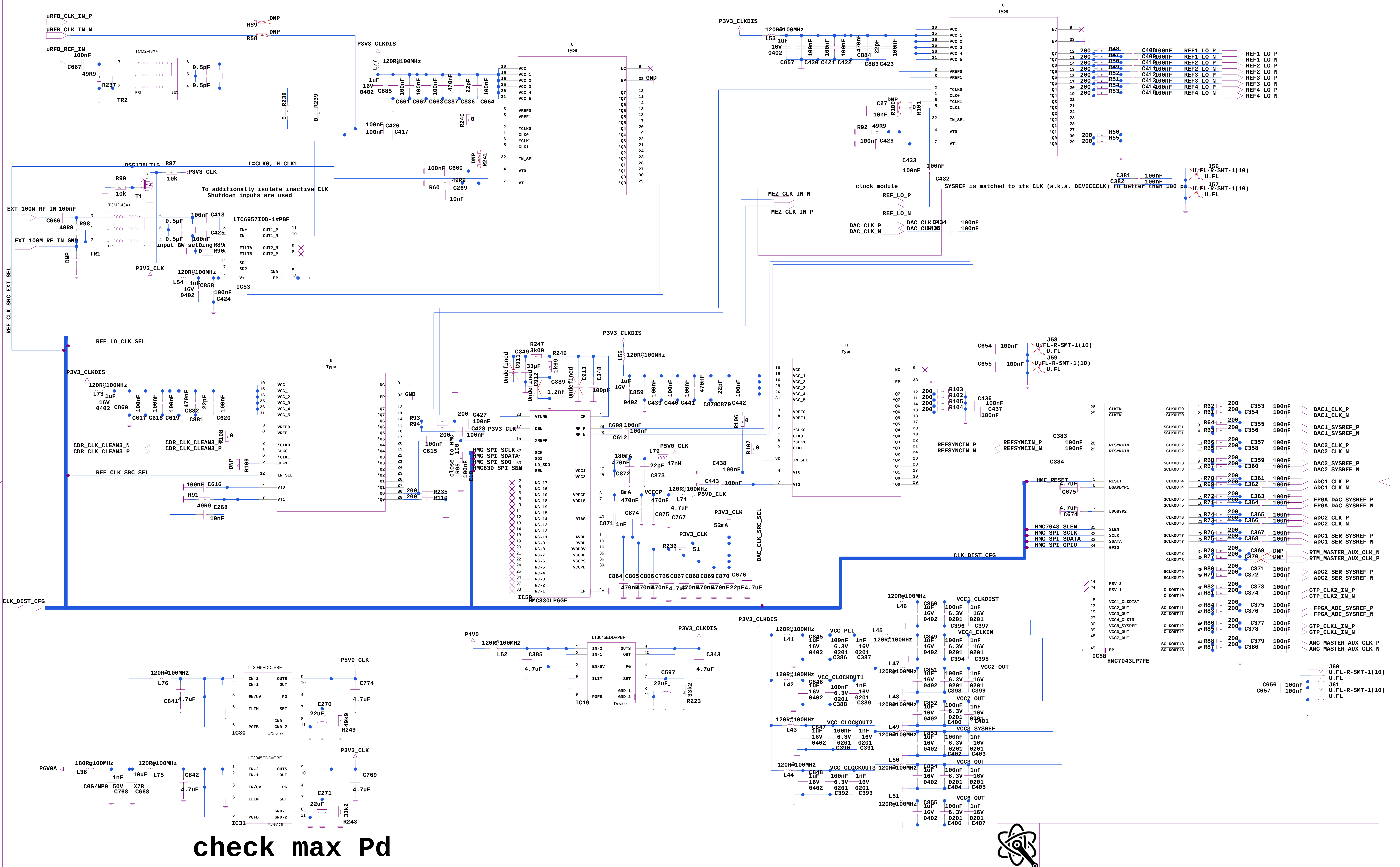
FPGA_7A15T — FPGA_DXP/N, RTM_SDA, RTM_SCL, TMS, TDI, TDO, TCK, USR_UART_N/P, FPGA_CFG_DIN, FPGA_CFG_CCLK, FPGA_CFG_PROGRAM_B, FPGA_CFG_DONE, FPGA_CFG_INIT_B, RTM_MASTER_AUX_CLK_N/P, RTM_FPGA_USR_IO_N/P, RTM_FPGA_GTP_Tx0_N/P, RTM_FPGA_GTP_Tx1_N/P, RESETn, RTM_FPGA_GTP_Rx0_N/P, RTM_FPGA_GTP_Rx1_N/P, RTM_FPGA_LVDS1_N/P, RTM_FPGA_LVDS2_N/P; ADC1_CFG, ADC2_CFG, DAC1_CFG, DAC2_CFG, MEZZ1_IO[15:0], MEZZ2_IO[15:0], MEZZ3_IO[15:0], MEZZ4_IO[15:0], CAL_ADC_CTRL, CLK_DIST_CFG, CLK_MEZZ_IO[15:0], MEZZ_IO[15:0], CDR_CLK_CLEAN2_P/N, CDR_CLK_CLEAN1_P/N, SI5324_INT_ALM, SI5324_RST, REC_CLOCK_P/N

ARTIQ

TITLE: ARTIQ Sinara Sayma_RTM

SIZE	DWG NO	REV
A2	1	v0.95

DRAWN BY	SHEET	of	
G.K.	1	23	03/12/2016:15:22



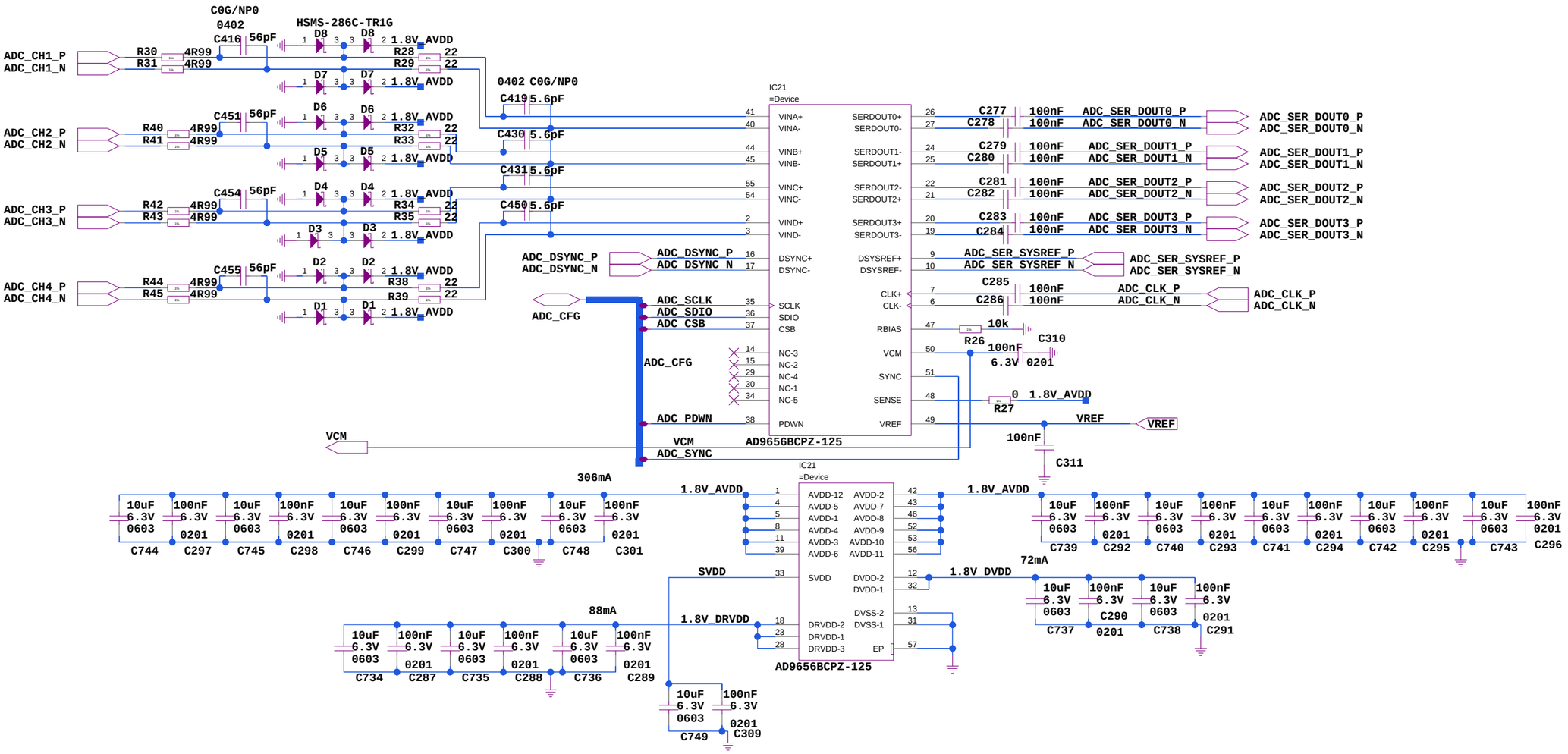
ARTIQ

TITLE

ARTIQ Sinara

SIZE	DWG NO	REV
A2	Clock_Distribution_PLL 1	v0.95

DRAWN BY	SHEET	of	
G.K.	2	23	03/12/2016:15:46



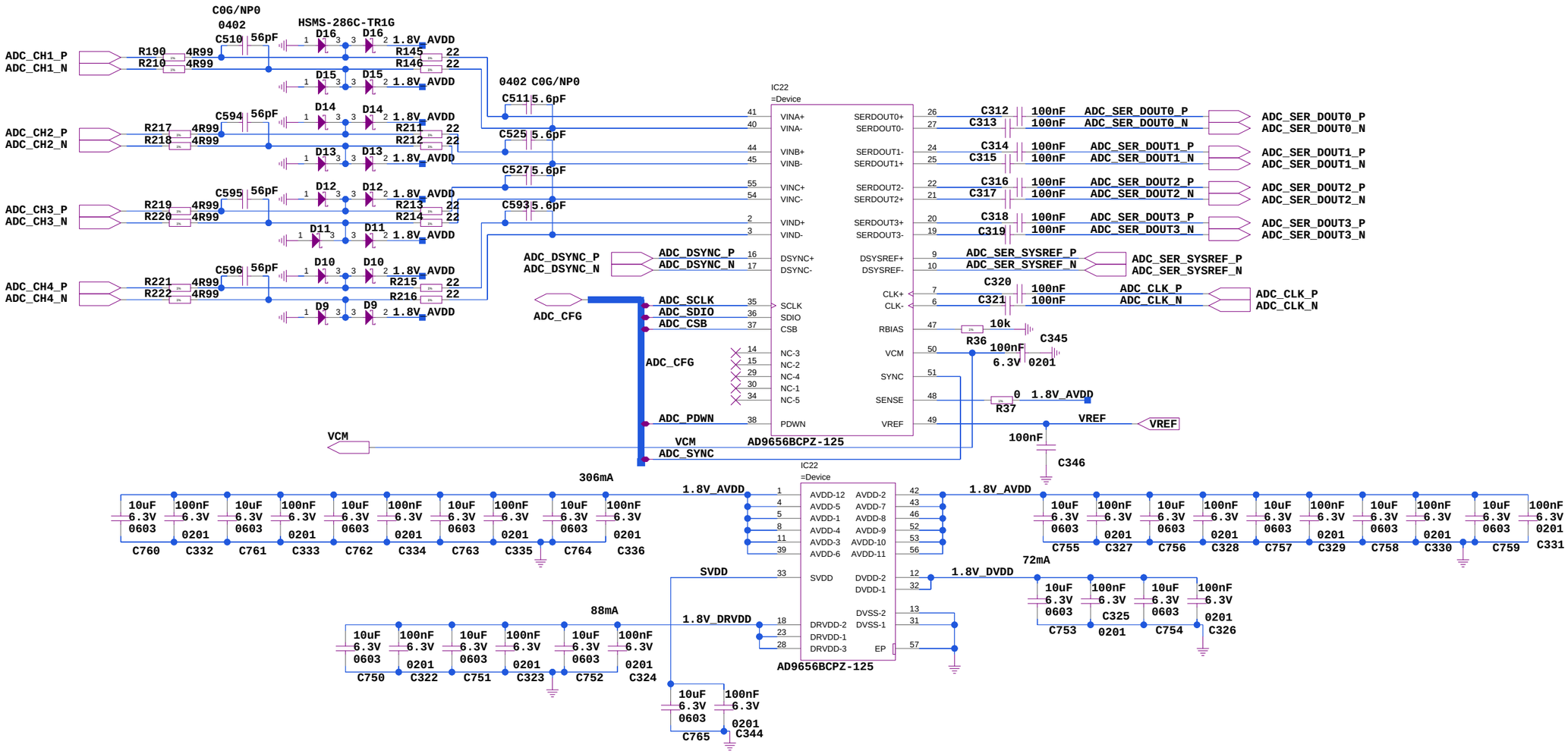
ARTIQ

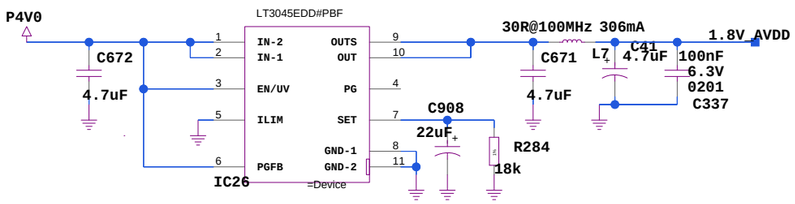
ADC_JESD204B

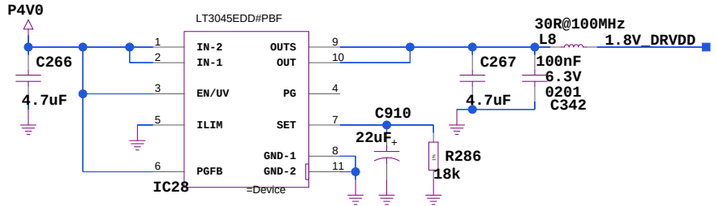
ARTIQ Sinara

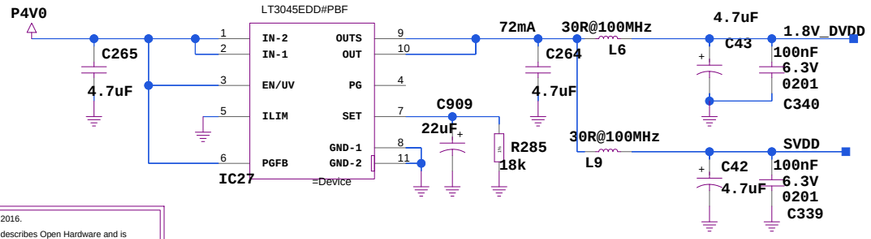
SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET		of	
G.K.	3	23		03/12/2016:13:44









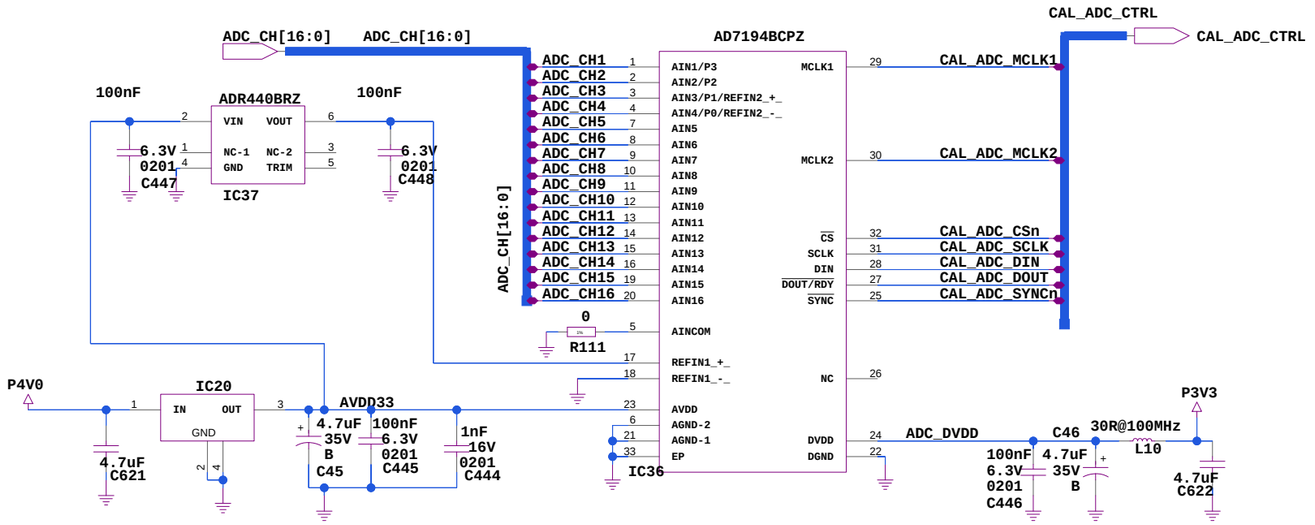
ARTIQ

ADC_JESD204B

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET		
G.K.	4	of 23	03/12/2016:13:44



ARTIQ

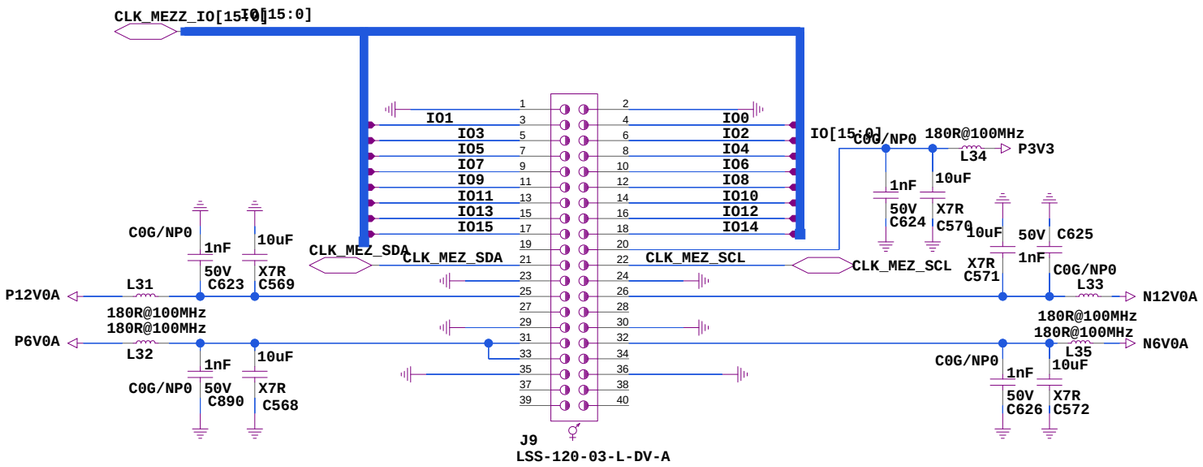
ARTIQ Sinara

TITLE

CAL_ADC

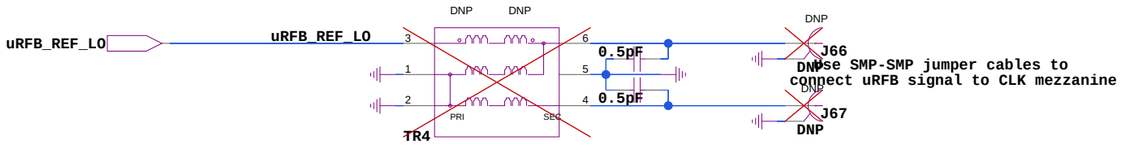
SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET		
G.K.	5	of 23	01/12/2016:18:22

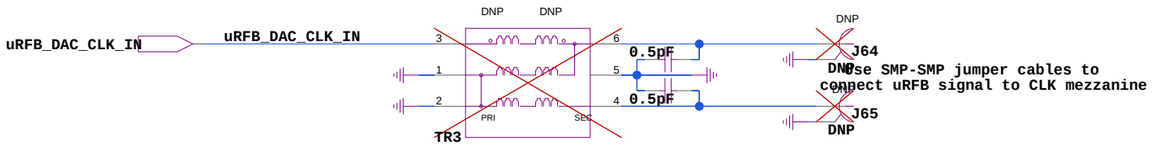


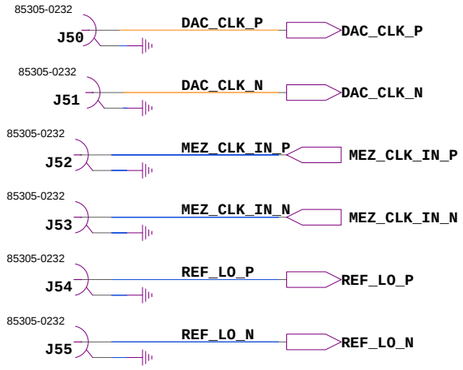
+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

optional RF path for LO signal distribution over RF backplane



optional RF path for DAC clock distribution over RF backplane





ARTIQ

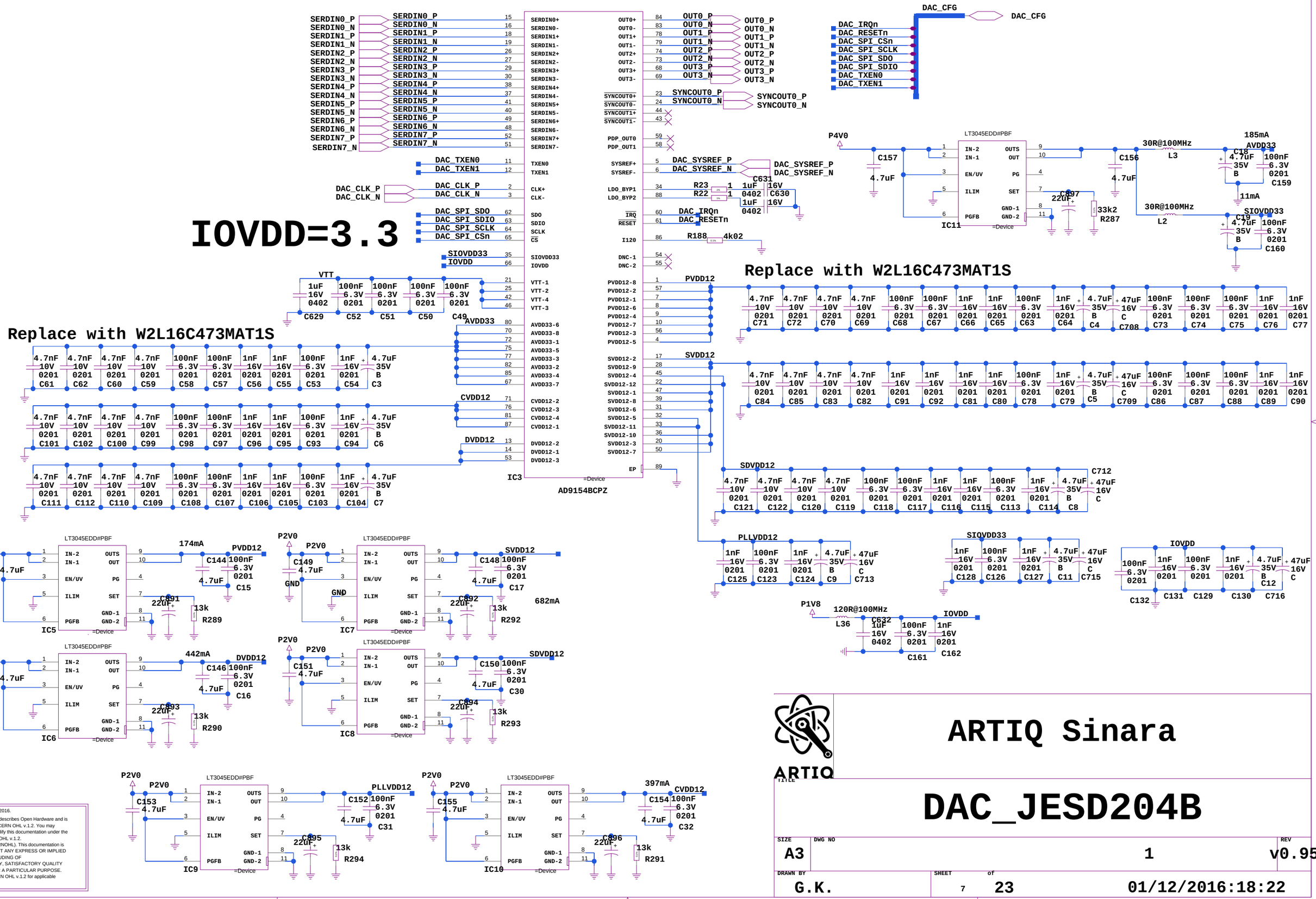
ARTIQ Sinara

TITLE

CLK_Mezzanine

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	6	23	03/12/2016:15:56


IOVDD=3.3
SERDIN0_P
SERDIN0_N
SERDIN1_P
SERDIN1_N
SERDIN2_P
SERDIN2_N
SERDIN3_P
SERDIN3_N
SERDIN4_P
SERDIN4_N
SERDIN5_P
SERDIN5_N
SERDIN6_P
SERDIN6_N
SERDIN7_P
SERDIN7_N
DAC_TXEN0
DAC_TXEN1
DAC_CLK_P
DAC_CLK_N
DAC_SPI_SDO
DAC_SPI_SDIO
DAC_SPI_SCLK
DAC_SPI_CSn
SIOVDD33
IOVDD
VTT
Replace with W2L16C473MAT1S
AVDD33
CVDD12
DVDD12
IC3
AD9154BCPZ
OUT0_P
OUT0_N
OUT1_P
OUT1_N
OUT2_P
OUT2_N
OUT3_P
OUT3_N
SYNCOUT0_P
SYNCOUT0_N
DAC_SYSREF_P
DAC_SYSREF_N
DAC_IRQn
DAC_RESETn
DAC_CFG
P4V0
LT3045EDD#PBF
IC11
30R@100MHz
L3
L2
185mA
AVDD33
11mA
SIOVDD33
Replace with W2L16C473MAT1S
SVDD12
SDVDD12
PLLVDD12
SIOVDD33
IOVDD
P1V8
120R@100MHz
L36
IC5
IC6
IC7
IC8
IC9
IC10
174mA
442mA
682mA
397mA
PVDD12
DVDD12
SVDD12
CVDD12
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ARTIQ Sinara
TITLE
DAC_JESD204B
SIZE
A3
DWG NO
1
REV
v0.95
DRAWN BY
G.K.
SHEET
7
of
23
01/12/2016:18:22

IOVDD=3.3

SERDIN0_P SERDIN0_N SERDIN1_P SERDIN1_N SERDIN2_P SERDIN2_N SERDIN3_P SERDIN3_N SERDIN4_P SERDIN4_N SERDIN5_P SERDIN5_N SERDIN6_P SERDIN6_N SERDIN7_P SERDIN7_N

DAC_TXEN0 DAC_TXEN1

DAC_CLK_P DAC_CLK_N

DAC_SPI_SDO DAC_SPI_SDIO DAC_SPI_SCLK DAC_SPI_CSn

SIOVDD33 IOVDD

VTT

C633 1uF 16V 0402 · C166 100nF 6.3V 0201 · C165 100nF 6.3V 0201 · C164 100nF 6.3V 0201 · C163 100nF 6.3V 0201

AVDD33

CVDD12

DVDD12

Replace with W2L16C473MAT1S

C175 4.7nF 10V 0201 · C176 4.7nF 10V 0201 · C174 4.7nF 10V 0201 · C173 4.7nF 10V 0201 · C172 100nF 6.3V 0201 · C171 100nF 6.3V 0201 · C170 1nF 16V 0201 · C169 1nF 16V 0201 · C167 100nF 6.3V 0201 · C168 1nF 16V 0201 · C20 4.7uF 35V B

C215 4.7nF 10V 0201 · C216 4.7nF 10V 0201 · C214 4.7nF 10V 0201 · C213 4.7nF 10V 0201 · C212 100nF 6.3V 0201 · C211 100nF 6.3V 0201 · C210 1nF 16V 0201 · C209 1nF 16V 0201 · C207 100nF 6.3V 0201 · C208 1nF 16V 0201 · C23 4.7uF 35V B

C225 4.7nF 10V 0201 · C226 4.7nF 10V 0201 · C224 4.7nF 10V 0201 · C223 4.7nF 10V 0201 · C222 100nF 6.3V 0201 · C221 100nF 6.3V 0201 · C220 1nF 16V 0201 · C219 1nF 16V 0201 · C217 100nF 6.3V 0201 · C218 1nF 16V 0201 · C24 4.7uF 35V B

IC4 AD9154BCPZ

DAC_CFG

DAC_IRQn DAC_RESETn DAC_SPI_CSn DAC_SPI_SCLK DAC_SPI_SDO DAC_SPI_SDIO DAC_TXEN0 DAC_TXEN1

SYNCOUT0_P SYNCOUT0_N

DAC_SYSREF_P DAC_SYSREF_N

R25 1 1uF 16V C635 · R24 1 0402 1uF 16V C634

DAC_IRQn DAC_RESETn

R189 4k02

PVDD12

C185 4.7nF 10V 0201 · C186 4.7nF 10V 0201 · C184 4.7nF 10V 0201 · C183 4.7nF 10V 0201 · C182 100nF 6.3V 0201 · C181 100nF 6.3V 0201 · C180 1nF 16V 0201 · C179 1nF 16V 0201 · C177 100nF 6.3V 0201 · C178 1nF 16V 0201 · C21 4.7uF 35V B · C718 47uF 16V C · C187 100nF 6.3V 0201 · C188 100nF 6.3V 0201 · C189 100nF 6.3V 0201 · C190 1nF 16V 0201 · C191 1nF 16V 0201

SVDD12

C198 4.7nF 10V 0201 · C199 4.7nF 10V 0201 · C197 4.7nF 10V 0201 · C196 4.7nF 10V 0201 · C205 1nF 16V 0201 · C206 1nF 16V 0201 · C195 1nF 16V 0201 · C194 1nF 16V 0201 · C192 100nF 6.3V 0201 · C193 1nF 16V 0201 · C22 4.7uF 35V B · C719 47uF 16V C · C200 100nF 6.3V 0201 · C201 100nF 6.3V 0201 · C202 100nF 6.3V 0201 · C203 1nF 16V 0201 · C204 1nF 16V 0201

SDVDD12

C235 4.7nF 10V 0201 · C236 4.7nF 10V 0201 · C234 4.7nF 10V 0201 · C233 4.7nF 10V 0201 · C232 100nF 6.3V 0201 · C231 100nF 6.3V 0201 · C230 1nF 16V 0201 · C229 1nF 16V 0201 · C227 100nF 6.3V 0201 · C228 1nF 16V 0201 · C25 4.7uF 35V B · C722 47uF 16V C

PLLVDD12

C239 1nF 16V 0201 · C237 100nF 6.3V 0201 · C238 1nF 16V 0201 · C26 4.7uF 35V B · C723 47uF 16V C

SIOVDD33

C242 1nF 16V 0201 · C240 100nF 6.3V 0201 · C241 1nF 16V 0201 · C28 4.7uF 35V B · C725 47uF 16V C

IOVDD

C246 100nF 6.3V 0201 · C245 1nF 16V 0201 · C243 100nF 6.3V 0201 · C244 1nF 16V 0201 · C726 4.7uF 35V B · C29 47uF 16V C

P4V0 · C259 4.7uF · IC18 LT3045EDD#PBF =Device · C258 4.7uF · C204 22uF · R288 33k2 · 30R@100MHz L40 · 185mA AVDD33 · C13 4.7uF 35V B · C33 100nF 6.3V 0201 · 11mA · 30R@100MHz L39 · SIOVDD33 · C14 4.7uF 35V B · C274 100nF 6.3V 0201

P1V8 · L37 120R@100MHz · C636 1uF 16V 0402 · IOVDD · C275 100nF 6.3V 0201 · C276 1nF 16V 0201

P2V0 · C247 4.7uF · IC12 LT3045EDD#PBF =Device · 174mA · PVDD12 · C158 100nF 6.3V 0201 · C34 4.7uF · C698 22uF · R295 13k

P2V0 · C251 4.7uF · GND · IC14 LT3045EDD#PBF =Device · SVDD12 · C250 100nF 6.3V 0201 · C36 4.7uF · C699 22uF · R298 13k · 682mA

P2V0 · C249 4.7uF · IC13 LT3045EDD#PBF =Device · 442mA · DVDD12 · C248 100nF 6.3V 0201 · C35 4.7uF · C900 22uF · R296 13k

P2V0 · C253 4.7uF · IC15 LT3045EDD#PBF =Device · SDVDD12 · C252 100nF 6.3V 0201 · C40 4.7uF · C901 22uF · R299 13k

P2V0 · C255 4.7uF · IC16 LT3045EDD#PBF =Device · PLLVDD12 · C254 100nF 6.3V 0201 · C44 4.7uF · C902 22uF · R300 13k

P2V0 · C257 4.7uF · IC17 LT3045EDD#PBF =Device · 397mA · CVDD12 · C256 100nF 6.3V 0201 · C143 4.7uF · C903 22uF · R297 13k

ARTIQ Sinara

TITLE: DAC_JESD204B

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	8	23	01/12/2016:18:22

P3V3F L78 120R@100MHz C352 100nF DNP OSC2 OE NC VDD CLK+ CLK- GND =Value

RTM_FPGA_GTP_Rx0_N RTM_FPGA_GTP_Rx0_P RTM_FPGA_GTP_Rx1_N RTM_FPGA_GTP_Rx1_P RTM_FPGA_GTP_CLK_N C458 100nF RTM_FPGA_GTP_CLK_P C459 100nF CDR_CLK_CLEAN1_P CDR_CLK_CLEAN1_N RTM_FPGA_GTP_Rx2_N RTM_FPGA_GTP_Rx2_P RTM_FPGA_GTP_Rx3_N RTM_FPGA_GTP_Rx3_P RTM_FPGA_GTP_Tx0_N C133 100nF RTM_FPGA_GTP_Tx0_P C134 100nF RTM_FPGA_GTP_Tx1_N C135 100nF RTM_FPGA_GTP_Tx1_P C136 100nF RTM_FPGA_GTP_Tx2_N C137 100nF RTM_FPGA_GTP_Tx2_P C138 100nF RTM_FPGA_GTP_Tx3_N C139 100nF RTM_FPGA_GTP_Tx3_P C140 100nF

XC7A15T-1CSG325_mgt__pcb

XC7A15T-1CSG325

MGTPRXN0_216 MGTPRXP0_216 MGTPRXN1_216 MGTPRXP1_216 MGTREFCLK0P_216 MGTREFCLK0N_216 MGTREFCLK1P_216 MGTREFCLK1N_216 MGTPRXN2_216 MGTPRXP2_216 MGTPRXN3_216 MGTPRXP3_216 MGTPTXN0_216 MGTPTXP0_216 MGTPTXN1_216 MGTPTXP1_216 MGTPTXN2_216 MGTPTXP2_216 MGTPTXN3_216 MGTPTXP3_216

XC7A15T-1CSG325_other_216_pcb

MGTAVTT 100 R113 MGTRREF_216

XC7A15T-1CSG325

MASTER SATA

J70 GND-3 A+_Tx_ A-_Tx_ GND-1 B-_Rx_ B+_Rx_ GND-2 KEY GND RTM_FPGA_GTP_Tx3_P RTM_FPGA_GTP_Tx3_N GND Rx3_C_N C452 100nF RTM_FPGA_GTP_Rx3_N Rx3_C_P C453 100nF RTM_FPGA_GTP_Rx3_P GND

SLAVE SATA

J71 GND-3 A+_Tx_ A-_Tx_ GND-1 B-_Rx_ B+_Rx_ GND-2 KEY GND Rx2_C_P C457 100nF RTM_FPGA_GTP_Rx2_P Rx2_C_N C456 100nF RTM_FPGA_GTP_Rx2_N GND RTM_FPGA_GTP_Tx2_N RTM_FPGA_GTP_Tx2_P GND

FPGA_7A15T_POWER

FPGA_DXP FPGA_DXN

XC7A15T-1CSG325_0_pcb

FPGA_CFG_CCLK R114 100 FPGA_CFG_DONE FPGA_CFG_INIT_B R116 0 R112 0 FPGA_CFG_PROGRAM_B TCK TDI TDO TMS

CCLK_0 CFGBVS_0 DONE_0 INIT_B_0 M0_0 M1_0 M2_0 PROGRAM_B_0 TCK_0 TDI_0 TDO_0 TMS_0

3V3 bank

text

XC7A15T-1CSG325

XC7A15T-1CSG325_34_pcb

MEZZ2_IO[15:0] MEZZ2_IO15 MEZZ2_IO14 MEZZ2_IO13 MEZZ2_IO12 MEZZ2_IO11 MEZZ2_IO10 MEZZ2_IO9 MEZZ2_IO8 MEZZ2_IO7 MEZZ2_IO6 MEZZ2_IO5 MEZZ2_IO4 MEZZ2_IO3 MEZZ2_IO2 MEZZ2_IO1 MEZZ2_IO0

MEZZ1_IO[15:0] MEZZ1_IO15 MEZZ1_IO14 MEZZ1_IO13 MEZZ1_IO12 MEZZ1_IO11 MEZZ1_IO10 MEZZ1_IO9 MEZZ1_IO8 MEZZ1_IO7 MEZZ1_IO6 MEZZ1_IO5 MEZZ1_IO4 MEZZ1_IO3 MEZZ1_IO2 MEZZ1_IO1 MEZZ1_IO0

MEZZ4_IO[15:0] MEZZ4_IO15 MEZZ4_IO14 MEZZ4_IO13 MEZZ4_IO12 MEZZ4_IO11 MEZZ4_IO10 MEZZ4_IO9 MEZZ4_IO8 MEZZ4_IO7 MEZZ4_IO6 MEZZ4_IO5 MEZZ4_IO4 MEZZ4_IO3 MEZZ4_IO2 MEZZ4_IO1 MEZZ4_IO0

RTM_SDA RTM_SCL

IO_25_34 IO_L24N_T3_34 IO_L24P_T3_34 IO_L23N_T3_34 IO_L23P_T3_34 IO_L22N_T3_34 IO_L22P_T3_34 IO_L21N_T3_DQS_34 IO_L21P_T3_DQS_34 IO_L20N_T3_34 IO_L20P_T3_34 IO_L19N_T3_VREF_34 IO_L19P_T3_34 IO_L18N_T2_34 IO_L18P_T2_34 IO_L17N_T2_34 IO_L17P_T2_34 IO_L16N_T2_34 IO_L16P_T2_34 IO_L15N_T2_DQS_34 IO_L15P_T2_DQS_34 IO_L14N_T2_SRCC_34 IO_L14P_T2_SRCC_34 IO_L13N_T2_MRCC_34 IO_L13P_T2_MRCC_34 IO_L12N_T1_MRCC_34 IO_L12P_T1_MRCC_34 IO_L11N_T1_SRCC_34 IO_L11P_T1_SRCC_34 IO_L10N_T1_34 IO_L10P_T1_34 IO_L9N_T1_DQS_34 IO_L9P_T1_DQS_34 IO_L8N_T1_34 IO_L8P_T1_34 IO_L7N_T1_34 IO_L7P_T1_34 IO_L6N_T0_VREF_34 IO_L6P_T0_34 IO_L5N_T0_34 IO_L5P_T0_34 IO_L4N_T0_34 IO_L4P_T0_34 IO_L3N_T0_DQS_34 IO_L3P_T0_DQS_34 IO_L2N_T0_34 IO_L2P_T0_34 IO_L1N_T0_34 IO_L1P_T0_34 IO_0_34

3V3 bank

XC7A15T-1CSG325

CLK_DIST_CFG

XC7A15T-1CSG325_15_pcb

MEZZ3_IO[15:0] MEZZ3_IO15 MEZZ3_IO14 MEZZ3_IO13 MEZZ3_IO12 MEZZ3_IO11 MEZZ3_IO10 MEZZ3_IO9 MEZZ3_IO8 MEZZ3_IO7 MEZZ3_IO6 MEZZ3_IO5 MEZZ3_IO4 MEZZ3_IO3 MEZZ3_IO2 MEZZ3_IO1 MEZZ3_IO0

IO_25_15 IO_L24N_T3_RS0_15 IO_L24P_T3_RS1_15 IO_L23N_T3_FWE_B_15 IO_L23P_T3_FOE_B_15 IO_L22N_T3_A16_15 IO_L22P_T3_A17_15 IO_L21N_T3_DQS_A18_15 IO_L21P_T3_DQS_15 IO_L20N_T3_A19_15 IO_L20P_T3_A20_15 IO_L19N_T3_A21_VREF_15 IO_L19P_T3_A22_15 IO_L18N_T2_A23_15 IO_L18P_T2_A24_15 IO_L17N_T2_A25_15 IO_L17P_T2_A26_15 IO_L16N_T2_A27_15 IO_L16P_T2_A28_15 IO_L15N_T2_DQS_ADV_B_15 IO_L15P_T2_DQS_15 IO_L14N_T2_SRCC_15 IO_L14P_T2_SRCC_15 IO_L13N_T2_MRCC_15 IO_L13P_T2_MRCC_15 IO_L12N_T1_MRCC_15 IO_L12P_T1_MRCC_15 IO_L11N_T1_SRCC_15 IO_L11P_T1_SRCC_15 IO_L10N_T1_AD11N_15 IO_L10P_T1_AD11P_15 IO_L9N_T1_DQS_AD3N_15 IO_L9P_T1_DQS_AD3P_15 IO_L8N_T1_AD10N_15 IO_L8P_T1_AD10P_15 IO_L7N_T1_AD2N_15 IO_L7P_T1_AD2P_15 IO_L6N_T0_VREF_15 IO_L6P_T0_15 IO_L5N_T0_AD9N_15 IO_L5P_T0_AD9P_15 IO_L4N_T0_15 IO_L4P_T0_15 IO_L3N_T0_DQS_AD1N_15 IO_L3P_T0_DQS_AD1P_15 IO_L2N_T0_AD8N_15 IO_L2P_T0_AD8P_15 IO_L1N_T0_AD0N_15 IO_L1P_T0_AD0P_15 IO_0_15

3V3 bank

XC7A15T-1CSG325

P3V3F OSC1 VCC OUT ST GND 50MHz 100nF C449 49R9 R115

SI5324_RST HMC_RESET HMC_RESET

USR_UART_N USR_UART_P HMC_SPI_SCLK HMC_SPI_SDATA HMC7043_SLEN

CLK_MEZZ_IO[15:0] CLK_MEZZ_IO14 CLK_MEZZ_IO15 CLK_MEZZ_IO13 CLK_MEZZ_IO12 CLK_MEZZ_IO11 CLK_MEZZ_IO10 CLK_MEZZ_IO9 CLK_MEZZ_IO8 CLK_MEZZ_IO7 CLK_MEZZ_IO6 CLK_MEZZ_IO5 CLK_MEZZ_IO4 CLK_MEZZ_IO3 CLK_MEZZ_IO2 CLK_MEZZ_IO1 CLK_MEZZ_IO0

CAL_ADC_CTRL CAL_ADC_CSn CAL_ADC_SYNCn CAL_ADC_DIN CAL_ADC_DOUT CAL_ADC_MCLK1 CAL_ADC_MCLK2 CAL_ADC_SCLK

HMC_SPI_SDO HMC8830_SPI_SEN HMC_SPI_GPIO SI5324_INT_ALM SI5324_INT_ALM

XC7A15T-1CSG325_14_pcb

ADC1_CFG ADC1_SDIO ADC_PDWN ADC1_CSB ADC1_SCLK ADC1_SYNC

ADC2_CFG ADC2_SDIO ADC2_CSB ADC2_SCLK ADC2_SYNC

DAC1_CFG DAC1_IRQn DAC1_SPI_CSn DAC1_SPI_SCLK DAC1_SPI_SDO DAC1_SPI_SDIO DAC1_TXEN0 DAC1_TXEN1 DAC_RESETn

IO_25_14 IO_L24N_T3_A00_D16_14 IO_L24P_T3_A01_D17_14 IO_L23N_T3_A02_D18_14 IO_L23P_T3_A03_D19_14 IO_L22N_T3_A04_D20_14 IO_L22P_T3_A05_D21_14 IO_L21N_T3_DQS_A06_D22_14 IO_L21P_T3_DQS_14 IO_L20N_T3_A07_D23_14 IO_L20P_T3_A08_D24_14 IO_L19N_T3_A09_D25_VREF_14 IO_L19P_T3_A10_D26_14 IO_L18N_T2_A11_D27_14 IO_L18P_T2_A12_D28_14 IO_L17N_T2_A13_D29_14 IO_L17P_T2_A14_D30_14 IO_L16N_T2_A15_D31_14 IO_L16P_T2_CSI_B_14 IO_L15N_T2_DQS_DOUT_CSO_B_14 IO_L15P_T2_DQS_RDWR_B_14 IO_L14N_T2_SRCC_14 IO_L14P_T2_SRCC_14 IO_L13N_T2_MRCC_14 IO_L13P_T2_MRCC_14 IO_L12N_T1_MRCC_14 IO_L12P_T1_MRCC_14 IO_L11N_T1_SRCC_14 IO_L11P_T1_SRCC_14 IO_L10N_T1_D15_14 IO_L10P_T1_D14_14 IO_L9N_T1_DQS_D13_14 IO_L9P_T1_DQS_14 IO_L8N_T1_D12_14 IO_L8P_T1_D11_14 IO_L7N_T1_D10_14 IO_L7P_T1_D09_14 IO_L6N_T0_D08_VREF_14 IO_L6P_T0_FCS_B_14 IO_L5N_T0_D07_14 IO_L5P_T0_D06_14 IO_L4N_T0_D05_14 IO_L4P_T0_D04_14 IO_L3N_T0_DQS_EMCCLK_14 IO_L3P_T0_DQS_PUDC_B_14 IO_L2N_T0_D03_14 IO_L2P_T0_D02_14 IO_L1N_T0_D01_DIN_14 IO_L1P_T0_D00_MOSI_14 IO_0_14

1V8 bank

XC7A15T-1CSG325

P3V3F HW ID an be read by toggling IO directions

0 R250 HW_ID0 10k R255 ADC1_SCLK
0 R251 HW_ID1 10k R256 ADC2_SCLK
0 R252 HW_ID2 10k R257 DAC1_SPI_SCLK
0 R253 HW_ID3 10k R258 DAC2_SPI_SCLK

10k R254 10k R173 10k R172 10k R174

RTM_FPGA_LVDS2_N RTM_FPGA_LVDS2_P RTM_FPGA_USR_IO_N RTM_FPGA_USR_IO_P RTM_FPGA_LVDS1_N RTM_FPGA_LVDS1_P CDR_CLK_CLEAN2_N CDR_CLK_CLEAN2_P RTM_MASTER_AUX_CLK_N RTM_MASTER_AUX_CLK_P DAC_CLK_SRC_SEL_1V8 REF_CLK_SRC_EXT_SEL_1V8

REC_CLOCK_N REC_CLOCK_P

RESETn 200 R259 REF_CLK_SRC_SEL_1V8 REF_LO_CLK_SEL_1V8 DAC2_CFG DAC_RESETn

FPGA_CFG_DIN R46 200

DIO0 DIO1 DIO2 DIO3 DIO4 DIO5 DIO6 DIO7

P1V8F J72 MTLW-106-07-L-D-250

IC35 P1V8F OE A1 A2 A3 A4 VCCA GND B1 B2 B3 B4 VCCB P3V3F TXB0304RUTR =Device

REF_CLK_SRC_SEL_1V8 REF_LO_CLK_SEL_1V8 DAC_CLK_SRC_SEL_1V8 REF_CLK_SRC_EXT_SEL_1V8

REF_CLK_SRC_SEL REF_LO_CLK_SEL DAC_CLK_SRC_SEL REF_CLK_SRC_EXT_SEL

P1V8F P3V3F 100nF C350 100nF C351

ARTIQ

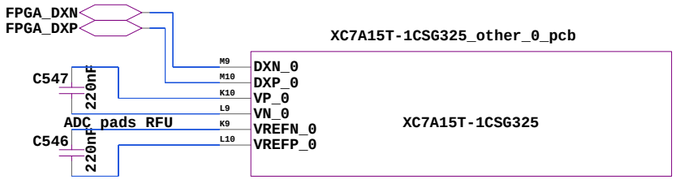
ARTIQ Sinara

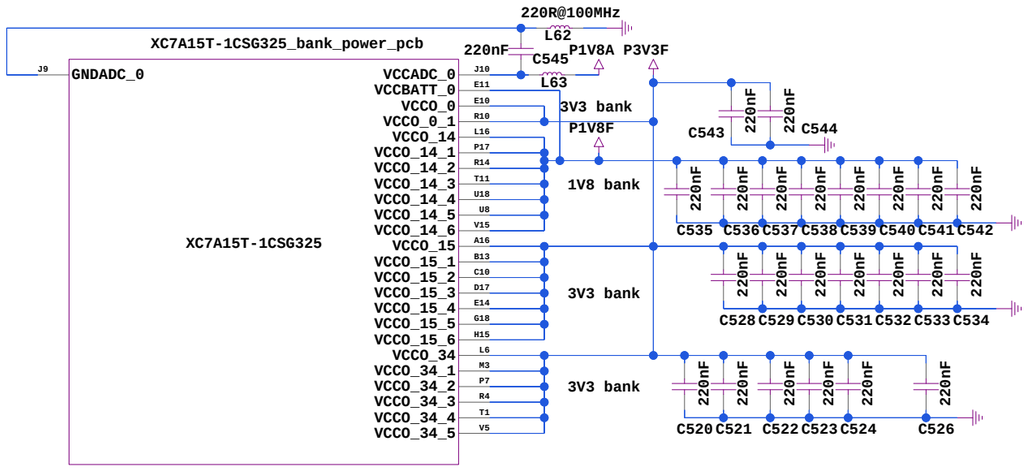
TITLE

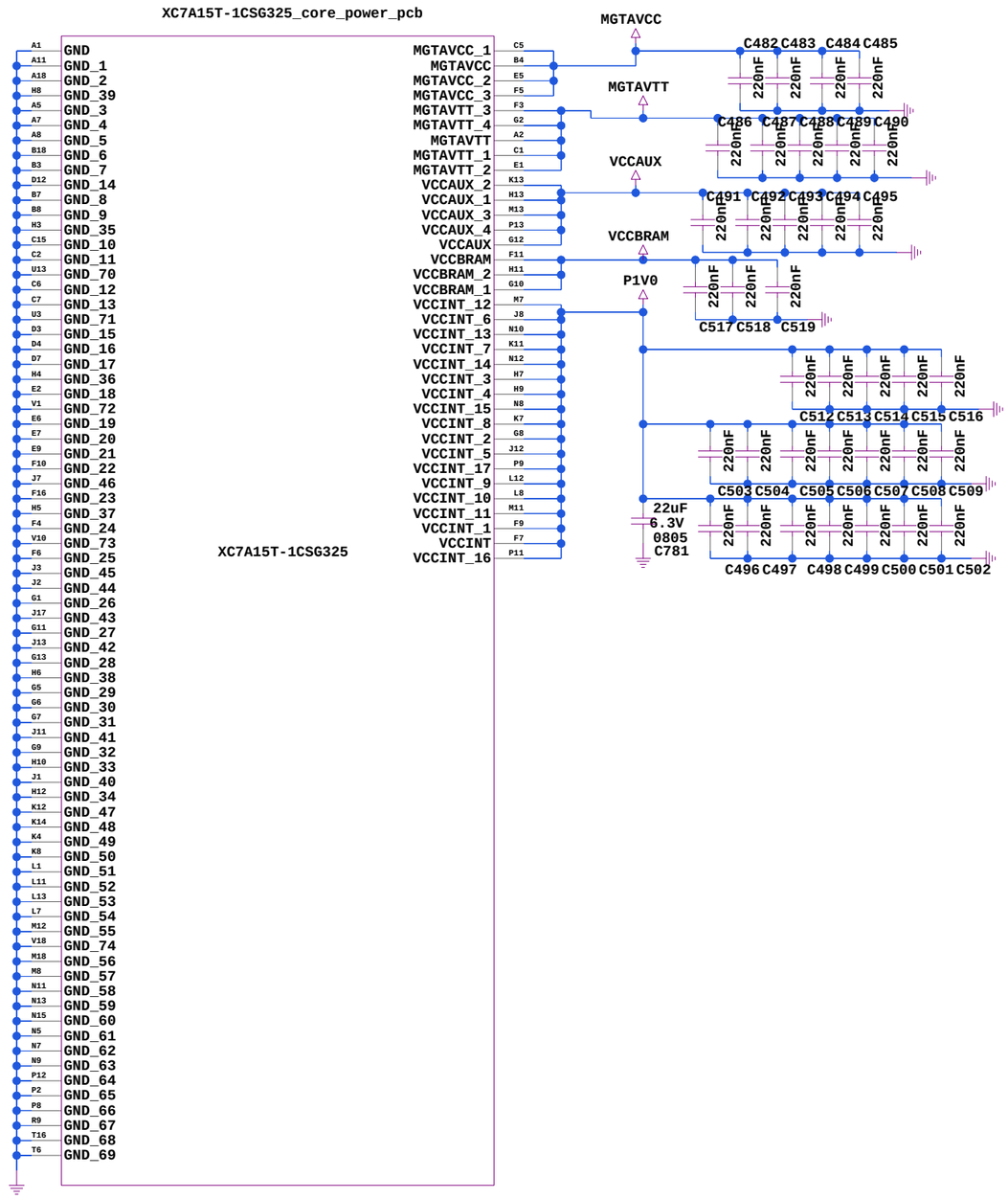
FPGA_7A15T

SIZE	DWG NO	REV
A2	1	v0.95

DRAWN BY	SHEET	OF	
G.K.	9	23	01/12/2016:18:22





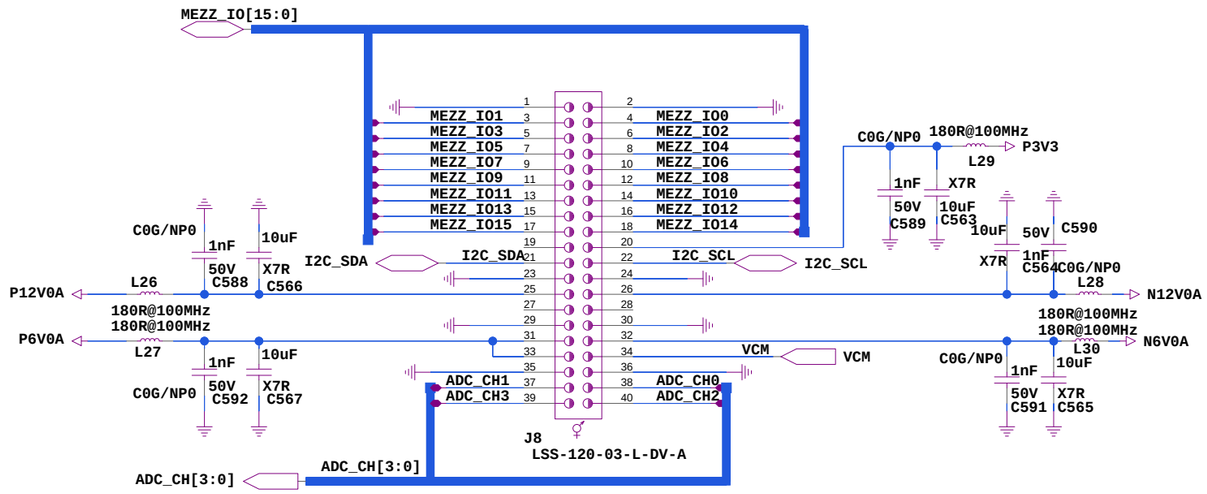


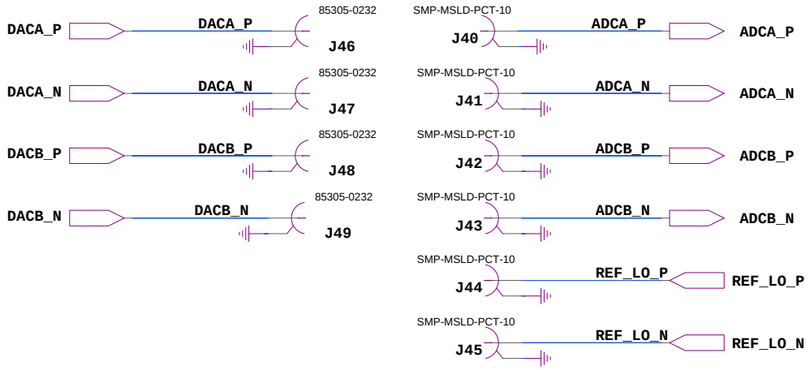
ARTIQ Sinara

TITLE: FPGA_7A15T_POWER

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	10	23	01/12/2016:18:22





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ

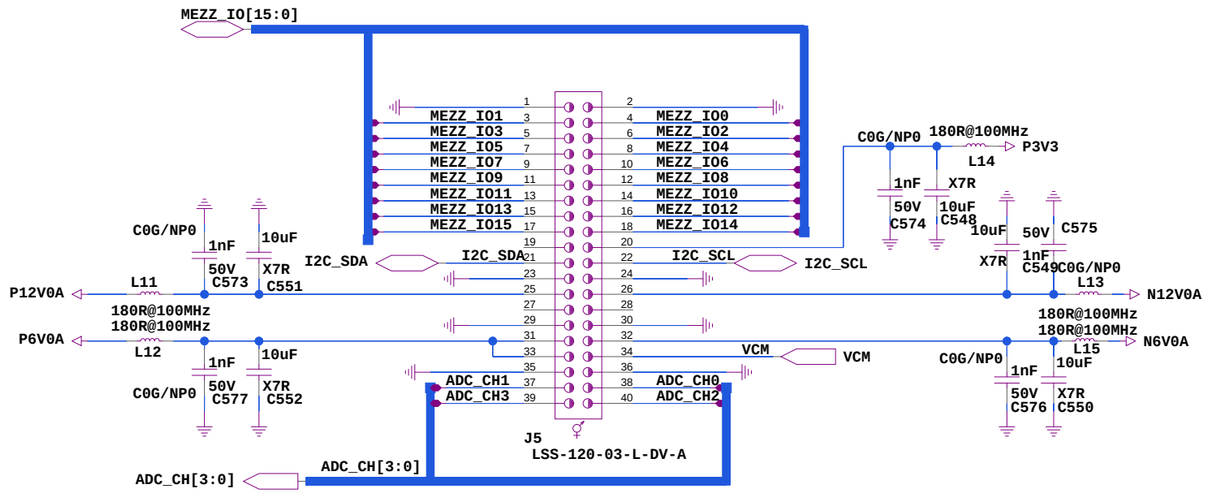
ADC_DAC_AFE_Mezzanine

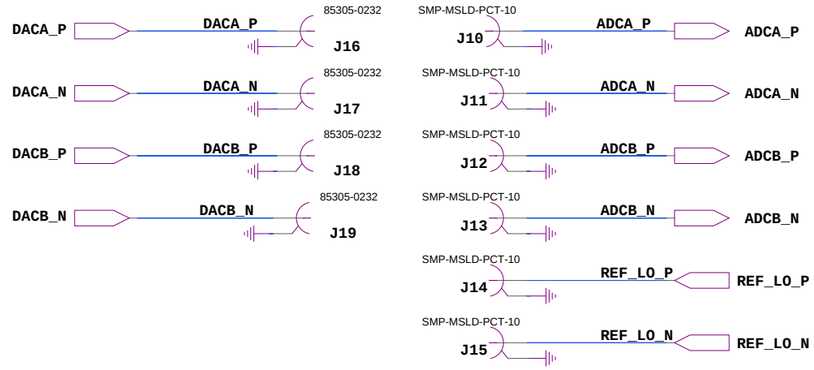
TITLE

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	11	23	03/12/2016:15:08





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ

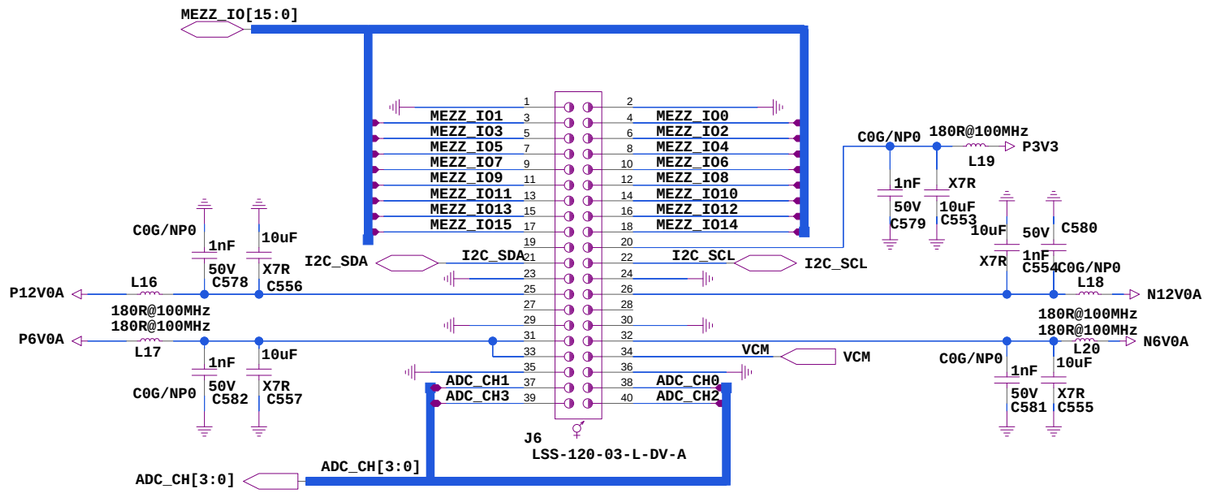
TITLE

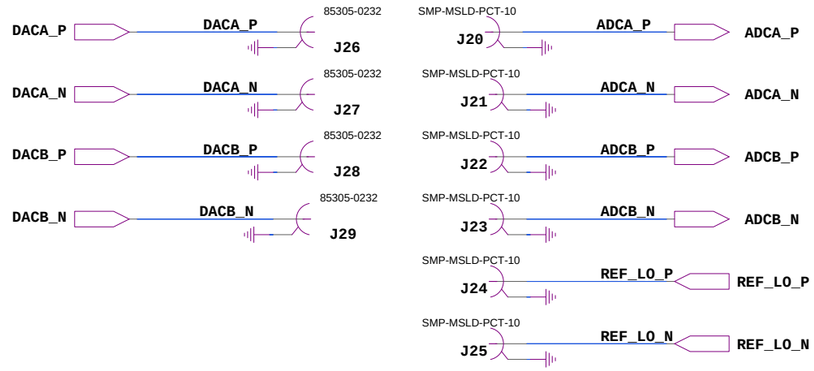
ADC_DAC_AFE_Mezzanine

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	12	23	03/12/2016:15:08





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ

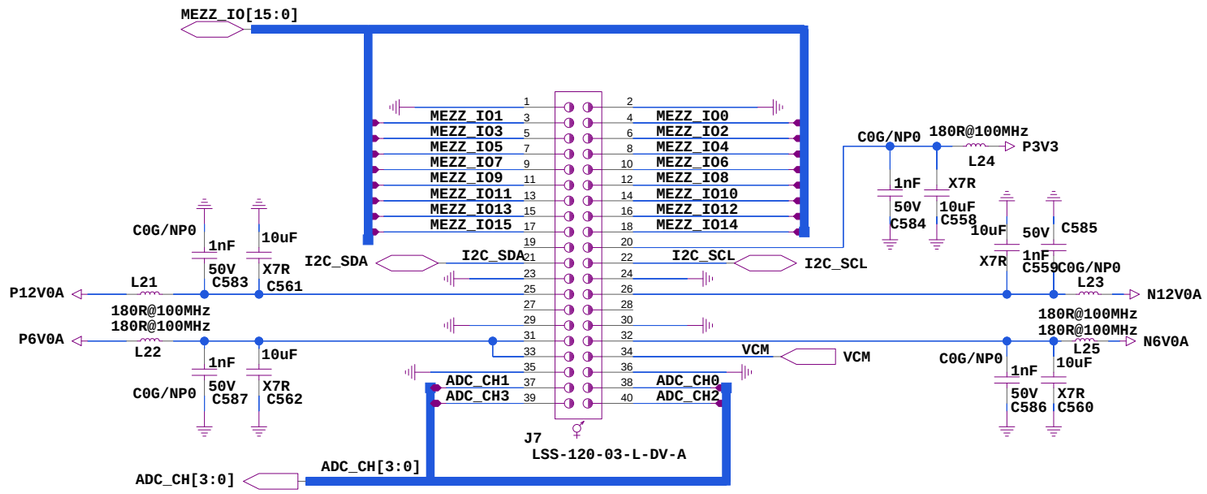
ADC_DAC_AFE_Mezzanine

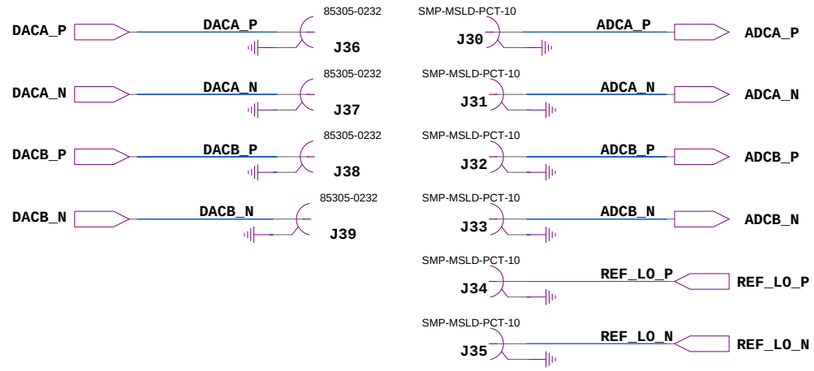
TITLE

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	13	23	03/12/2016:15:08





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ

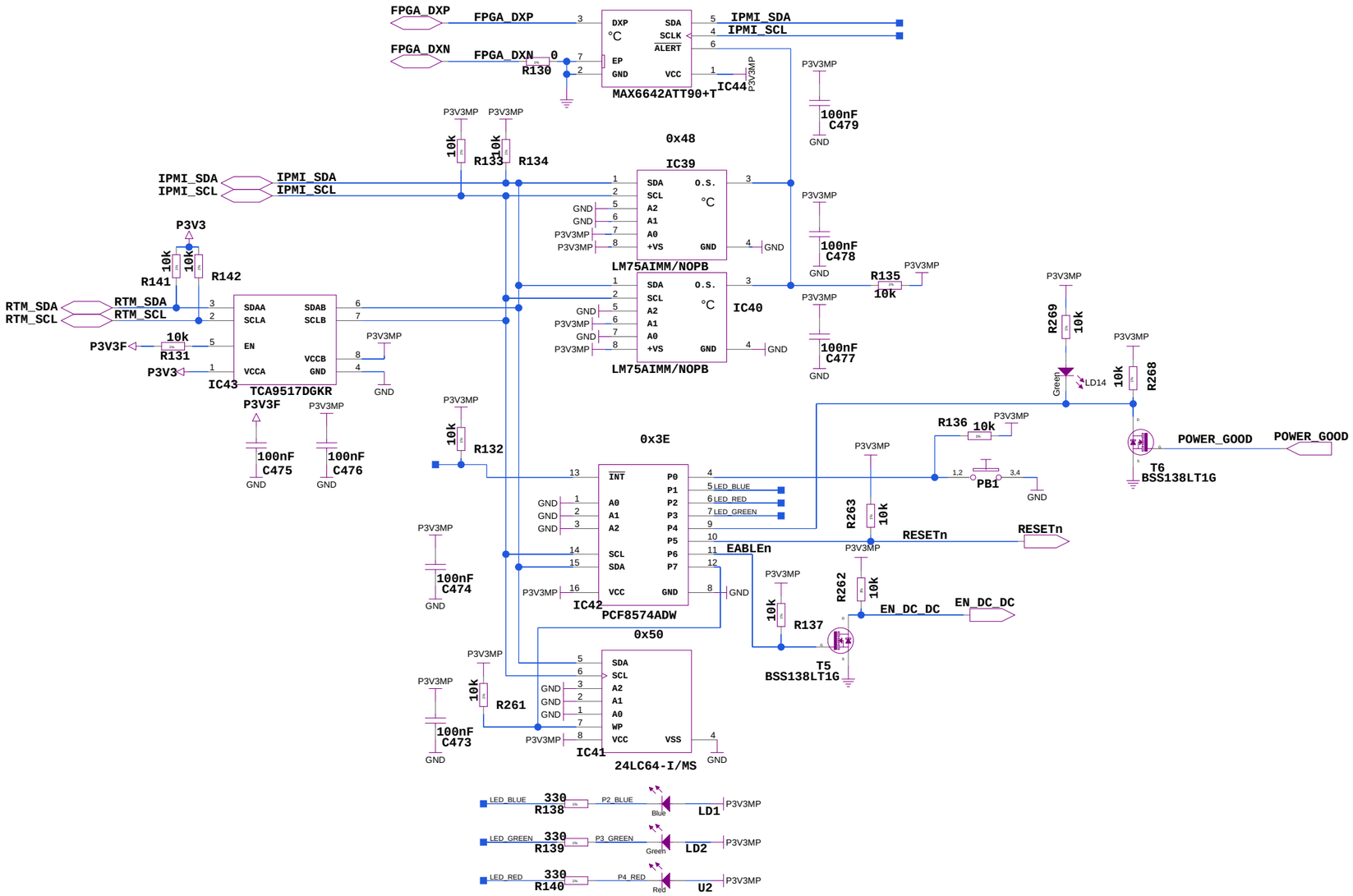
ADC_DAC_AFE_Mezzanine

TITLE

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	14	23	03/12/2016:15:08



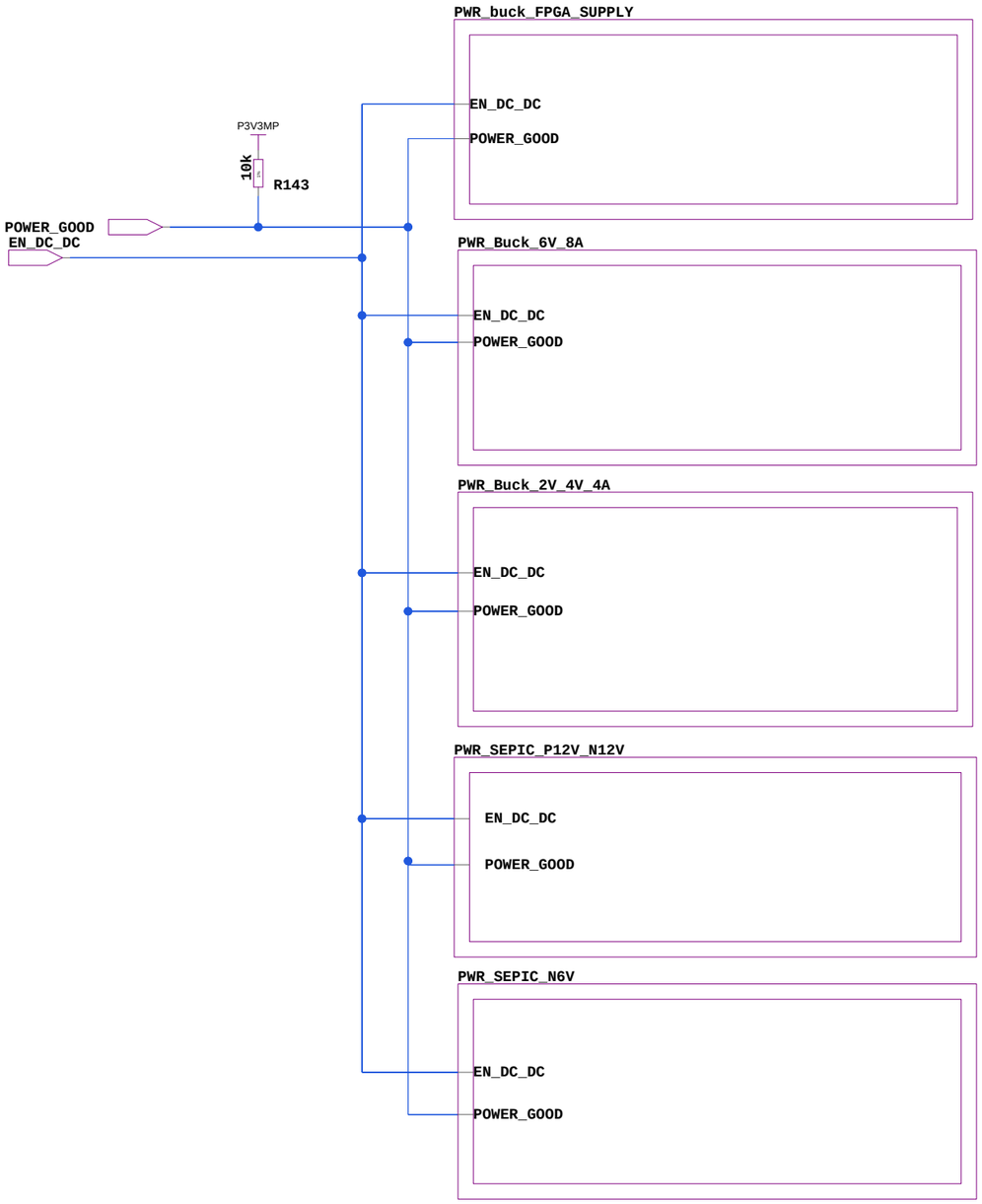
check addresses

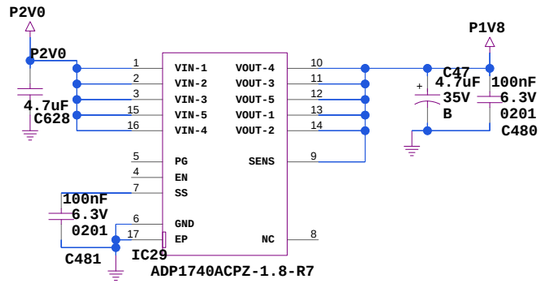
ARTIQ Sinara

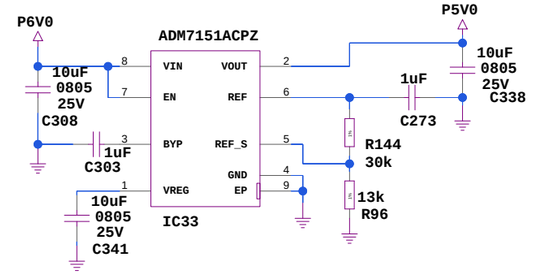
TITLE: RTM_IPMI

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	15	23	01/12/2016:18:22







RTM modules power requirements

+12VDC @ 1A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 250 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 8 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 750 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

RTM power requirements

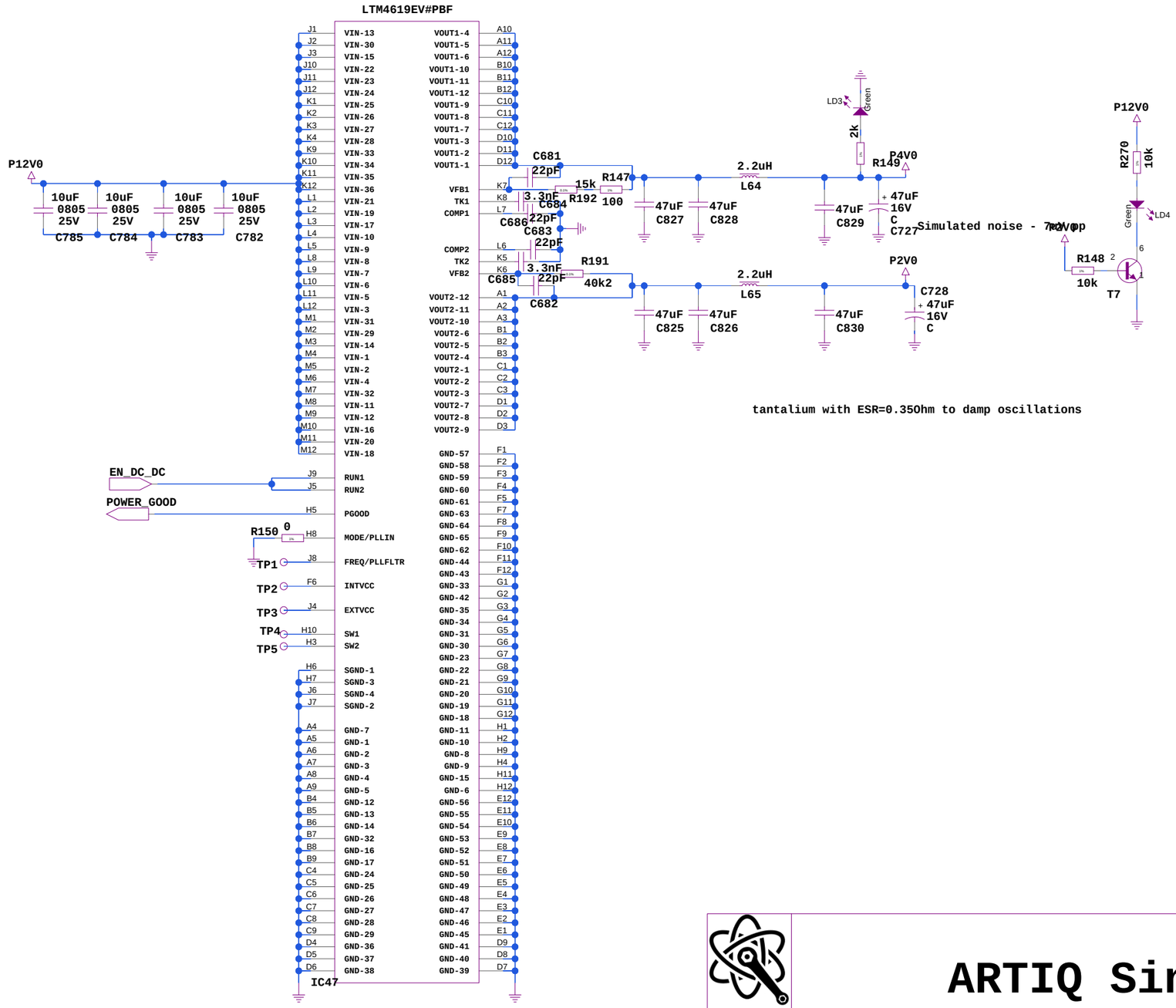
+4VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz
+2VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ Sinara

TITLE: RTM_POWER_SUPPLY

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	16	23	01/12/2016:18:22

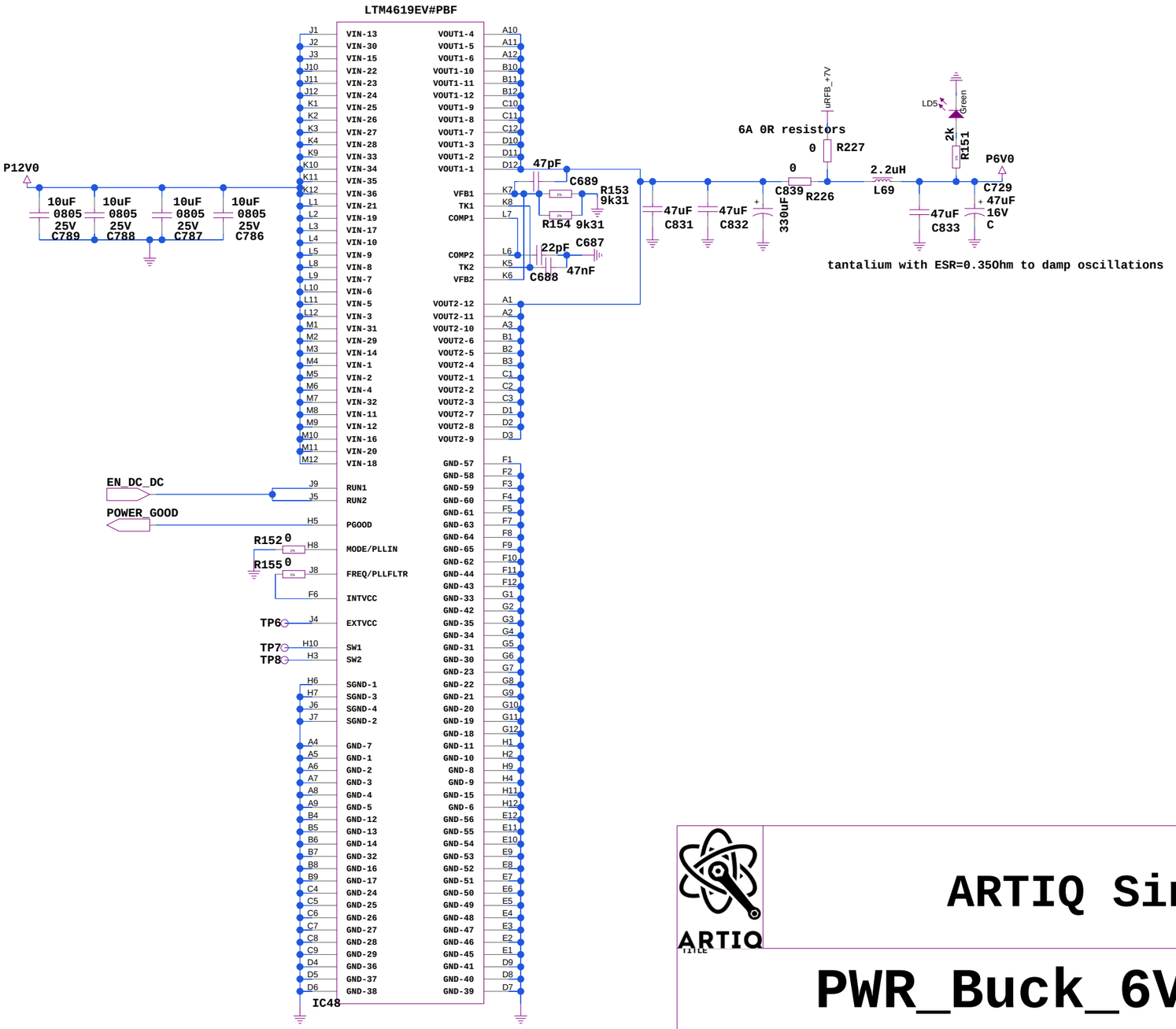


ARTIQ Sinara

TITLE: PWR_Buck_2V_4V_4A

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET			
G.K.	17	of	23	01/12/2016:18:22



ARTIQ

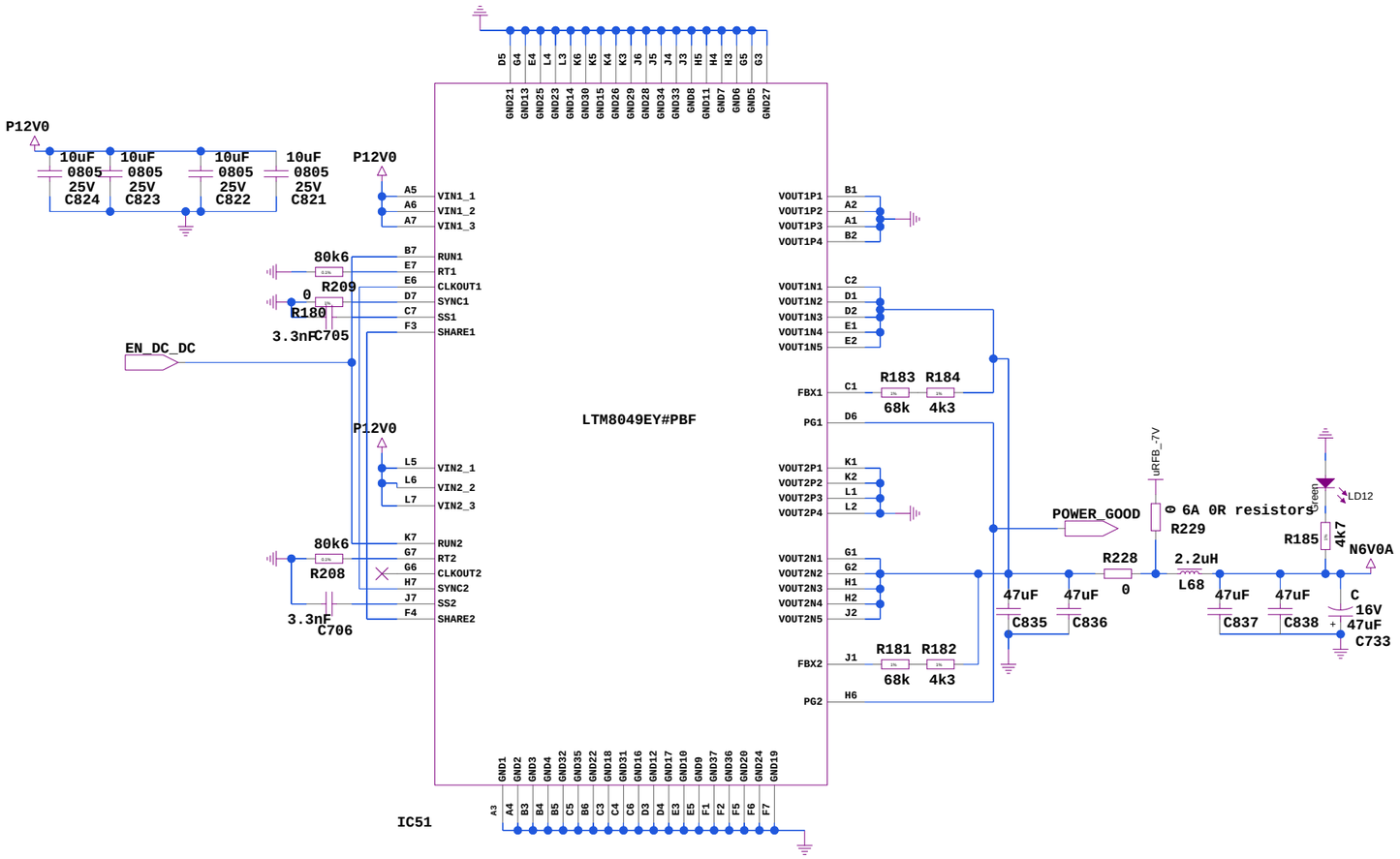
ARTIQ Sinara

TITLE

PWR_Buck_6V_8A

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	18	23	01/12/2016:18:22

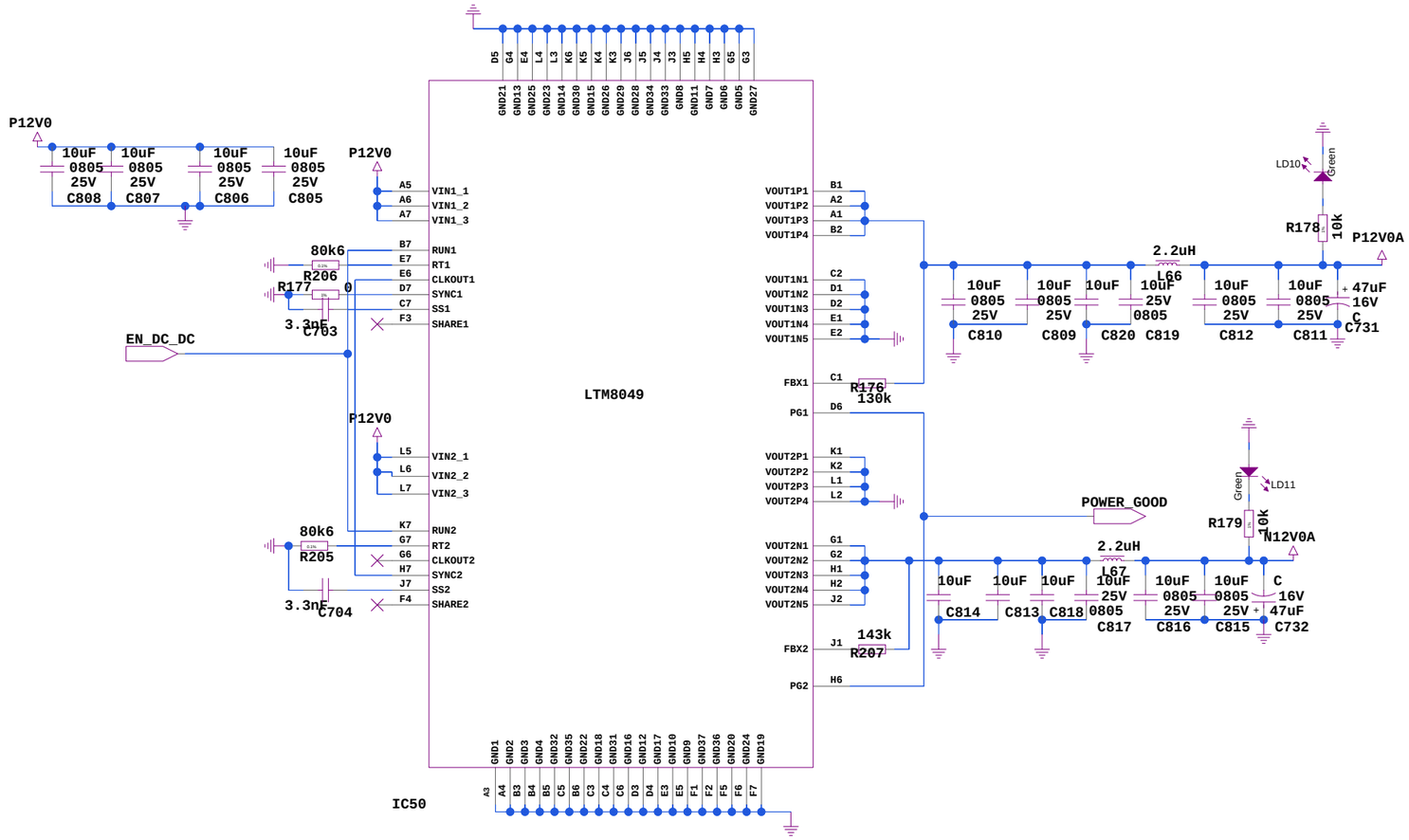


ARTIQ Sinara

TITLE: PWR_SEPIC_N6V

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	19	23	01/12/2016:18:22

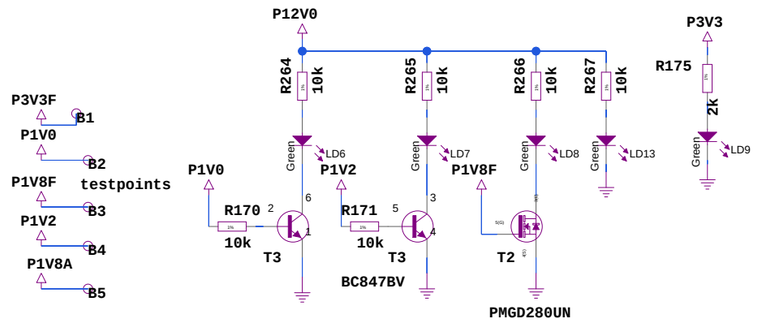


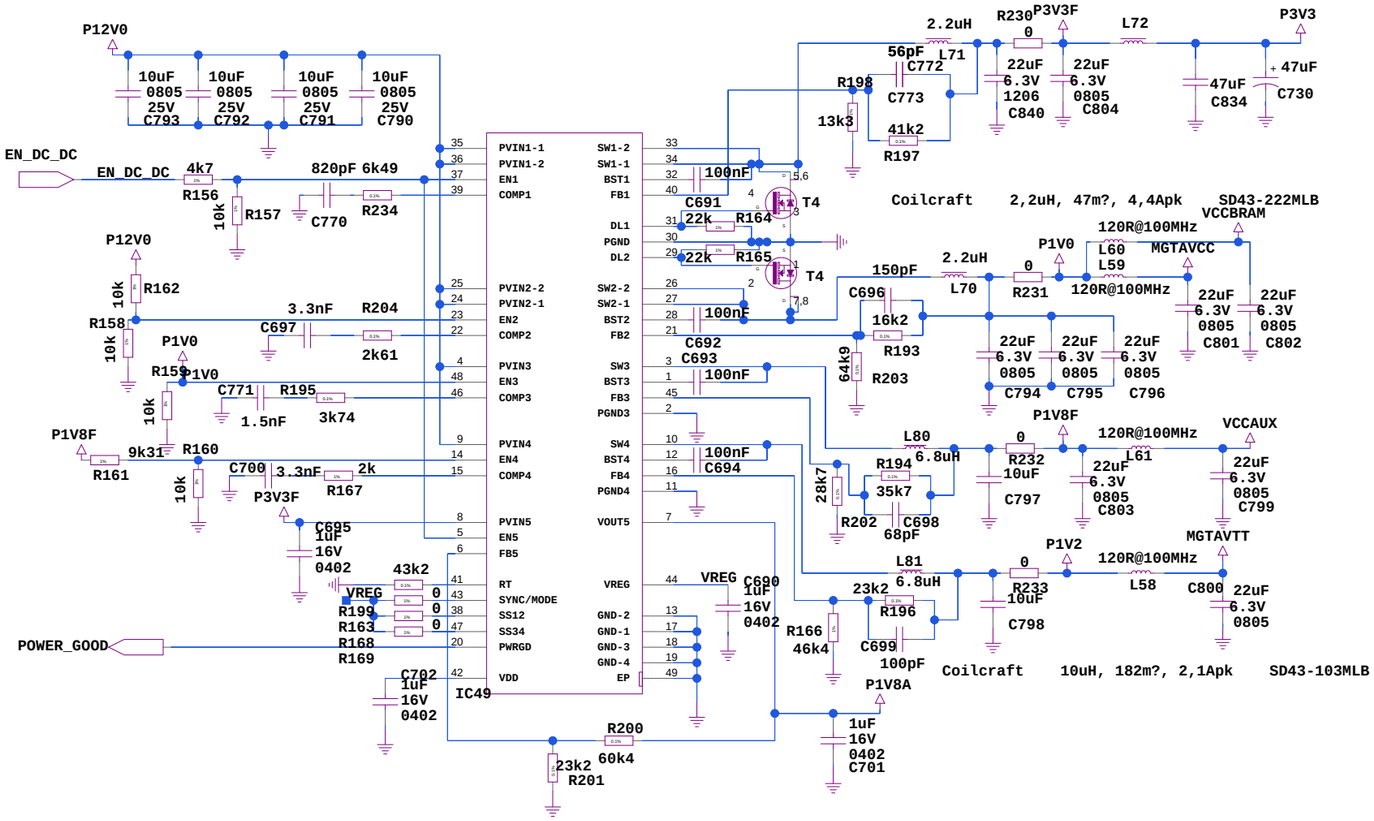
ARTIQ Sinara

PWR_SEPIC_P12V_N12V

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	20	23	01/12/2016:18:22



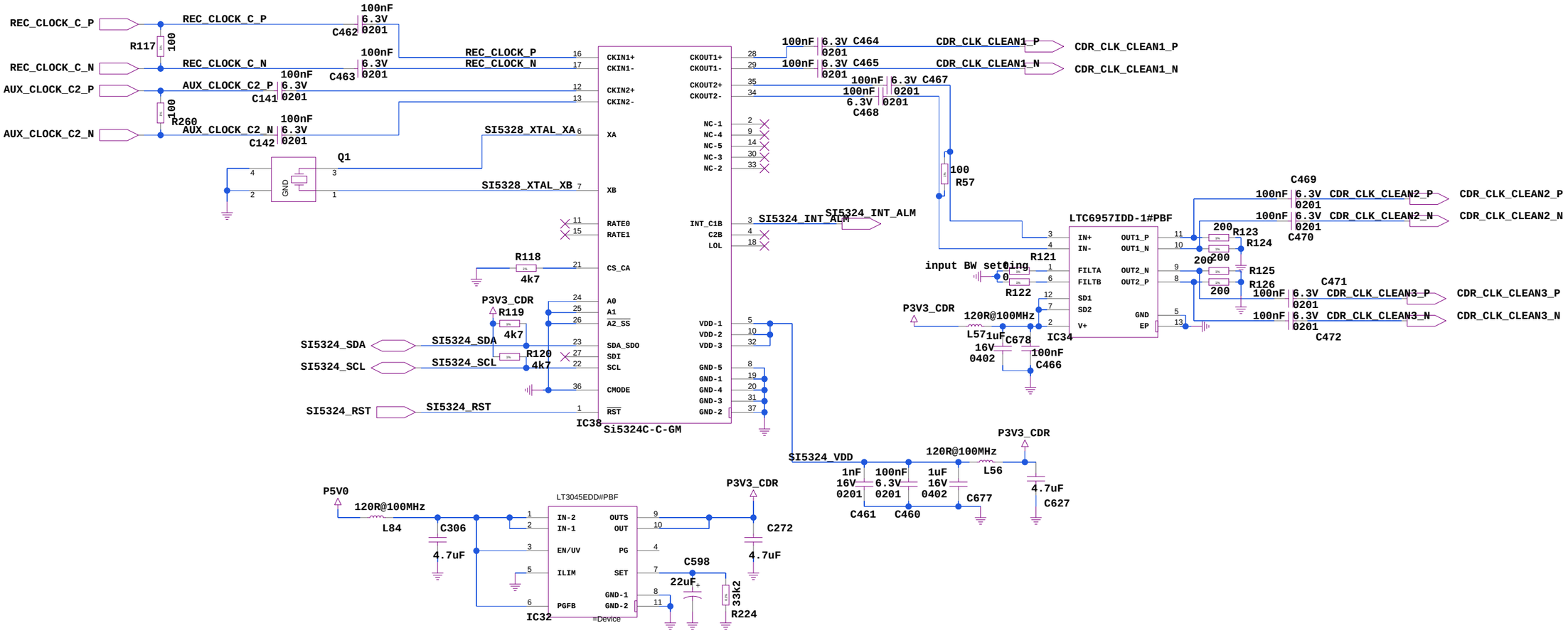


ARTIQ Sinara

TITLE: PWR_buck_FPGA_SUPPLY

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	21	23	01/12/2016:18:22



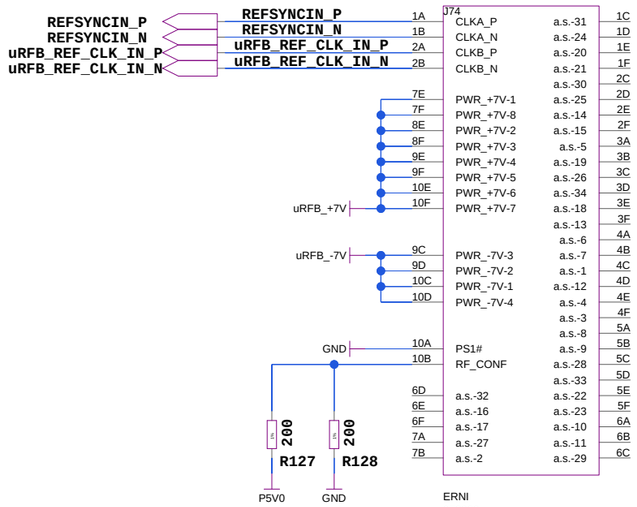
ARTIQ Sinara

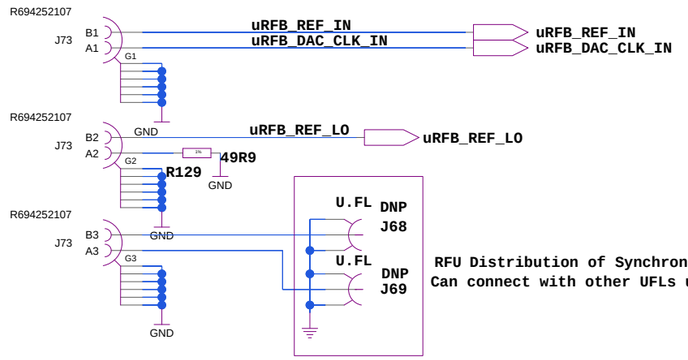
TITLE

SI5324_CLK_RECOVERY

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	22	23	03/12/2016:13:42





RFU Distribution of Synchronisation signals.
Can connect with other UFLs using jumper cables

uRFB_Connectors

TITLE

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	23	23	03/12/2016:13:55