Class D1

Interfaces with Sayma_AMC
Impedance: 100Ohm diff
gigabit interfaces: CML
other diff lines: LVDS
control signals: 3.3V LVCMOS

RFU LVDS1 Not used RX ports of GTX - left for compatibility reasons

RFU LVDS2

Not used RX ports of GTX

J1 — RTM_FPGA_GTP_Tx0_N/P, RTM_FPGA_GTP_Tx1_N/P, RTM_FPGA_GTP_Rx0_N/P, RTM_FPGA_GTP_Rx1_N/P, ADC1_SYNC_P/N, ADC2_SYNC_P/N, RTM_FPGA_USR_IO_N/P, AMC_MASTER_AUX_CLK_N/P, P12V0

J1 — SYNCOUT20_N/P, IPMI_SCL, IPMI_SDA, P3V3MP

J1 — GTP10TX_N/P, GTP11TX_N/P, GTP12TX_N/P, GTP13TX_N/P, GTP14TX_N/P, GTP15TX_N/P, SYNCOUT10_N/P, TMS, TDI, TDO, TCK

J2 — FPGA_CFG_DIN, FPGA_CFG_CCLK, FPGA_CFG_PROGRAM_B, FPGA_CFG_DONE, FPGA_CFG_INIT_B, USR_UART_N/P, RTM_FPGA_LVDS1_N/P, GTP_CLK2_IN_N/P, RTM_FPGA_LVDS2_N/P, FPGA_ADC_SYSREF_N/P, FPGA_DAC_SYSREF_N/P, GTP_CLK1_IN_N/P

J2 — GTP0RX_N/P, GTP1RX_N/P, GTP2RX_N/P, GTP3RX_N/P, GTP4RX_N/P, GTP5RX_N/P, GTP6RX_N/P, GTP7RX_N/P

J2 — GTP0TX_N/P, GTP1TX_N/P, GTP2TX_N/P, GTP3TX_N/P, GTP4TX_N/P, GTP5TX_N/P, GTP6TX_N/P, GTP7TX_N/P, GTP8TX_N/P, GTP9TX_N/P

J3 — 1M R309, GND

I2C switch footprint is compatible with MAX7358 which has interesting anti-lock capabilities

Lack of FPGA power resets the switch

IC1 TCA9548ARGER — MEZ_SDA1/SCL1, MEZ_SDA2/SCL2, MEZ_SDA3/SCL3, MEZ_SDA4/SCL4, CLK_MEZ_SDA/SCL, SI5324_SDA/SCL, TMP_SENS_SDA/SCL, SDA_EXAR, SCL_EXAR, RESET

IC43 TCA9548ARGER — RTM_FPGA_SDA, RTM_FPGA_SCL, RESET

ESDSTRIP1, ESDSTRIP2

IC56 ADT7420UCPZ-R2 — TMP_SENS_SDA/SCL

IC57 ADT7420UCPZ-R2 — TMP_SENS_SDA/SCL

CAL_ADC — ADC_CH[16:1], CAL_ADC_CTRL

Mezzanine_connectors1 — DAC1 (DAC_SYSREF_P/N, DAC_CLK_P/N, SERDIN0_N/P, SERDIN1_N/P, SERDIN2_N/P, SERDIN3_N/P, SERDIN4_N/P, SERDIN5_N/P, SERDIN6_N/P, SERDIN7_N/P, DAC_CFG), DAC_OUT1_P/N, DAC_OUT2_P/N, DAC_OUT3_P/N, DAC_OUT4_P/N, REF1_LO_P, REF2_LO_P, ADC_CH[16:13], ADC_CH[4:1], DAC1_CFG, SYNCOUT10_P/N, MEZZ1_IO[15:0], MEZZ2_IO[15:0], I2C_SDA, I2C_SCL, MEZ_SDA4, MEZ_SCL4, MEZ_SDA1, MEZ_SCL1, VCM1

Mezzanine_connectors2 — DAC1 (DAC_SYSREF_P/N, DAC_CLK_P/N, SERDIN0_N/P, SERDIN1_N/P, SERDIN2_N/P, SERDIN3_N/P, SERDIN4_N/P, SERDIN5_N/P, SERDIN6_N/P, SERDIN7_N/P, DAC_CFG), DAC_OUT1_P/N, DAC_OUT2_P/N, DAC_OUT3_P/N, DAC_OUT4_P/N, REF1_LO_P, REF2_LO_P, ADC_CH[8:5], ADC_CH[4:1], DAC1_CFG, SYNCOUT10_P/N, MEZZ1_IO[15:0], MEZZ2_IO[15:0], I2C_SDA, I2C_SCL, MEZ_SDA1, MEZ_SCL1, VCM1

Mezzanine_connectors3 — DAC2 (DAC_SYSREF_P/N, DAC_CLK_P/N, SERDIN0_N/P, SERDIN1_N/P, SERDIN2_N/P, SERDIN3_N/P, SERDIN4_N/P, SERDIN5_N/P, SERDIN6_N/P, SERDIN7_N/P, DAC_CFG), DAC_OUT5_P/N, DAC_OUT6_P/N, DAC_OUT7_P/N, DAC_OUT8_P/N, REF3_LO_P, REF4_LO_P, ADC_CH[8:5], ADC_CH[12:9], DAC2_CFG, SYNCOUT20_P/N, MEZZ3_IO[15:0], MEZZ4_IO[15:0], I2C_SDA, I2C_SCL, MEZ_SDA2, MEZ_SCL2, MEZ_SDA3, MEZ_SCL3, VCM2

Mezzanine_connectors4 — DAC2 (DAC_SYSREF_P/N, DAC_CLK_P/N, SERDIN0_N/P, SERDIN1_N/P, SERDIN2_N/P, SERDIN3_N/P, SERDIN4_N/P, SERDIN5_N/P, SERDIN6_N/P, SERDIN7_N/P, DAC_CFG), DAC_OUT5_P/N, DAC_OUT6_P/N, DAC_OUT7_P/N, DAC_OUT8_P/N, REF3_LO_P, REF4_LO_P, ADC_CH[12:9], DAC2_CFG, SYNCOUT20_P/N, MEZZ3_IO[15:0], MEZZ4_IO[15:0], I2C_SDA, I2C_SCL, MEZ_SDA3, MEZ_SCL3, VCM2

P1V8, 30R@100MHz L1, C2 4.7uF 35V B, 100nF 6.3V, C48 0201, LM4140ACM-1.2/NOPB IC2, C1 4.7uF 35V B

ADC1 — ADC_CH1_P/N, ADC_IN1_P/N, ADC_IN2_P/N, ADC_IN3_P/N, ADC_IN4_P/N, VCM, ADC_DSYNC_P/N, ADC_CLK_P/N, ADC1_SYNC_P/N, ADC1_CLK_P/N, ADC1_SER_SYSREF_P/N, ADC_SER_SYSREF_P/N, ADC_SER_DOUT0_N/P, ADC_SER_DOUT1_N/P, ADC_SER_DOUT2_N/P, ADC_SER_DOUT3_N/P, ADC_CFG, VREF, ADC1_CFG

ADC2 — ADC_CH1_P/N, ADC_IN5_P/N, ADC_IN6_P/N, ADC_IN7_P/N, ADC_IN8_P/N, VCM, ADC_DSYNC_P/N, ADC_CLK_P/N, ADC2_SYNC_P/N, ADC2_CLK_P/N, ADC2_SER_SYSREF_P/N, ADC_SER_SYSREF_P/N, ADC_SER_DOUT0_N/P, ADC_SER_DOUT1_N/P, ADC_SER_DOUT2_N/P, ADC_SER_DOUT3_N/P, ADC_CFG, VREF, ADC2_CFG

GTP4RX_N/P, GTP5RX_N/P, GTP6RX_N/P, GTP7RX_N/P, ADC1_CFG, CDR_CLK_CLEAN2_P/N, CDR_CLK_CLEAN1_P/N, CLK_DIST_CFG, CLK_MEZZ_IO[15:0], CAL_ADC_CTRL, GTP0RX_N/P, GTP1RX_N/P, GTP2RX_N/P, GTP3RX_N/P, ADC2_CFG, SI5324_INT_ALM, SI5324_RST, REC_CLOCK_P/N

uRFB_Connectors — uRFB_REF_IN, uRFB_REF_CLK_IN_P/N, REFSYNCIN_P/N, uRFB_DAC_CLK_IN, uRFB_REF_LO

CLK_Mezzanine — CLK_MEZZ_IO[15:0], CLK_MEZ_SDA, CLK_MEZ_SCL, DAC_CLK_P/N, MEZ_CLK_IN_P/N, REF_LO_P/N, CDR_CLK_CLEAN3_P/N, EXT_100M_RF_IN, EXT_100M_RF_IN_GND

142-0761-801 SMA J4 — SMA ground loop isolation C347 10pF, 100k R307

CLK_DIST_CFG — FPGA_DAC_SYSREF_P/N, DAC1_SYSREF_P/N, DAC1_CLK_P/N, DAC1_SER_SYSREF_P/N, FPGA_ADC_SYSREF_P/N, DAC2_SYSREF_P/N, DAC2_CLK_P/N, DAC2_SER_SYSREF_P/N, GTP_CLK1_IN_N/P, RTM_MASTER_AUX_CLK_N/P, GTP_CLK2_IN_N/P, AMC_MASTER_AUX_CLK_N/P, REF1_LO_P, REF2_LO_P, REF3_LO_P, REF4_LO_P, ADC1_CLK_P/N, ADC2_CLK_P/N, CDR_CLK_CLEAN3_P/N

RTM_POWER_SUPPLY — SDA_EXAR, SCL_EXAR, POWER_GOOD, EN_DC_DC

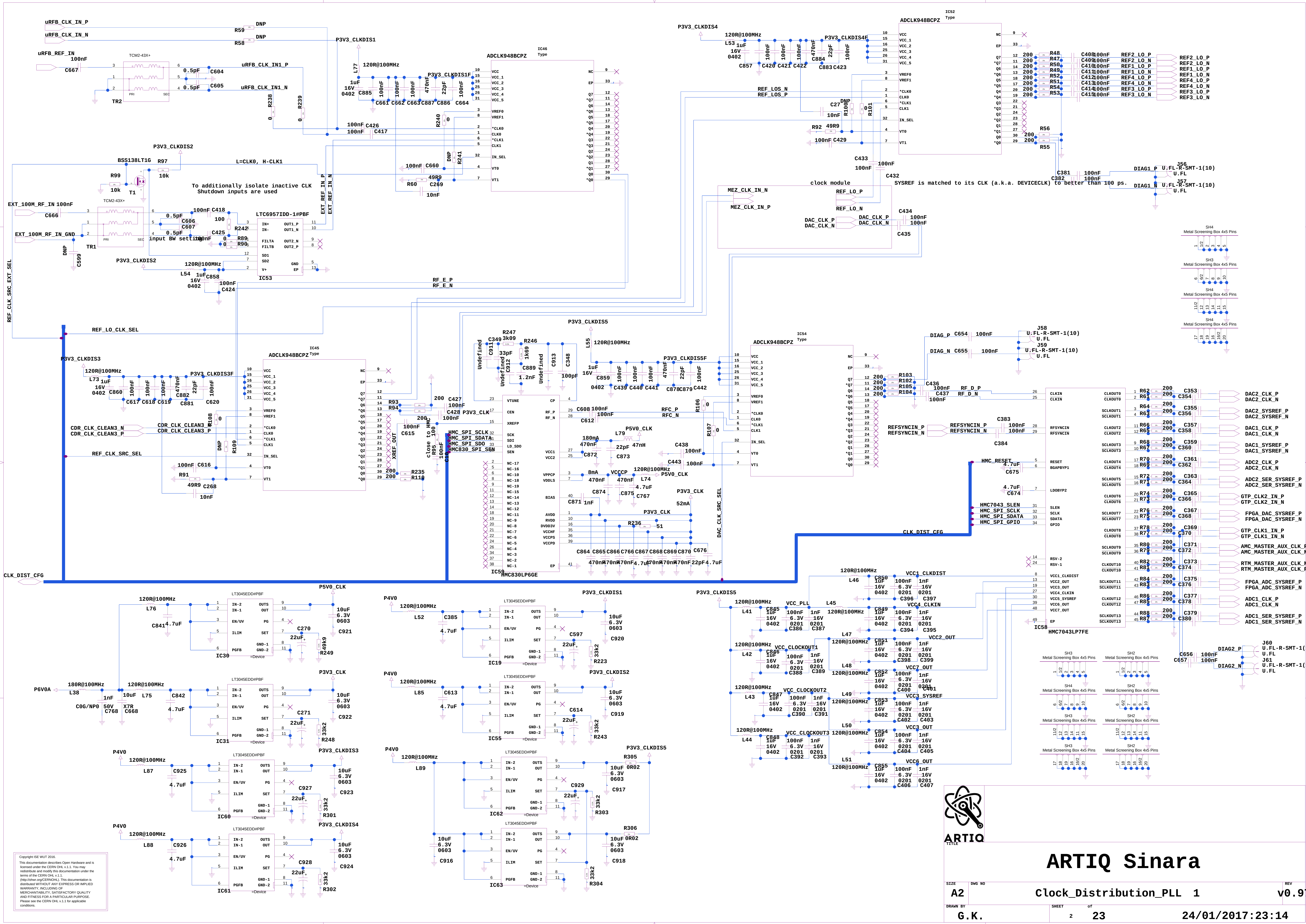
SI5324_INT_ALM — SI5324_SDA, SI5324_SCL, SI5324_RST, SI5324_I2C, SI5324_RST, Si5324 Clock recovery, REC_CLOCK_C_P, REC_CLOCK_C_N, CDR_CLK_CLEAN2_P/N, CDR_CLK_CLEAN1_P/N, CDR_CLK_CLEAN1_N, AUX_CLOCK_C2_P, AUX_CLOCK_C2_N, CDR_CLK_CLEAN3_P/N

J62 U.FL, optional CLK input J63

RTM_IPMI — EN_DC_DC, FPGA_DXP/N, POWER_GOOD, IPMI_SCL, IPMI_SDA, RESETn

FPGA_7A15T — FPGA_DXP/N, TMS, TDI, TDO, TCK, RTM_FPGA_SDA, RTM_FPGA_SCL, USR_UART_N/P, FPGA_CFG_DIN, FPGA_CFG_CCLK, FPGA_CFG_PROGRAM_B, FPGA_CFG_DONE, FPGA_CFG_INIT_B, MEZZ1_IO[15:0], MEZZ2_IO[15:0], MEZZ3_IO[15:0], MEZZ4_IO[15:0], RTM_MASTER_AUX_CLK_N/P, GTP_CLK2_IN_N/P, RTM_FPGA_USR_IO_N/P, CAL_ADC_CTRL, CLK_DIST_CFG, RTM_FPGA_GTP_Tx0_N/P, RTM_FPGA_GTP_Tx1_N/P, CDR_CLK_CLEAN2_P/N, RESETn, CDR_CLK_CLEAN1_P/N, RTM_FPGA_GTP_Rx0_N/P, RTM_FPGA_GTP_Rx1_N/P, SI5324_INT_ALM, SI5324_RST, REC_CLOCK_P/N, RTM_FPGA_LVDS1_N/P, RTM_FPGA_LVDS2_N/P

TITLE	ARTIQ Sinara Sayma_RTM
SIZE	A2
DWG NO	1
REV	v0.97
DRAWN BY	G.K.
SHEET	1 of 23
	24/01/2017:23:13



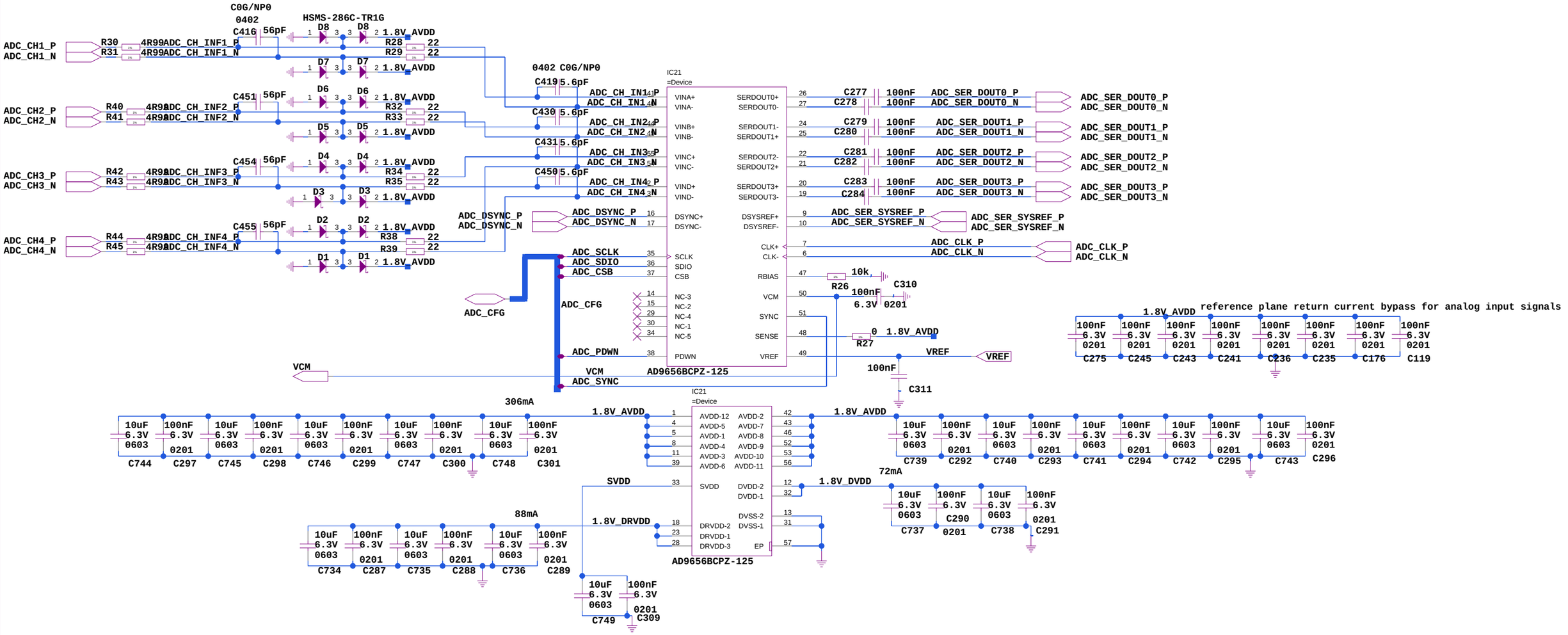
ARTIQ

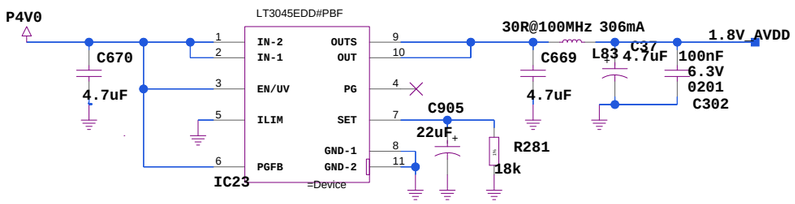
TITLE

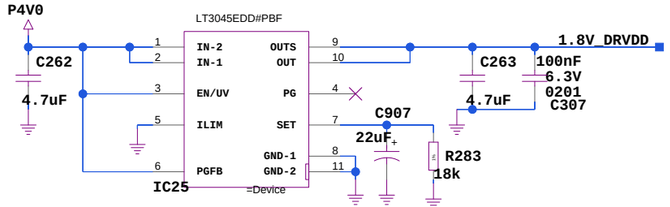
ARTIQ Sinara

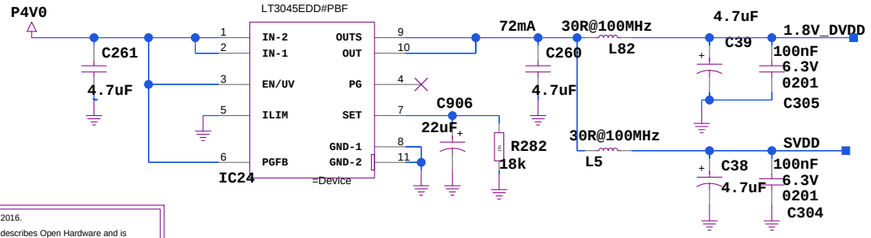
SIZE	DWG NO	REV
A2	Clock_Distribution_PLL 1	v0.97

DRAWN BY	SHEET	of	
G.K.	2	23	24/01/2017:23:14









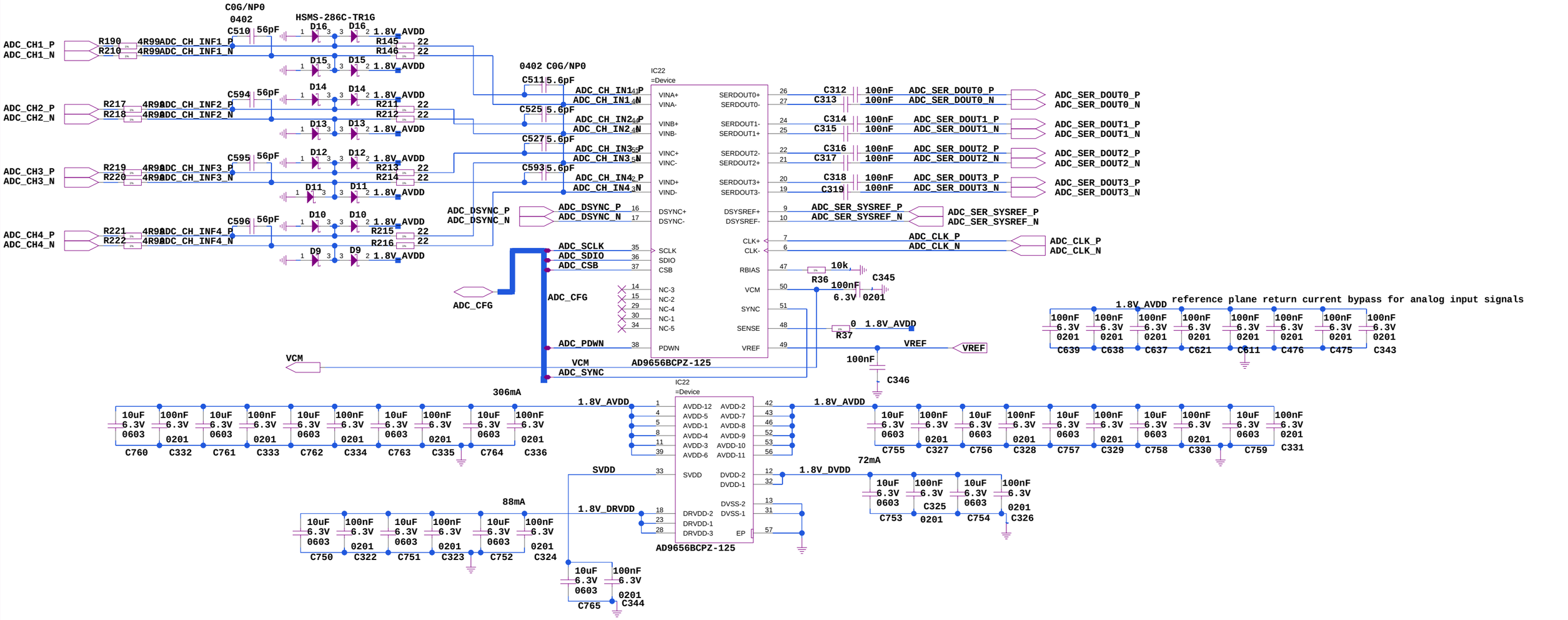
ARTIQ

ADC_JESD204B

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET			
G.K.	3	of	23	24/01/2017:23:13



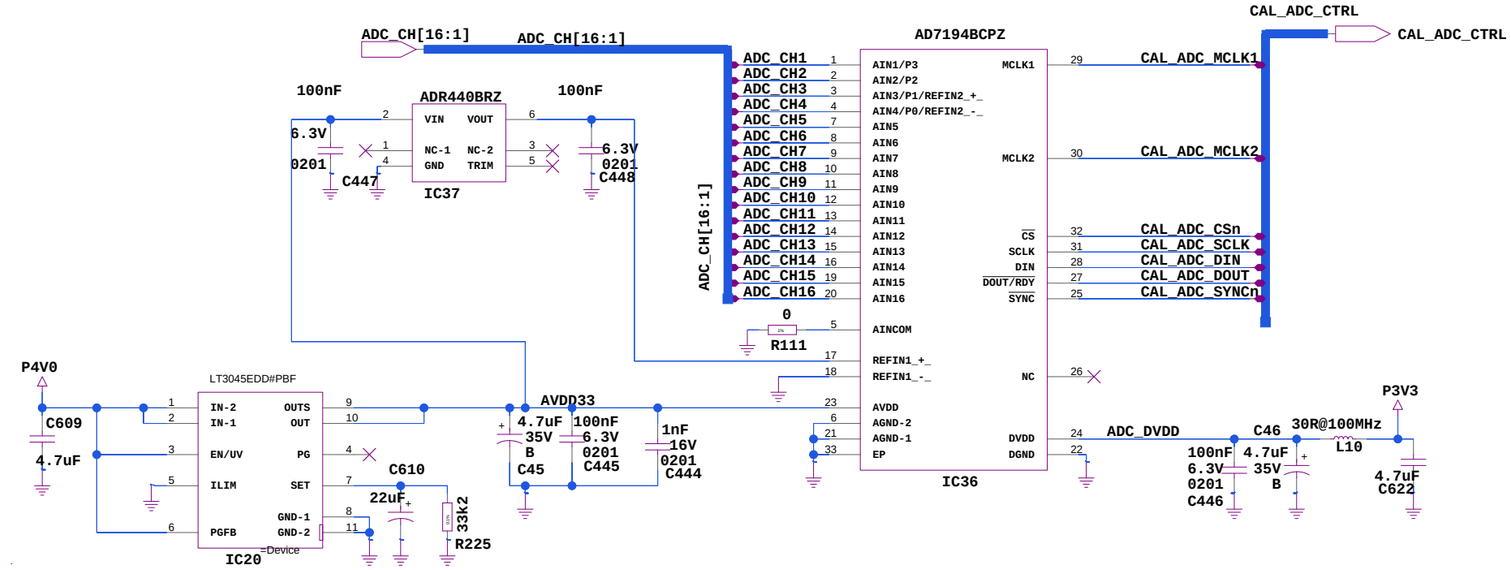
ARTIQ

ADC_JESD204B

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET		
G.K.	4	of 23	24/01/2017:23:13



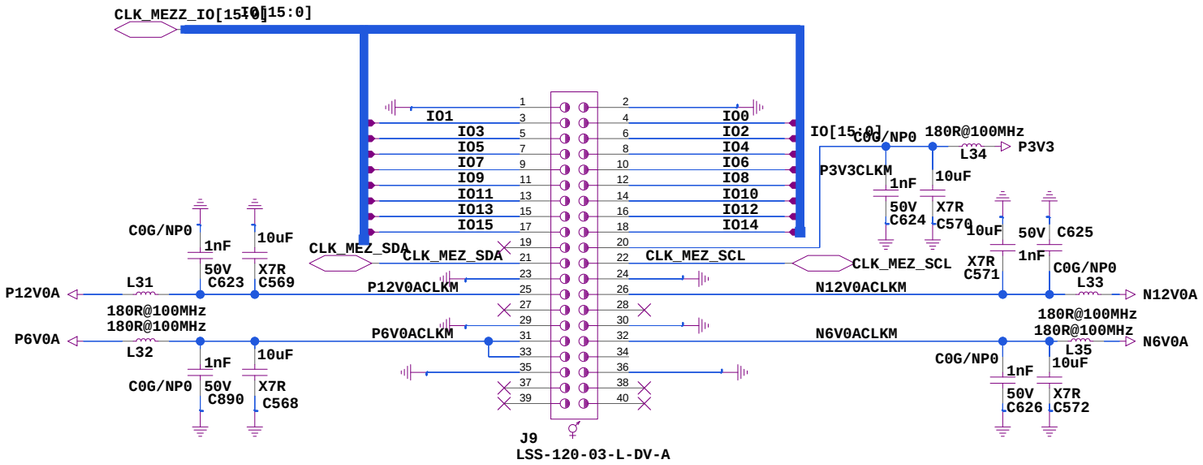
ARTIQ Sinara

TITLE

CAL_ADC

SIZE	DWG NO	REV
A3	1	v0.97

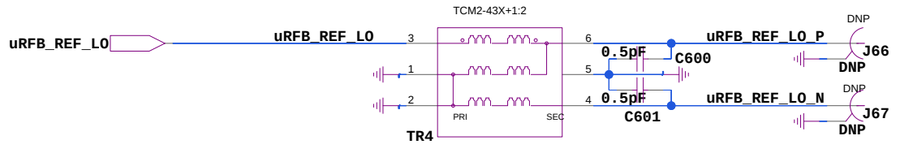
DRAWN BY	SHEET			
G.K.	5	of	23	24/01/2017:23:14



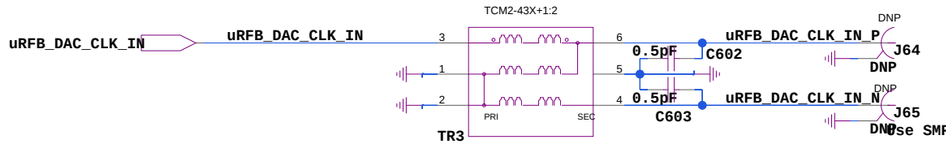
Use SMP-SMP jumper cables to

connect uRFB signal to CLK mezzanine LO outputs

optional RF path for LO signal distribution over RF backplane

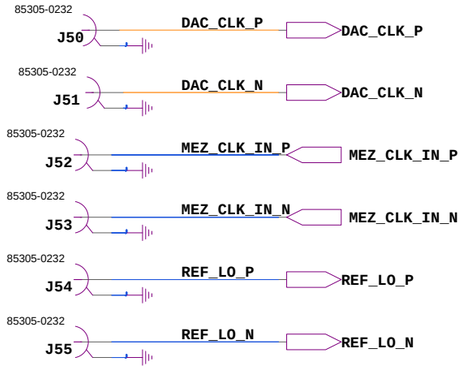


optional RF path for DAC clock distribution over RF backplane



Use SMP-SMP jumper cables to

connect uRFB signal to CLK mezzanine DAC output



Interfaces with PCB_mezzanine_clock or PCB_mezzanine_clock_template
DAC_CLK : LVPECL
REF_LO: LVPECL
MEZ_CLK_IN - LVPECL
Impedance 100Ohm diff
Control signals: LVCMOS 3.3V
I2C signals: LVCMOS 3.3V
+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ Sinara

TITLE

CLK_Mezzanine

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	6	23	24/01/2017:23:14

IOVDD=3.3

SERDIN0_P SERDIN0_N SERDIN1_P SERDIN1_N SERDIN2_P SERDIN2_N SERDIN3_P SERDIN3_N SERDIN4_P SERDIN4_N SERDIN5_P SERDIN5_N SERDIN6_P SERDIN6_N SERDIN7_P SERDIN7_N

DAC_TXEN0 DAC_TXEN1

DAC_CLK_P DAC_CLK_N

DAC_SPI_SDO DAC_SPI_SDIO DAC_SPI_SCLK DAC_SPI_CSn

SIOVDD33 IOVDD

VTT: 1uF 16V 0402 C629; 100nF 6.3V 0201 C52; 100nF 6.3V 0201 C51; 100nF 6.3V 0201 C50

AVDD33: 100nF 6.3V 0201 C49; 100nF 6.3V 0201 C58; 100nF 6.3V 0201 C57; 1nF 16V 0201 C56; 1nF 16V 0201 C55; 100nF 6.3V 0201 C53; 1nF 16V 0201 C54; 4.7uF 35V B C3

CVDD12: 100nF 6.3V 0201 C98; 100nF 6.3V 0201 C97; 1nF 16V 0201 C96; 1nF 16V 0201 C95; 100nF 6.3V 0201 C93; 1nF 16V 0201 C94; 4.7uF 35V B C6

DVDD12: 100nF 6.3V 0201 C108; 100nF 6.3V 0201 C107; 1nF 16V 0201 C106; 1nF 16V 0201 C105; 100nF 6.3V 0201 C103; 1nF 16V 0201 C104; 4.7uF 35V B C7

W2L16C473MAT1S: C59, C60, C61

IC3 AD9154BCPZ

OUT0_P OUT0_N OUT1_P OUT1_N OUT2_P OUT2_N OUT3_P OUT3_N

SYNCOUT0_P SYNCOUT0_N

PDP_OUT0 PDP_OUT1

SYSREF_P SYSREF_N

LDO_BYP1 LDO_BYP2

IRQ RESET

I120

DNC-1 DNC-2

PVDD12: 100nF 6.3V 0201 C68; 100nF 6.3V 0201 C67; 1nF 16V 0201 C66; 1nF 16V 0201 C65; 100nF 6.3V 0201 C63; 1nF 16V 0201 C64; 4.7uF 35V B C4; 47uF 16V C C708

SVDD12: 1nF 16V 0201 C91; 1nF 16V 0201 C92; 1nF 16V 0201 C81; 1nF 16V 0201 C80; 100nF 6.3V 0201 C78; 1nF 16V 0201 C79; 4.7uF 35V B C5; 47uF 16V C C709; 100nF 6.3V 0201 C86; 100nF 6.3V 0201 C87; 100nF 6.3V 0201 C88; 1nF 16V 0201 C89; 1nF 16V 0201 C90

SDVDD12: 100nF 6.3V 0201 C118; 1nF 16V 0201 C116; 1nF 16V 0201 C115; 1nF 16V 0201 C114; 4.7uF 35V B C8; C712 47uF 16V C

DAC_CFG

DAC_IRQn DAC_RESETn DAC_SPI_CSn DAC_SPI_SCLK DAC_SPI_SDO DAC_SPI_SDIO DAC_TXEN0 DAC_TXEN1

P4V0

IC11 LT3045EDD#PBF =Device: C157 4.7uF; C156 4.7uF; C897 22uF; R287 33k2; 30R@100MHz L3; 30R@100MHz L2; 185mA AVDD33: 100nF 6.3V 0201 C159; 11mA SIOVDD33: 100nF 6.3V 0201 C160

IC5 LT3045EDD#PBF =Device: P2V0; C145 4.7uF; C144 4.7uF; C891; 22uF; R289 13k; 174mA; PVDD12: 100nF 6.3V 0201 C15

IC7 LT3045EDD#PBF =Device: P2V0; C149 4.7uF; C148 4.7uF; C892; 22uF; R292 13k; 682mA; SVDD12: 100nF 6.3V 0201 C17

IC6 LT3045EDD#PBF =Device: P2V0; C147 4.7uF; C146 4.7uF; C893; 22uF; R290 13k; 442mA; DVDD12: 100nF 6.3V 0201 C16

IC8 LT3045EDD#PBF =Device: P2V0; C151 4.7uF; C150 4.7uF; C894; 22uF; R293 13k; SDVDD12: 100nF 6.3V 0201 C914

IC9 LT3045EDD#PBF =Device: P2V0; C153 4.7uF; C152 4.7uF; C895; 22uF; R294 13k; PLLVDD12: 100nF 6.3V 0201 C31

IC10 LT3045EDD#PBF =Device: P2V0; C155 4.7uF; C154 4.7uF; C896; 22uF; R291 13k; 397mA; CVDD12: 100nF 6.3V 0201 C32

PLLVDD12: 1nF 16V 0201 C125; 100nF 6.3V 0201 C123; 1nF 16V 0201 C124; 4.7uF 35V B C9; 47uF 16V C C713

SIOVDD33: 1nF 16V 0201 C128; 100nF 6.3V 0201 C126; 4.7uF 35V B C915; 47uF 16V C C715

IOVDD: 100nF 6.3V 0201 C132; 1nF 16V 0201 C130; 4.7uF 35V B C12; 47uF 16V C C716

P1V8 — L36 120R@100MHz — C632 1uF 16V 0402 — IOVDD: 1nF 16V 0201 C162

ARTIQ Sinara

TITLE: DAC_JESD204B

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	7	23	24/01/2017:23:13

IOVDD=3.3

SERDIN0_P SERDIN0_N SERDIN1_P SERDIN1_N SERDIN2_P SERDIN2_N SERDIN3_P SERDIN3_N SERDIN4_P SERDIN4_N SERDIN5_P SERDIN5_N SERDIN6_P SERDIN6_N SERDIN7_P SERDIN7_N

DAC_TXEN0 DAC_TXEN1

DAC_CLK_P DAC_CLK_N

DAC_SPI_SDO DAC_SPI_SDIO DAC_SPI_SCLK DAC_SPI_CSn

SIOVDD33 IOVDD

VTT: 1uF 16V 0402 C633; 100nF 6.3V 0201 C166; 100nF 6.3V 0201 C165; 100nF 6.3V 0201 C164; 100nF 6.3V 0201 C163

AVDD33: 100nF 6.3V 0201 C172; 100nF 6.3V 0201 C171; 1nF 16V 0201 C170; 1nF 16V 0201 C169; 100nF 6.3V 0201 C167; 1nF 16V 0201 C168; 4.7uF 35V B C20

CVDD12: 100nF 6.3V 0201 C212; 100nF 6.3V 0201 C211; 1nF 16V 0201 C210; 1nF 16V 0201 C209; 100nF 6.3V 0201 C207; 1nF 16V 0201 C208; 4.7uF 35V B C23

100nF 6.3V 0201 C222; 100nF 6.3V 0201 C221; 1nF 16V 0201 C220; 1nF 16V 0201 C219; 100nF 6.3V 0201 C217; 1nF 16V 0201 C218; 4.7uF 35V B C24

DVDD12

IC4 AD9154BCPZ

OUT0_P OUT0_N OUT1_P OUT1_N OUT2_P OUT2_N OUT3_P OUT3_N

SYNCOUT0_P SYNCOUT0_N

PDP_OUT0 PDP_OUT1

DAC_SYSREF_P DAC_SYSREF_N

C635 1uF 16V 0402; C634 1uF 16V 0402

R25 1; R24 1

DAC_IRQn DAC_RESETn

R189 4k02

PVDD12: 100nF 6.3V 0201 C182; 100nF 6.3V 0201 C181; 1nF 16V 0201 C180; 1nF 16V 0201 C179; 100nF 6.3V 0201 C177; 1nF 16V 0201 C178; 4.7uF 35V B C21; 47uF 16V C C718; 100nF 6.3V 0201 C187; 100nF 6.3V 0201 C188; 100nF 6.3V 0201 C189; 1nF 16V 0201 C190; 1nF 16V 0201 C191

SVDD12: 1nF 16V 0201 C205; 1nF 16V 0201 C206; 1nF 16V 0201 C195; 1nF 16V 0201 C194; 100nF 6.3V 0201 C192; 1nF 16V 0201 C193; 4.7uF 35V B C22; 47uF 16V C C719; 100nF 6.3V 0201 C200; 100nF 6.3V 0201 C201; 100nF 6.3V 0201 C202; 1nF 16V 0201 C203; 1nF 16V 0201 C204

SDVDD12: 100nF 6.3V 0201 C232; 1nF 16V 0201 C230; 1nF 16V 0201 C229; 1nF 16V 0201 C228; 4.7uF 35V B C25; C722 47uF 16V C

DAC_CFG

DAC_IRQn DAC_RESETn DAC_SPI_CSn DAC_SPI_SCLK DAC_SPI_SDO DAC_SPI_SDIO DAC_TXEN0 DAC_TXEN1

P4V0

LT3045EDD#PBF

IC18 =Device

C259 4.7uF; C258 4.7uF; C904 22uF; R288 33k2

30R@100MHz L40; 30R@100MHz L39

185mA AVDD33: 100nF 6.3V 0201 C33

11mA SIOVDD33: 100nF 6.3V 0201 C274

P2V0

IC12 =Device: C247 4.7uF; C898; 22uF; R295 13k; C158 100nF 6.3V 0201; 4.7uF C34; 174mA PVDD12

IC14 =Device: C251 4.7uF; C899 22uF; R298 13k; C250 100nF 6.3V 0201; 4.7uF C36; 682mA

IC13 =Device: C249 4.7uF; C900 22uF; R296 13k; C248 100nF 6.3V 0201; 4.7uF C35; 442mA DVDD12

IC15 =Device: C253 4.7uF; C901 22uF; R299 13k; C252 100nF 6.3V 0201; 4.7uF C40; SDVDD12

IC16 =Device: C255 4.7uF; C902 22uF; R300 13k; C254 100nF 6.3V 0201; 4.7uF C44; PLLVDD12

IC17 =Device: C257 4.7uF; C903 22uF; R297 13k; C256 100nF 6.3V 0201; 4.7uF C143; 397mA CVDD12

PLLVDD12: 1nF 16V 0201 C239; 100nF 6.3V 0201 C237; 1nF 16V 0201 C238; 4.7uF 35V B C26; 47uF 16V C C723

SIOVDD33: 1nF 16V 0201 C242; 100nF 6.3V 0201 C240; 4.7uF 35V B C28; 47uF 16V C C725

IOVDD: 100nF 6.3V 0201 C246; 1nF 16V 0201 C244; 4.7uF 35V B C29; 47uF 16V C C726

P1V8 L37 120R@100MHz; C636 1uF 16V 0402; IOVDD 1nF 16V 0201 C276

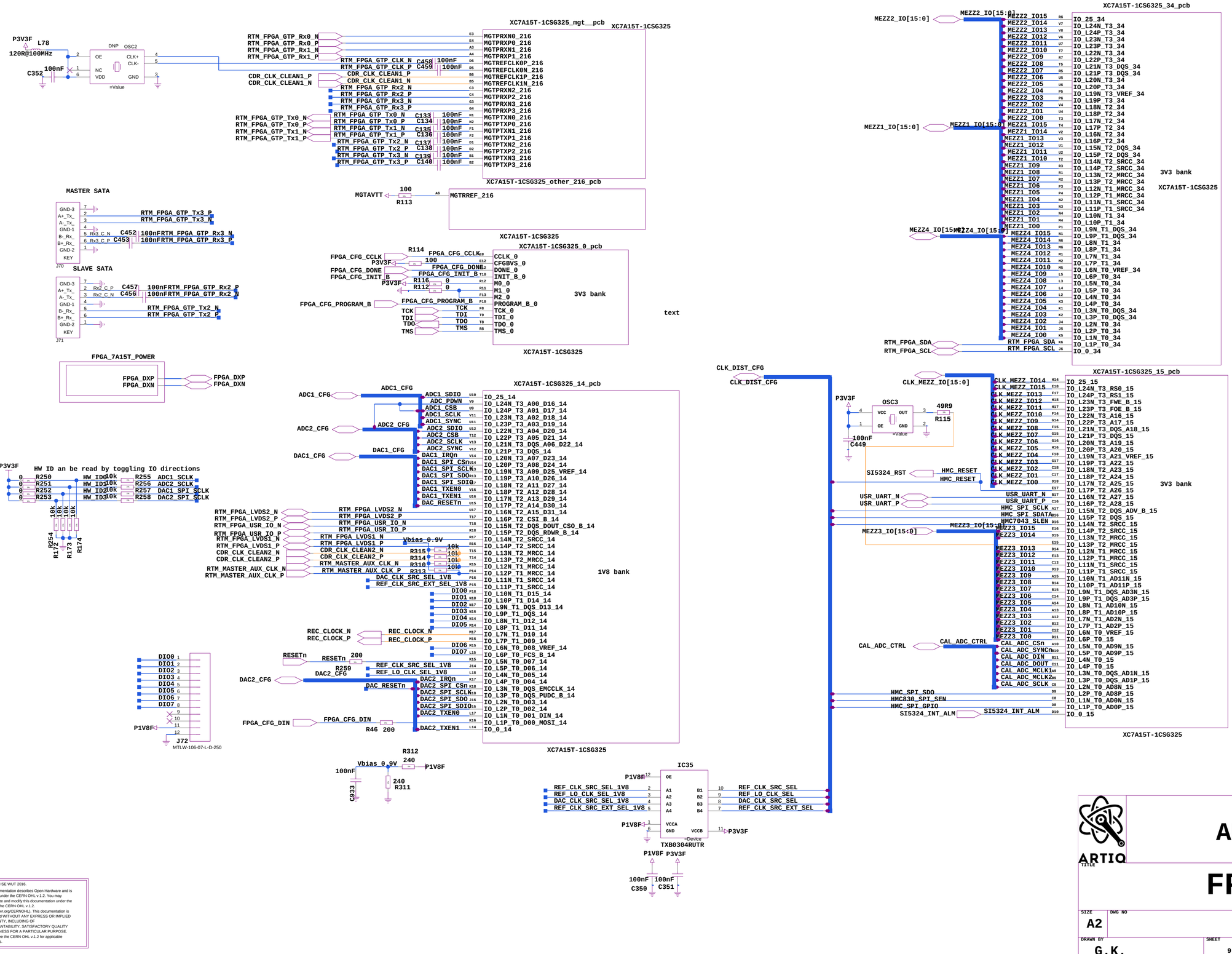
W2L16C473MAT1S C71 C72 C82 C83 C84 C85

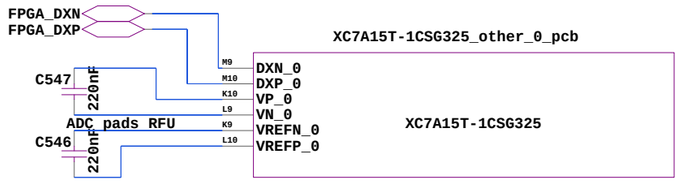
ARTIQ Sinara

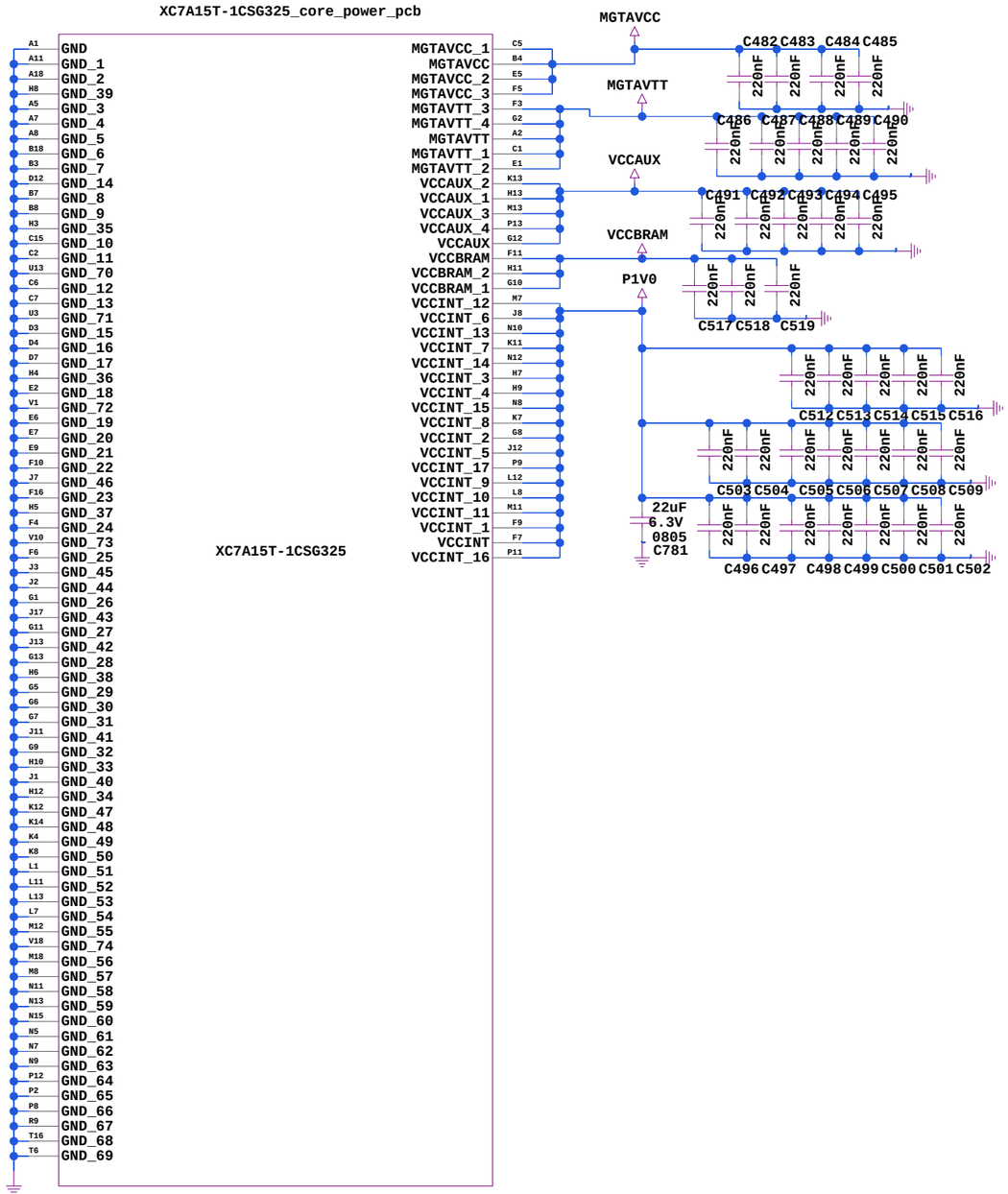
TITLE: DAC_JESD204B

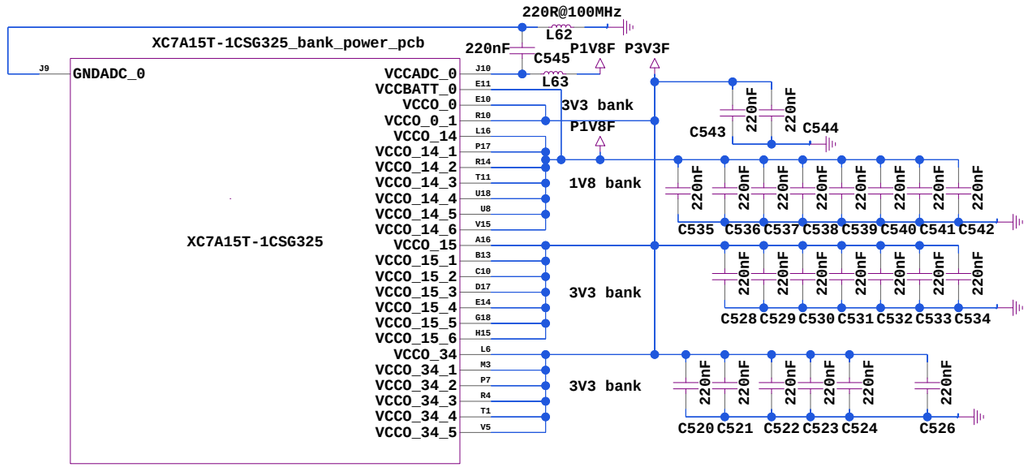
SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	8	23	24/01/2017:23:13









ARTIQ Sinara

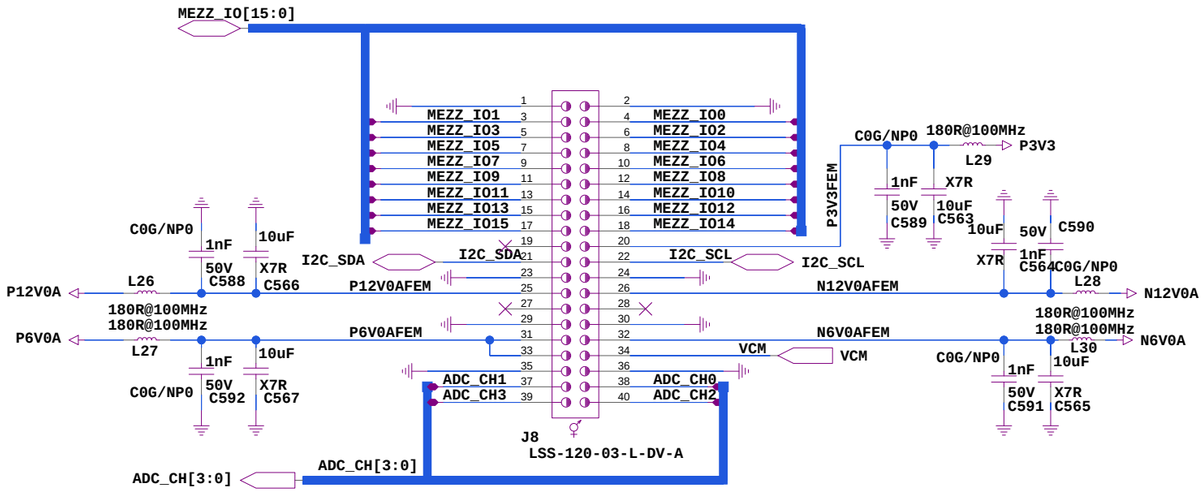
TITLE

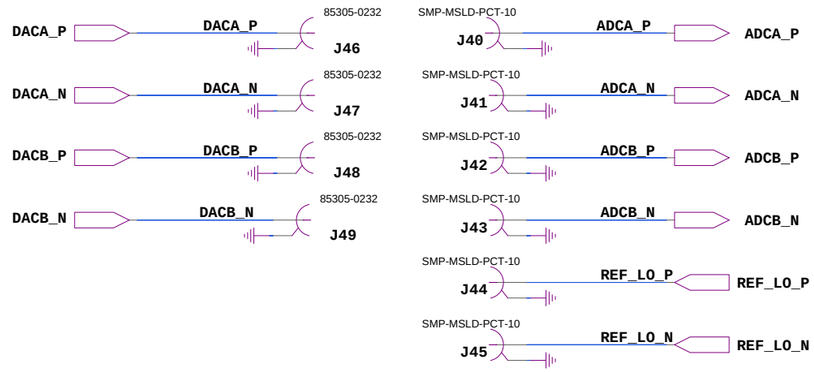
FPGA_7A15T_POWER

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	10	23	24/01/2017:23:14

Interfaces with:
PCB_mezzanine analog Bo mezzanine_analog_allaki
Input signal 1.2vpp
Output signal DAC: 4.17mA....20.85mA
Impedance 100Ohm diff
Control signals: LVCMOS 3.3V
I2C signals: LVCMOS 3.3V
REF_LO - LVPECL
+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz





ARTIQ

ADC_DAC_AFE_Mezzanine

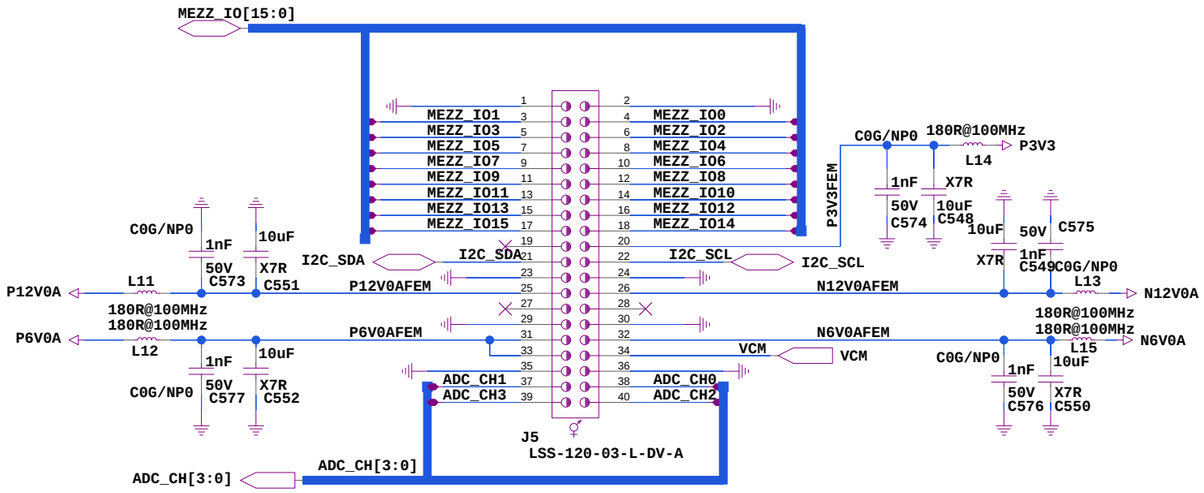
TITLE

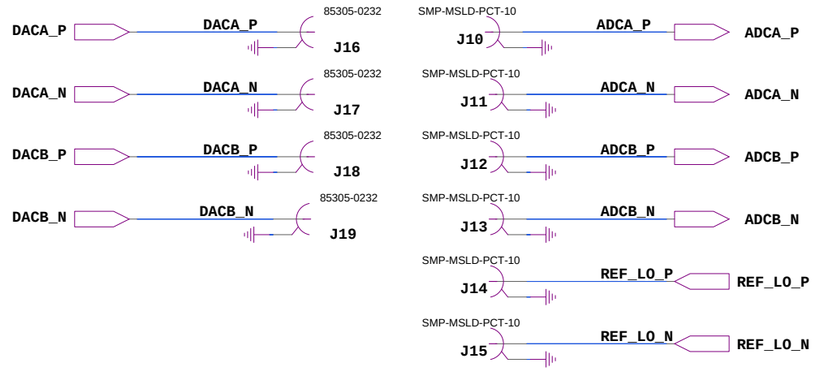
ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	11	23	24/01/2017:23:14

Interfaces with:
PCB_mezzanine analog Board
Input signal 1.2vpp
Output signal DAC: 4.17mA....20.85mA
Impedance 100Ohm diff
Control signals: LVCMOS 3.3V
I2C signals: LVCMOS 3.3V
REF_LO - LVPECL
+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz





ARTIQ

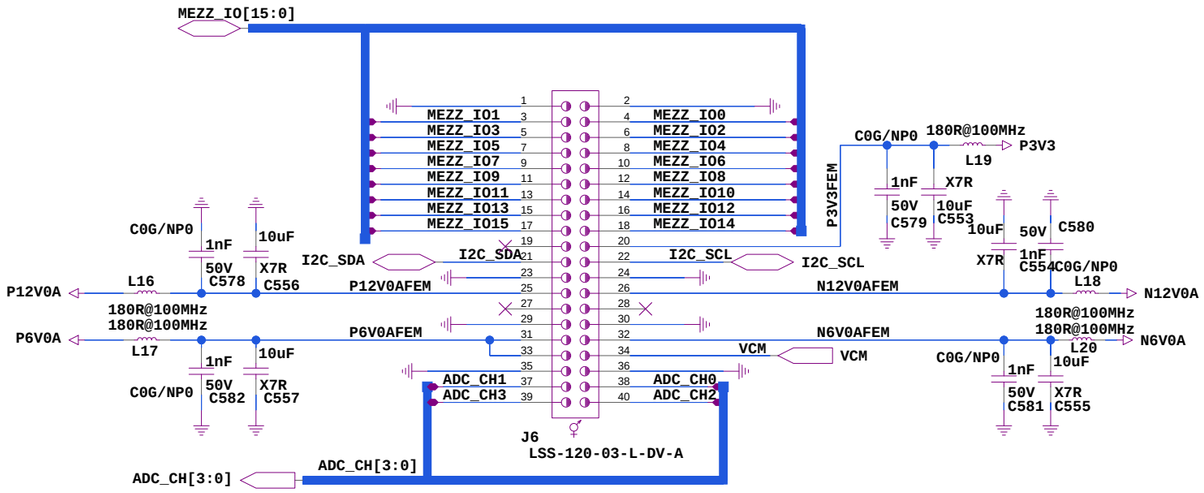
ADC_DAC_AFE_Mezzanine

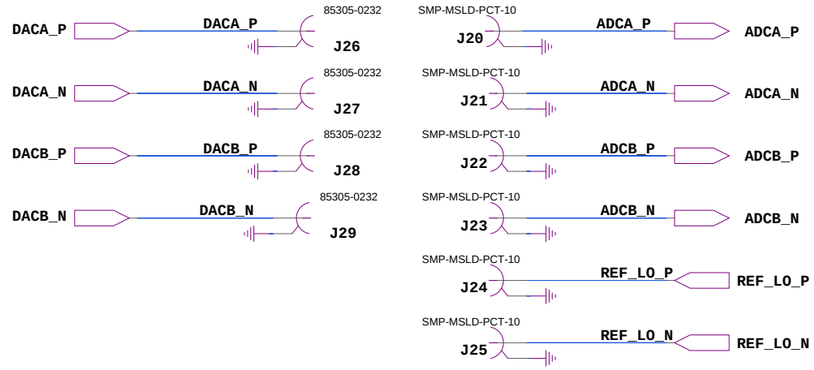
ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET		
G.K.	12	of 23	24/01/2017:23:14

Interfaces with:
PCB_mezzanine analog Bo mezzanine_analog_allaki
Input signal 1.2vpp
Output signal DAC: 4.17mA....20.85mA
Impedance 100Ohm diff
Control signals: LVCMOS 3.3V
I2C signals: LVCMOS 3.3V
REF_LO - LVPECL
+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz





ARTIQ

ADC_DAC_AFE_Mezzanine

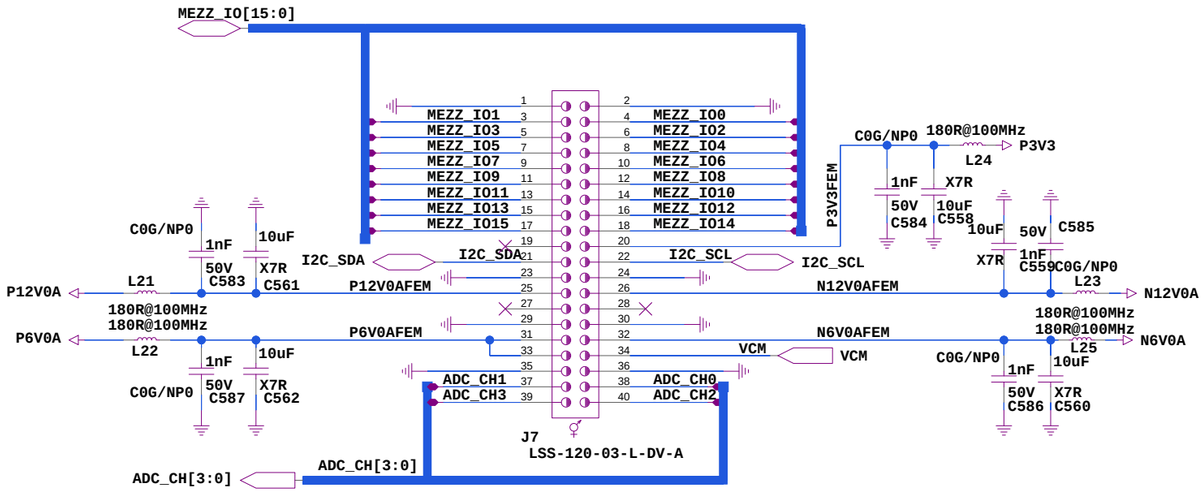
TITLE

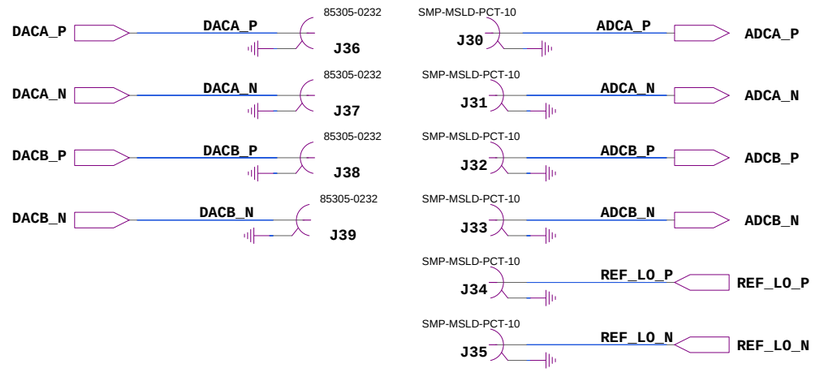
ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	13	23	24/01/2017:23:14

Interfaces with:
PCB_mezzanine analog BQBoard_mezzanine_analog_allaki
Input signal 1.2vpp
Output signal DAC: 4.17mA....20.85mA
Impedance 100Ohm diff
Control signals: LVCMOS 3.3V
I2C signals: LVCMOS 3.3V
REF_LO - LVPECL
+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz





ARTIQ

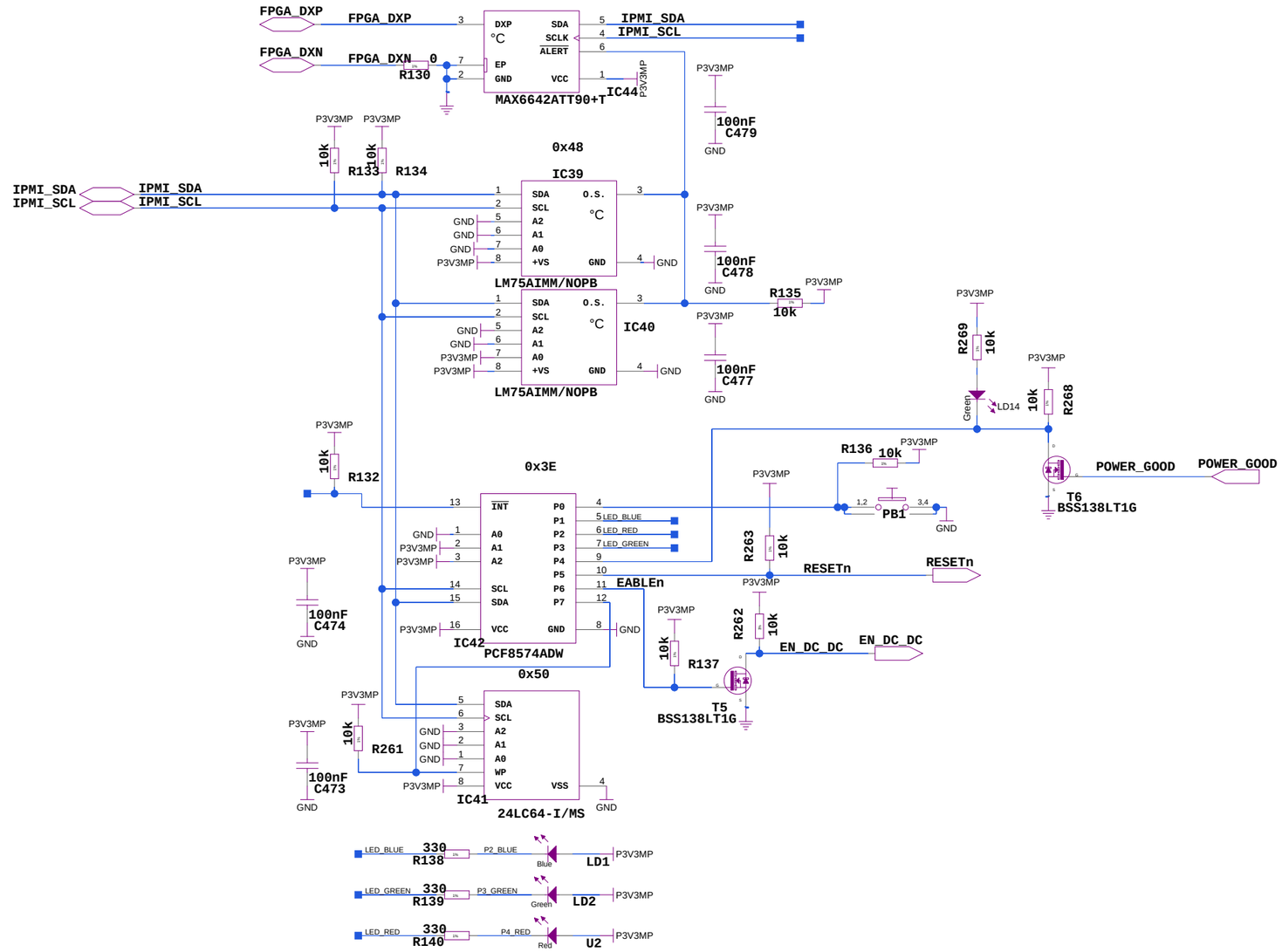
TITLE

ADC_DAC_AFE_Mezzanine

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	14	23	24/01/2017:23:14



check addresses

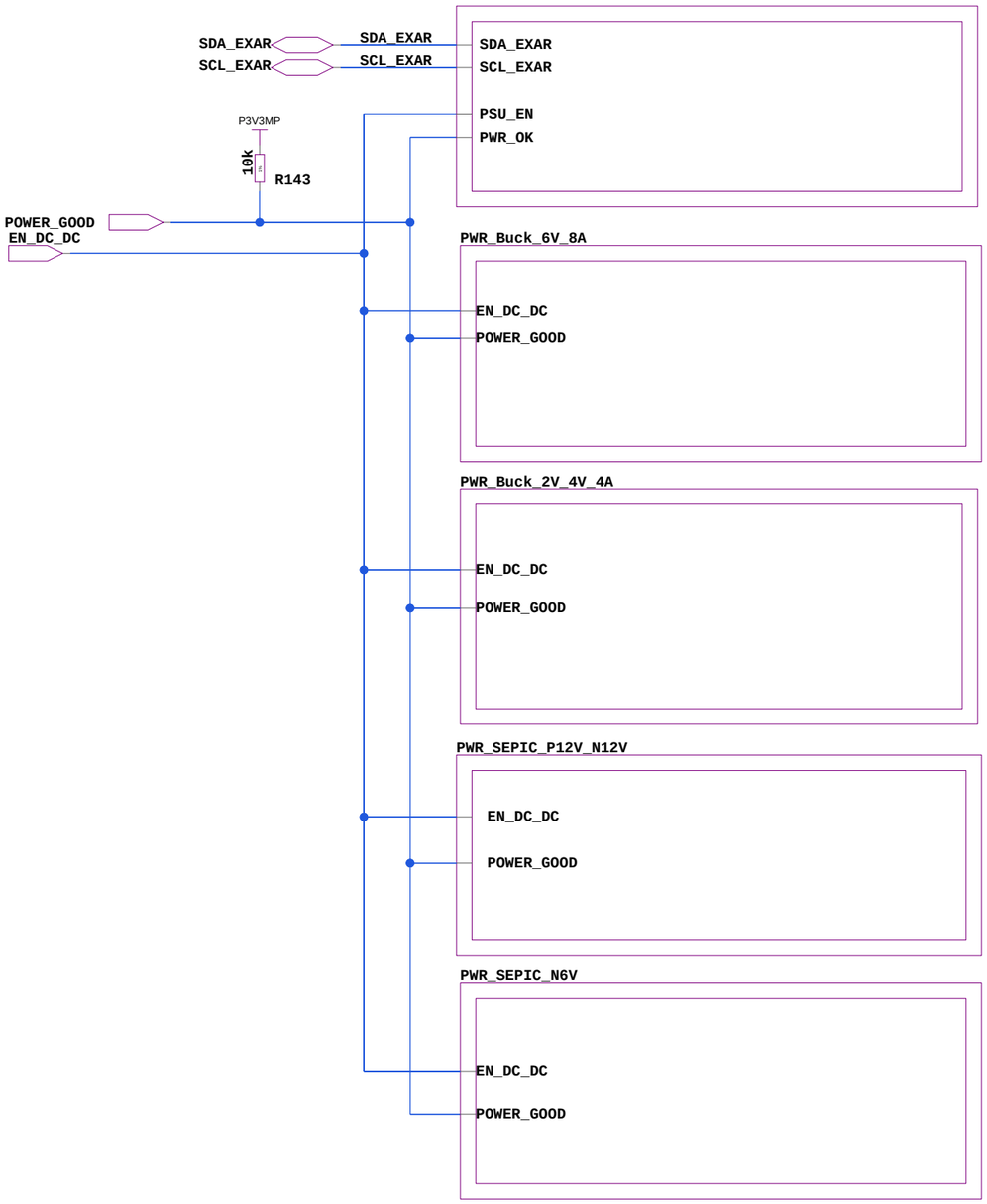
ARTIQ Sinara

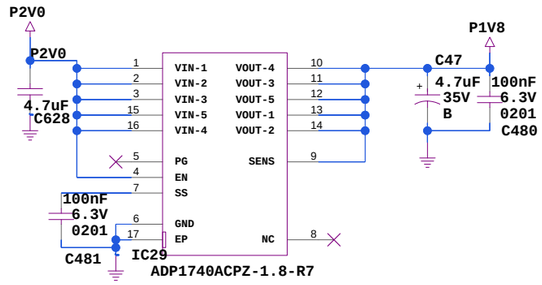
TITLE

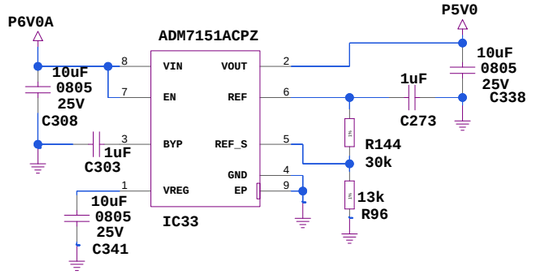
RTM_IPMI

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	15	23	24/01/2017:23:14







RTM modules power requirements

+12VDC @ 1A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 250 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 8 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 750 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

RTM power requirements

+4VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz
+2VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

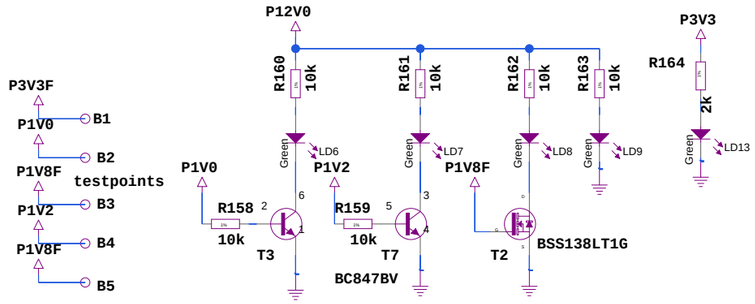
ARTIQ Sinara

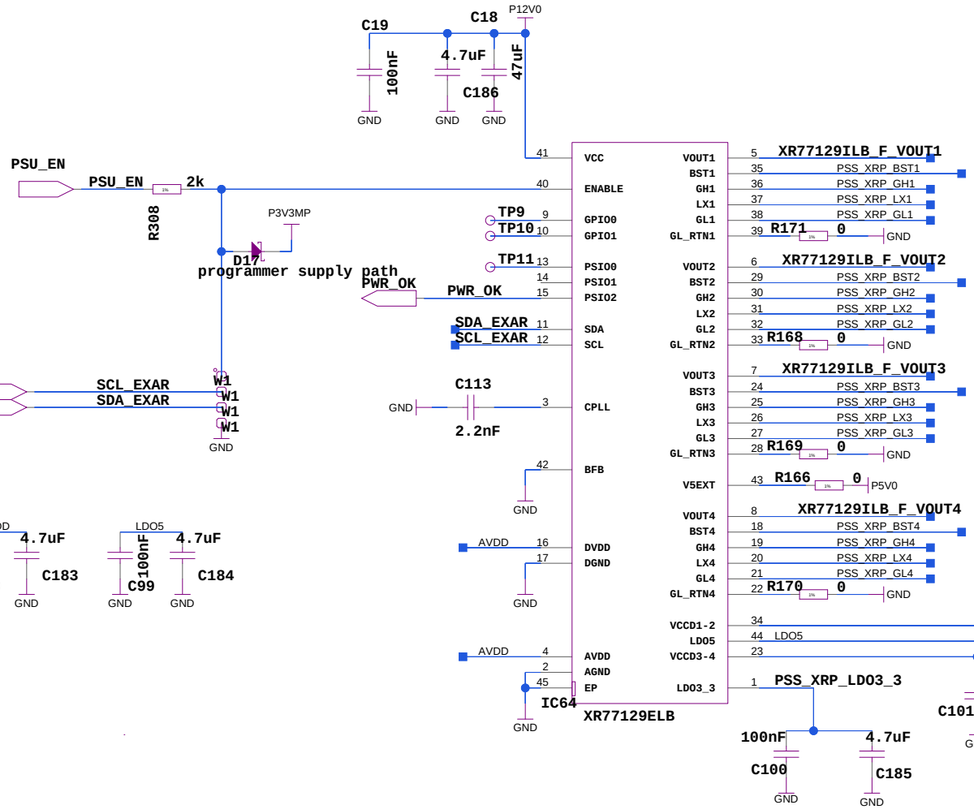
TITLE

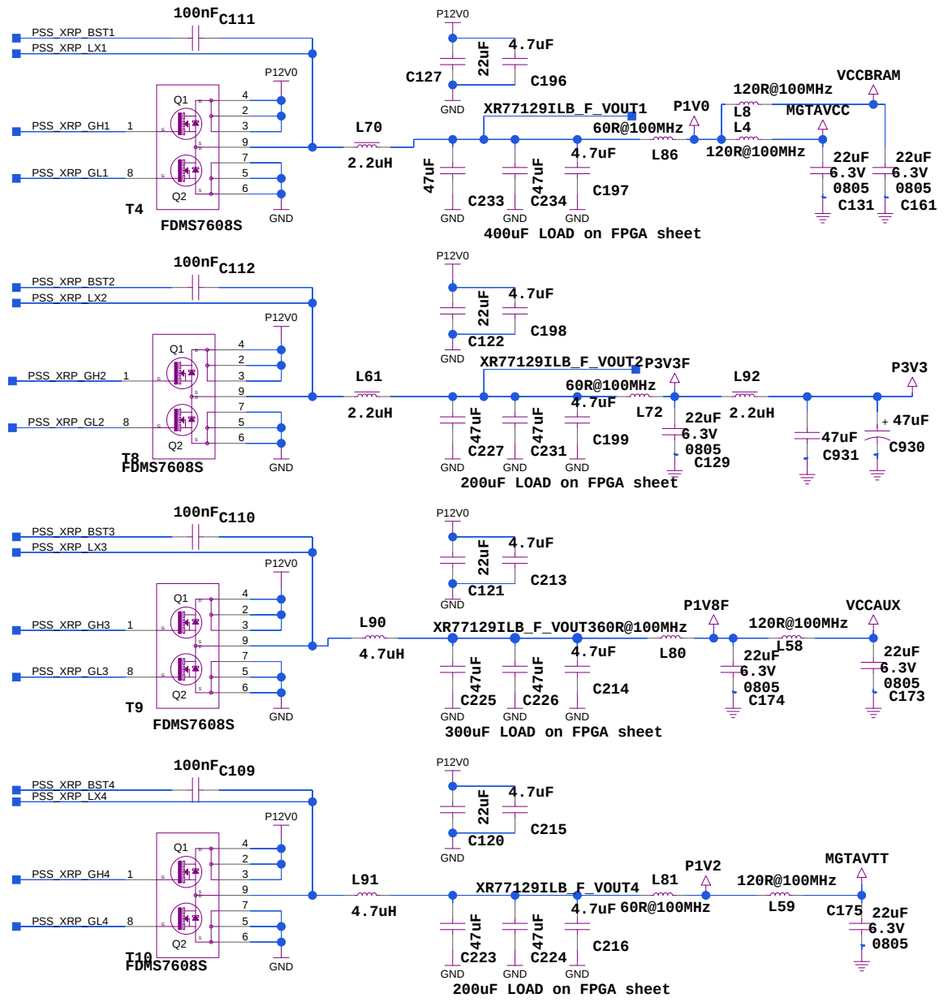
RTM_POWER_SUPPLY

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	16	23	24/01/2017:23:14







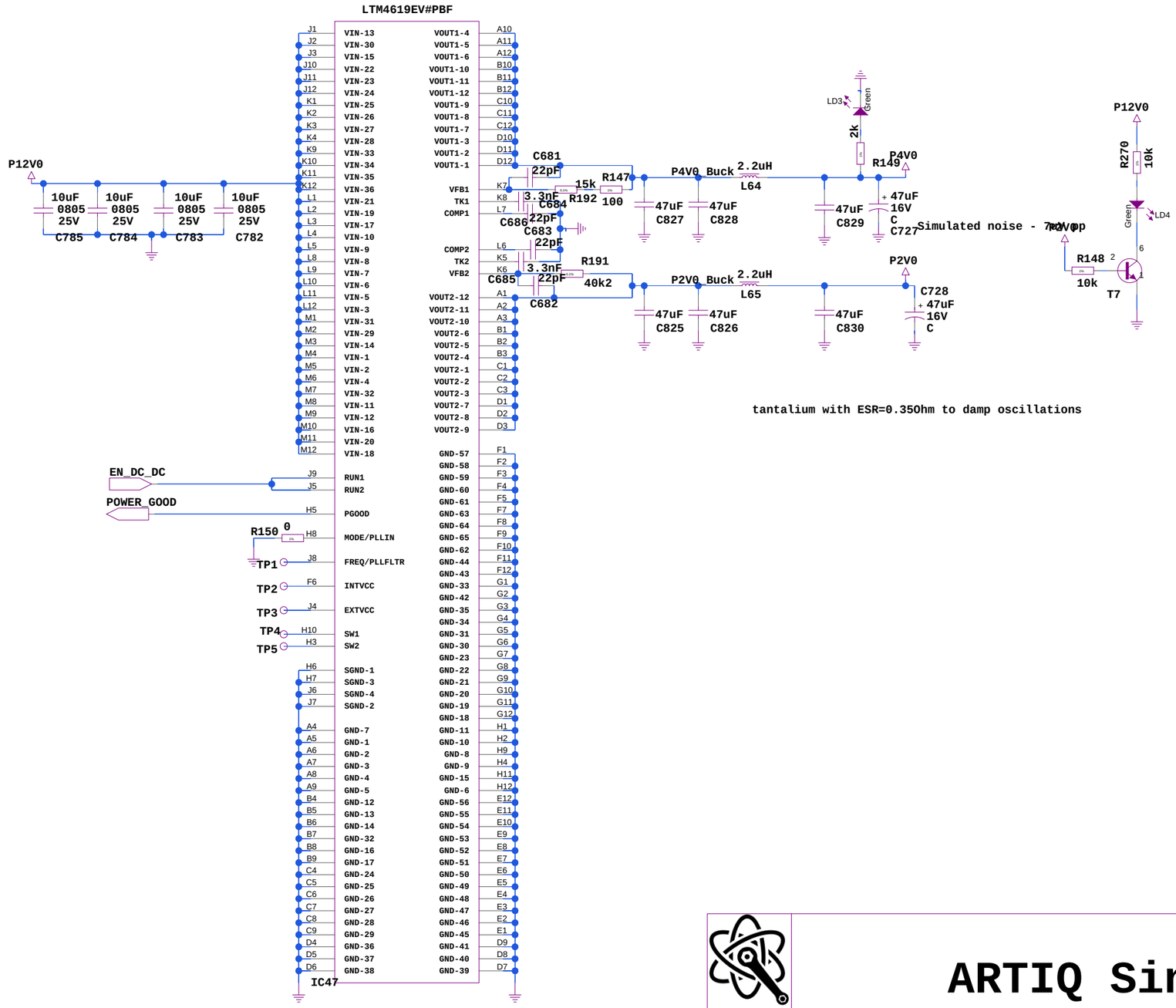
ARTIQ Sinara

TITLE

PWR_buck_FPGA_EXAR

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	17	23	24/01/2017:23:14

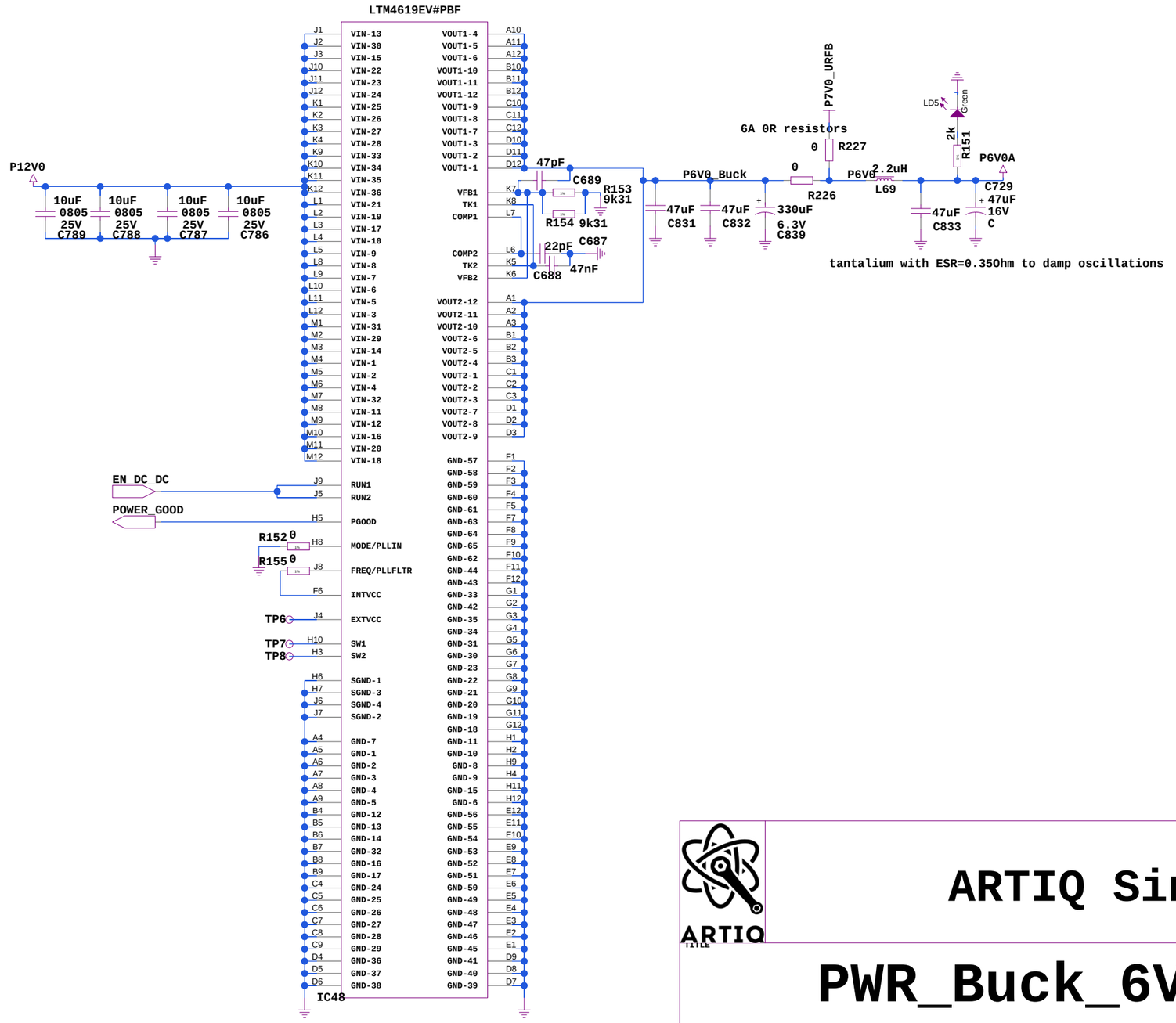


ARTIQ Sinara

TITLE: PWR_Buck_2V_4V_4A

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET		
G.K.	18	of 23	24/01/2017:23:14

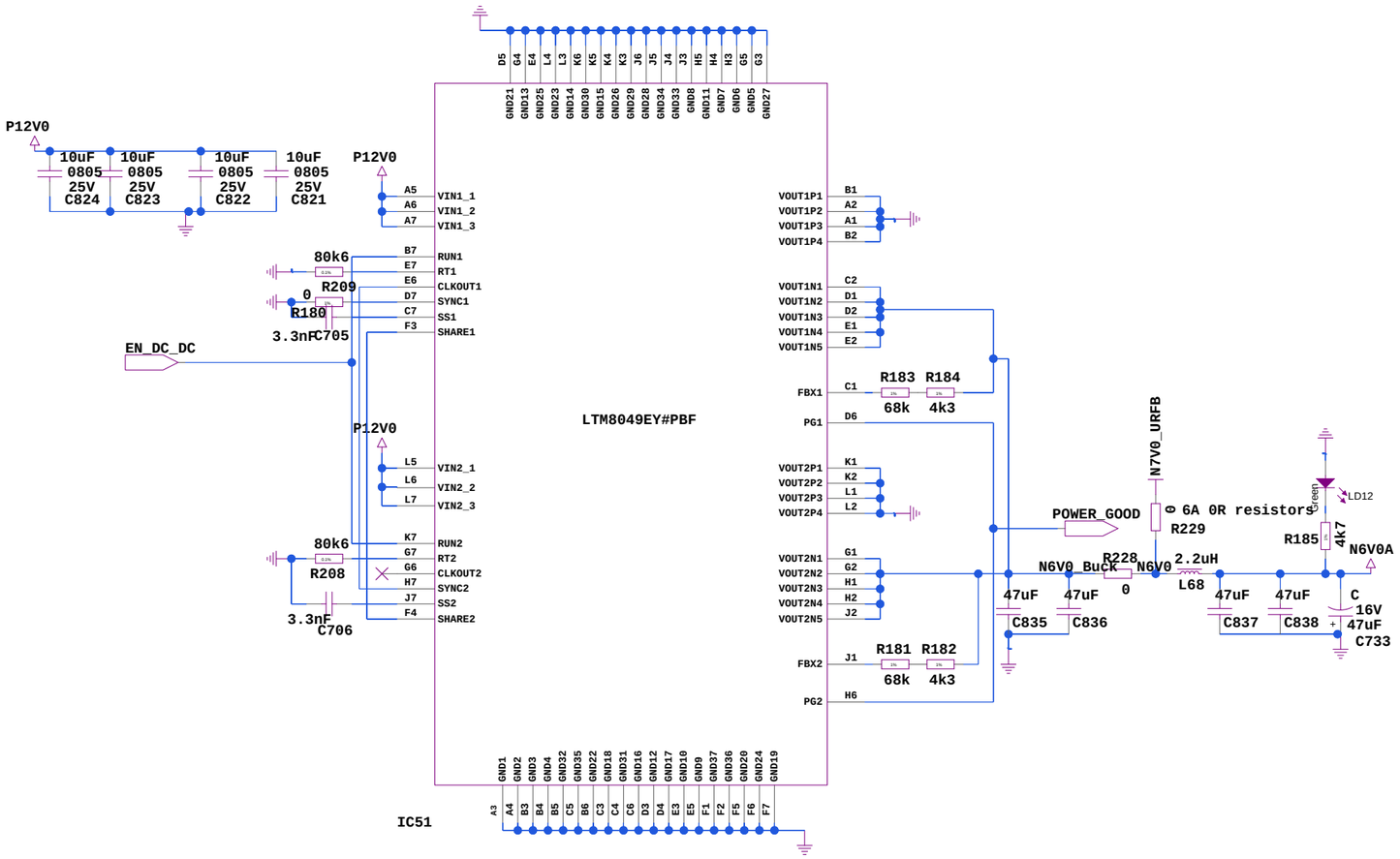


ARTIQ Sinara

TITLE: PWR_Buck_6V_8A

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	19	23	24/01/2017:23:14



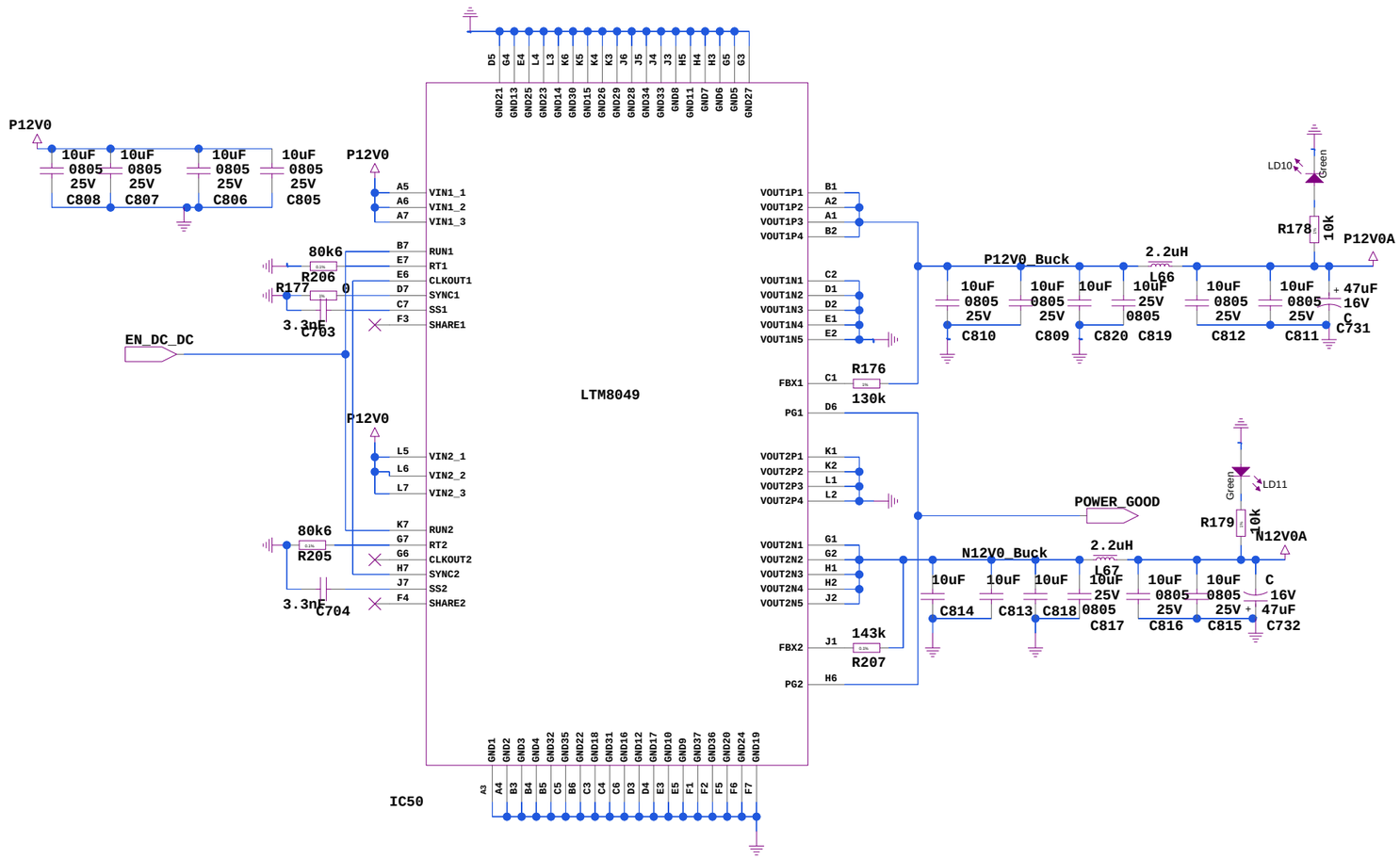
ARTIQ Sinara

TITLE

PWR_SEPIC_N6V

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET		
G.K.	20	of 23	24/01/2017:23:14

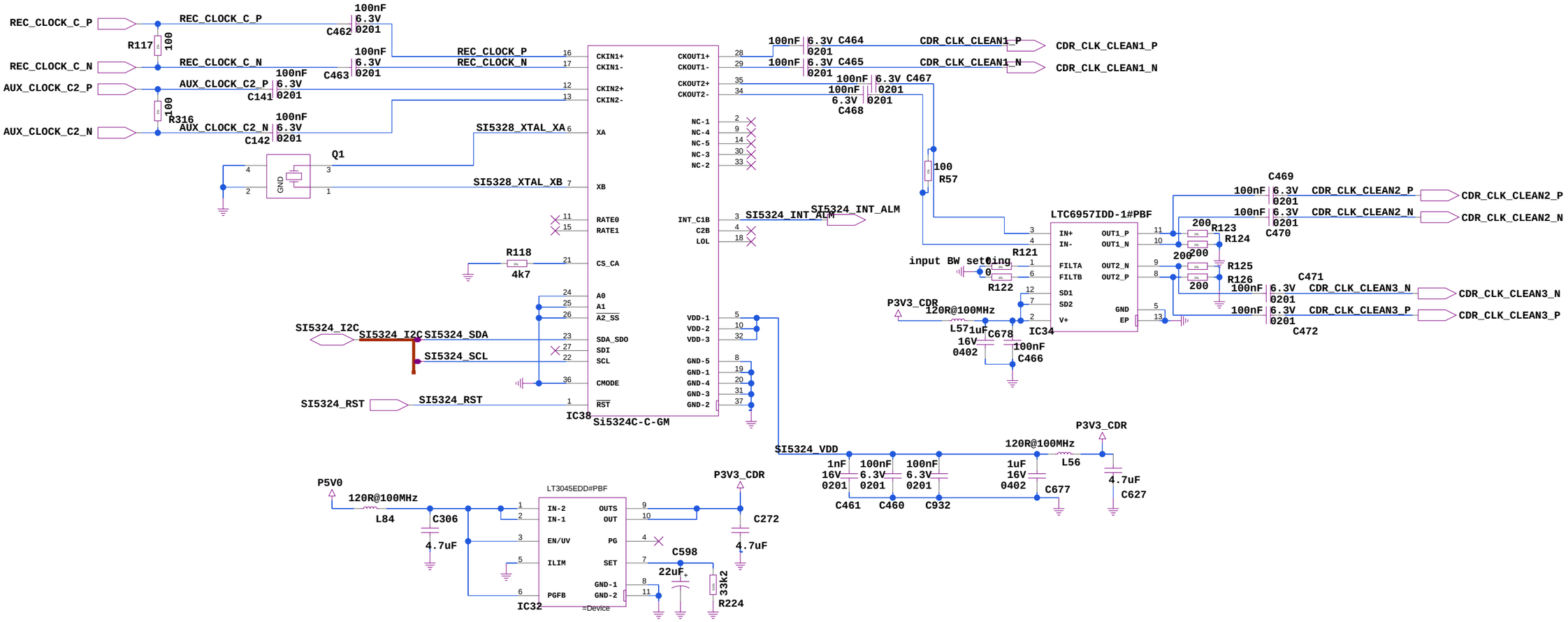


ARTIQ Sinara

PWR_SEPIC_P12V_N12V

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET		
G.K.	21	of 23	24/01/2017:23:14



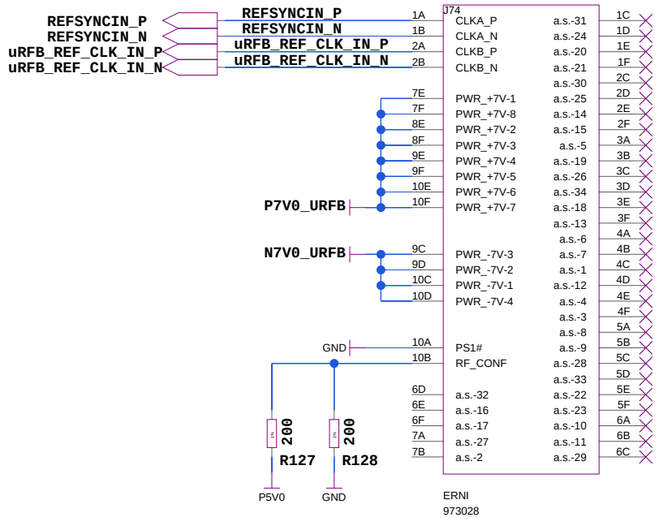
ARTIQ Sinara

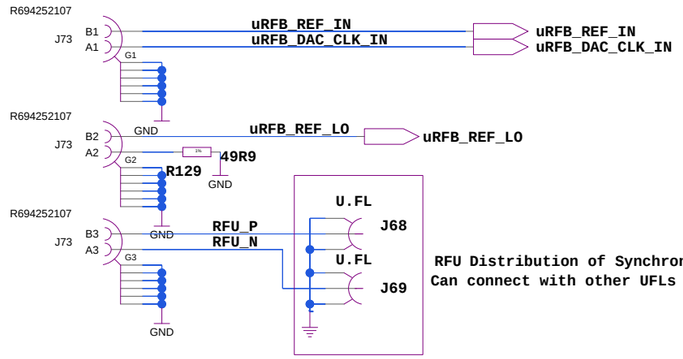
TITLE

SI5324_CLK_RECOVERY

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	22	23	24/01/2017:23:14





Interfaces uRFB:
uRFB_REF_IN : LVPECL
uRFB_DAC_CLK_IN: LVPECL
uRFB_REF_LO - LVPECL
Impedance 50Ohm SE, 100Ohm diff
REFSYNCIN_P/N : LVPECL
uRFB_REF_CLK_IN_P/N: LVPECL

RFU Distribution of Synchronisation signals.
Can connect with other UFLs using jumper cables

uRFB_Connectors

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.97

DRAWN BY	SHEET	of	
G.K.	23	23	24/01/2017:23:14