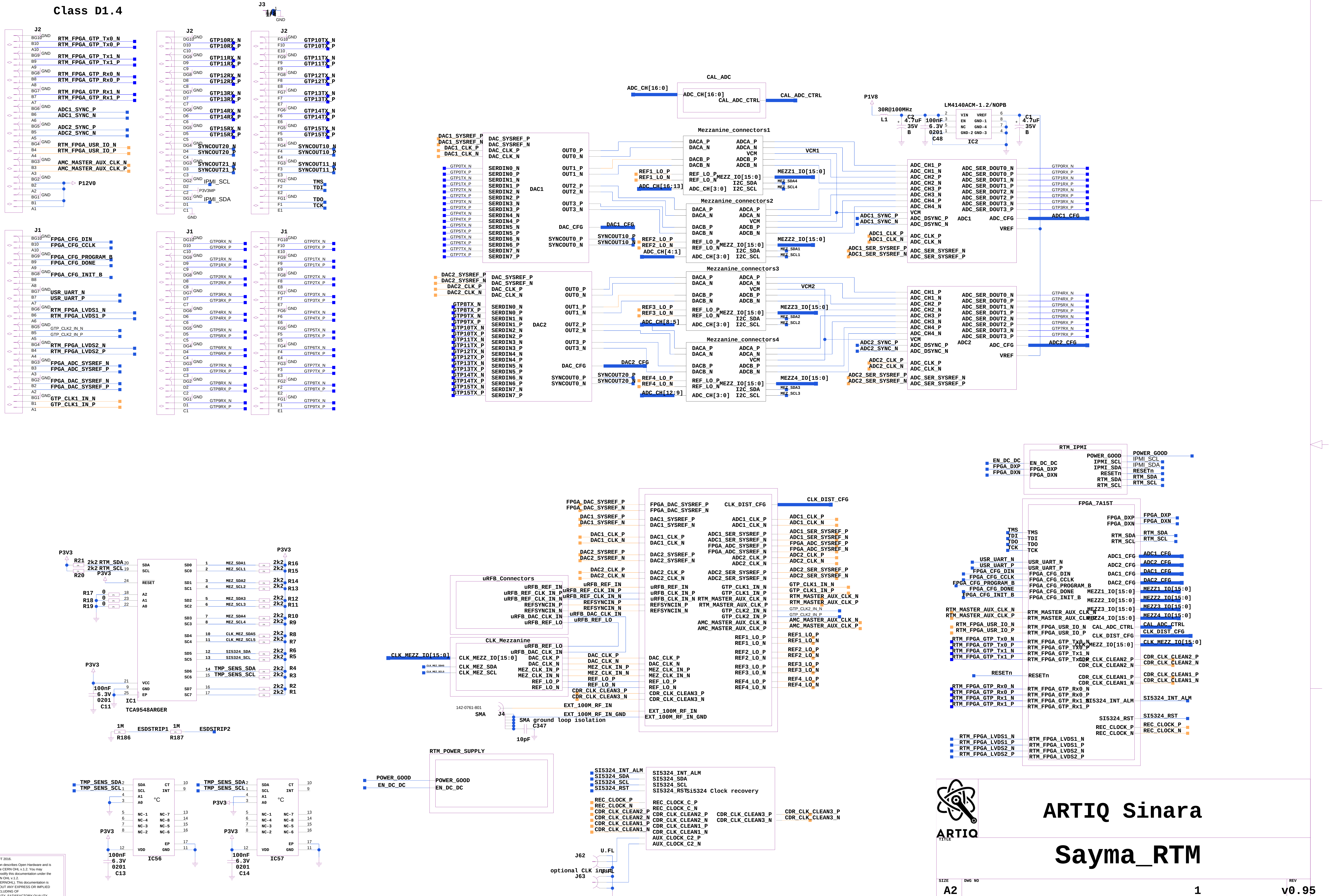

ARTIQ Sinara

TITLE

Sayma_RTM

SIZE	DWG NO	REV
A2	1	v0.95

DRAWN BY	SHEET	of	
G.K.	1	23	07/12/2016:23:59

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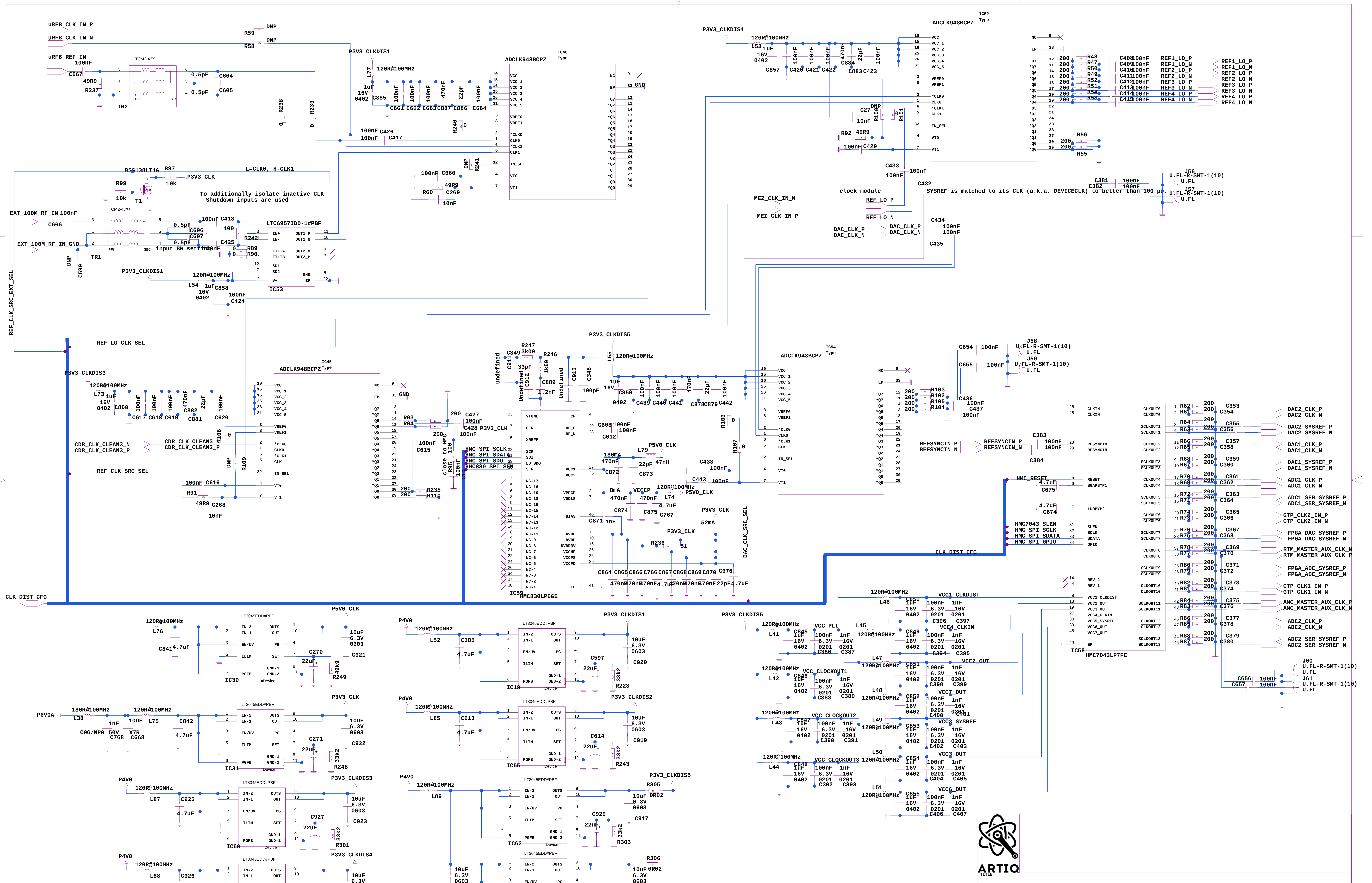

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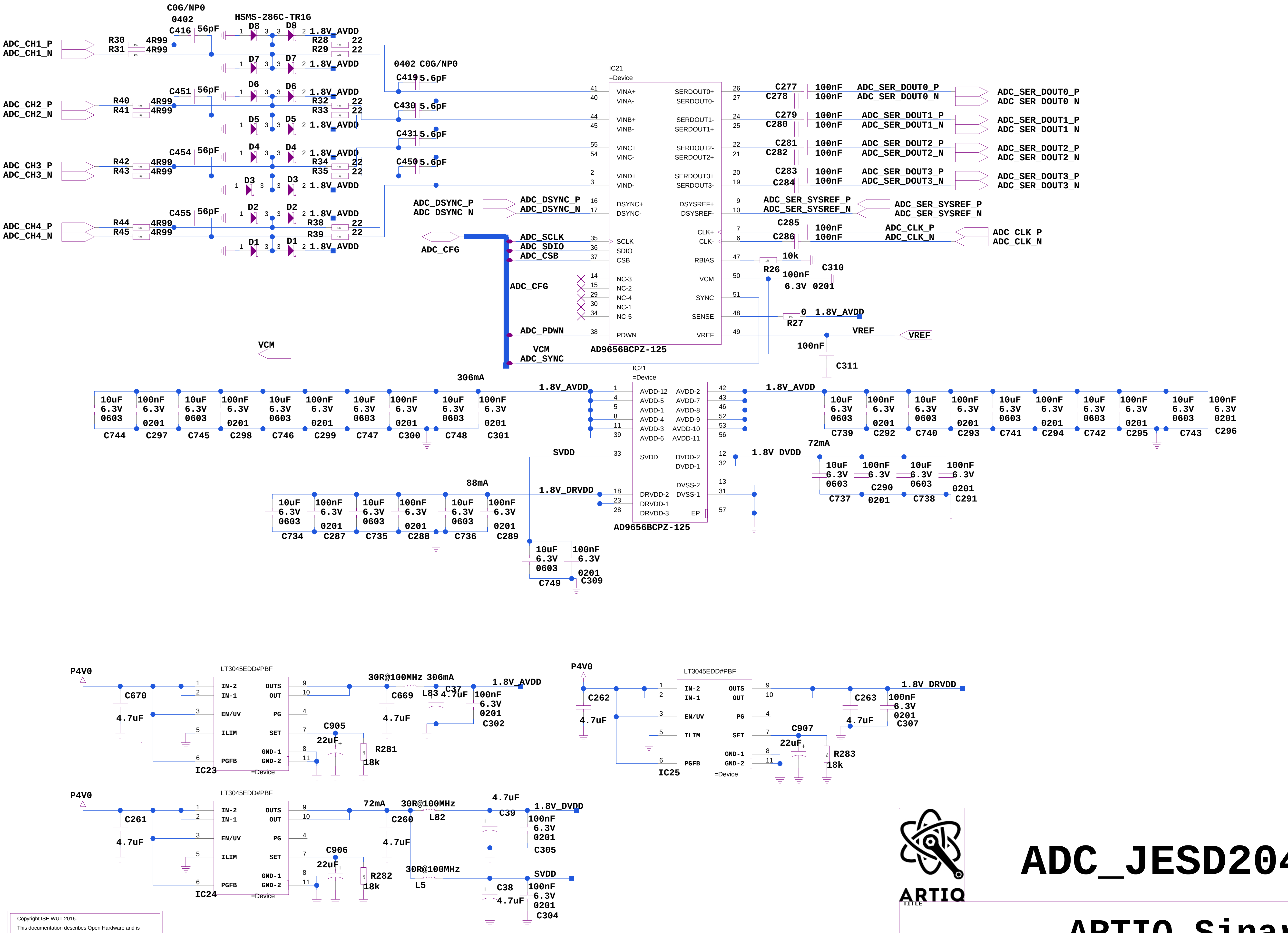
ARTIQ

TITLE

ARTIQ Sinara

SIZE	DWG NO	REV
A2	Clock_Distribution_PLL 1	v0.95

DRAWN BY	SHEET	of	
G.K.	2	23	05/12/2016:18:51



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ARTIQ

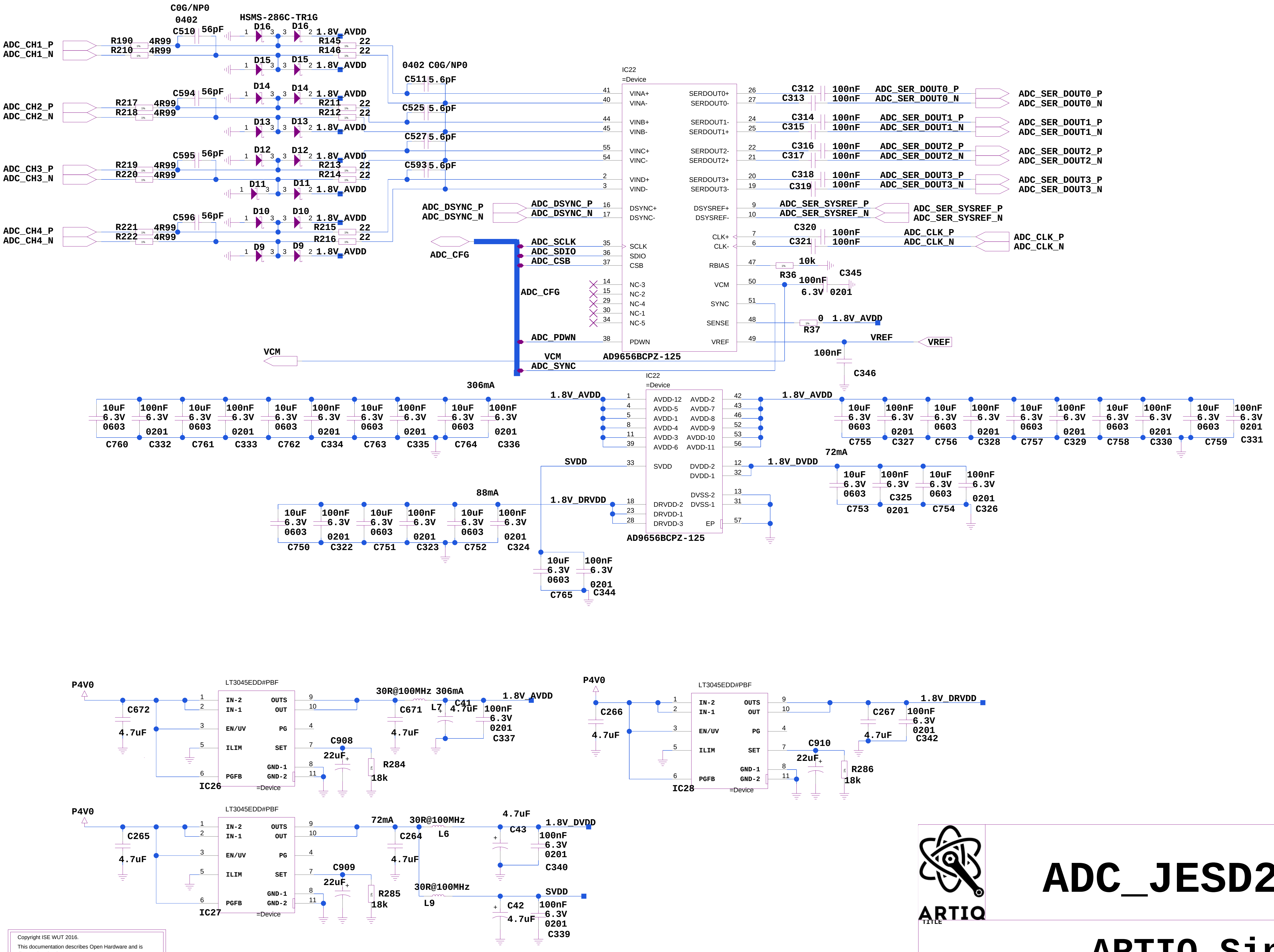
ADC_JESD204B

TITLE

ARTIQ Sinara

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	3	23	08/12/2016:01:02



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ARTIQ

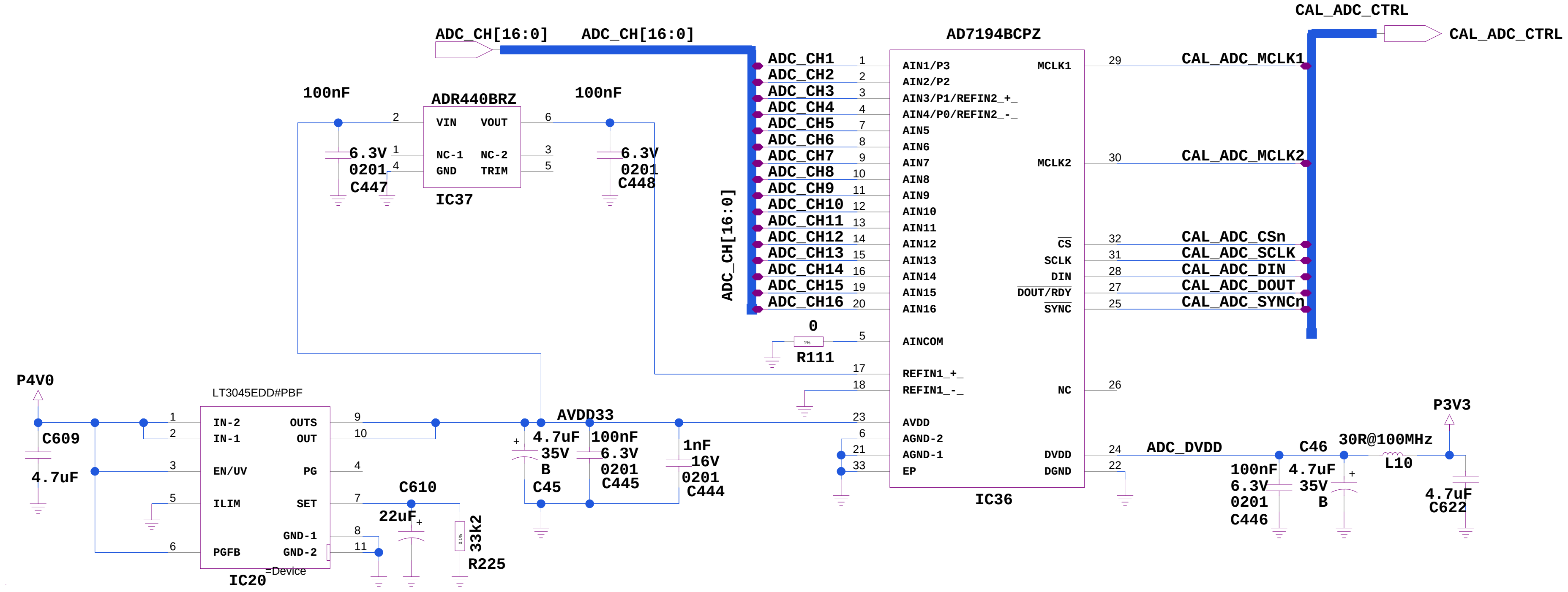
ADC_JESD204B

TITLE

ARTIQ Sinara

SIZE	DWG NO		REV
A3		1	v0.95

DRAWN BY	SHEET	of	
G.K.	4	23	08/12/2016:01:02



ARTIQ Sinara

TITLE

CAL_ADC

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	5	23	03/12/2016:19:04

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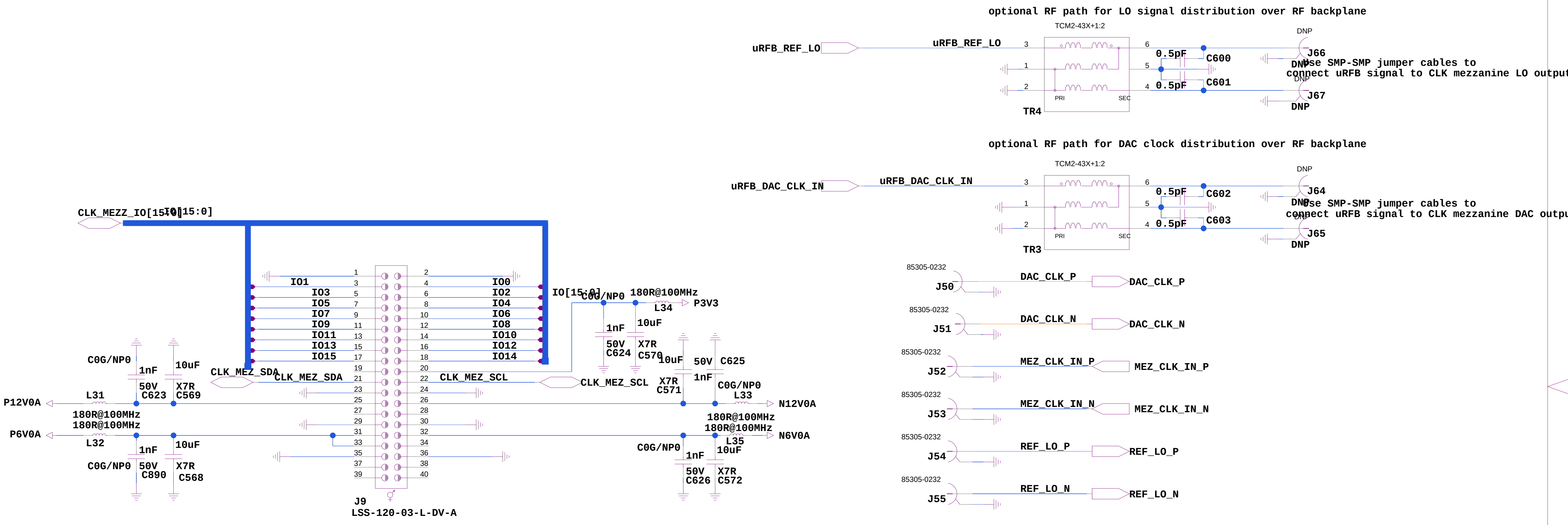

+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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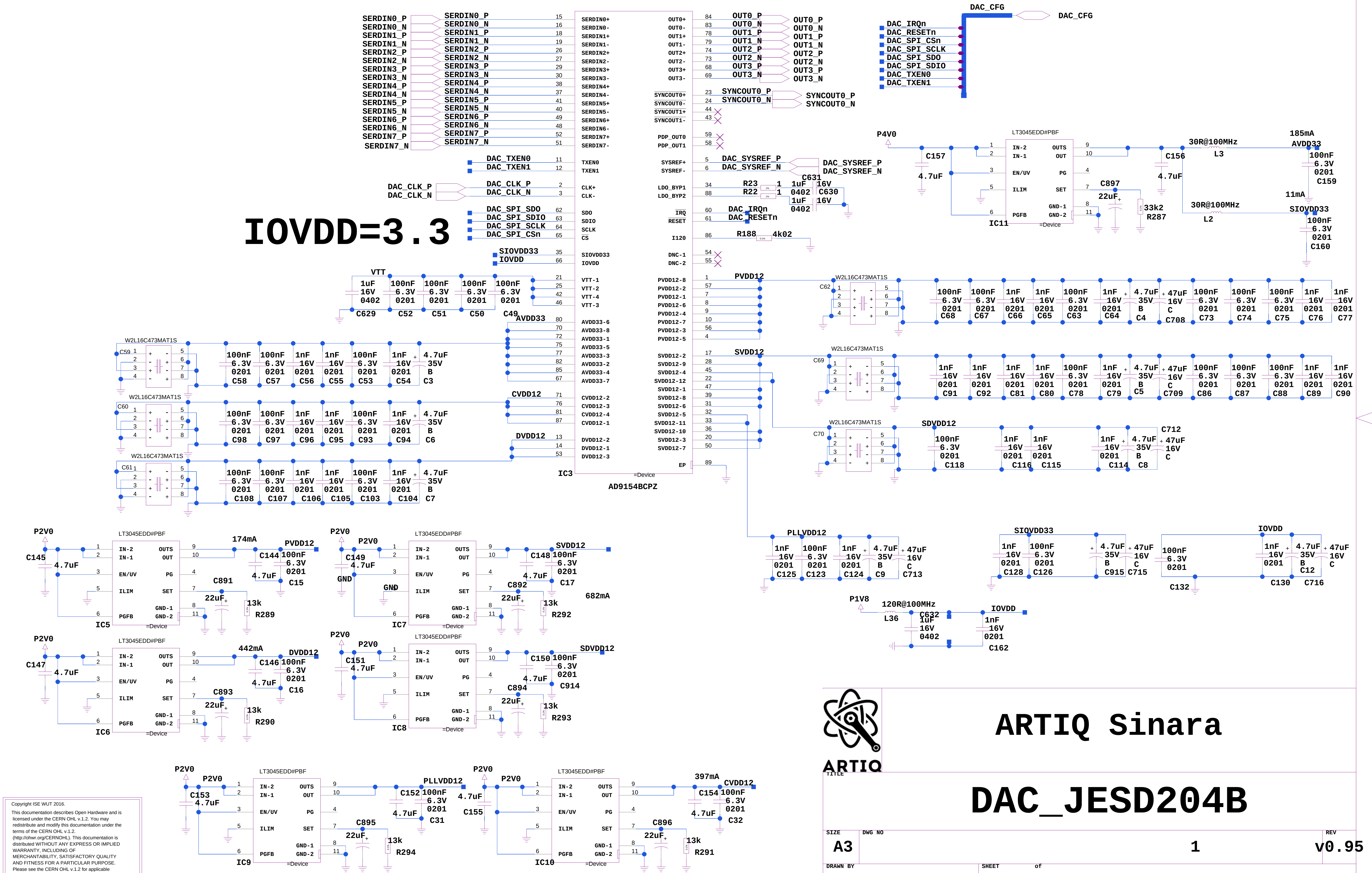
ARTIQ

ARTIQ Sinara

TITLE
CLK_Mezzanine

SIZE A3
DWG NO 1
REV v0.95
DRAWN BY G.K.
SHEET 6 of 23
03/12/2016:17:22



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ARTIQ

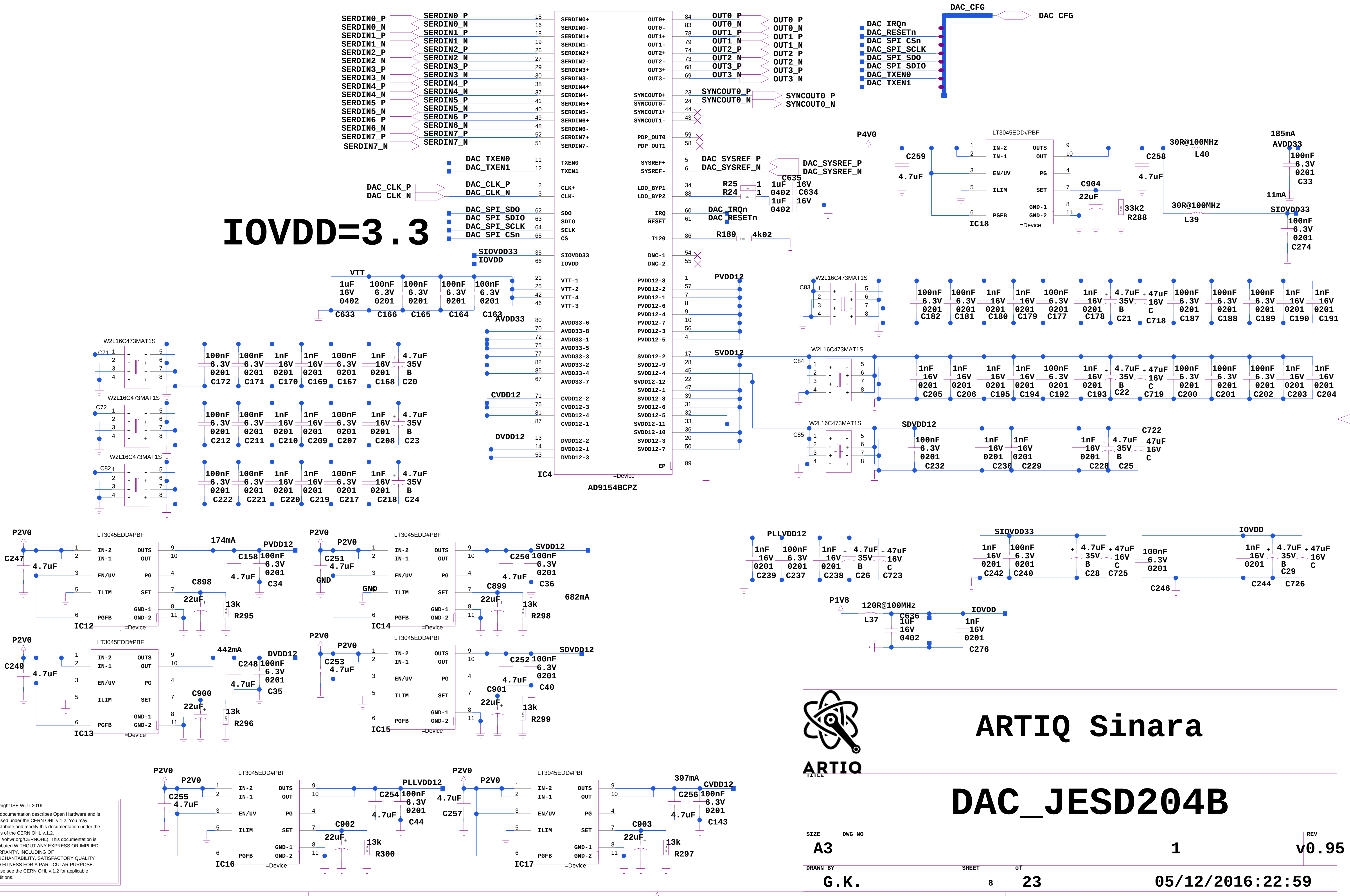
ARTIQ Sinara

TITLE

DAC_JESD204B

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	7	23	05/12/2016:22:59



ARTIQ Sinara

TITLE

DAC_JESD204B

SIZE A3

DWG NO 1

REV v0.95

DRAWN BY G.K.

SHEET 8 of 23

05/12/2016:22:59

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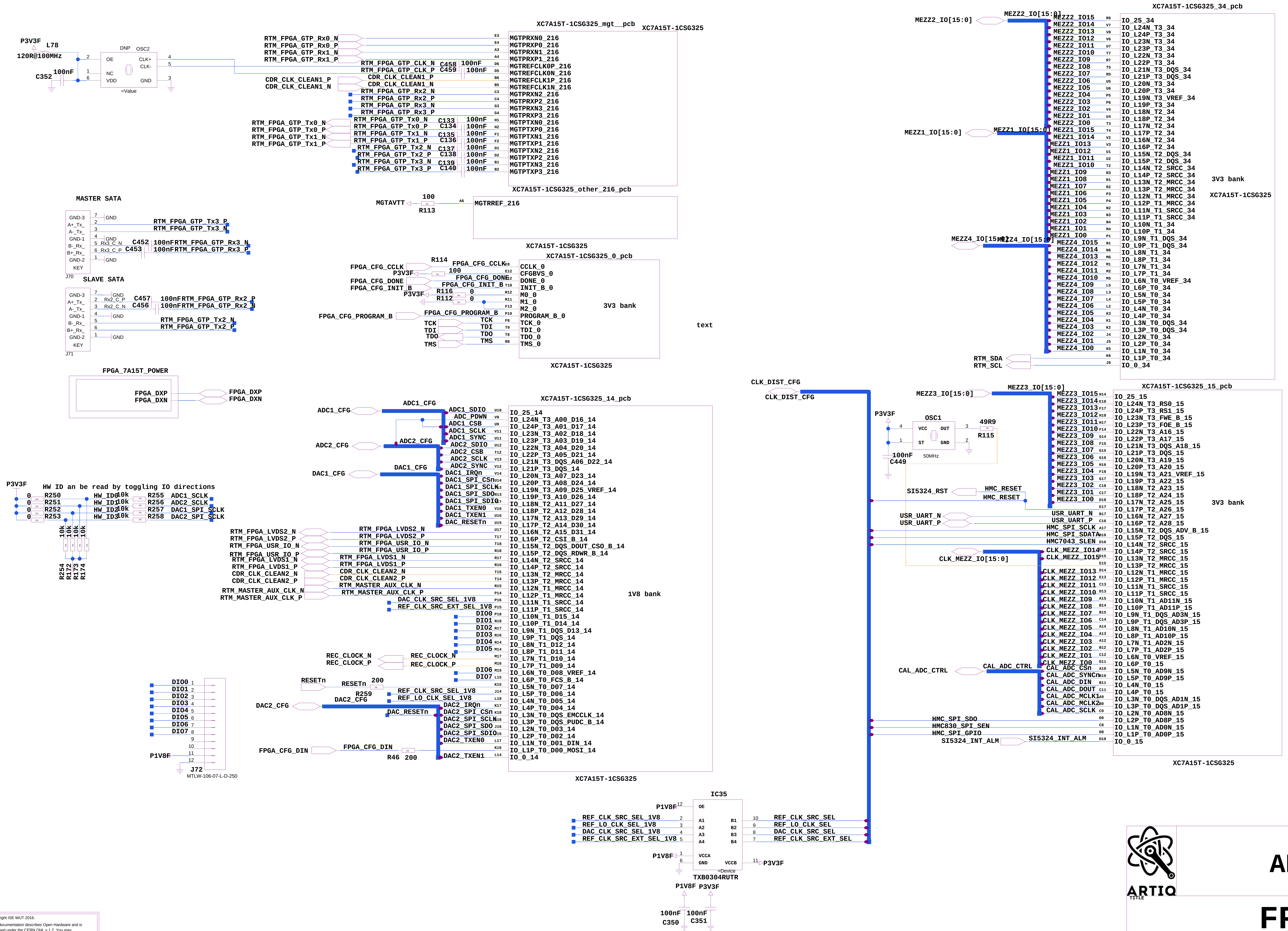

ARTIQ

ARTIQ Sinara

TITLE

FPGA_7A15T

SIZE	DWG NO		REV
A2		1	v0.95

DRAWN BY	SHEET	of	
G.K.	9	23	01/12/2016:18:22

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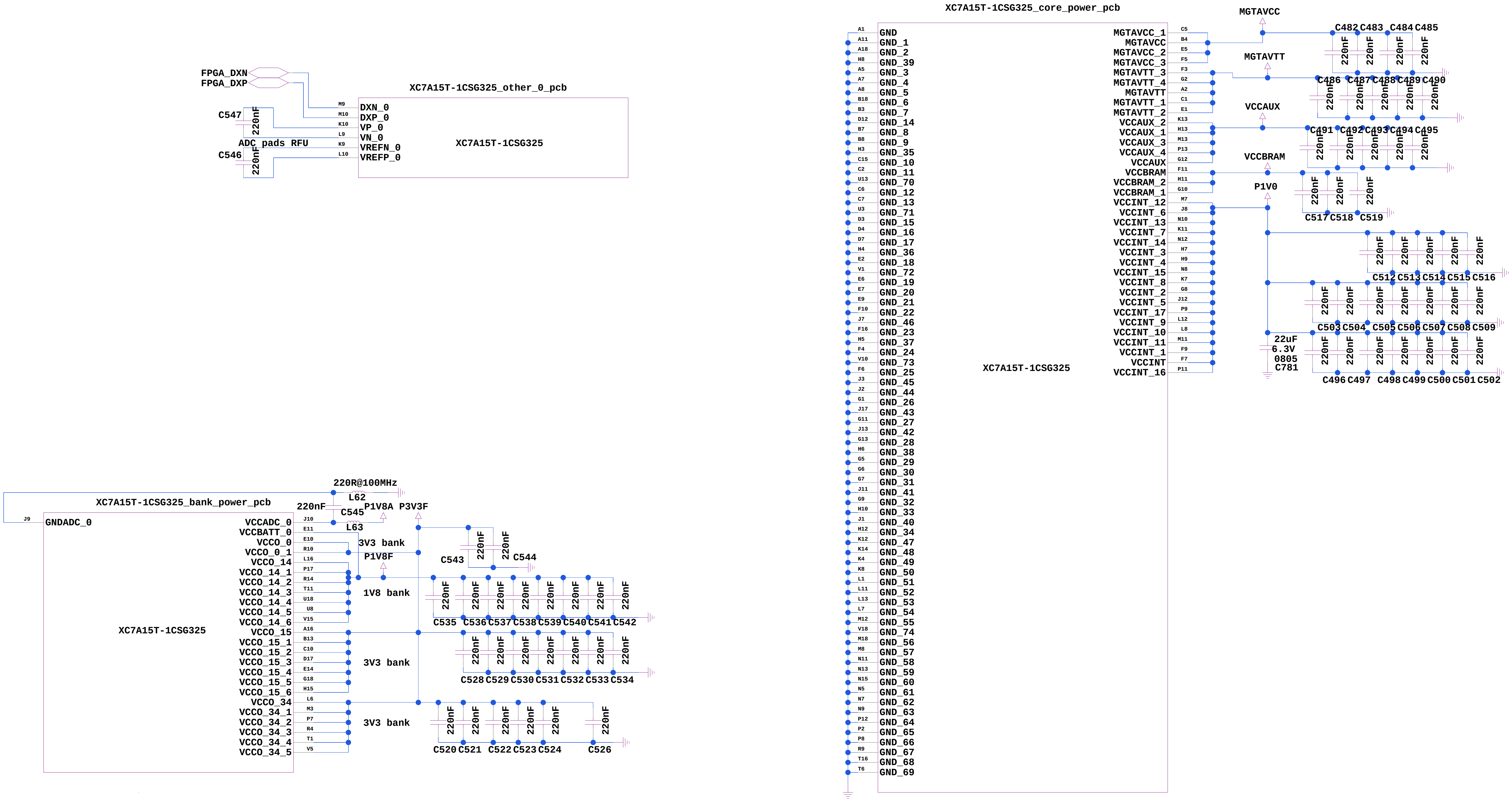

ARTIQ Sinara

TITLE

FPGA_7A15T_POWER

SIZE	DWG NO		REV
A3		1	v0.95

DRAWN BY	SHEET	of	
G.K.	10	23	01/12/2016:18:22

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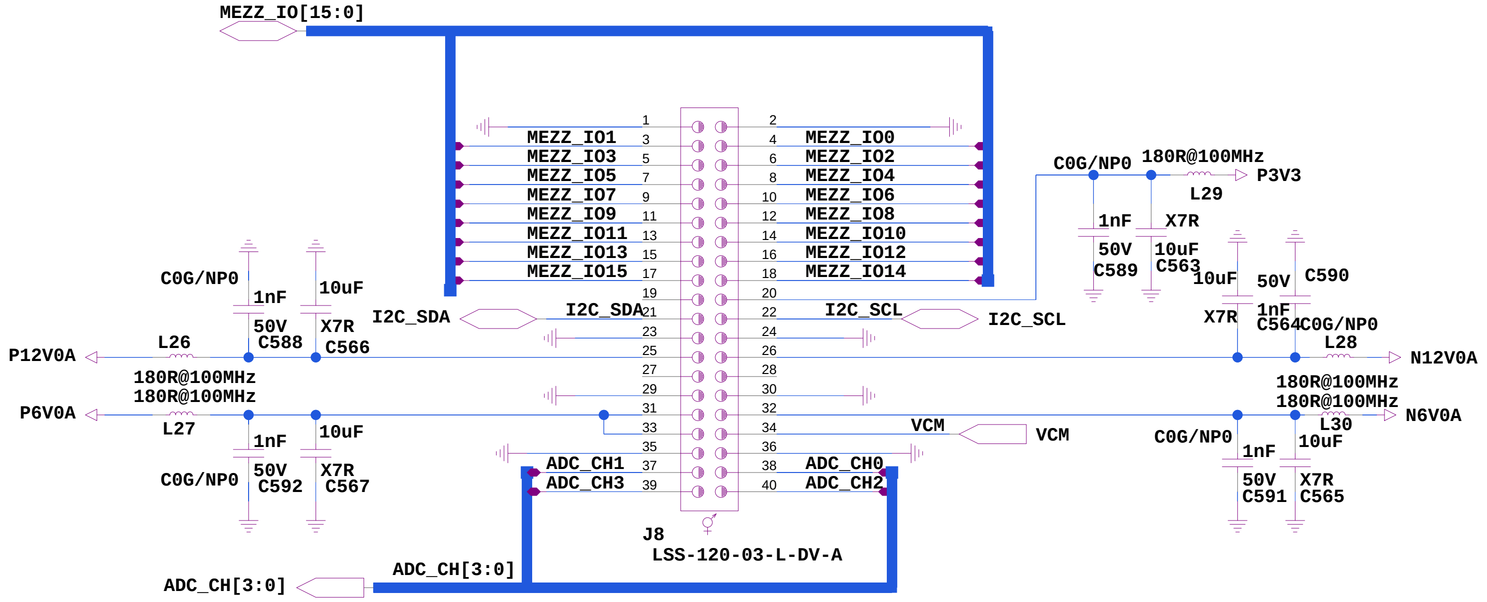

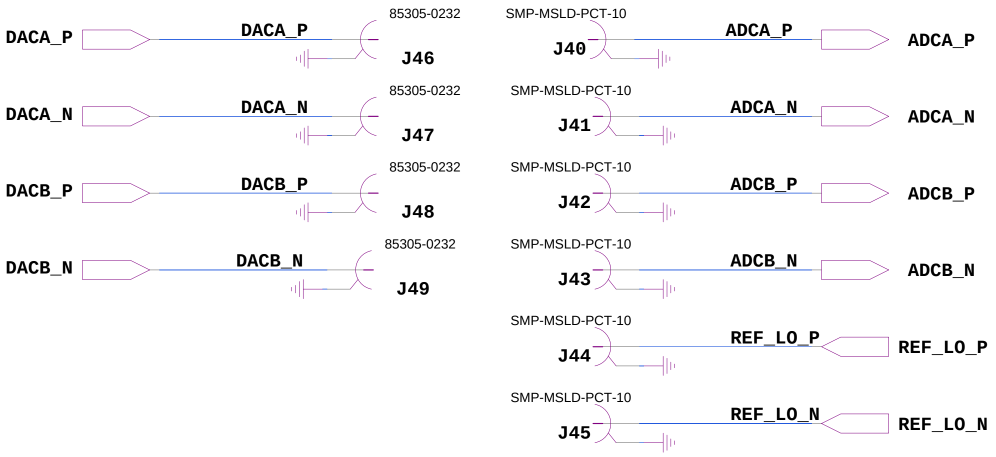

+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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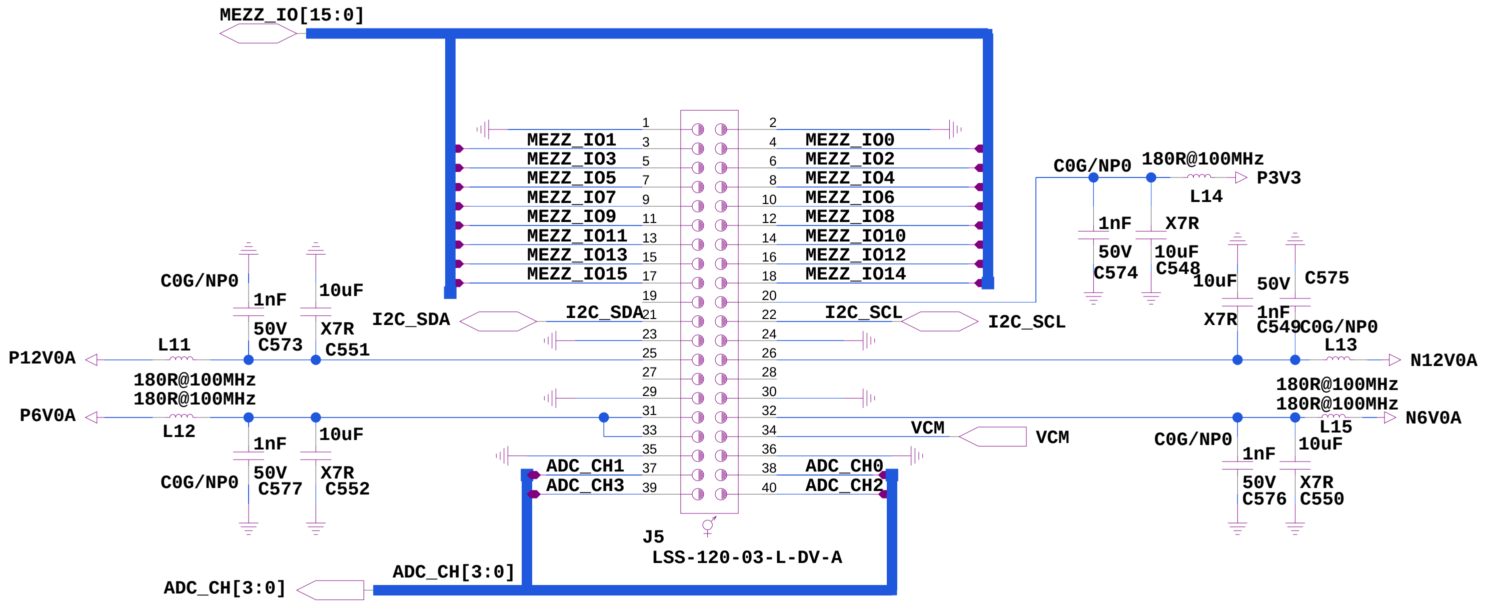
ARTIQ

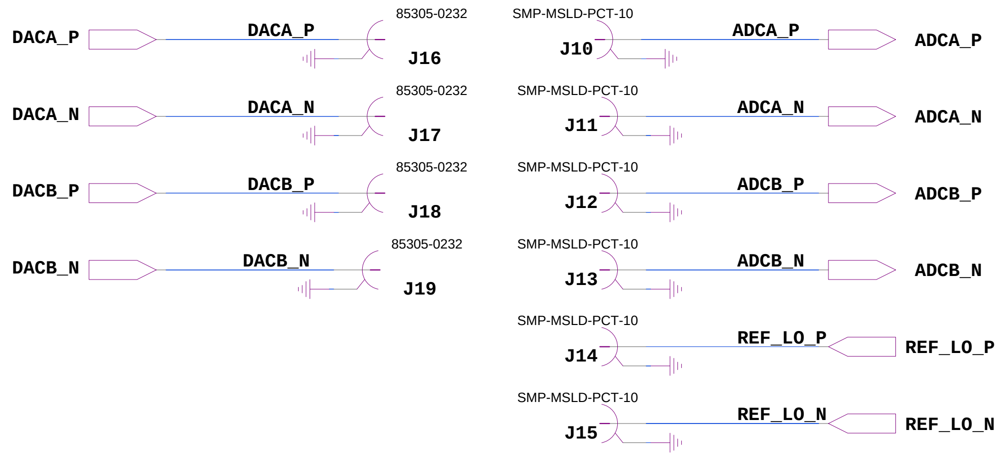
ADC_DAC_AFE_Mezzanine

TITLE

ARTIQ Sinara

SIZE A3
DWG NO 1
REV v0.95
DRAWN BY G.K.
SHEET 11 of 23
03/12/2016:19:15





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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ARTIQ

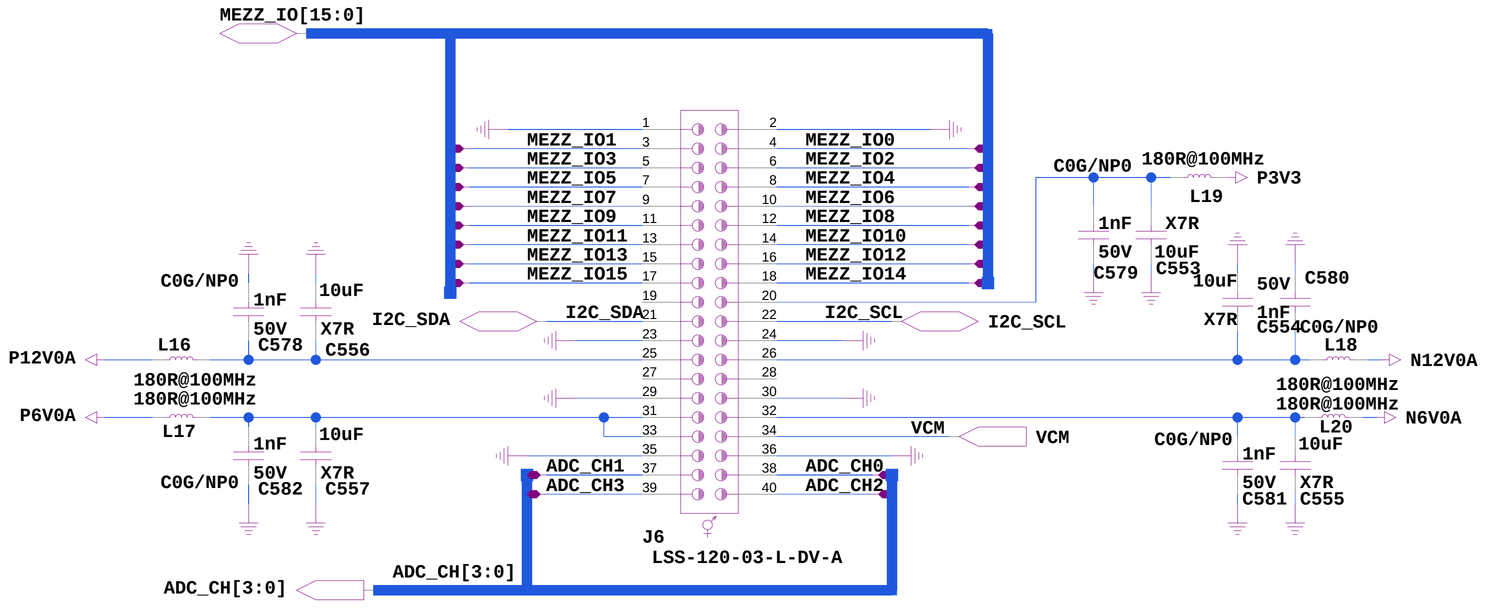
ADC_DAC_AFE_Mezzanine

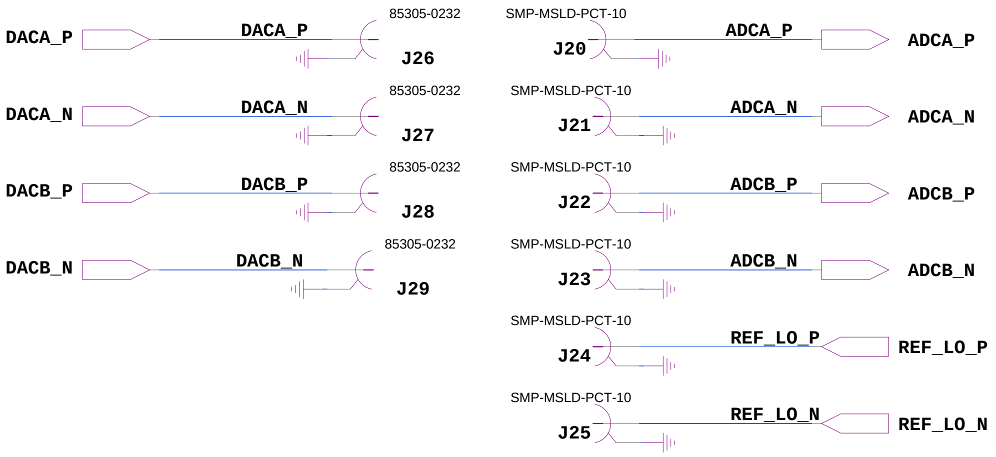
TITLE

ARTIQ Sinara

SIZE	DWG NO		REV
A3		1	v0.95

DRAWN BY	SHEET	of	
G.K.	12	23	03/12/2016:19:15





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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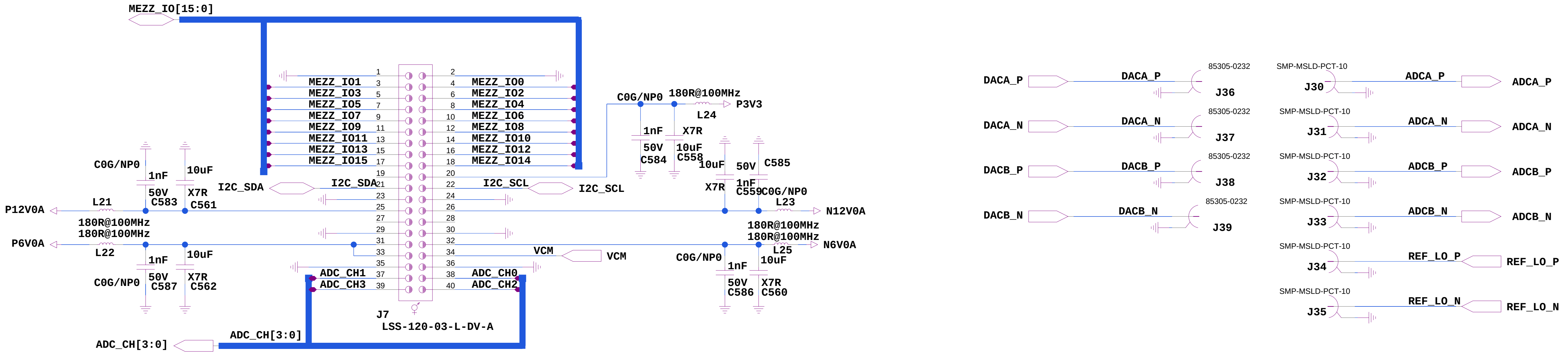
ARTIQ

ADC_DAC_AFE_Mezzanine

TITLE

ARTIQ Sinara

SIZE A3
DWG NO 1
REV v0.95
DRAWN BY G.K.
SHEET 13 of 23
03/12/2016:19:15



+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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ARTIQ

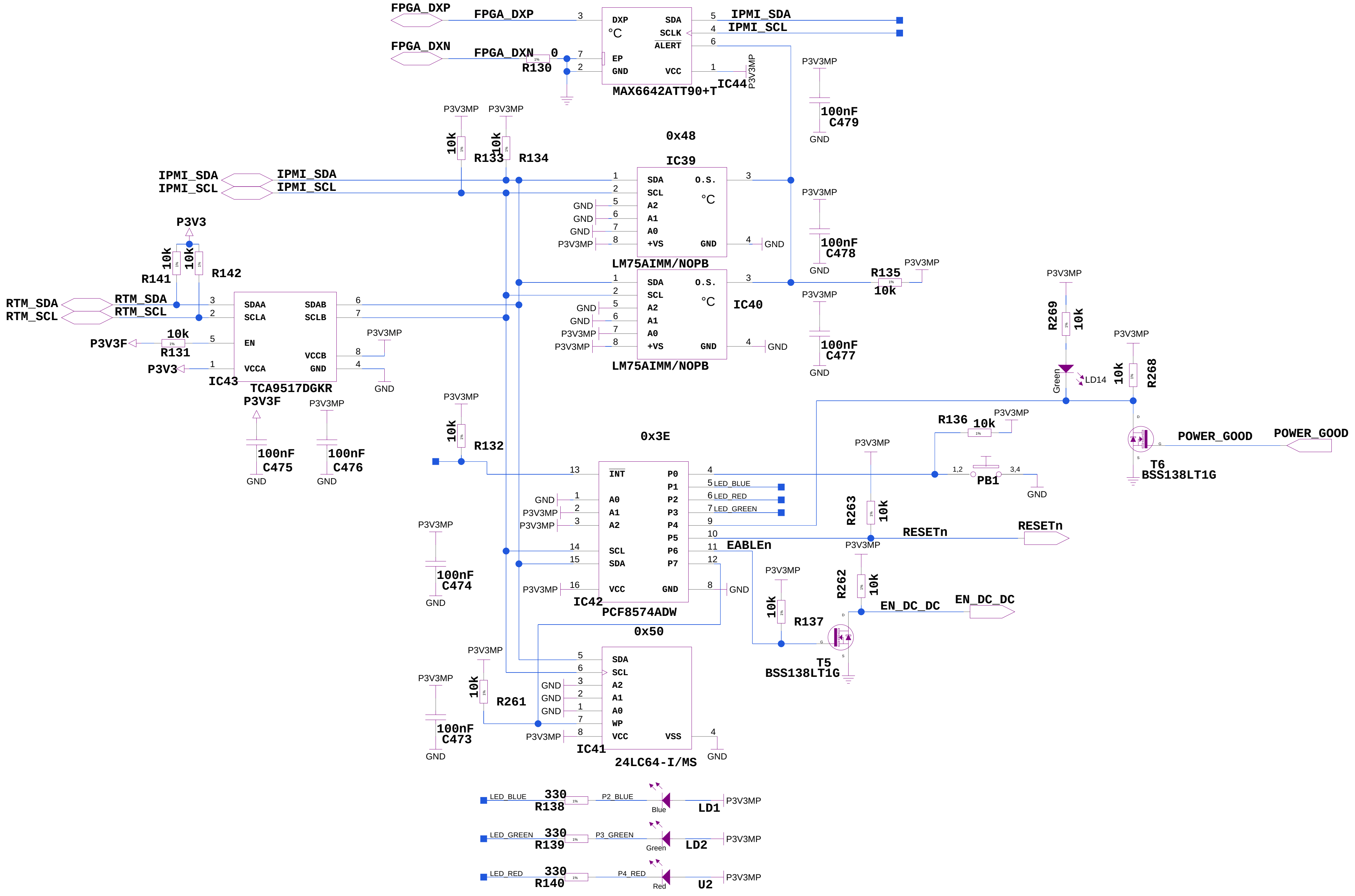
ADC_DAC_AFE_Mezzanine

TITLE

ARTIQ Sinara

SIZE	DWG NO		REV
A3		1	v0.95

DRAWN BY	SHEET	of	
G.K.	14	23	03/12/2016:19:15



check addresses

ARTIQ Sinara

TITLE

RTM_IPMI

SIZE	DWG NO		REV
A3		1	v0.95

DRAWN BY	SHEET	of	
G.K.	15	23	06/12/2016:15:39

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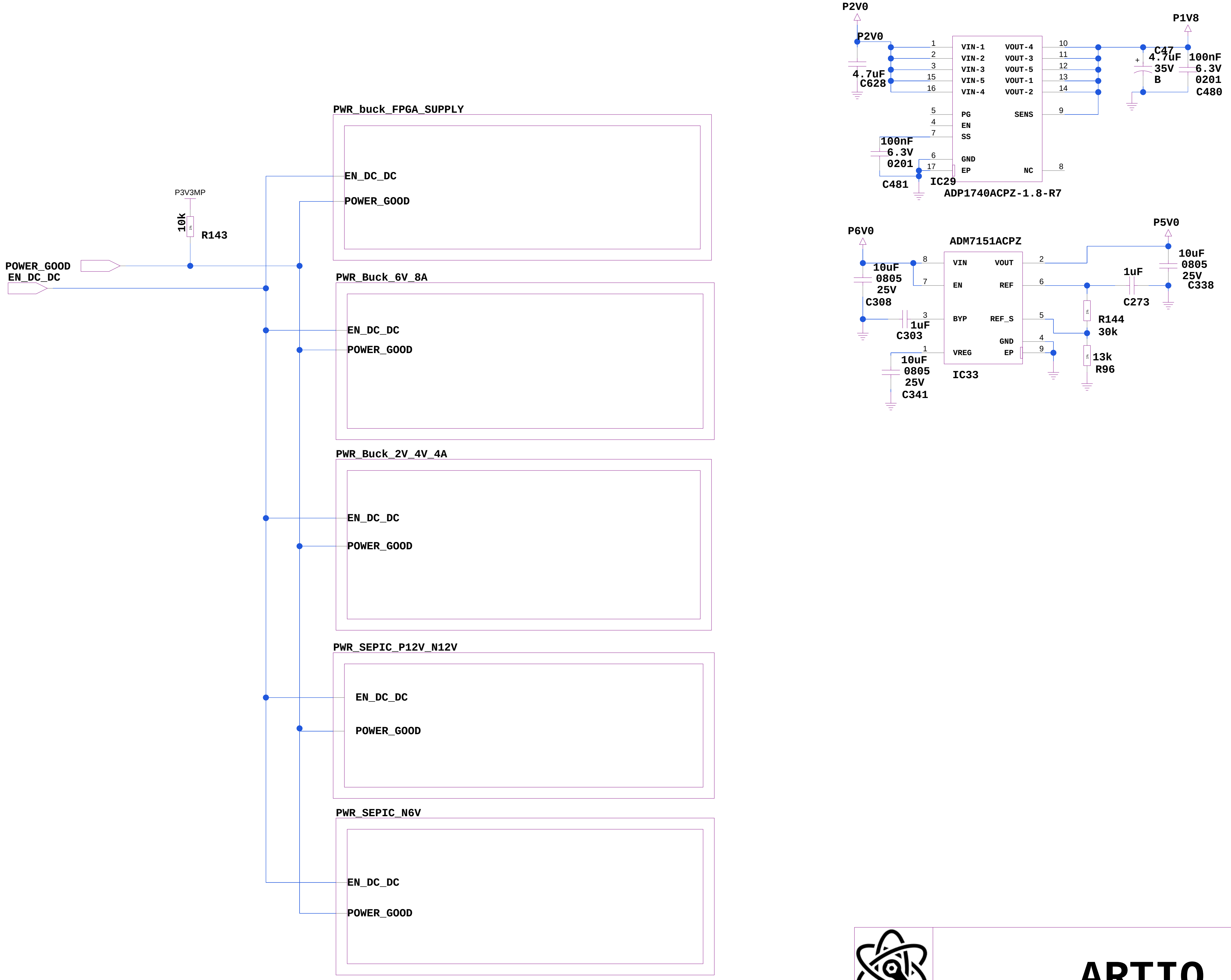

RTM modules power requirements

+12VDC @ 1A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 250 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 8 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 750 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

RTM power requirements

+4VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz
+2VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

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ARTIQ

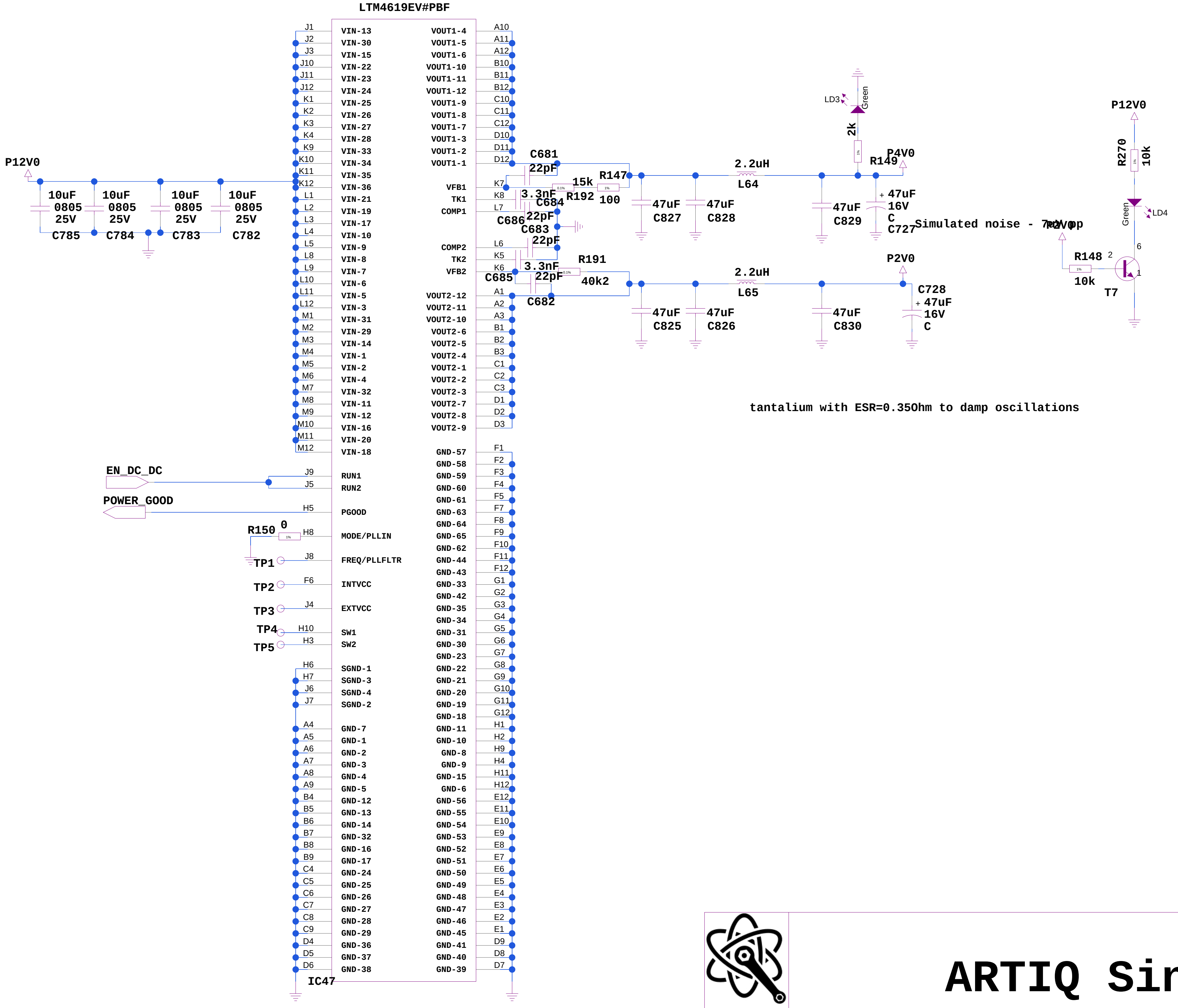
ARTIQ Sinara

TITLE

RTM_POWER_SUPPLY

SIZE A3
DWG NO 1
REV v0.95

DRAWN BY G.K.
SHEET 16 of 23
07/12/2016:17:22



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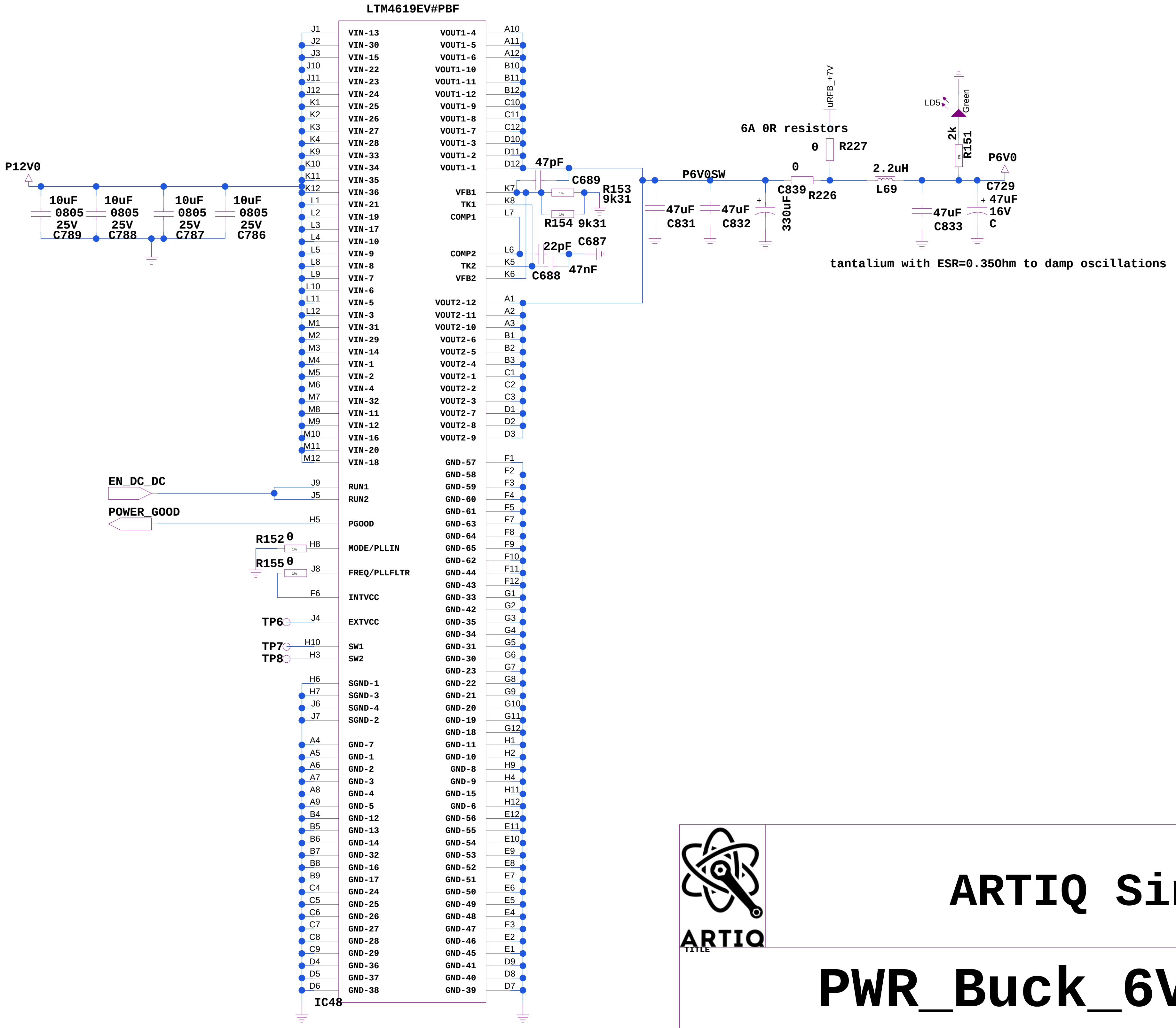
ARTIQ Sinara

TITLE

PWR_Buck_2V_4V_4A

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	17	23	01/12/2016:18:22



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ARTIQ

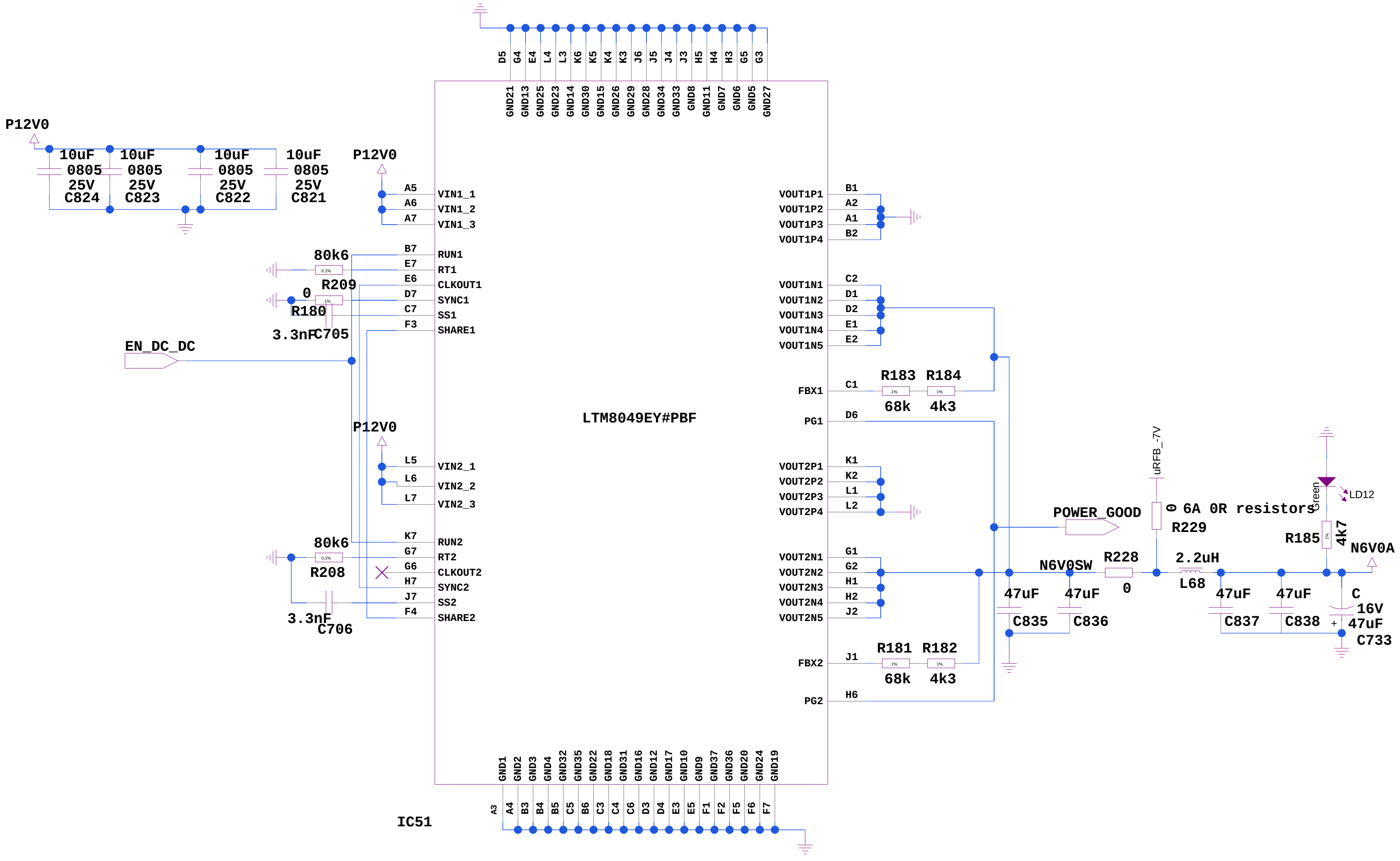
ARTIQ Sinara

TITLE

PWR_Buck_6V_8A

SIZE	DWG NO		REV
A3		1	v0.95

DRAWN BY	SHEET	of	
G.K.	18	23	05/12/2016:00:10



ARTIQ Sinara

TITLE

PWR_SEPIC_N6V

SIZE A3

DWG NO 1

REV v0.95

DRAWN BY G.K.

SHEET 19 of 23

05/12/2016:00:11

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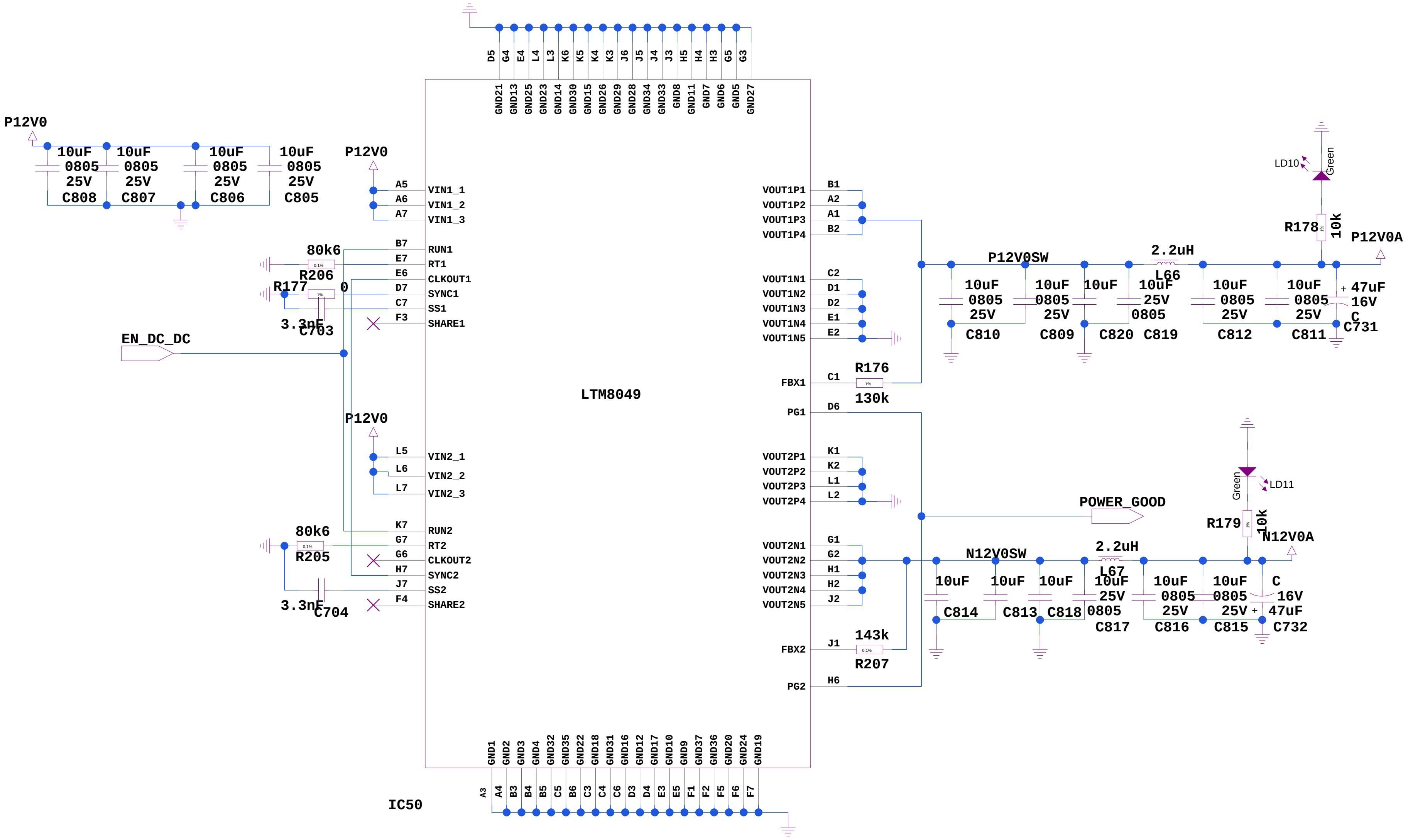

ARTIQ Sinara

TITLE

PWR_SEPIC_P12V_N12V

SIZE
A3

DWG NO
1

REV
v0.95

DRAWN BY
G.K.

SHEET 20 of 23

05/12/2016:00:11

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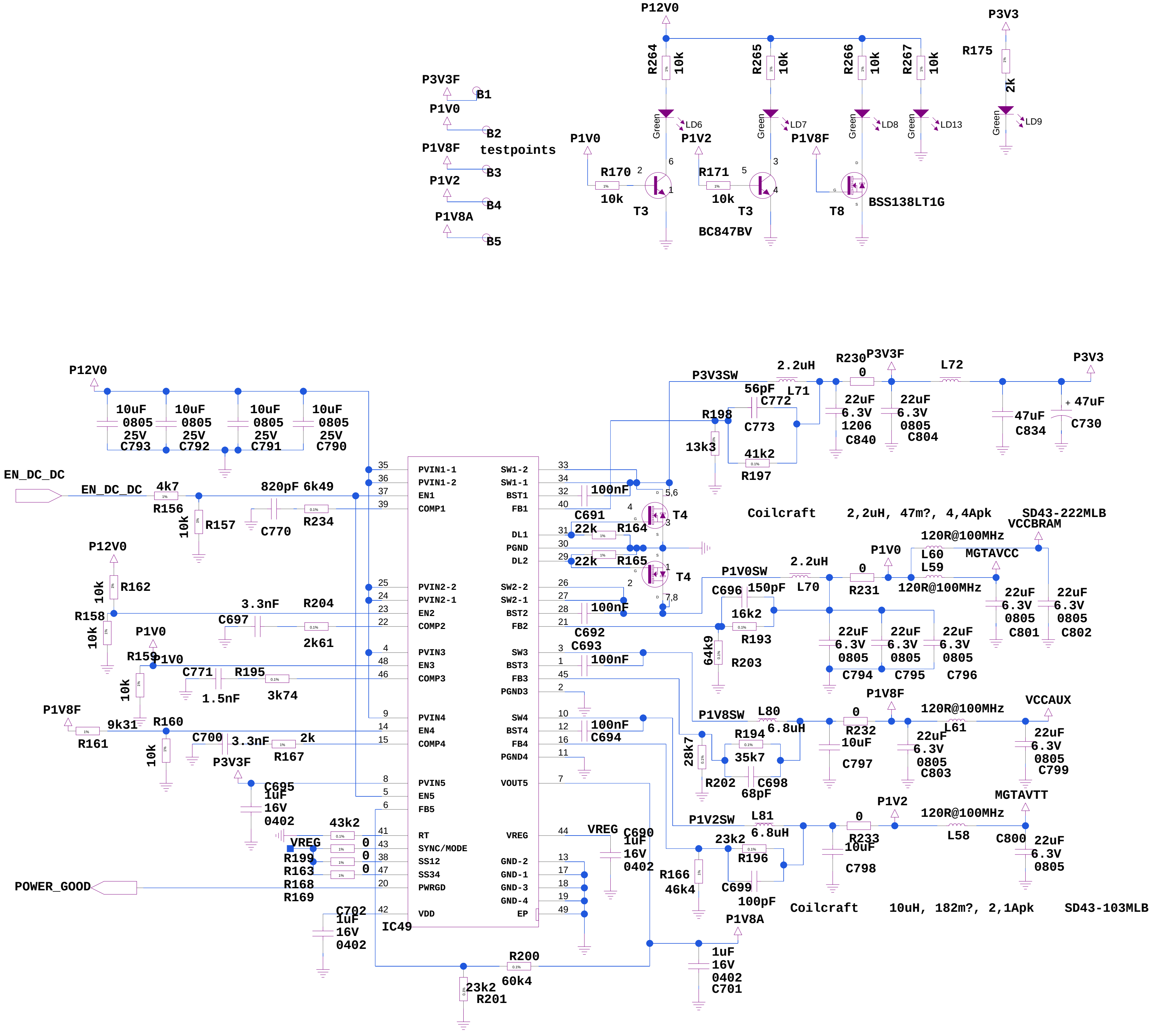

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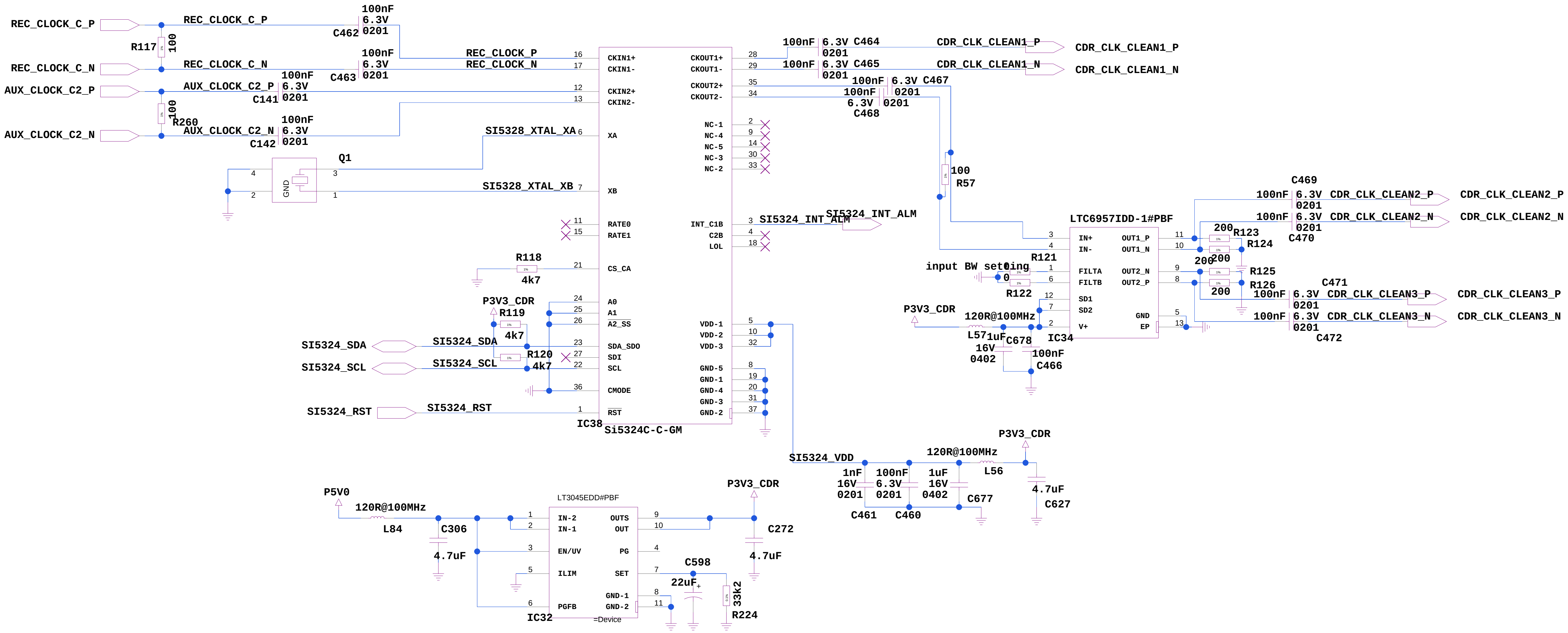
ARTIQ

ARTIQ Sinara

TITLE
PWR_buck_FPGA_SUPPLY

SIZE	DWG NO	REV
A3	1	v0.95

DRAWN BY	SHEET	of	
G.K.	21	23	07/12/2016:17:22



ARTIQ Sinara

TITLE

SI5324_CLK_RECOVERY

SIZE A3
DWG NO 1
REV v0.95
DRAWN BY G.K.
SHEET 22 of 23
03/12/2016:13:42

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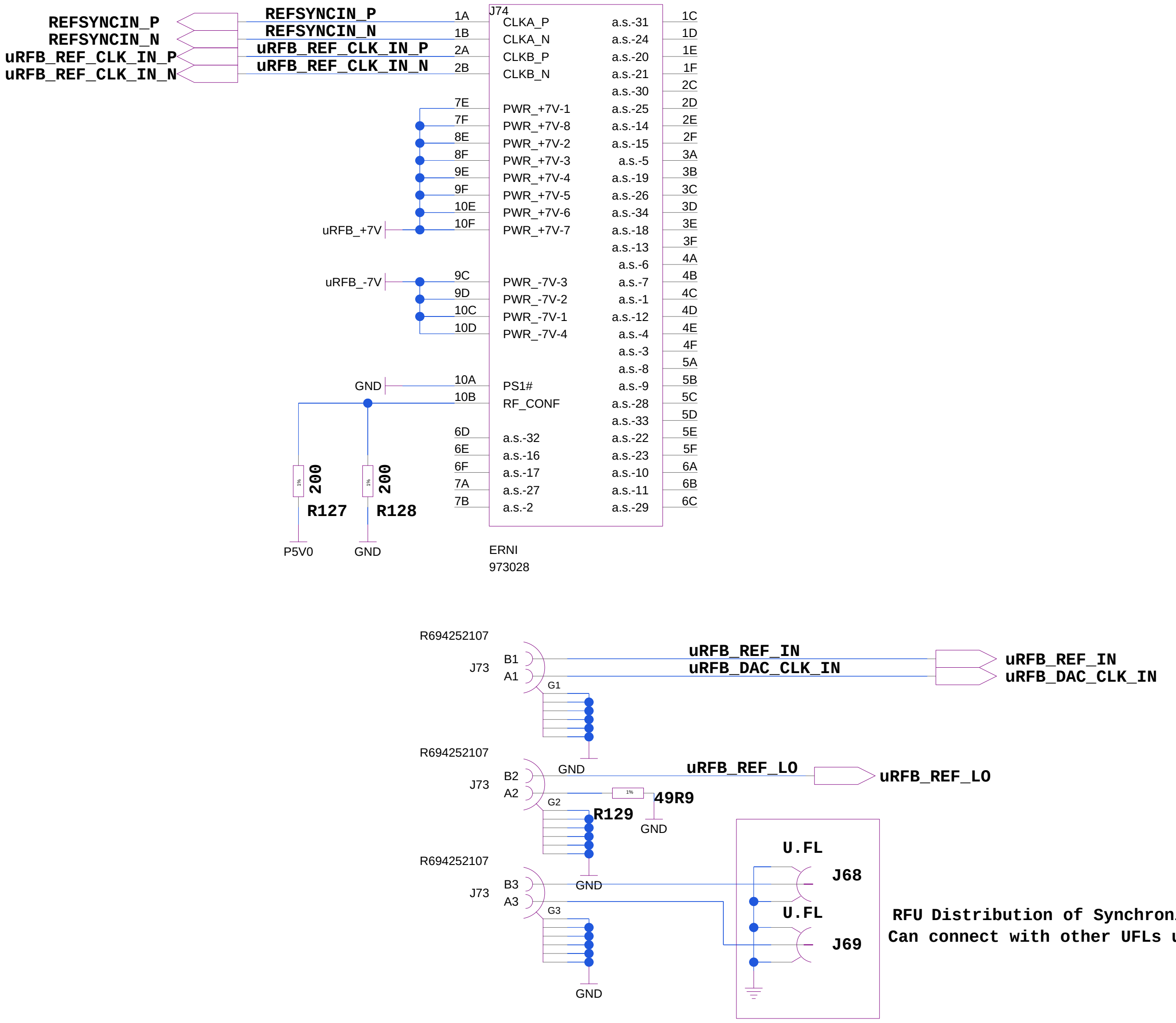

RFU Distribution of Synchronisation signals.
Can connect with other UFLs using jumper cables

uRFB_Connectors

TITLE

ARTIQ Sinara

SIZE A3
DWG NO 1
REV v0.95
DRAWN BY G.K.
SHEET 23 of 23
03/12/2016:13:55

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