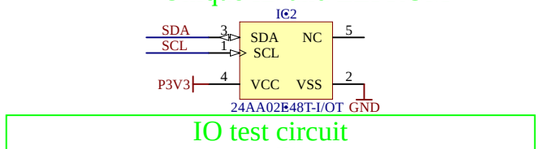
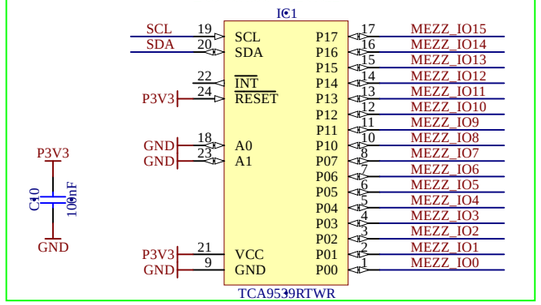
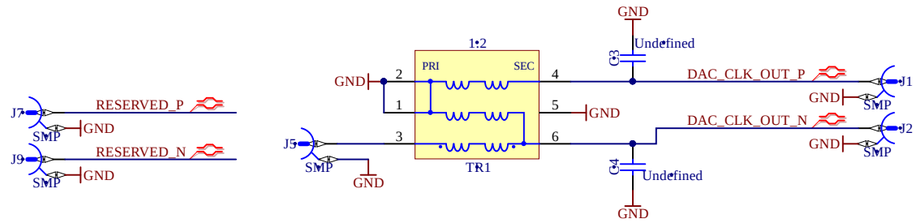
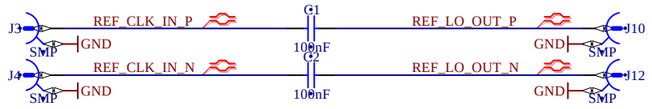
Unique ID and EEPROM



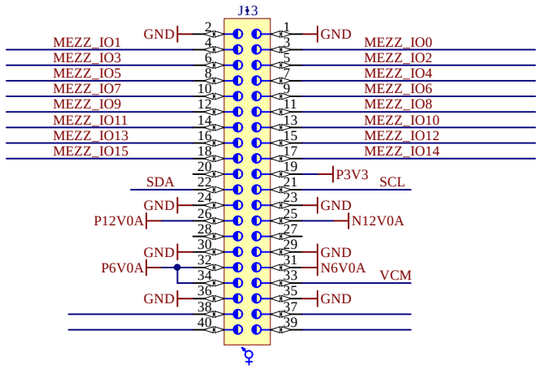
IO test circuit

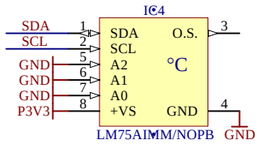




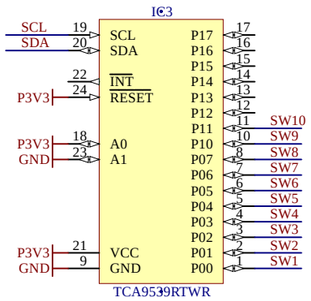


4x M2.5 Standoff M1256-2545-AL

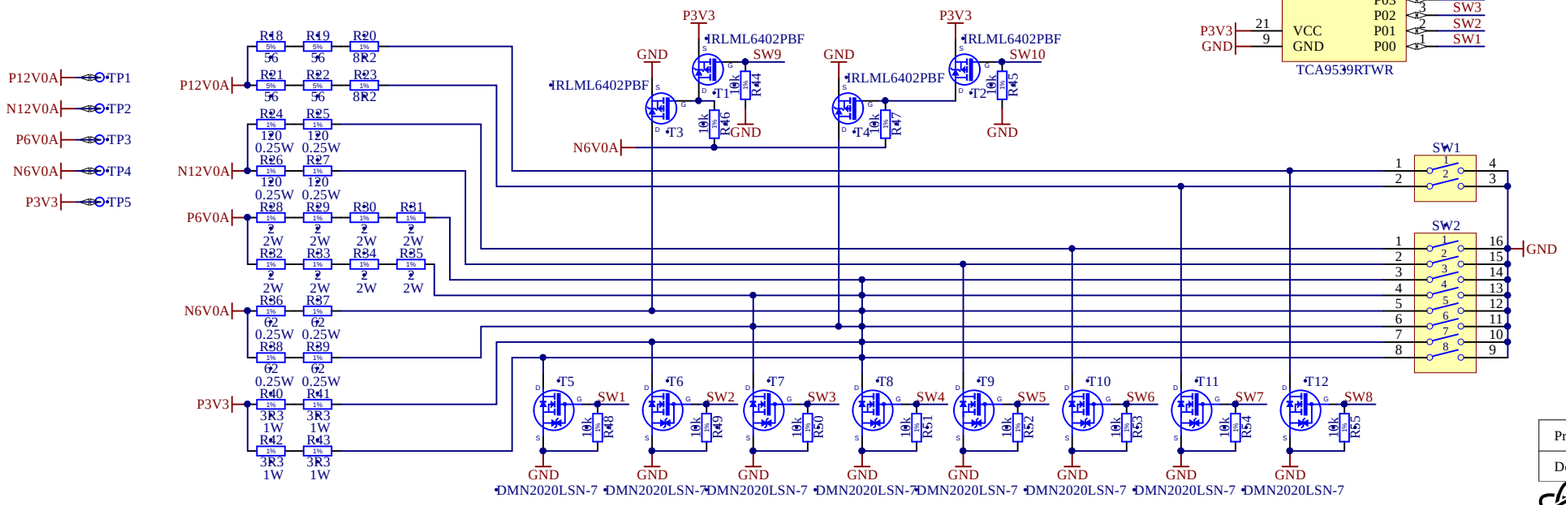




Interfaces with: Sayma RTM connector
DAC_CLK : LVPECL
REF_LO: LVPECL
MEZ_CLK_IN - LVPECL
Impedance 100Ohm diff
Control signals: LVCMOS 3.3V
I2C signals: LVCMOS 3.3V
+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

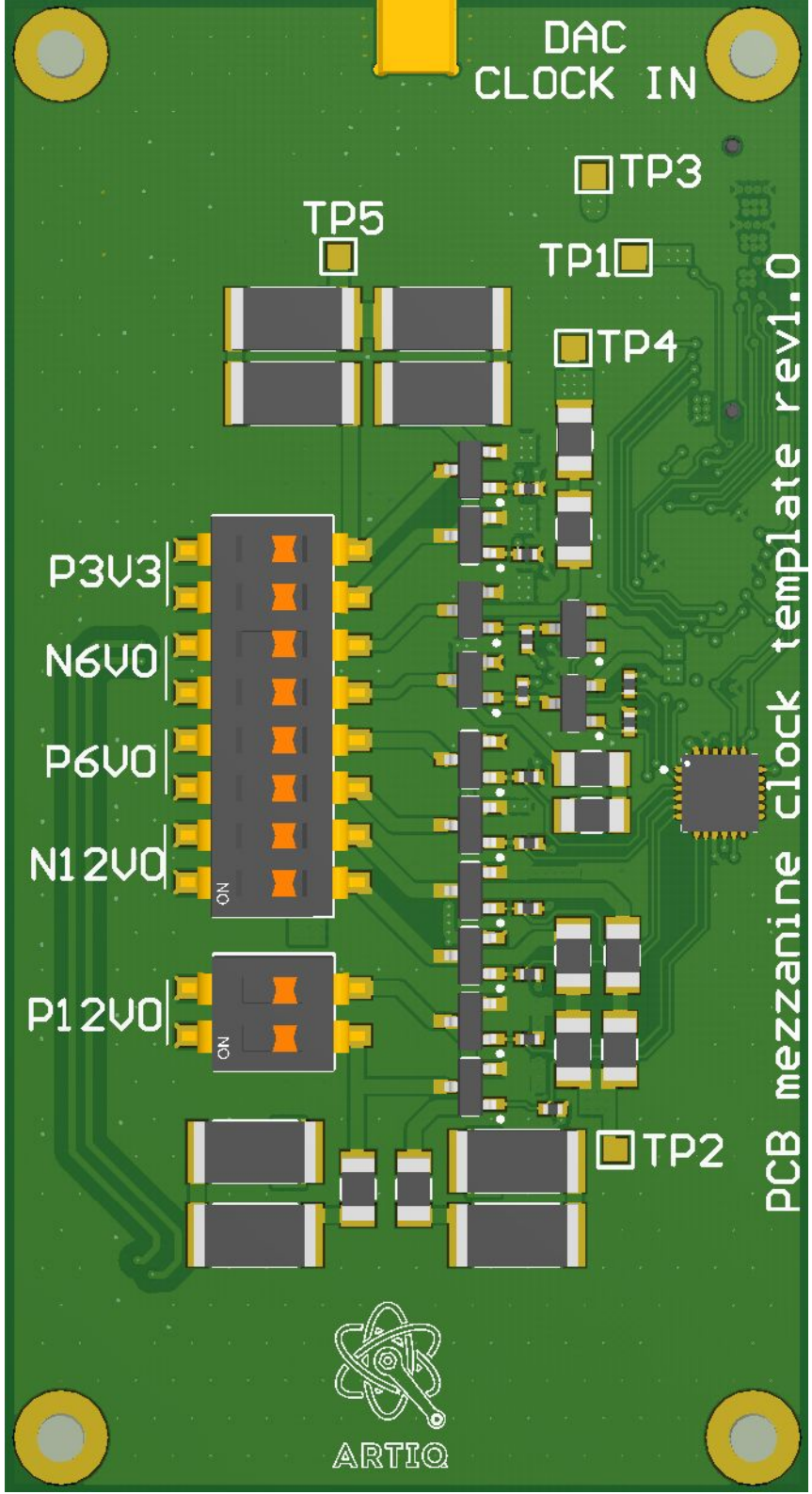


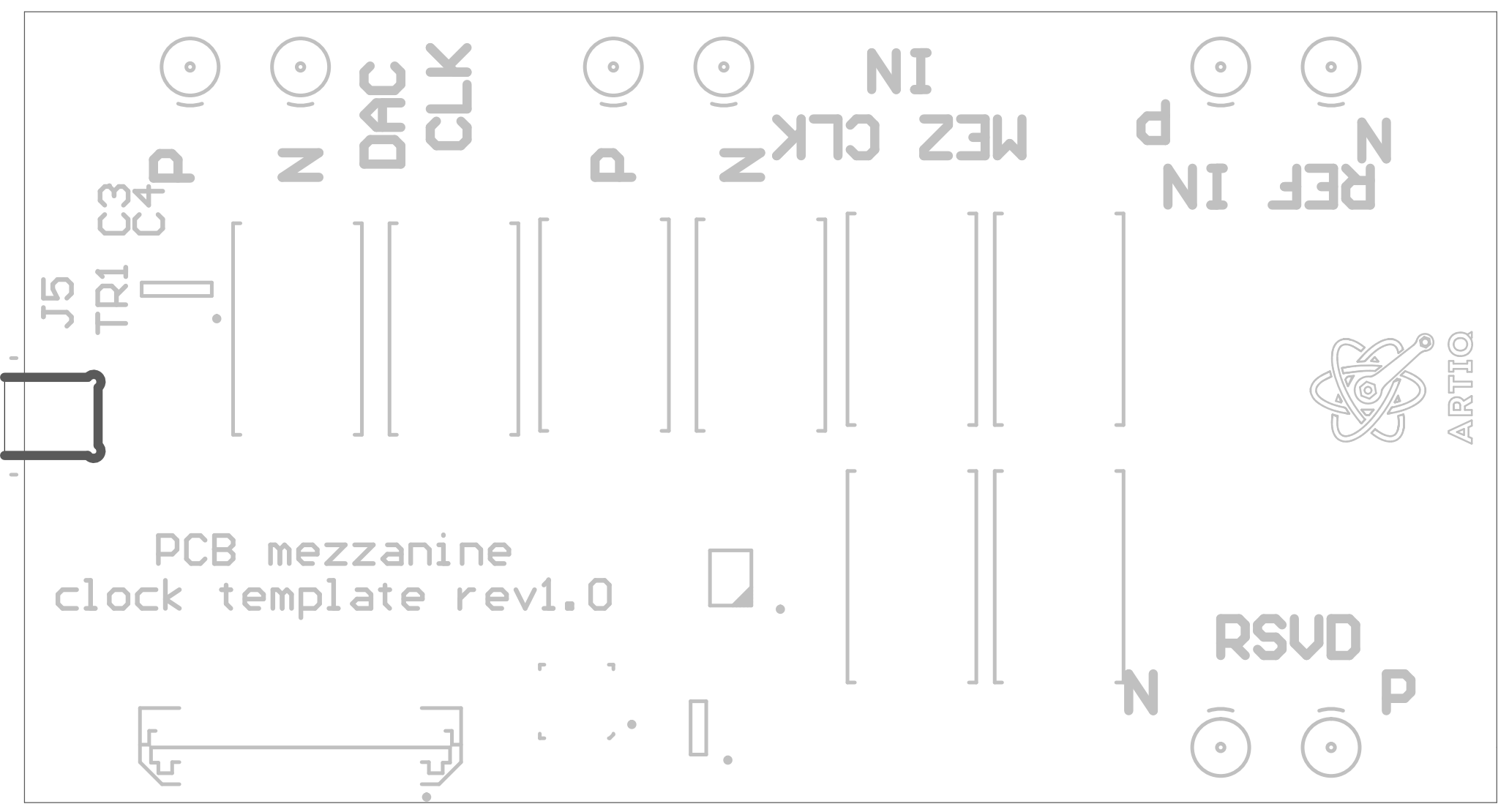
4x M2.5 Standoff M1256-2545-AL

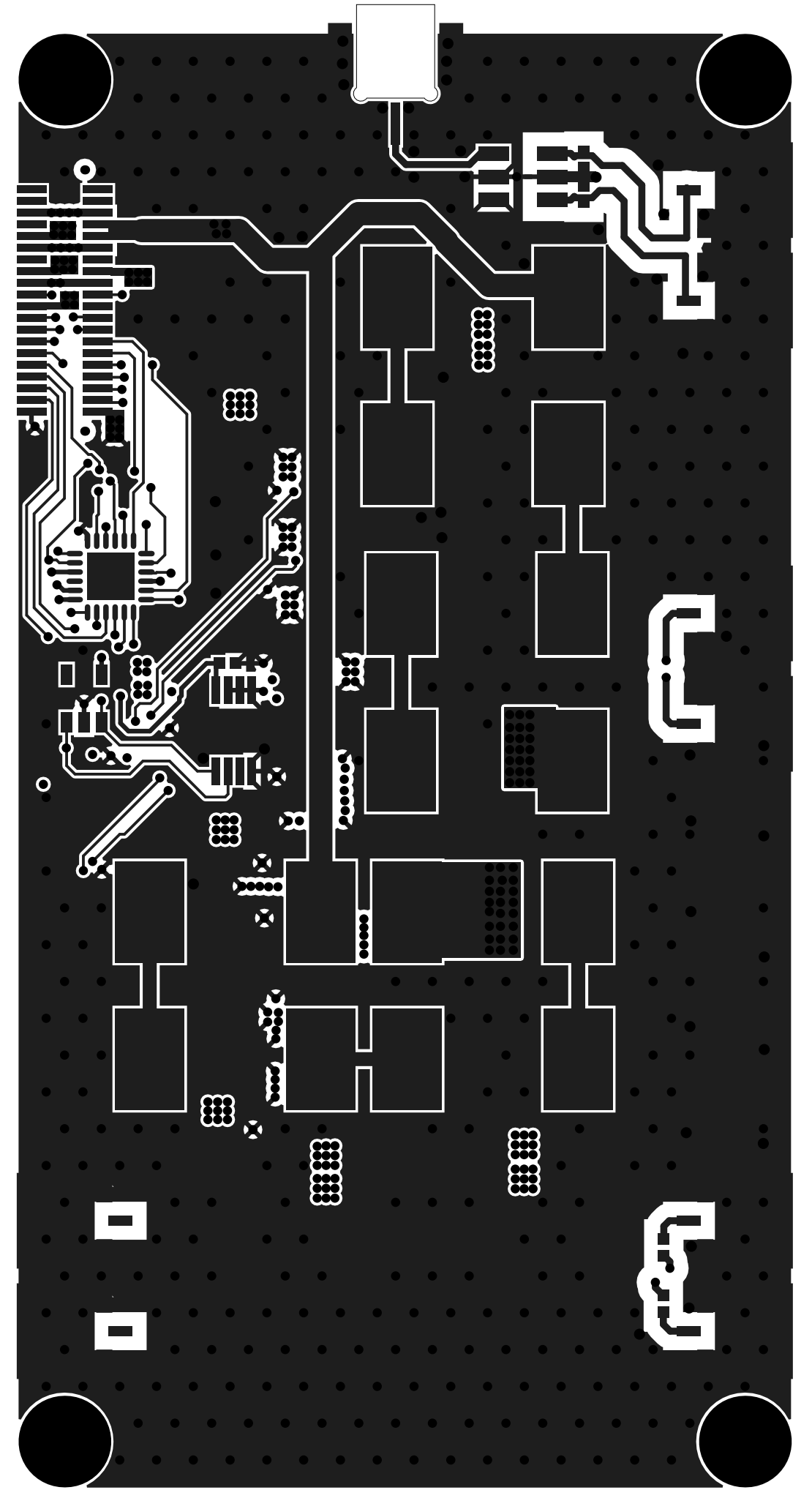


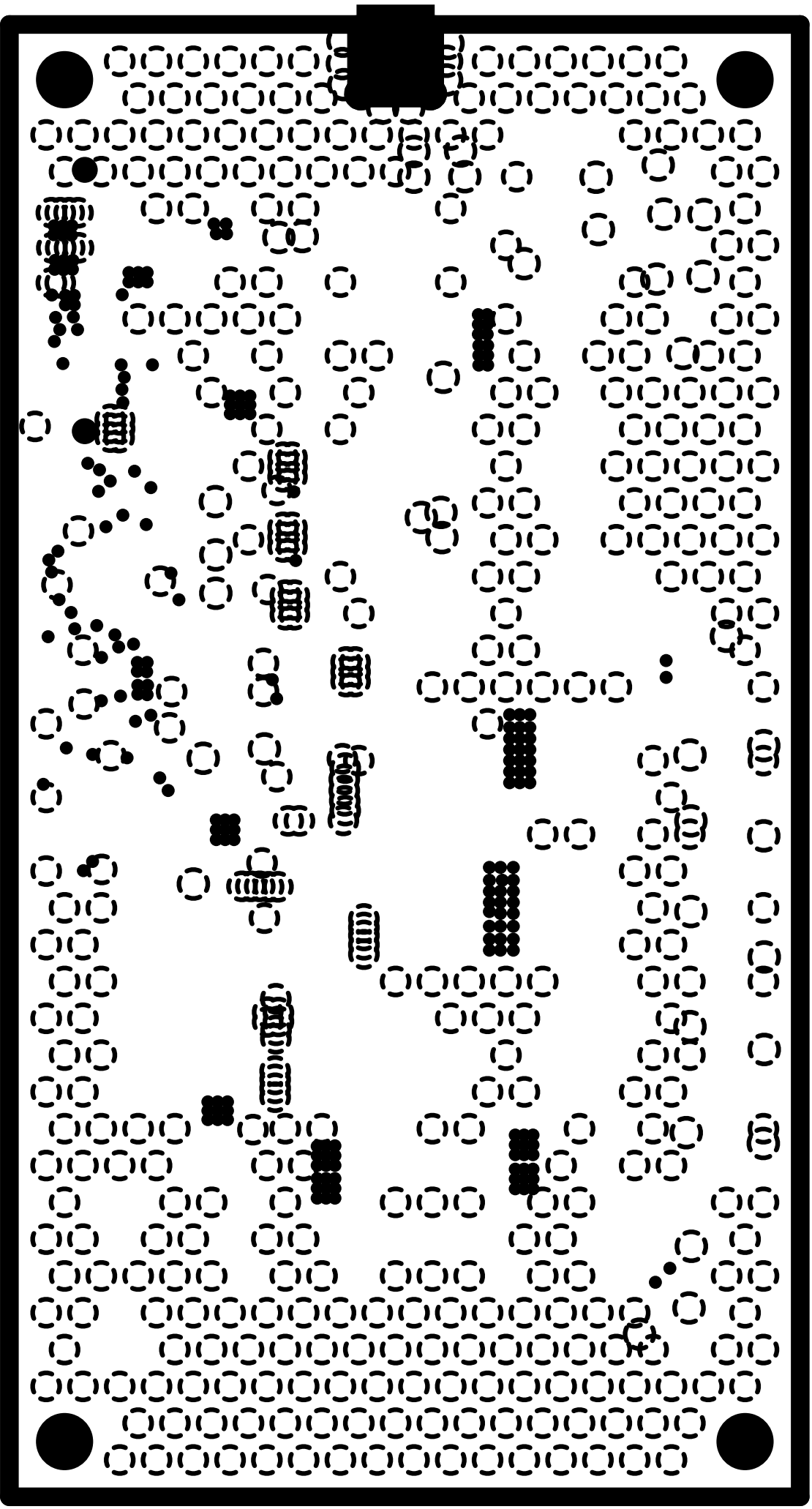
Project/Equipment	ADC/DAC MEZZANINE		
Document	ADC/DAC mezzanine Top entity	Designer G.K.	
		Drawn by G.K.	XX/XX/XXXX
		Check.by	-
		Last Mod. -	01.02.2017
		File	PCB_mezzanine_clock_template.SchDoc
		Print Date 02.02.2017 02:09:25	Sheet - of -
Warsaw Univeristy of Technology Nowowiejska 15/19	ISE	ARTIQ	Size A3 / Rev -

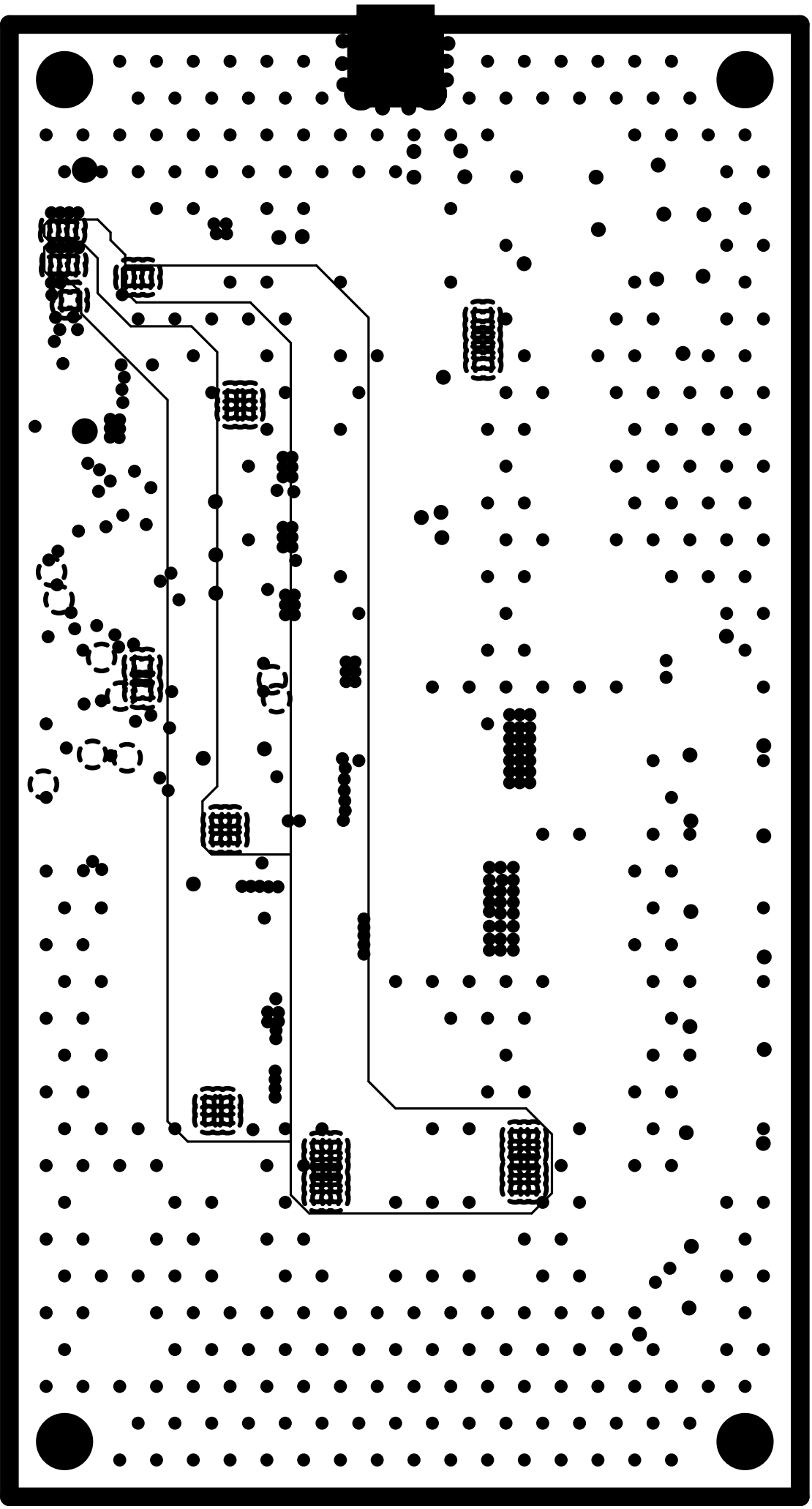
PCB mezzanine
clock template rev1.0
J5
TR1
C3
C4
P
N
DAC
CLK
P
N
MEZ CLK
IN
N
RSVD
P
REF IN
P
N
ARTIQ

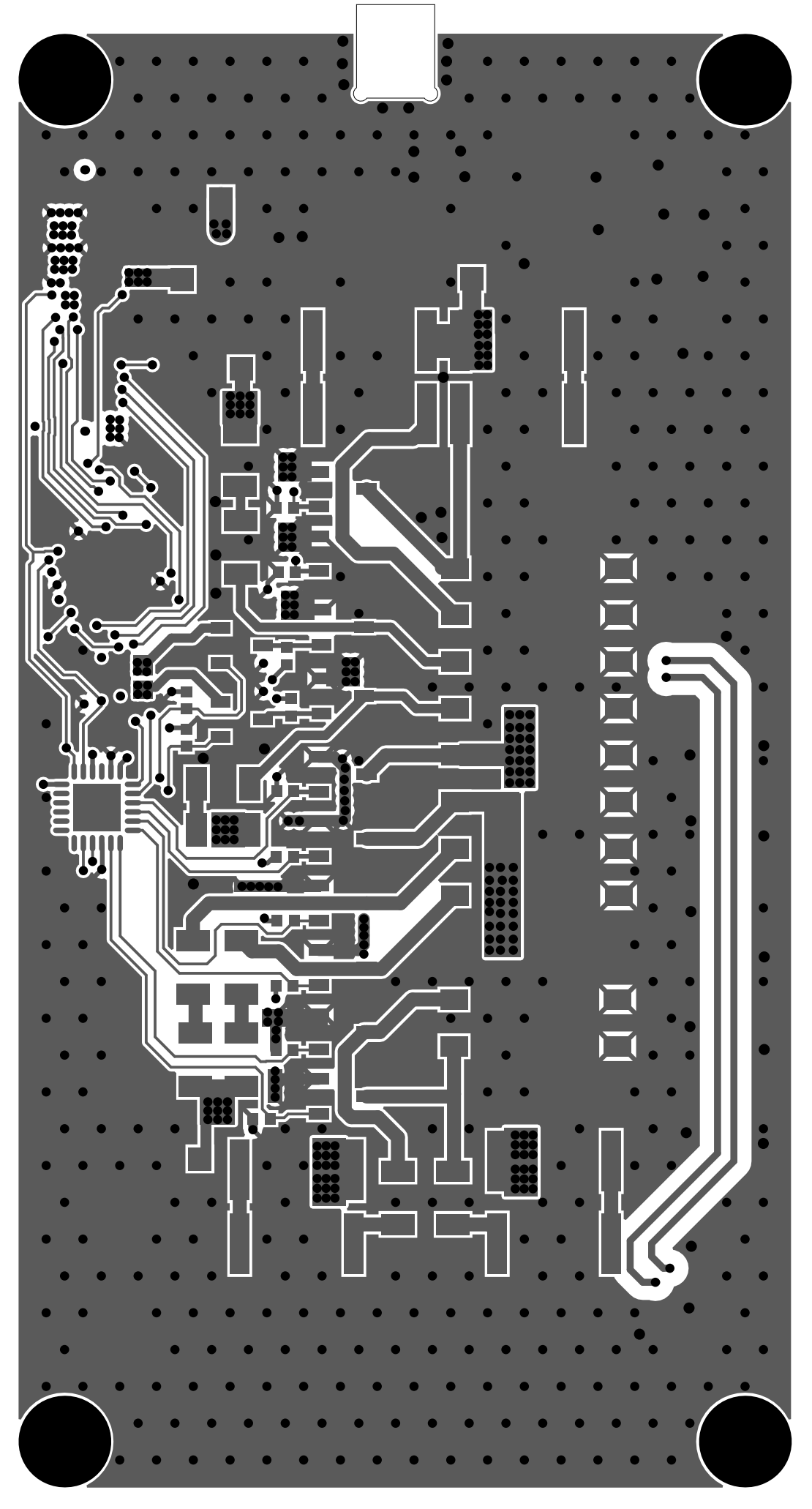

DAC
CLOCK IN
TP3
TP5
TP1
TP4
P3V3
N6V0
P6V0
N12V0
P12V0
ON
ON
TP2
PCB mezzanine clock template rev1.0
ARTIQ

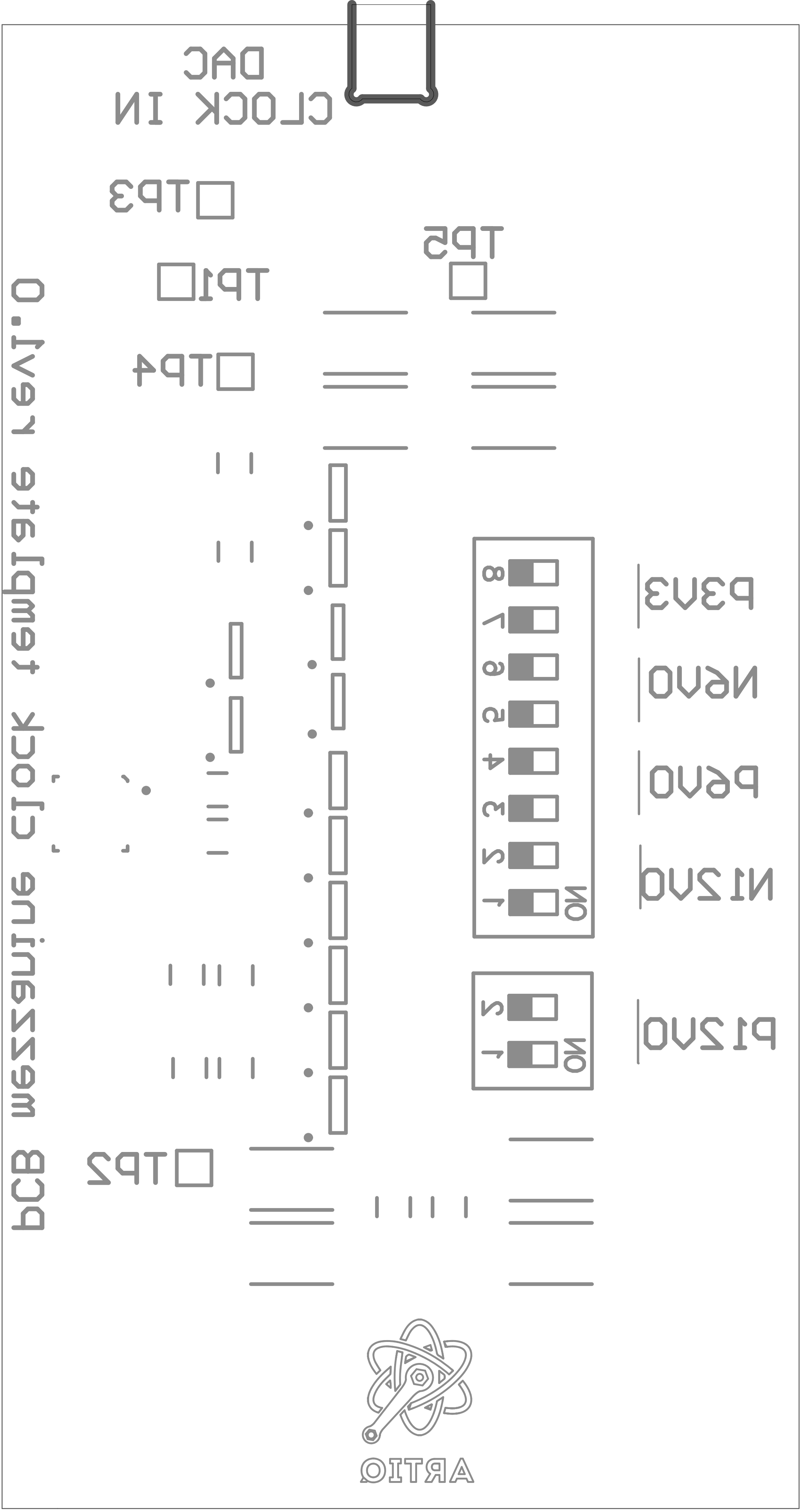

P
N
DAC CLK
P
N
MEZ CLK
N
P
REF IN
J5
TR1
C3
C4
ARTIQ
PCB mezzanine
clock template rev1.0
RSVD
N
P










DAC
CLOCK IN
TP3
TP1
TP5
TP4
TP2
pcb mezzanine clock template rev1.0
P3V3
N6V0
P6V0
N12V0
P12V0
ON
ARTIO