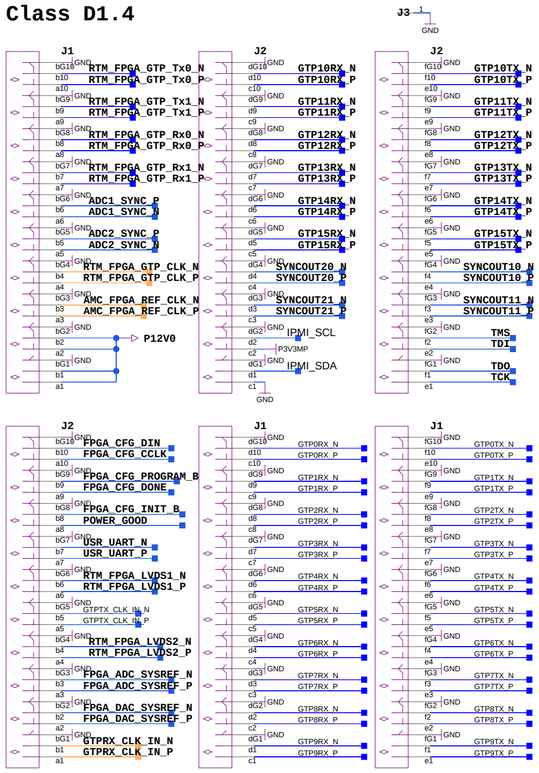
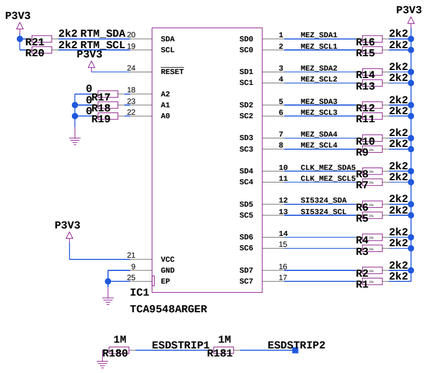
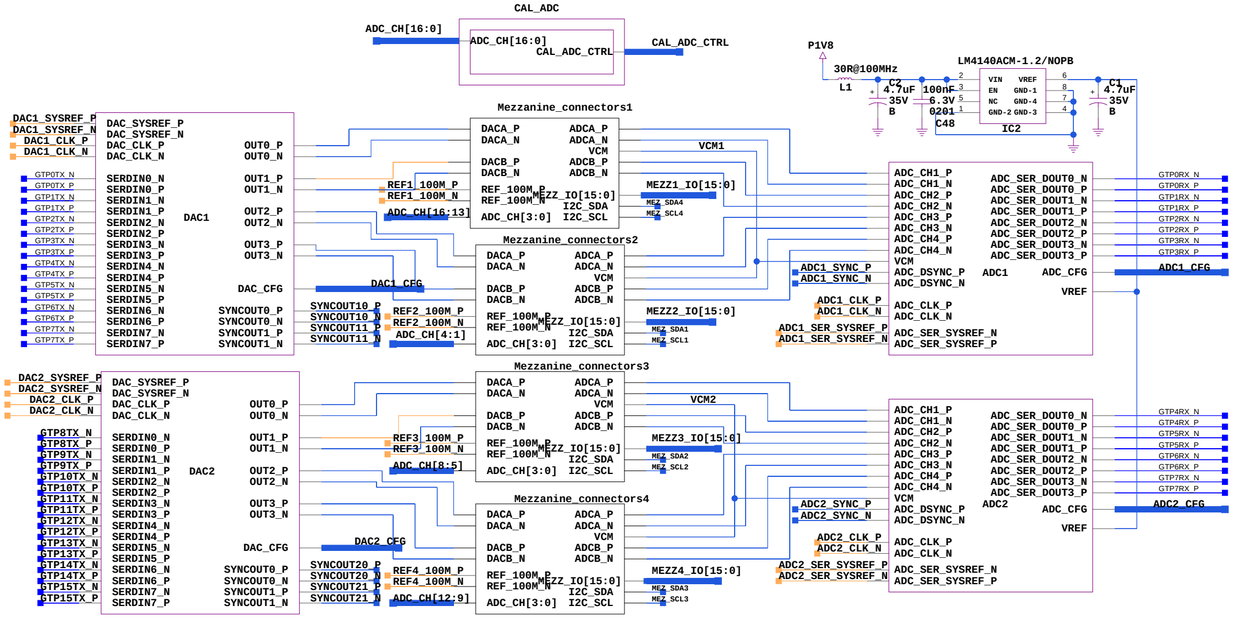
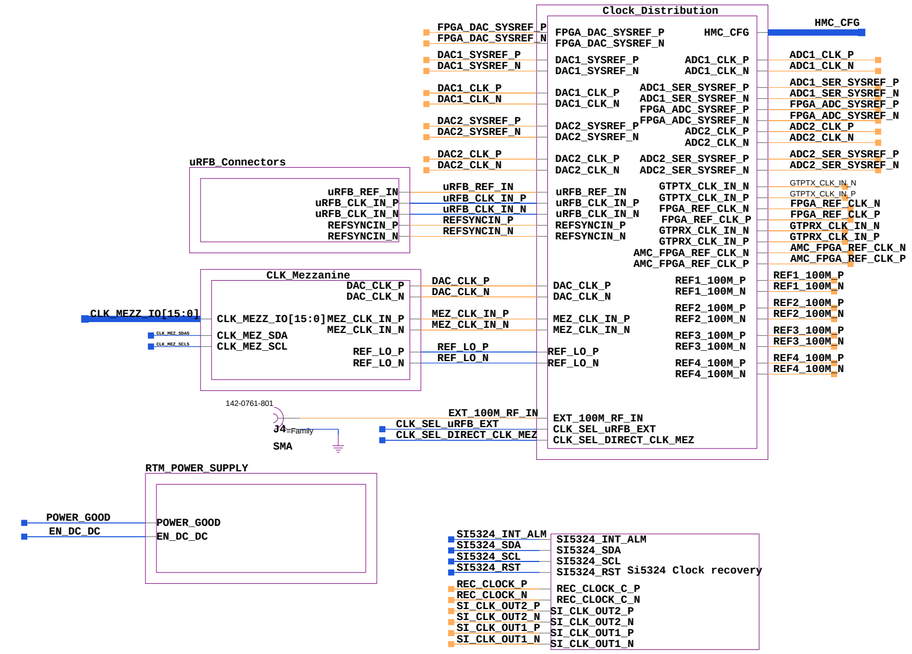
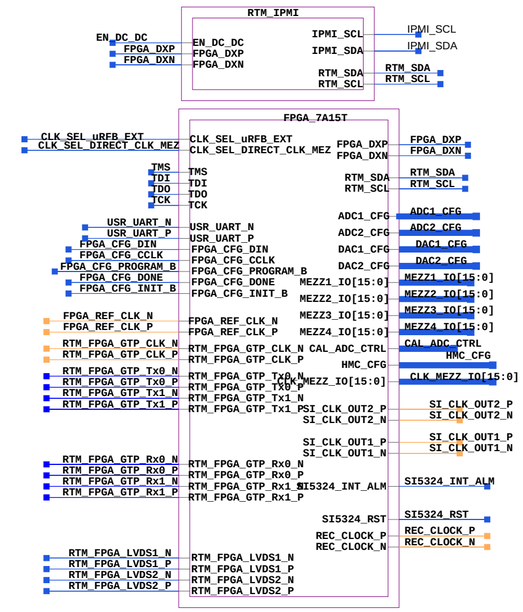
Class D1.4







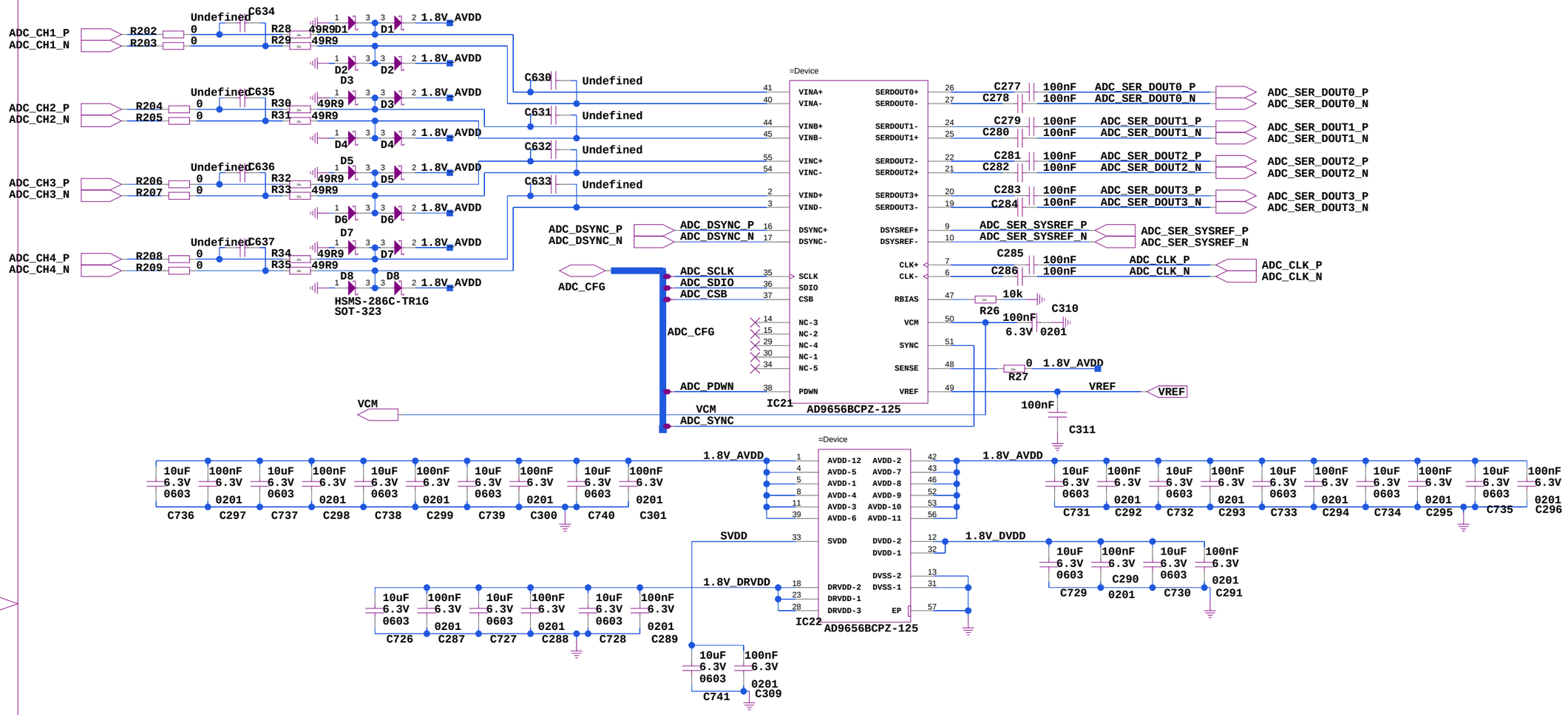


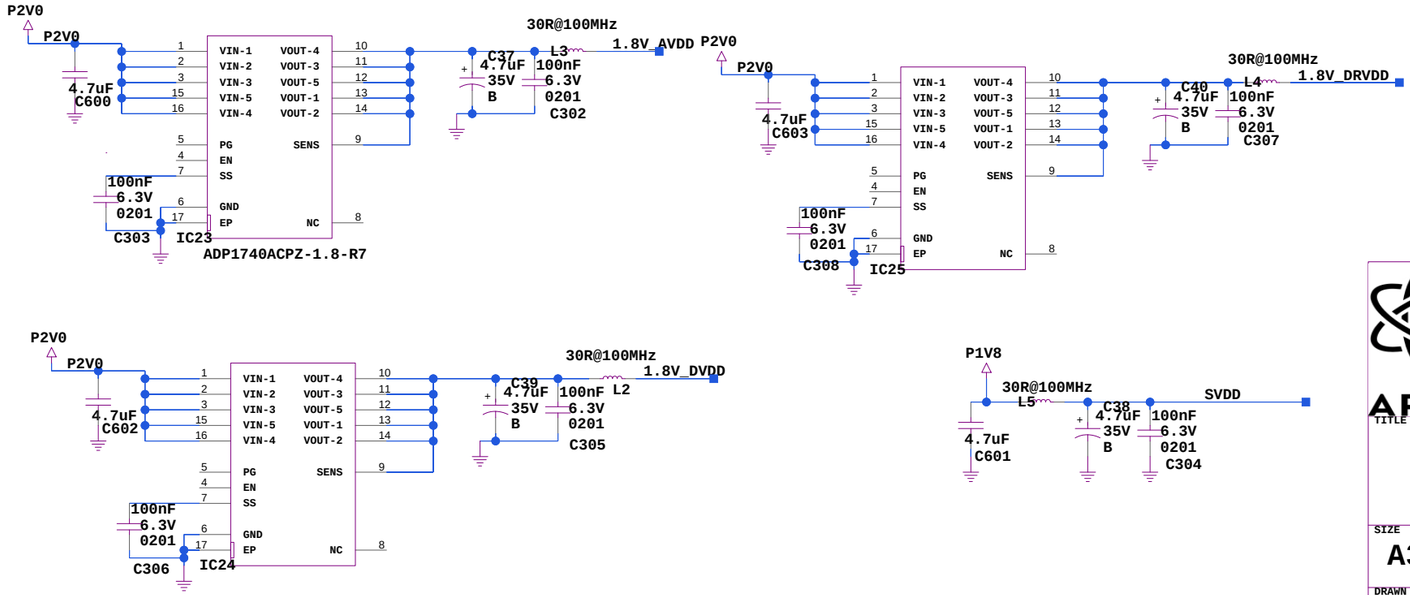


ARTIQ Sayma

Sayma_RTM

TITLE		
SIZE: A2	DWG NO: 1	REV: v0.9
DRAWN BY: G.K.	SHEET: 1 of 18	2016/11/07:18:08:30





ARTIQ

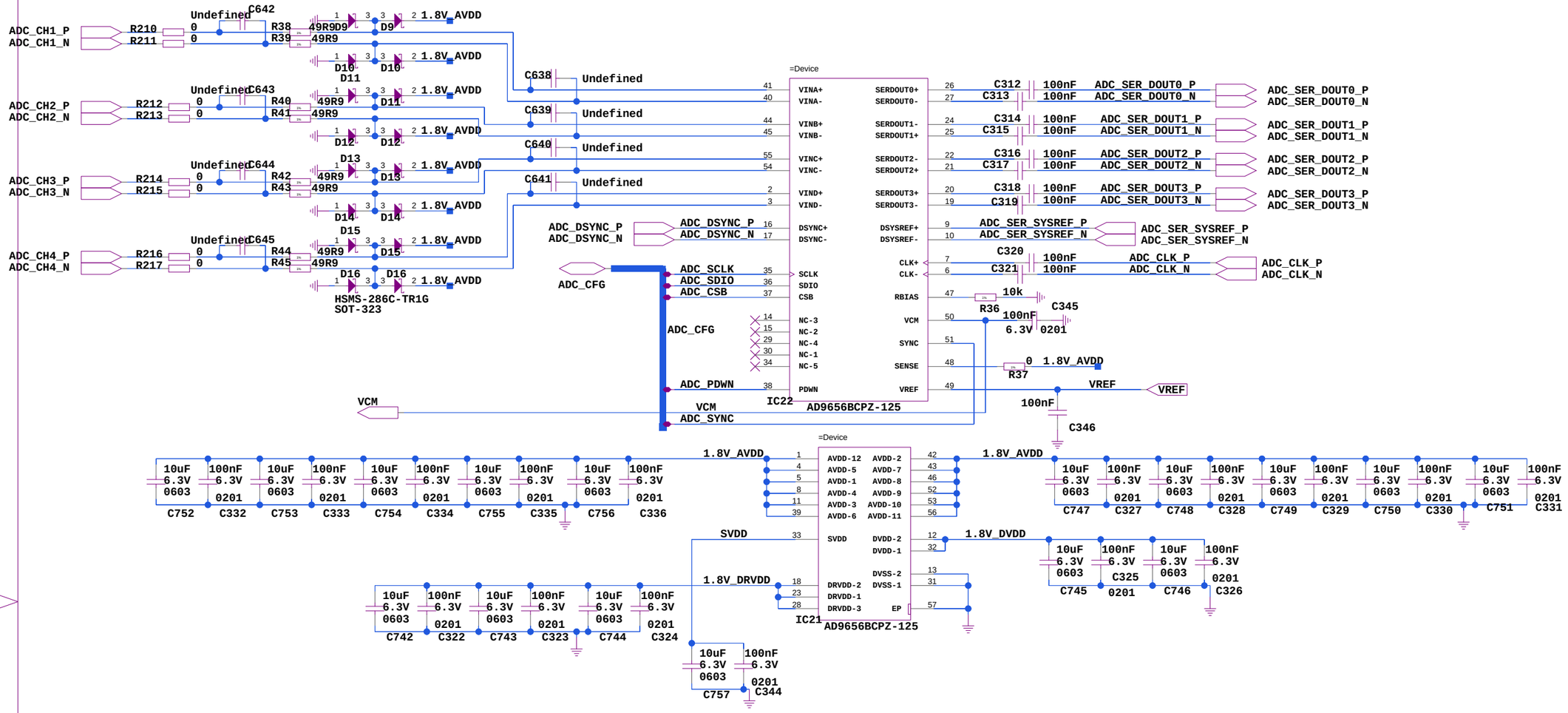
TITLE

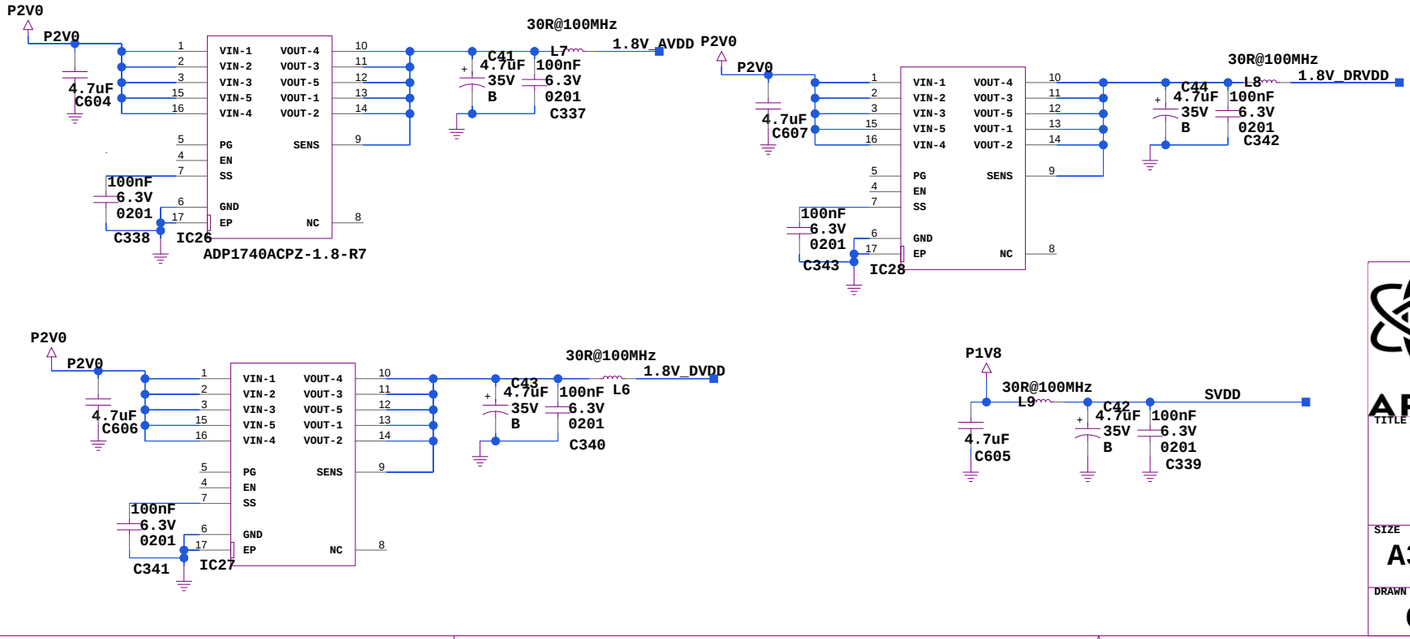
ADC_JESD204B

ARTIQ Sayma

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	2	18	2016/11/07:18:03:54



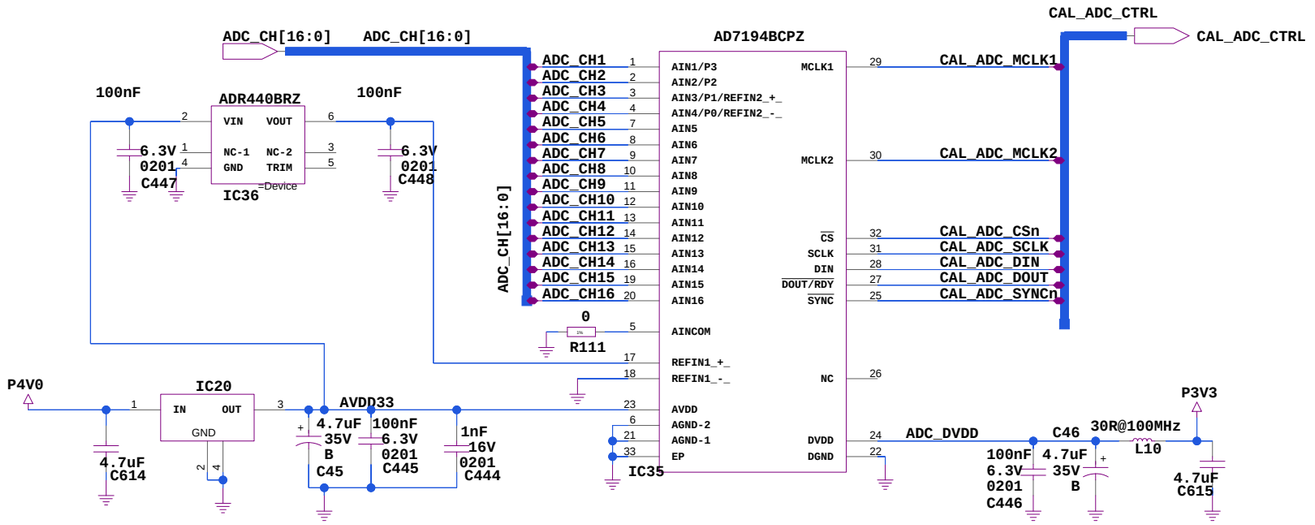


ADC_JESD204B

ARTIQ Sayma

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	3	18	2016/11/07:18:03:54



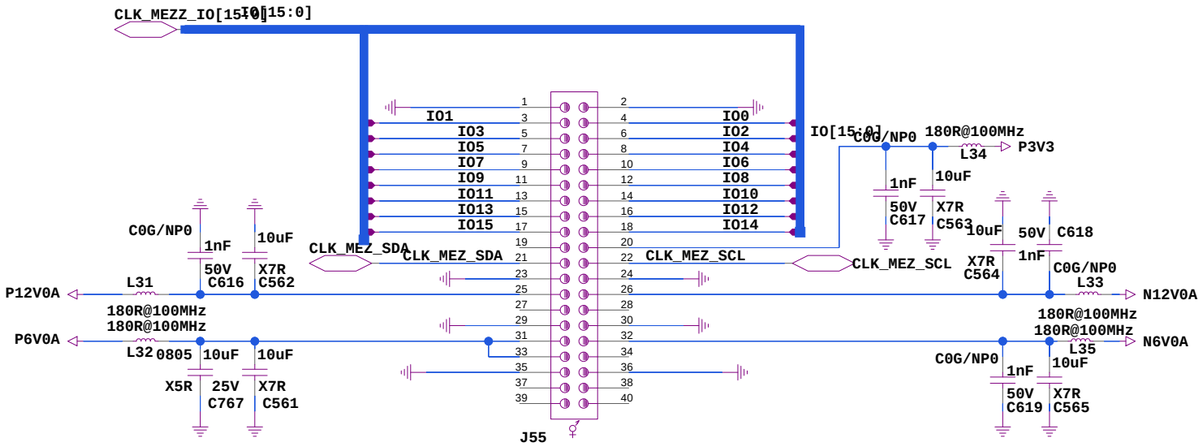
ARTIQ Sayma

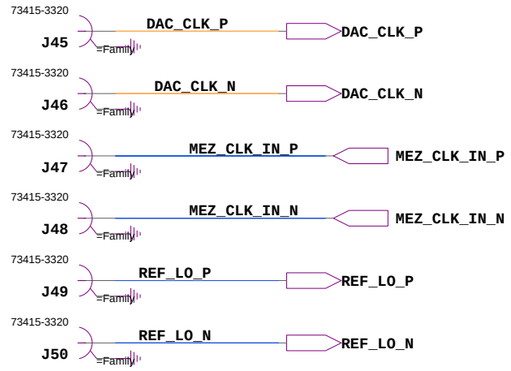
TITLE

CAL_ADC

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	4	18	2016/11/07:18:03:57





LSS-120-03-L-DV-A
+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth

+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth

+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ

ARTIQ Sayma

TITLE

CLK_Mezzanine

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	5	18	2016/11/07:18:04:03

Clock_Distribution

ARTIQ

TITLE	ARTIQ Sayma		
SIZE A3	DWG NO	1	REV v0.9
DRAWN BY G.K.	SHEET 6 of 18	2016/11/07:18:03:57	

IC31 Type ADCLK948BCPZ

P3V3_CLK 120R@100MHz L50 1uF 16V 0402 C658; 100nF C414 C415 C416 C417 C418 C419

VCC VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VREF0 VREF1 *CLK0 CLK0 *CLK1 CLK1 IN_SEL VR0 VT1

100nF C433 C434; 100nF C413 C432; 100nF C436 C435

R100 0 R101 0

CLK_SEL_DIRECT_CLK_MEZ

NC EP Q7 *Q7 Q6 *Q6 Q5 *Q5 Q4 *Q4 Q3 *Q3 Q2 *Q2 Q1 *Q1 Q0 *Q0

200 R47 R46 R49 R48 R51 R50 R53 R52 R104 R103 R55 R54

C402 100nF REF1_100M_P; C403 100nF REF1_100M_N; C404 100nF REF2_100M_P; C405 100nF REF2_100M_N; C406 100nF REF3_100M_P; C407 100nF REF3_100M_N; C408 100nF REF4_100M_P; C409 100nF REF4_100M_N

REF1_100M_P REF1_100M_N REF2_100M_P REF2_100M_N REF3_100M_P REF3_100M_N REF4_100M_P REF4_100M_N

SYSREF is matched to its CLK (a.k.a. DEVICECLK) to better than 100 ps.

uRFB_CLK_IN_P DNP C442; uRFB_CLK_IN_N DNP C443 100nF; uRFB_REF_IN C427 100nF

49R9 R98 C411 0 R56 0 R57 input BW setting

LTC6957IDD-1#PBF: IN+ IN- FILTA FILTB SD1 SD2 V+ OUT1_P OUT1_N OUT2_N OUT2_P GND EP =Device

P3V3_CLK 120R@100MHz L49 1uF 16V 0402 C410; C657 100nF IC32

200R58 R59 200

Si53307: CLK0_P CLK0_N CLK1_P CLK1_N CLK_SEL VDD Vddo Q0_P Q0_N Q1_P Q1_N SFOUT0 SFOUT1 OE GND1 GND2 PAD

200 R94 R95; 200 R92 R93; 100nF C428 C429

clock module: MEZ_CLK_IN_N REF_LO_P MEZ_CLK_IN_P REF_LO_N

DAC_CLK_P DAC_CLK_N

REFSYNCIN_P REFSYNCIN_N

C377 C378 C438 C439 C375 C376 100nF

CLK_SEL_uRFB_EXT R96 10k P3V3_CLK L=CLK0, H-CLK1

R99 10k T1

To additionally isolate inactive CLK Shutdown inputs are used

IC30

P3V3_CLK L54 120R@100MHz; C663 1uF 16V 0402; C431 C430 100nF

LVPECL mode -> SFOUT[1:0] = open

EXT_100M_RF_IN 49R9 R97; 100nF C412; 100nF C426; input BW setting R88 0 R89

LTC6957IDD-1#PBF IC33 =Device

R90 200 R91 200

P3V3_CLK 120R@100MHz L53 1uF 16V 0402 C662; 100nF C425

OSC1 VC OE VDD CLK CLK GND =Value

P3V3_CLK L55 120R@100MHz 1uF 16V 0402 C664; 100nF C437 RC place holder

Oscillator place holder

200 R108 200 R107

HMC_CFG R106 0 R105 0

HMC_SPI_SYNC HMC_SPI_SDATA HMC_SPI_SLEN HMC_SPI_SCLK HMC_RESET HMC_SPI_GPIO

C440 C441 100nF

Undefined R109 R110 C669; C665 C666 C667 C668

120R@100MHz L52 C681 1uF 16V 0402; 100nF 6.3V 0201 C423; 1nF 16V 0201 C424

VCC1_VCO

430 R102; C751 150pF C760 6.8nF C759 10pF C758 150pF

RC place holder

120R@100MHz L51 C660 1uF 16V 0402; 100nF 6.3V 0201 C421; 1nF 16V 0201 C422

VCC5_PLL1

4.7uF C609; 4.7uF C608; 4.7uF 25V 0603 C611; 1uF 16V 0402 C659; 100nF 6.3V 0201 C420; 4.7uF C613; 4.7uF C612

P4V0 IC19 LT1963AEST-3.3#PBF IN OUT GND 4.7uF C610

P3V3_CLK 22uF 6.3V 0805 C766; 100nF 6.3V 0201 C379

120R@100MHz L38 C646 1uF 16V 0402; 100nF 6.3V 0201 C380; 1nF 16V 0201 C381

VCC_PLL

120R@100MHz L43 C651 1uF 16V 0402; 100nF 6.3V 0201 C390; 1nF 16V 0201 C391

VCC6_OSCOUT

120R@100MHz L42 C650 1uF 16V 0402; 100nF 6.3V 0201 C388; 1nF 16V 0201 C389

VCC7_PLL2

120R@100MHz L39 C647 1uF 16V 0402; 100nF 6.3V 0201 C382; 1nF 16V 0201 C383

VCC_CLOCKOUT1

120R@100MHz L44 C652 1uF 16V 0402; 100nF 6.3V 0201 C392; 1nF 16V 0201 C393

VCC2_OUT

120R@100MHz L40 C648 1uF 16V 0402; 100nF 6.3V 0201 C384; 1nF 16V 0201 C385

VCC_CLOCKOUT2

120R@100MHz L45 C653 1uF 16V 0402; 100nF 6.3V 0201 C394; 1nF 16V 0201 C395

VCC9_OUT

120R@100MHz L41 C649 1uF 16V 0402; 100nF 6.3V 0201 C386; 1nF 16V 0201 C387

VCC_CLOCKOUT3

120R@100MHz L46 C654 1uF 16V 0402; 100nF 6.3V 0201 C396; 1nF 16V 0201 C397

VCC3_SYSREF

120R@100MHz L47 C655 1uF 16V 0402; 100nF 6.3V 0201 C398; 1nF 16V 0201 C399

VCC4_OUT

120R@100MHz L48 C656 1uF 16V 0402; 100nF 6.3V 0201 C400; 1nF 16V 0201 C401

VCC8_OUT

IC34

CLKIN0/RFSYNCIN CLKIN0/RFSYNCIN CLKIN1/FIN CLKIN1/FIN CLKIN2/OSCOUT0 CLKIN2/OSCOUT0 CLKIN3 CLKIN3 SYNC SDATA SLEN SCLK RESET GPIO1 GPIO2 GPIO3 GPIO4 CPOUT1 CPOUT2 OSCIN OSCIN OSCOUT1 OSCOUT1 BGABYP1 LDOBYP2 LDOBYP3 LDOBYP4 LDOBYP5 LDOBYP6 LDOBYP7 VCC1_VCO VCC2_OUT VCC3_SYSREF VCC4_OUT VCC5_PLL1 VCC6_OSCOUT VCC7_PLL2 VCC8_OUT VCC9_OUT RSV EP

CLKOUT0 CLKOUT0 SCLKOUT1 SCLKOUT1 CLKOUT2 CLKOUT2 SCLKOUT3 SCLKOUT3 CLKOUT4 CLKOUT4 SCLKOUT5 SCLKOUT5 CLKOUT6 CLKOUT6 SCLKOUT7 SCLKOUT7 CLKOUT8 CLKOUT8 SCLKOUT9 SCLKOUT9 CLKOUT10 CLKOUT10 SCLKOUT11 SCLKOUT11 CLKOUT12 CLKOUT12 SCLKOUT13 SCLKOUT13

200 R61 R60 C347 C348 100nF; DAC1_CLK_P DAC1_CLK_N

200 R63 R62 C349 C350 100nF; DAC1_SYSREF_P DAC1_SYSREF_N

200 R65 R64 C351 C352 100nF; DAC2_CLK_P DAC2_CLK_N

200 R67 R66 C353 C354 100nF; DAC2_SYSREF_P DAC2_SYSREF_N

200 R69 R68 C355 C356 100nF; ADC1_CLK_P ADC1_CLK_N

200 R71 R70 C357 C358 100nF; FPGA_DAC_SYSREF_P FPGA_DAC_SYSREF_N

200 R73 R72 C359 C360 100nF; ADC2_CLK_P ADC2_CLK_N

200 R75 R74 C361 C362 100nF; ADC1_SER_SYSREF_P ADC1_SER_SYSREF_N

200 R77 R76 C363 C364 100nF; FPGA_REF_CLK_N FPGA_REF_CLK_P

200 R79 R78 C365 C366 100nF; ADC2_SER_SYSREF_P ADC2_SER_SYSREF_N

200 R81 R80 C367 C368 100nF; GTPTX_CLK_IN_P GTPTX_CLK_IN_N

200 R83 R82 C369 C370 100nF; FPGA_ADC_SYSREF_P FPGA_ADC_SYSREF_N

200 R85 R84 C371 C372 100nF; GTPRX_CLK_IN_P GTPRX_CLK_IN_N

200 R87 R86 C373 C374 100nF; AMC_FPGA_REF_CLK_N AMC_FPGA_REF_CLK_P

HMC7044LP10BE

IOVDD=3.3

SERDIN0_P SERDIN0_N SERDIN1_P SERDIN1_N SERDIN2_P SERDIN2_N SERDIN3_P SERDIN3_N SERDIN4_P SERDIN4_N SERDIN5_P SERDIN5_N SERDIN6_P SERDIN6_N SERDIN7_P SERDIN7_N
C134 C133 C136 C135 C138 C137 C140 C139 C142 C141 C144 C143 C146 C145 C148 C147 6.3V 100nF
15 16 18 19 26 27 29 30 38 37 41 40 49 48 52 51
SERDIN0+ SERDIN0- SERDIN1+ SERDIN1- SERDIN2+ SERDIN2- SERDIN3+ SERDIN3- SERDIN4+ SERDIN4- SERDIN5+ SERDIN5- SERDIN6+ SERDIN6- SERDIN7+ SERDIN7-

DAC_TXEN0 DAC_TXEN1 — 11 12 — TXEN0 TXEN1

DAC_CLK_P DAC_CLK_N — 2 3 — CLK+ CLK-

DAC_SPI_SDO DAC_SPI_SDIO DAC_SPI_SCLK DAC_SPI_CSn — 62 63 64 65 — SDO SDIO SCLK CS

SIOVDD33 IOVDD — 35 66 — SIOVDD33 IOVDD

VTT: 1uF 16V 0402 C622; 100nF 6.3V 0201 C52, C51, C50; 100nF 6.3V 0201 C49
21 25 42 46 — VTT-1 VTT-2 VTT-4 VTT-3

AVDD33: 4.7nF 10V 0201 C61 C62 C60 C59; 100nF 6.3V 0201 C58 C57; 1nF 16V 0201 C56 C55; 100nF 6.3V 0201 C53; 1nF 16V 0201 C54; 4.7uF 35V B C3; 47uF 16V C C699
80 70 72 75 77 82 85 67 — AVDD33-6 AVDD33-8 AVDD33-1 AVDD33-5 AVDD33-3 AVDD33-2 AVDD33-4 AVDD33-7

CVDD12: 4.7nF 10V 0201 C101 C102 C100 C99; 100nF 6.3V 0201 C98 C97; 1nF 16V 0201 C96 C95; 100nF 6.3V 0201 C93; 1nF 16V 0201 C94; 4.7uF 35V B C6; 47uF 16V C C702
71 76 81 87 — CVDD12-2 CVDD12-3 CVDD12-4 CVDD12-1

DVDD12: 4.7nF 10V 0201 C111 C112 C110 C109; 100nF 6.3V 0201 C108 C107; 1nF 16V 0201 C106 C105; 100nF 6.3V 0201 C103; 1nF 16V 0201 C104; 4.7uF 35V B C7; 47uF 16V C C703
13 14 53 — DVDD12-2 DVDD12-1 DVDD12-3

IC3 =Device AD9154BCPZ

OUT0+ OUT0- OUT1+ OUT1- OUT2+ OUT2- OUT3+ OUT3-
84 83 78 79 74 73 68 69
OUT0_P OUT0_N OUT1_P OUT1_N OUT2_P OUT2_N OUT3_P OUT3_N
OUT0_P OUT0_N OUT1_P OUT1_N OUT2_P OUT2_N OUT3_P OUT3_N

SYNCOUT0+ SYNCOUT0- SYNCOUT1+ SYNCOUT1-
23 24 44 43
SYNCOUT0_P SYNCOUT0_N SYNCOUT1_P SYNCOUT1_N
SYNCOUT0_P SYNCOUT0_N SYNCOUT1_P SYNCOUT1_N

PDP_OUT0 PDP_OUT1 — 59 58

SYSREF+ SYSREF- — 5 6 — DAC_SYSREF_P DAC_SYSREF_N — DAC_SYSREF_P DAC_SYSREF_N

LDO_BYP1 LDO_BYP2 — 34 88 — C624 1uF 16V 0402; R23 1 1%; R22 1 1%; C623 1uF 16V 0402

IRQ RESET — 60 61 — DAC_IRQn DAC_RESETn

I120 — 86 — R182 4k02 1%

DNC-1 DNC-2 — 54 55

DAC_CFG — DAC_CFG

DAC_IRQn DAC_RESETn DAC_SPI_CSn DAC_SPI_SCLK DAC_SPI_SDO DAC_SPI_SDIO DAC_TXEN0 DAC_TXEN1

Replace with W2L16C473MAT1S

PVDD12: 4.7nF 10V 0201 C71 C72 C70 C69; 100nF 6.3V 0201 C68 C67; 1nF 16V 0201 C66 C65; 100nF 6.3V 0201 C63; 1nF 16V 0201 C64; 4.7uF 35V B C4; 47uF 16V C C700; 100nF 6.3V 0201 C73 C74 C75; 1nF 16V 0201 C76 C77
1 57 7 8 9 10 56 4 — PVDD12-8 PVDD12-2 PVDD12-1 PVDD12-6 PVDD12-4 PVDD12-7 PVDD12-3 PVDD12-5

SVDD12: 4.7nF 10V 0201 C84 C85 C83 C82; 1nF 16V 0201 C91 C92; 1nF 16V 0201 C81 C80; 100nF 6.3V 0201 C78 C79; 4.7uF 35V B C5; 47uF 16V C C701; 100nF 6.3V 0201 C86 C87 C88 C89; 1nF 16V 0201 C90
17 28 45 22 47 39 31 32 33 36 20 50 — SVDD12-2 SVDD12-9 SVDD12-4 SVDD12-12 SVDD12-1 SVDD12-8 SVDD12-6 SVDD12-5 SVDD12-11 SVDD12-10 SVDD12-3 SVDD12-7

EP — 89

SDVDD12: 4.7nF 10V 0201 C121 C122 C120 C119; 100nF 6.3V 0201 C118 C117; 1nF 16V 0201 C116 C115; 100nF 6.3V 0201 C113; 1nF 16V 0201 C114; 4.7uF 35V B C8; C704 47uF 16V C

XVDD33: C10 4.7uF 35V B; C706 47uF 16V C

PLLVDD12: 1nF 16V 0201 C125; 100nF 6.3V 0201 C123; 1nF 16V 0201 C124; 4.7uF 35V B C9; 47uF 16V C C705

SIOVDD33: 1nF 16V 0201 C128; 100nF 6.3V 0201 C126; 1nF 16V 0201 C127; 4.7uF 35V B C11; 47uF 16V C C707

IOVDD: 100nF 6.3V 0201 C132; 1nF 16V 0201 C131; 100nF 6.3V 0201 C129; 1nF 16V 0201 C130; 4.7uF 35V B C12; 47uF 16V C C708

P1V8 — L36 120R@100MHz — C625 1uF 16V 0402; 100nF 6.3V 0201 C161; 1nF 16V 0201 C162 — IOVDD

Replace with W2L16C473MAT1S

P2V0 — 4.7uF C586 — IC5 VIN-1 VIN-2 VIN-3 VIN-5 VIN-4 VOUT-4 VOUT-3 VOUT-5 VOUT-1 VOUT-2 PG EN SS GND EP SENS NC — 100nF 6.3V 0201 C150 — PVDD12: C13 4.7uF 35V B; 100nF 6.3V 0201 C149

P2V0 — 4.7uF C588 — IC7 — 100nF 6.3V 0201 C154 — SVDD12: C15 4.7uF 35V B; 100nF 6.3V 0201 C153

P2V0 — 4.7uF C587 — IC6 — 100nF 6.3V 0201 C152 — DVDD12: C14 4.7uF 35V B; 100nF 6.3V 0201 C151

P2V0 — 4.7uF C589 — IC8 — 100nF 6.3V 0201 C156 — PLLVDD12: C16 4.7uF 35V B; 100nF 6.3V 0201 C155

P2V0 — 4.7uF C590 — IC9 — 100nF 6.3V 0201 C158 — CVDD12: C17 4.7uF 35V B; 100nF 6.3V 0201 C157

P4V0 — LT1963AEST-3.3#PBF — IN OUT GND — 4.7uF C591 — IC15 — AVDD33: C18 4.7uF 35V B; 100nF 6.3V 0201 C159

P4V0 — C592 4.7uF — IC16 IN OUT GND — SIOVDD33: C19 4.7uF 35V B; 100nF 6.3V 0201 C160

ARTIQ Sayma

TITLE: DAC_JESD204B

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	7	18	2016/11/07:18:03:54

SERDIN0_P
SERDIN0_N
SERDIN1_P
SERDIN1_N
SERDIN2_P
SERDIN2_N
SERDIN3_P
SERDIN3_N
SERDIN4_P
SERDIN4_N
SERDIN5_P
SERDIN5_N
SERDIN6_P
SERDIN6_N
SERDIN7_P
SERDIN7_N

C248 6.3V 100nF
C247 6.3V 100nF
C250 6.3V 100nF
C249 6.3V 100nF
C252 6.3V 100nF
C251 6.3V 100nF
C254 6.3V 100nF
C253 6.3V 100nF
C256 6.3V 100nF
C255 6.3V 100nF
C258 6.3V 100nF
C257 6.3V 100nF
C260 6.3V 100nF
C259 6.3V 100nF
C262 6.3V 100nF
C261 6.3V 100nF

15 16 18 19 26 27 29 30 38 37 41 40 49 48 52 51

SERDIN0+ SERDIN0- SERDIN1+ SERDIN1- SERDIN2+ SERDIN2- SERDIN3+ SERDIN3- SERDIN4+ SERDIN4- SERDIN5+ SERDIN5- SERDIN6+ SERDIN6- SERDIN7+ SERDIN7-

DAC_TXEN0 11 TXEN0
DAC_TXEN1 12 TXEN1

DAC_CLK_P 2 CLK+
DAC_CLK_N 3 CLK-

DAC_SPI_SDO 62 SDO
DAC_SPI_SDIO 63 SDIO
DAC_SPI_SCLK 64 SCLK
DAC_SPI_CSn 65 CS

SIOVDD33 35 SIOVDD33
IOVDD 66 IOVDD

IOVDD=3.3

VTT
1uF 16V 0402 C626
100nF 6.3V 0201 C166
100nF 6.3V 0201 C165
100nF 6.3V 0201 C164
100nF 6.3V 0201 C163

21 25 42 46 VTT-1 VTT-2 VTT-4 VTT-3

AVDD33 80 AVDD33-6
70 AVDD33-8
72 AVDD33-1
75 AVDD33-5
77 AVDD33-3
82 AVDD33-2
85 AVDD33-4
67 AVDD33-7

CVDD12 71 CVDD12-2
76 CVDD12-3
81 CVDD12-4
87 CVDD12-1

DVDD12 13 DVDD12-2
14 DVDD12-1
53 DVDD12-3

IC4 AD9154BCPZ =Device

OUT0+ OUT0- OUT1+ OUT1- OUT2+ OUT2- OUT3+ OUT3-

84 OUT0_P
83 OUT0_N
78 OUT1_P
79 OUT1_N
74 OUT2_P
73 OUT2_N
68 OUT3_P
69 OUT3_N

OUT0_P OUT0_N OUT1_P OUT1_N OUT2_P OUT2_N OUT3_P OUT3_N

SYNCOUT0+ SYNCOUT0- SYNCOUT1+ SYNCOUT1-

23 SYNCOUT0_P
24 SYNCOUT0_N
44 SYNCOUT1_P
43 SYNCOUT1_N

SYNCOUT0_P SYNCOUT0_N SYNCOUT1_P SYNCOUT1_N

PDP_OUT0 59
PDP_OUT1 58

SYSREF+ 5 DAC_SYSREF_P
SYSREF- 6 DAC_SYSREF_N

DAC_SYSREF_P DAC_SYSREF_N

LDO_BYP1 34 R25 1 1uF 16V C628
LDO_BYP2 88 R24 1 0402 C627
1uF 16V 0402

IRQ 60 DAC_IRQn
RESET 61 DAC_RESETn

I120 86 R183 4k02

DNC-1 54
DNC-2 55

DAC_CFG

DAC_IRQn
DAC_RESETn
DAC_SPI_CSn
DAC_SPI_SCLK
DAC_SPI_SDO
DAC_SPI_SDIO
DAC_TXEN0
DAC_TXEN1

Replace with W2L16C473MAT1S

PVDD12 1 57 7 8 9 10 56 4
PVDD12-8 PVDD12-2 PVDD12-1 PVDD12-6 PVDD12-4 PVDD12-7 PVDD12-3 PVDD12-5

4.7nF 10V 0201 C185
4.7nF 10V 0201 C186
4.7nF 10V 0201 C184
4.7nF 10V 0201 C183
100nF 6.3V 0201 C182
100nF 6.3V 0201 C181
1nF 16V 0201 C180
1nF 16V 0201 C179
100nF 6.3V 0201 C177
1nF 16V 0201 C178
4.7uF 35V B C21
47uF 16V C C710
100nF 6.3V 0201 C187
100nF 6.3V 0201 C188
100nF 6.3V 0201 C189
1nF 16V 0201 C190
1nF 16V 0201 C191

SVDD12 17 28 45 22 47 39 31 32 33 36 20 50
SVDD12-2 SVDD12-9 SVDD12-4 SVDD12-12 SVDD12-1 SVDD12-8 SVDD12-6 SVDD12-5 SVDD12-11 SVDD12-10 SVDD12-3 SVDD12-7

4.7nF 10V 0201 C198
4.7nF 10V 0201 C199
4.7nF 10V 0201 C197
4.7nF 10V 0201 C196
1nF 16V 0201 C205
1nF 16V 0201 C206
1nF 16V 0201 C195
1nF 16V 0201 C194
100nF 6.3V 0201 C192
1nF 16V 0201 C193
4.7uF 35V B C22
47uF 16V C C711
100nF 6.3V 0201 C200
100nF 6.3V 0201 C201
100nF 6.3V 0201 C202
1nF 16V 0201 C203
1nF 16V 0201 C204

SDVDD12
4.7nF 10V 0201 C235
4.7nF 10V 0201 C236
4.7nF 10V 0201 C234
4.7nF 10V 0201 C233
100nF 6.3V 0201 C232
100nF 6.3V 0201 C231
1nF 16V 0201 C230
1nF 16V 0201 C229
100nF 6.3V 0201 C227
1nF 16V 0201 C228
4.7uF 35V B C25
47uF 16V C C714
4.7uF 35V B C27
47uF 16V C C716
XVDD33

EP 89

PLLVDD12
1nF 16V 0201 C239
100nF 6.3V 0201 C237
1nF 16V 0201 C238
4.7uF 35V B C26
47uF 16V C C715

SIOVDD33
1nF 16V 0201 C242
100nF 6.3V 0201 C240
1nF 16V 0201 C241
4.7uF 35V B C28
47uF 16V C C717

IOVDD
100nF 6.3V 0201 C246
1nF 16V 0201 C245
100nF 6.3V 0201 C243
1nF 16V 0201 C244
4.7uF 35V B C29
47uF 16V C C718

P1V8 L37 120R@100MHz
C629 1uF 16V 0402
100nF 6.3V 0201 C275
1nF 16V 0201 C276
IOVDD

Replace with W2L16C473MAT1S

4.7nF 10V 0201 C175
4.7nF 10V 0201 C176
4.7nF 10V 0201 C174
4.7nF 10V 0201 C173
100nF 6.3V 0201 C172
100nF 6.3V 0201 C171
1nF 16V 0201 C170
1nF 16V 0201 C169
100nF 6.3V 0201 C167
1nF 16V 0201 C168
4.7uF 35V B C20
47uF 16V C C709

4.7nF 10V 0201 C215
4.7nF 10V 0201 C216
4.7nF 10V 0201 C214
4.7nF 10V 0201 C213
100nF 6.3V 0201 C212
100nF 6.3V 0201 C211
1nF 16V 0201 C210
1nF 16V 0201 C209
100nF 6.3V 0201 C207
1nF 16V 0201 C208
4.7uF 35V B C23
47uF 16V C C712

4.7nF 10V 0201 C225
4.7nF 10V 0201 C226
4.7nF 10V 0201 C224
4.7nF 10V 0201 C223
100nF 6.3V 0201 C222
100nF 6.3V 0201 C221
1nF 16V 0201 C220
1nF 16V 0201 C219
100nF 6.3V 0201 C217
1nF 16V 0201 C218
4.7uF 35V B C24
47uF 16V C C713

P2V0
4.7uF C593
IC10 VIN-1 VIN-2 VIN-3 VIN-5 VIN-4 VOUT-4 VOUT-3 VOUT-5 VOUT-1 VOUT-2 PG EN SS GND EP SENS NC
100nF 6.3V 0201 C264
PVDD12 C30 4.7uF 35V B 100nF 6.3V 0201 C263

P2V0
4.7uF C595
IC12
100nF 6.3V 0201 C268
SVDD12 C32 4.7uF 35V B 100nF 6.3V 0201 C267

P2V0
4.7uF C594
IC11
100nF 6.3V 0201 C266
DVDD12 C31 4.7uF 35V B 100nF 6.3V 0201 C265

P2V0
4.7uF C596
IC13
100nF 6.3V 0201 C270
PLLVDD12 C33 4.7uF 35V B 100nF 6.3V 0201 C269

P2V0
4.7uF C597
IC14
100nF 6.3V 0201 C272
CVDD12 C34 4.7uF 35V B 100nF 6.3V 0201 C271

P4V0
LT1963AEST-3.3#PBF IN OUT GND
4.7uF C598
IC17
AVDD33 C35 4.7uF 35V B 100nF 6.3V 0201 C273

P4V0
4.7uF C599
IC18 IN OUT GND
SIOVDD33 C36 4.7uF 35V B 100nF 6.3V 0201 C274

ARTIQ Sayma

TITLE
DAC_JESD204B

SIZE	DWG NO	REV
A3		1 v0.9

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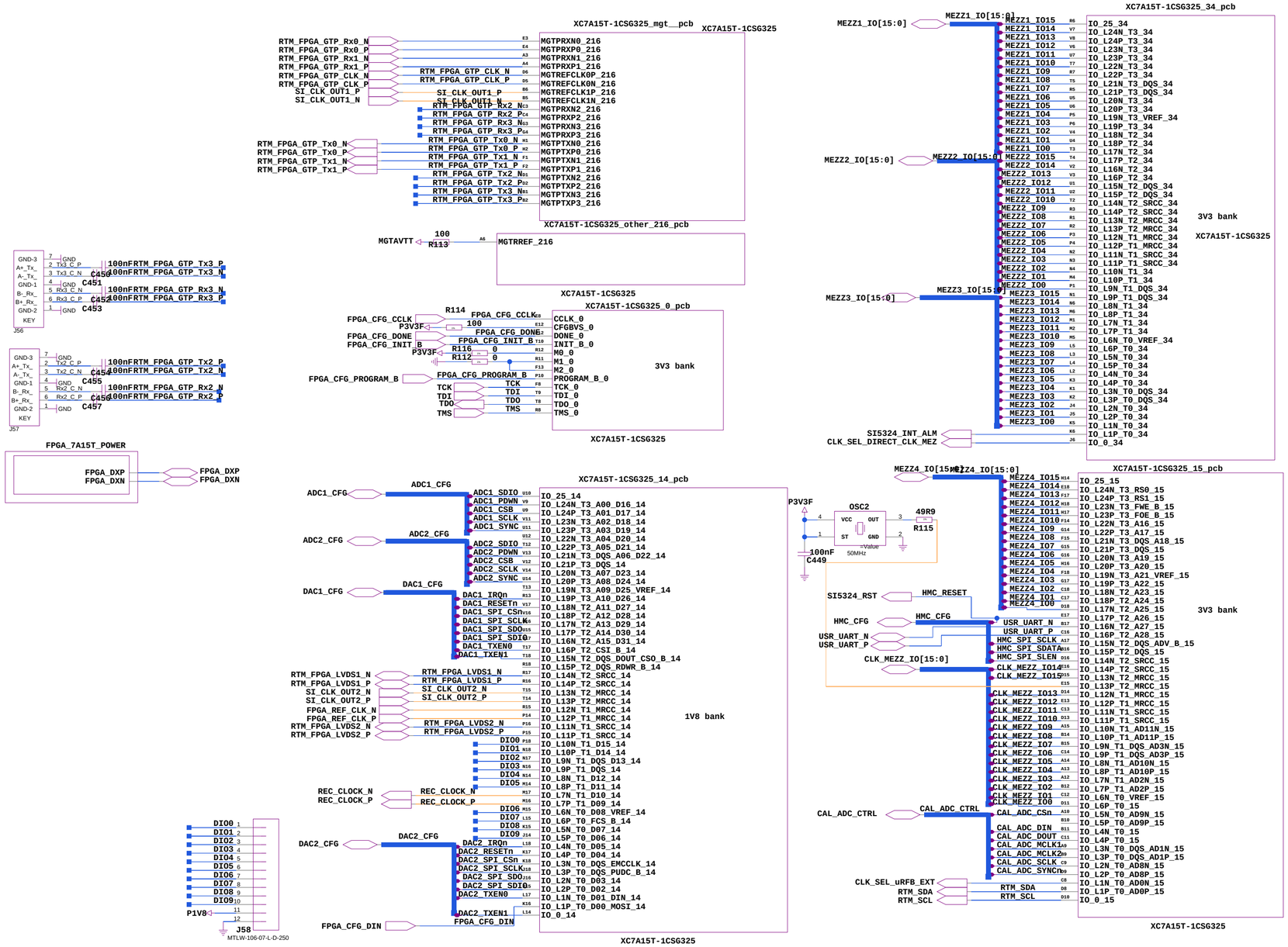
G.K.	8	18	2016/11/07:18:03:54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XC7A15T-1CSG325
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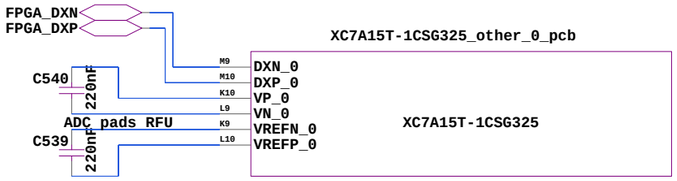
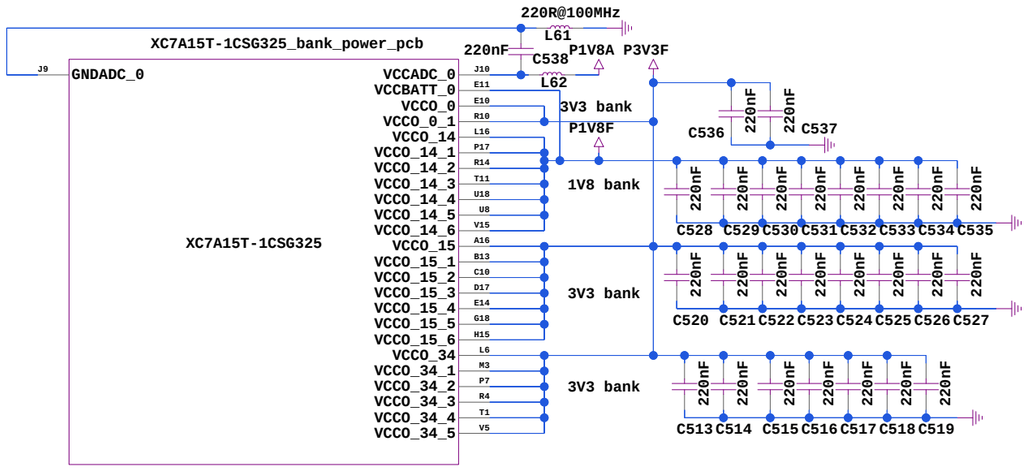
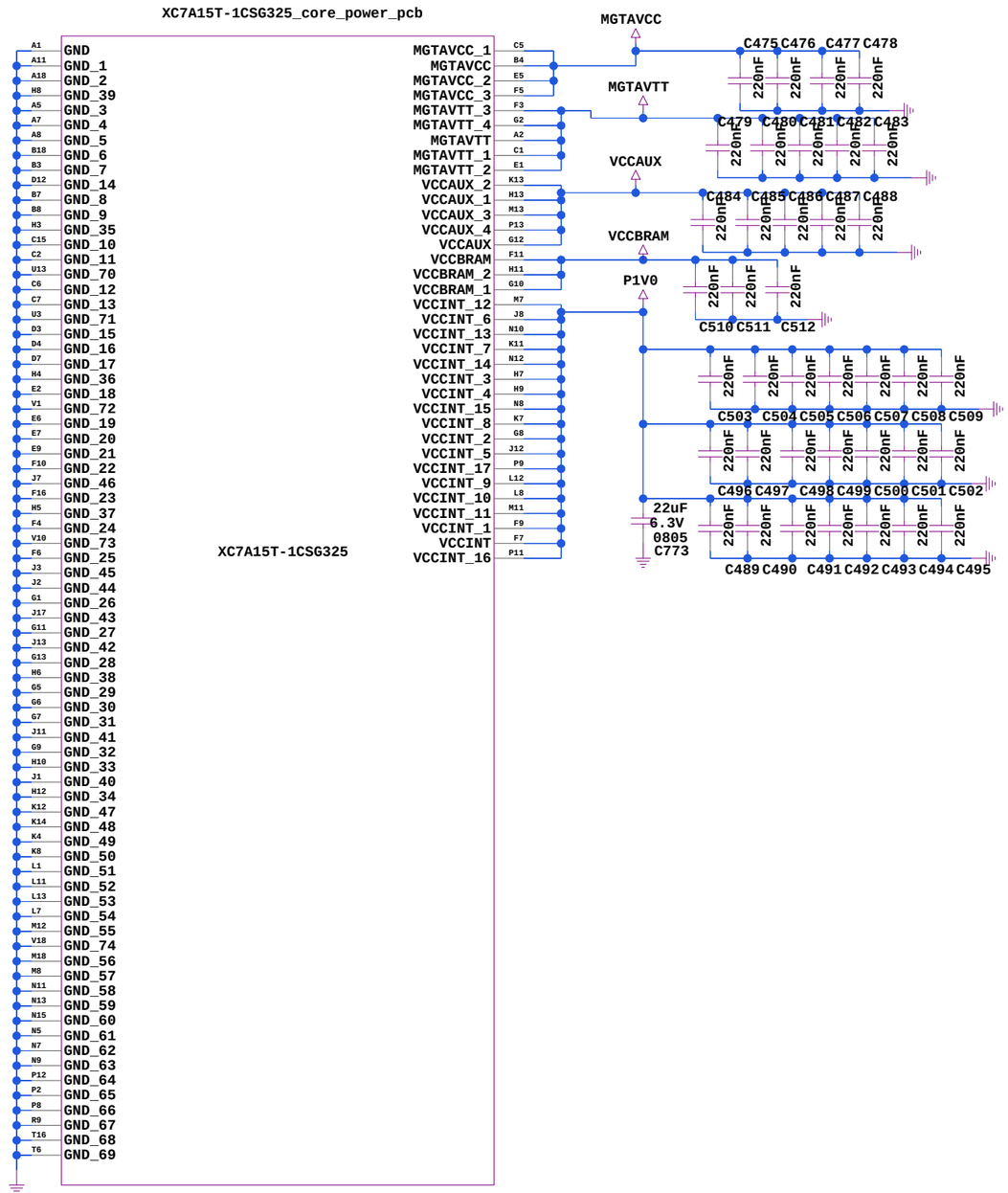
RTM_FPGA_GTP_Rx0_P
RTM_FPGA_GTP_Rx1_N
RTM_FPGA_GTP_Rx1_P
RTM_FPGA_GTP_CLK_N
RTM_FPGA_GTP_CLK_P
SI_CLK_OUT1_P
SI_CLK_OUT1_N
RTM_FPGA_GTP_Rx2_N
RTM_FPGA_GTP_Rx2_P
RTM_FPGA_GTP_Rx3_N
RTM_FPGA_GTP_Rx3_P
RTM_FPGA_GTP_Tx0_N
RTM_FPGA_GTP_Tx0_P
RTM_FPGA_GTP_Tx1_N
RTM_FPGA_GTP_Tx1_P
RTM_FPGA_GTP_Tx2_N
RTM_FPGA_GTP_Tx2_P
RTM_FPGA_GTP_Tx3_N
RTM_FPGA_GTP_Tx3_P
MGTPRXN0_216
MGTPRXP0_216
MGTPRXN1_216
MGTPRXP1_216
MGTREFCLK0P_216
MGTREFCLK0N_216
MGTREFCLK1P_216
MGTREFCLK1N_216
MGTPRXN2_216
MGTPRXP2_216
MGTPRXN3_216
MGTPRXP3_216
MGTPTXN0_216
MGTPTXP0_216
MGTPTXN1_216
MGTPTXP1_216
MGTPTXN2_216
MGTPTXP2_216
MGTPTXN3_216
MGTPTXP3_216
XC7A15T-1CSG325_other_216_pcb
MGTAVTT
100
R113
MGTRREF_216
XC7A15T-1CSG325
XC7A15T-1CSG325_0_pcb
FPGA_CFG_CCLK
P3V3F
FPGA_CFG_DONE
FPGA_CFG_INIT_B
R114
R116
R112
FPGA_CFG_PROGRAM_B
TCK
TDI
TDO
TMS
CCLK_0
CFGBVS_0
DONE_0
INIT_B_0
M0_0
M1_0
M2_0
PROGRAM_B_0
TCK_0
TDI_0
TDO_0
TMS_0
3V3 bank
XC7A15T-1CSG325
XC7A15T-1CSG325_34_pcb
MEZZ1_IO[15:0]
MEZZ2_IO[15:0]
MEZZ3_IO[15:0]
SI5324_INT_ALM
CLK_SEL_DIRECT_CLK_MEZ
IO_25_34
IO_L24N_T3_34
IO_L24P_T3_34
IO_L23N_T3_34
IO_L23P_T3_34
IO_L22N_T3_34
IO_L22P_T3_34
IO_L21N_T3_DQS_34
IO_L21P_T3_DQS_34
IO_L20N_T3_34
IO_L20P_T3_34
IO_L19N_T3_VREF_34
IO_L19P_T3_34
IO_L18N_T2_34
IO_L18P_T2_34
IO_L17N_T2_34
IO_L17P_T2_34
IO_L16N_T2_34
IO_L16P_T2_34
IO_L15N_T2_DQS_34
IO_L15P_T2_DQS_34
IO_L14N_T2_SRCC_34
IO_L14P_T2_SRCC_34
IO_L13N_T2_MRCC_34
IO_L13P_T2_MRCC_34
IO_L12N_T1_MRCC_34
IO_L12P_T1_MRCC_34
IO_L11N_T1_SRCC_34
IO_L11P_T1_SRCC_34
IO_L10N_T1_34
IO_L10P_T1_34
IO_L9N_T1_DQS_34
IO_L9P_T1_DQS_34
IO_L8N_T1_34
IO_L8P_T1_34
IO_L7N_T1_34
IO_L7P_T1_34
IO_L6N_T0_VREF_34
IO_L6P_T0_34
IO_L5N_T0_34
IO_L5P_T0_34
IO_L4N_T0_34
IO_L4P_T0_34
IO_L3N_T0_DQS_34
IO_L3P_T0_DQS_34
IO_L2N_T0_34
IO_L2P_T0_34
IO_L1N_T0_34
IO_L1P_T0_34
IO_0_34
3V3 bank
XC7A15T-1CSG325
XC7A15T-1CSG325_15_pcb
MEZZ4_IO[15:0]
CAL_ADC_CTRL
CLK_SEL_uRFB_EXT
RTM_SDA
RTM_SCL
IO_25_15
IO_L24N_T3_RS0_15
IO_L24P_T3_RS1_15
IO_L23N_T3_FWE_B_15
IO_L23P_T3_FOE_B_15
IO_L22N_T3_A16_15
IO_L22P_T3_A17_15
IO_L21N_T3_DQS_A18_15
IO_L21P_T3_DQS_15
IO_L20N_T3_A19_15
IO_L20P_T3_A20_15
IO_L19N_T3_A21_VREF_15
IO_L19P_T3_A22_15
IO_L18N_T2_A23_15
IO_L18P_T2_A24_15
IO_L17N_T2_A25_15
IO_L17P_T2_A26_15
IO_L16N_T2_A27_15
IO_L16P_T2_A28_15
IO_L15N_T2_DQS_ADV_B_15
IO_L15P_T2_DQS_15
IO_L14N_T2_SRCC_15
IO_L14P_T2_SRCC_15
IO_L13N_T2_MRCC_15
IO_L13P_T2_MRCC_15
IO_L12N_T1_MRCC_15
IO_L12P_T1_MRCC_15
IO_L11N_T1_SRCC_15
IO_L11P_T1_SRCC_15
IO_L10N_T1_AD11N_15
IO_L10P_T1_AD11P_15
IO_L9N_T1_DQS_AD3N_15
IO_L9P_T1_DQS_AD3P_15
IO_L8N_T1_AD10N_15
IO_L8P_T1_AD10P_15
IO_L7N_T1_AD2N_15
IO_L7P_T1_AD2P_15
IO_L6N_T0_VREF_15
IO_L6P_T0_15
IO_L5N_T0_AD9N_15
IO_L5P_T0_AD9P_15
IO_L4N_T0_15
IO_L4P_T0_15
IO_L3N_T0_DQS_AD1N_15
IO_L3P_T0_DQS_AD1P_15
IO_L2N_T0_AD8N_15
IO_L2P_T0_AD8P_15
IO_L1N_T0_AD0N_15
IO_L1P_T0_AD0P_15
IO_0_15
3V3 bank
XC7A15T-1CSG325
GND-3
A+_Tx_
A-_Tx_
GND-1
B-_Rx_
B+_Rx_
GND-2
KEY
J56
Tx3_C_P
Tx3_C_N
Rx3_C_P
Rx3_C_N
C450
C451
C452
C453
100nF
RTM_FPGA_GTP_Tx3_P
RTM_FPGA_GTP_Tx3_N
RTM_FPGA_GTP_Rx3_N
RTM_FPGA_GTP_Rx3_P
J57
Tx2_C_P
Tx2_C_N
Rx2_C_P
Rx2_C_N
C454
C455
C456
C457
RTM_FPGA_GTP_Tx2_P
RTM_FPGA_GTP_Tx2_N
RTM_FPGA_GTP_Rx2_N
RTM_FPGA_GTP_Rx2_P
FPGA_7A15T_POWER
FPGA_DXP
FPGA_DXN
XC7A15T-1CSG325_14_pcb
ADC1_CFG
ADC2_CFG
DAC1_CFG
DAC2_CFG
ADC1_SDIO
ADC1_PDWN
ADC1_CSB
ADC1_SCLK
ADC1_SYNC
ADC2_SDIO
ADC2_PDWN
ADC2_CSB
ADC2_SCLK
ADC2_SYNC
DAC1_IRQn
DAC1_RESETn
DAC1_SPI_CSn
DAC1_SPI_SCLK
DAC1_SPI_SDO
DAC1_SPI_SDIO
DAC1_TXEN0
DAC1_TXEN1
DAC2_IRQn
DAC2_RESETn
DAC2_SPI_CSn
DAC2_SPI_SCLK
DAC2_SPI_SDO
DAC2_SPI_SDIO
DAC2_TXEN0
DAC2_TXEN1
RTM_FPGA_LVDS1_N
RTM_FPGA_LVDS1_P
SI_CLK_OUT2_N
SI_CLK_OUT2_P
FPGA_REF_CLK_N
FPGA_REF_CLK_P
RTM_FPGA_LVDS2_N
RTM_FPGA_LVDS2_P
REC_CLOCK_N
REC_CLOCK_P
FPGA_CFG_DIN
DIO0
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
DIO9
P1V8
J58
MTLW-106-07-L-D-250
IO_25_14
IO_L24N_T3_A00_D16_14
IO_L24P_T3_A01_D17_14
IO_L23N_T3_A02_D18_14
IO_L23P_T3_A03_D19_14
IO_L22N_T3_A04_D20_14
IO_L22P_T3_A05_D21_14
IO_L21N_T3_DQS_A06_D22_14
IO_L21P_T3_DQS_14
IO_L20N_T3_A07_D23_14
IO_L20P_T3_A08_D24_14
IO_L19N_T3_A09_D25_VREF_14
IO_L19P_T3_A10_D26_14
IO_L18N_T2_A11_D27_14
IO_L18P_T2_A12_D28_14
IO_L17N_T2_A13_D29_14
IO_L17P_T2_A14_D30_14
IO_L16N_T2_A15_D31_14
IO_L16P_T2_CSI_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L14N_T2_SRCC_14
IO_L14P_T2_SRCC_14
IO_L13N_T2_MRCC_14
IO_L13P_T2_MRCC_14
IO_L12N_T1_MRCC_14
IO_L12P_T1_MRCC_14
IO_L11N_T1_SRCC_14
IO_L11P_T1_SRCC_14
IO_L10N_T1_D15_14
IO_L10P_T1_D14_14
IO_L9N_T1_DQS_D13_14
IO_L9P_T1_DQS_14
IO_L8N_T1_D12_14
IO_L8P_T1_D11_14
IO_L7N_T1_D10_14
IO_L7P_T1_D09_14
IO_L6N_T0_D08_VREF_14
IO_L6P_T0_FCS_B_14
IO_L5N_T0_D07_14
IO_L5P_T0_D06_14
IO_L4N_T0_D05_14
IO_L4P_T0_D04_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L2N_T0_D03_14
IO_L2P_T0_D02_14
IO_L1N_T0_D01_DIN_14
IO_L1P_T0_D00_MOSI_14
IO_0_14
1V8 bank
XC7A15T-1CSG325
P3V3F
OSC2
VCC
OUT
ST
GND
50MHz
+Value
100nF
C449
49R9
R115
SI5324_RST
HMC_RESET
HMC_CFG
USR_UART_N
USR_UART_P
CLK_MEZZ_IO[15:0]
HMC_SPI_SCLK
HMC_SPI_SDATA
HMC_SPI_SLEN
CAL_ADC_DIN
CAL_ADC_DOUT
CAL_ADC_MCLK1
CAL_ADC_MCLK2
CAL_ADC_SCLK
CAL_ADC_SYNCn
ARTIQ_Sayma
FPGA_7A15T
SIZE
A2
DWG NO
1
REV
v0.9
DRAWN BY
G.K.
SHEET
9
OF
18
2016/11/07:18:03:57







ARTIQ Sayma

TITLE: FPGA_7A15T_POWER

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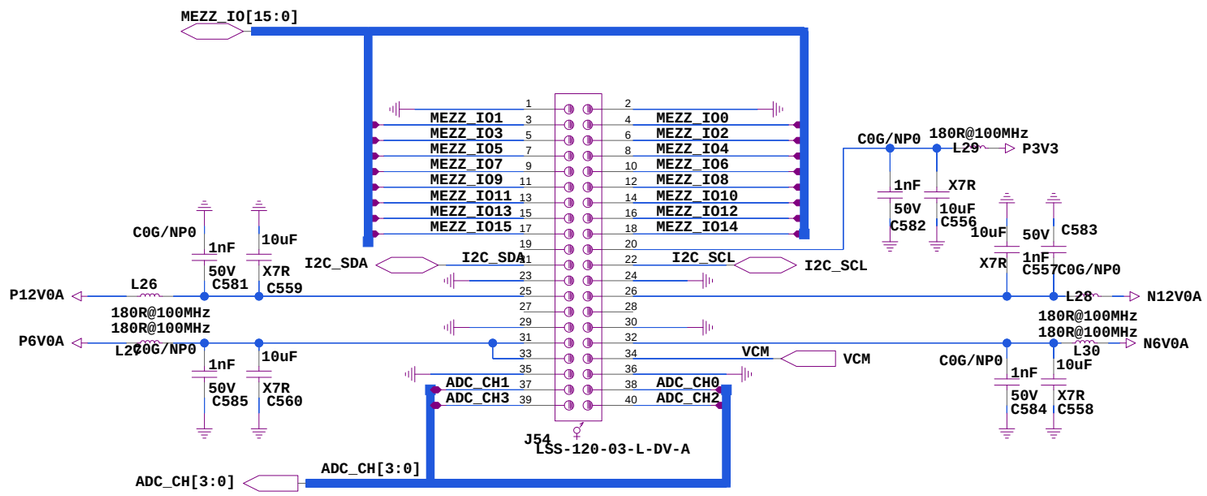

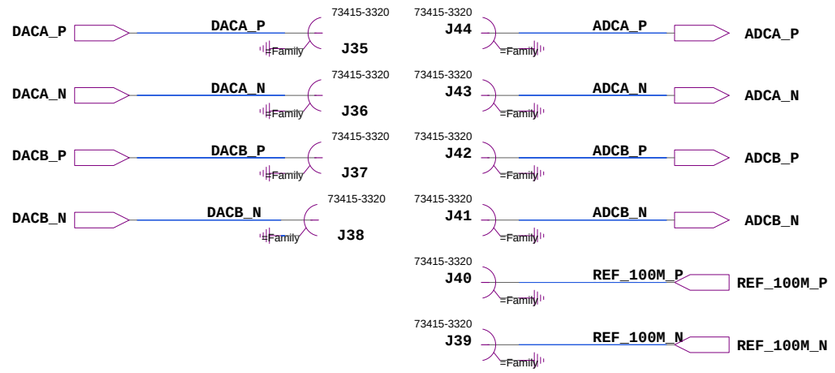

+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

ADC_DAC_AFE_Mezzanine

ARTIQ

TITLE

ARTIQ Sayma

SIZE	DWG NO	REV
A3		v0.9

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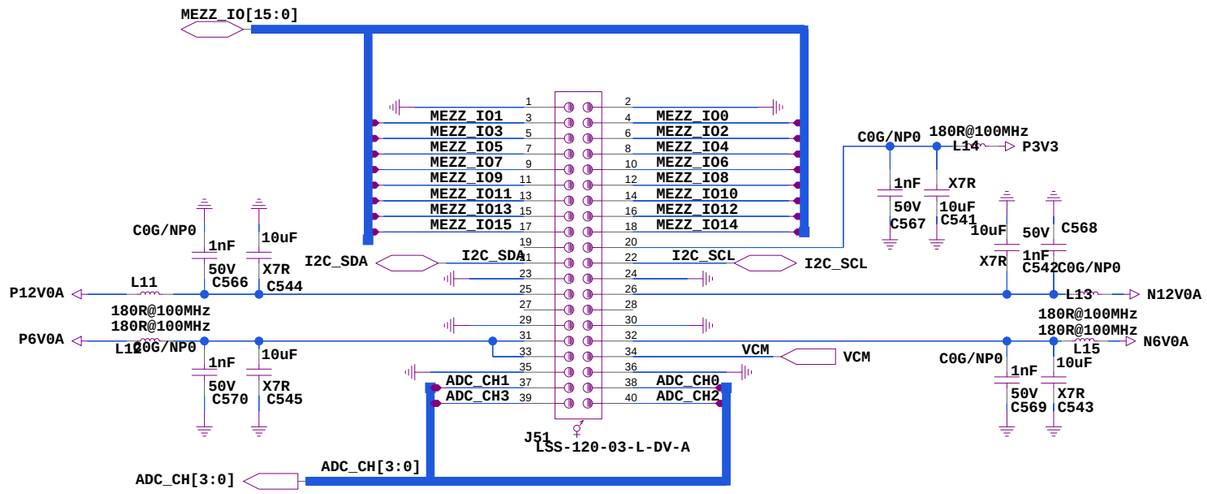
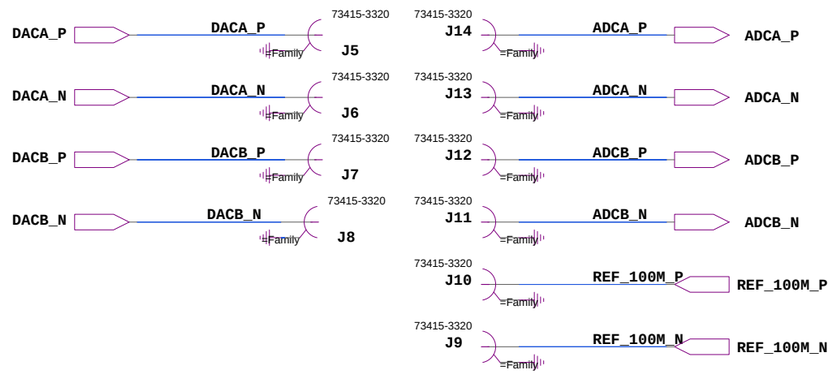
G.K.	11	18	2016/11/07:18:03:56





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ

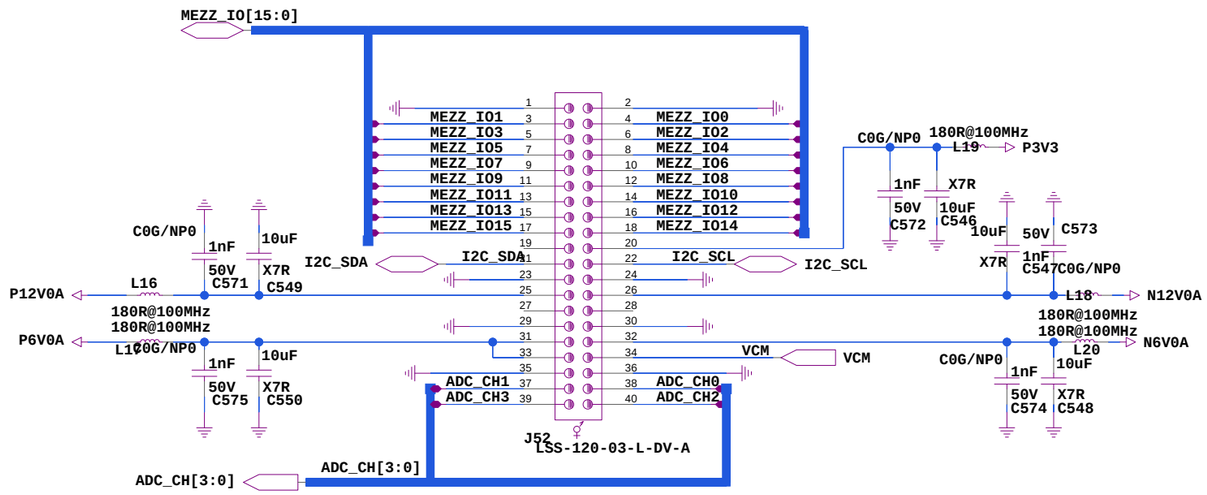
ADC_DAC_AFE_Mezzanine

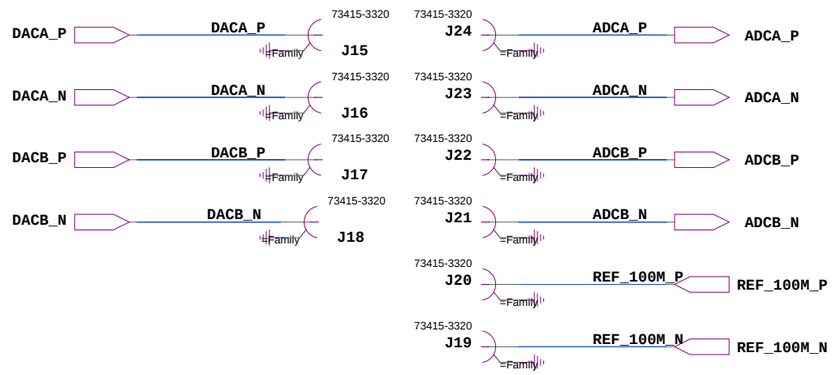
TITLE

ARTIQ Sayma

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	12	18	2016/11/07:18:03:56





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

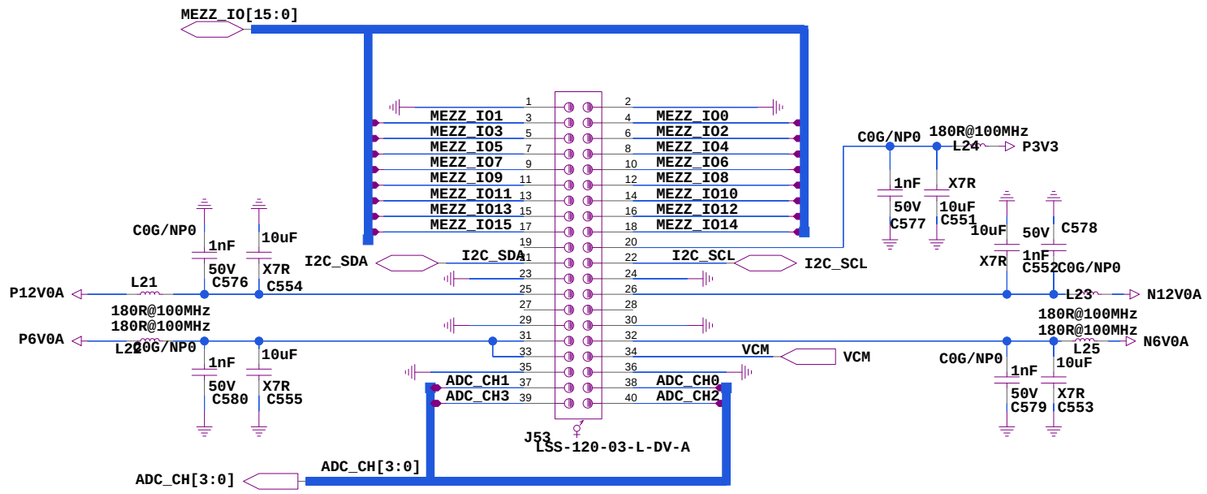
ARTIQ

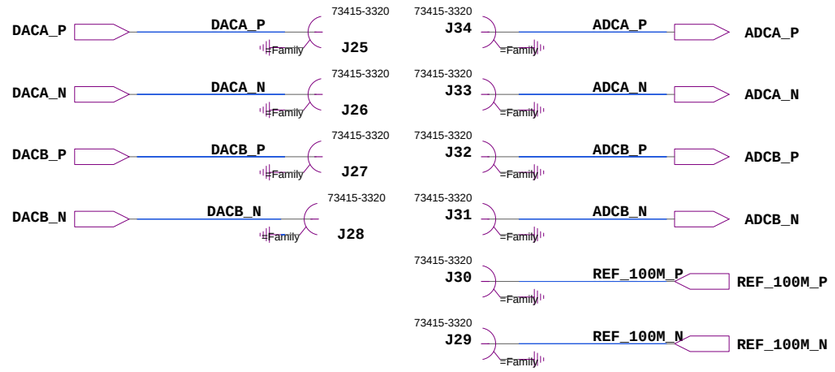
ADC_DAC_AFE_Mezzanine

TITLE: ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	13	18	2016/11/07:18:03:56





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

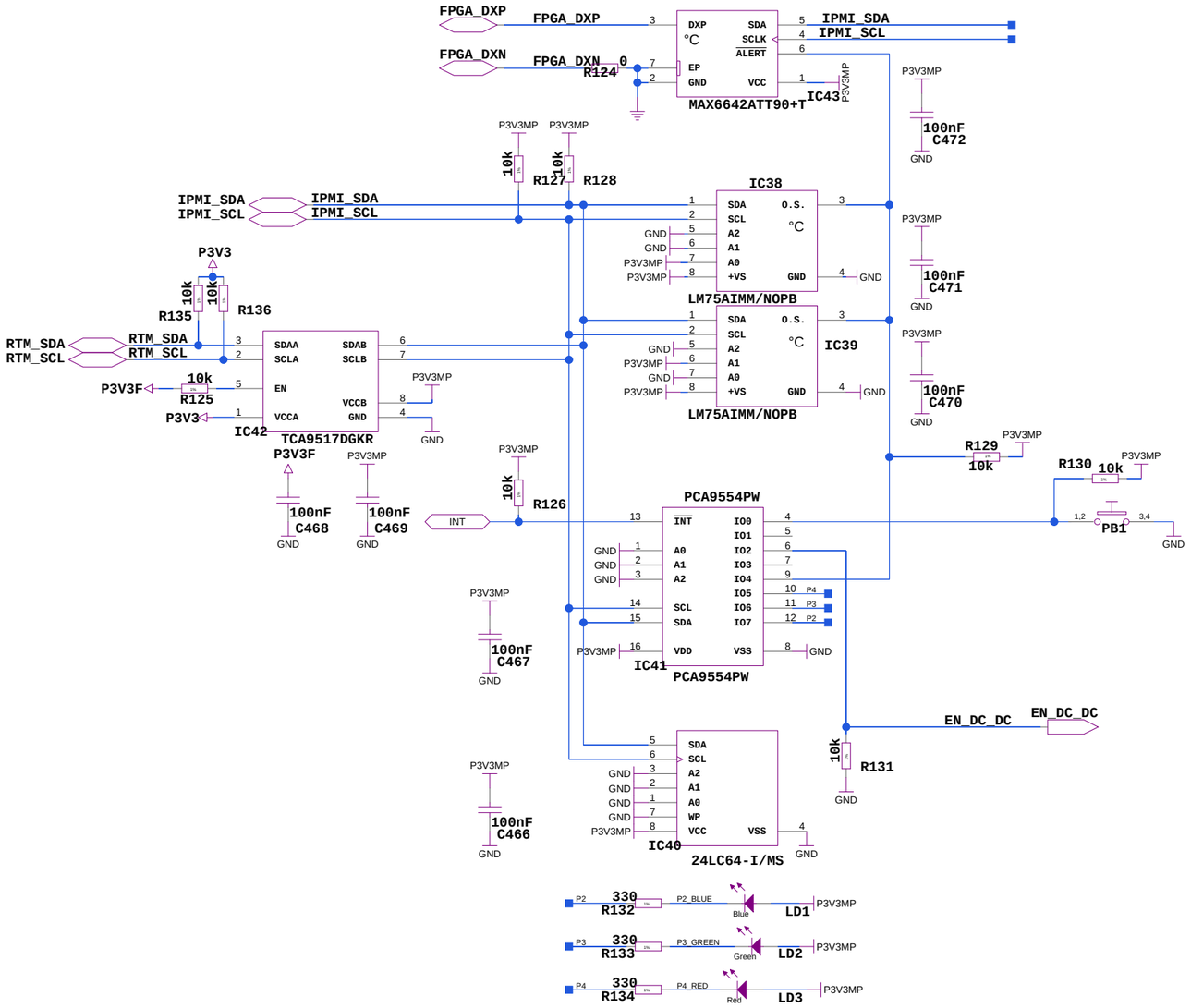
ARTIQ

ADC_DAC_AFE_Mezzanine

TITLE: ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	14	18	2016/11/07:18:03:56

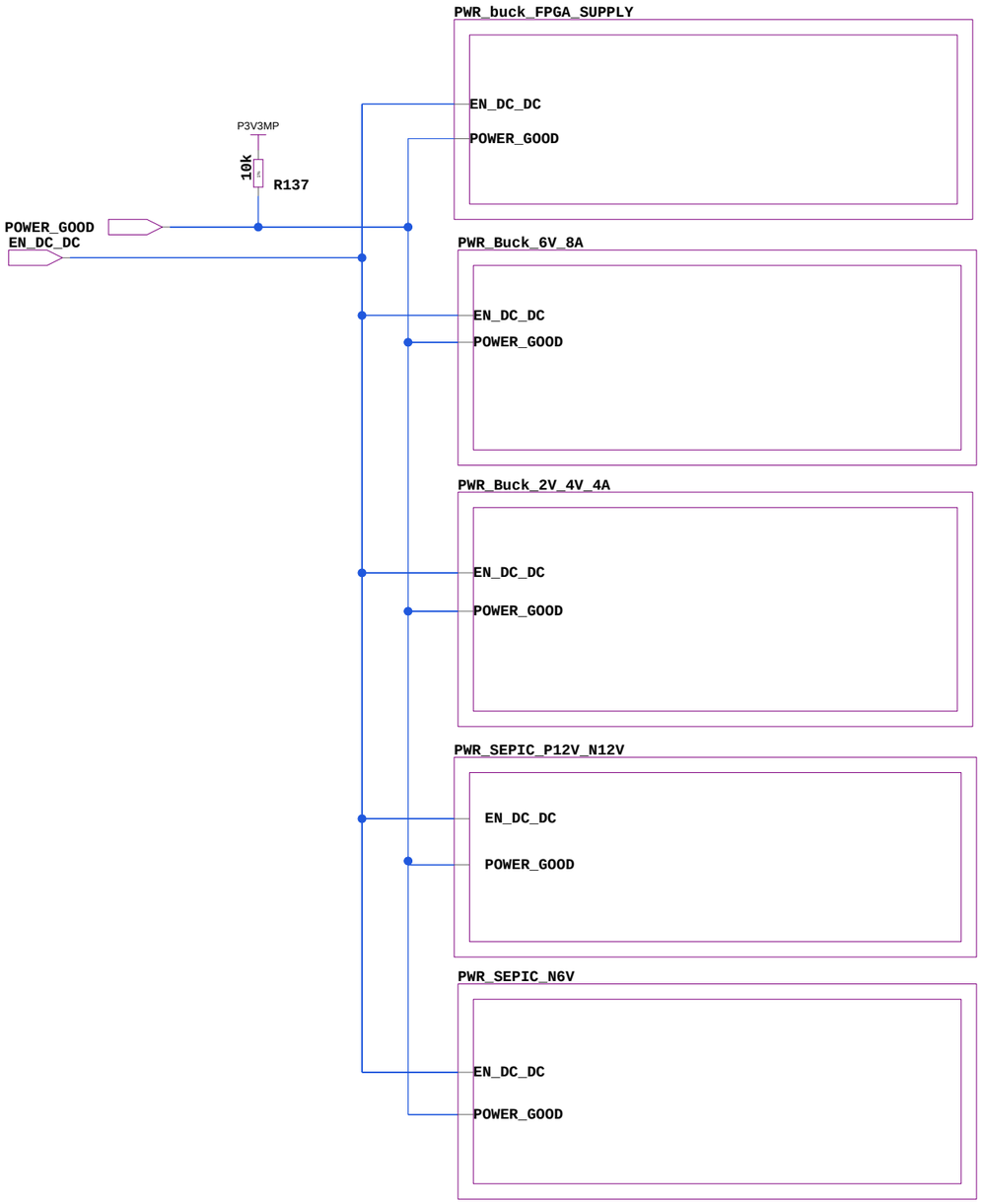


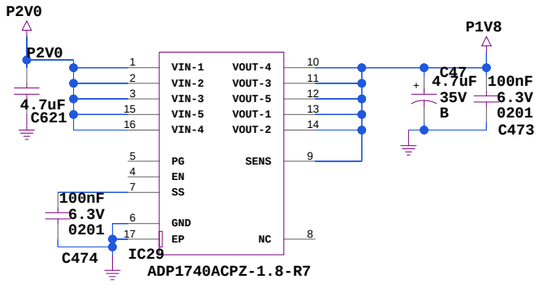
ARTIQ Sayma

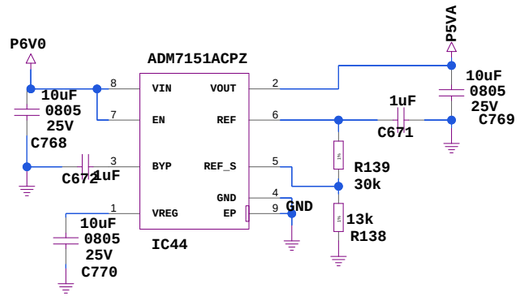
RTM_IPMI

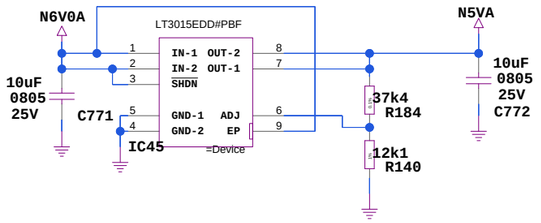
SIZE	DWG NO	REV
A3		v0.9

DRAWN BY	SHEET		
G.K.	15	of 18	2016/11/07:18:03:59









RTM modules power requirements

+12VDC @ 1A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 250 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 8 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 750 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

RTM power requirements

+4VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz
+2VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

ARTIQ

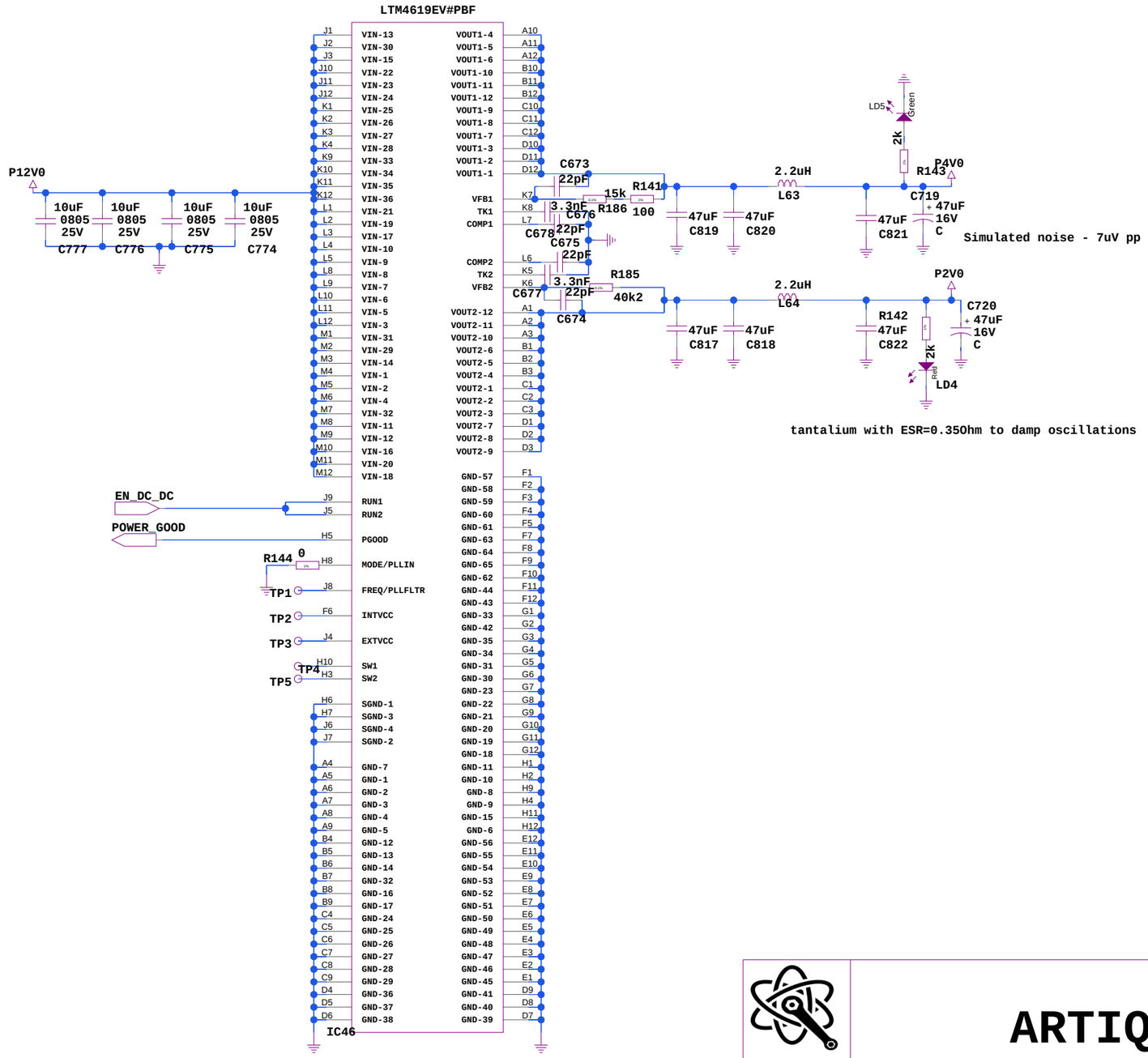
ARTIQ Sayma

TITLE

RTM_POWER_SUPPLY

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	16	18	2016/11/07:18:03:59



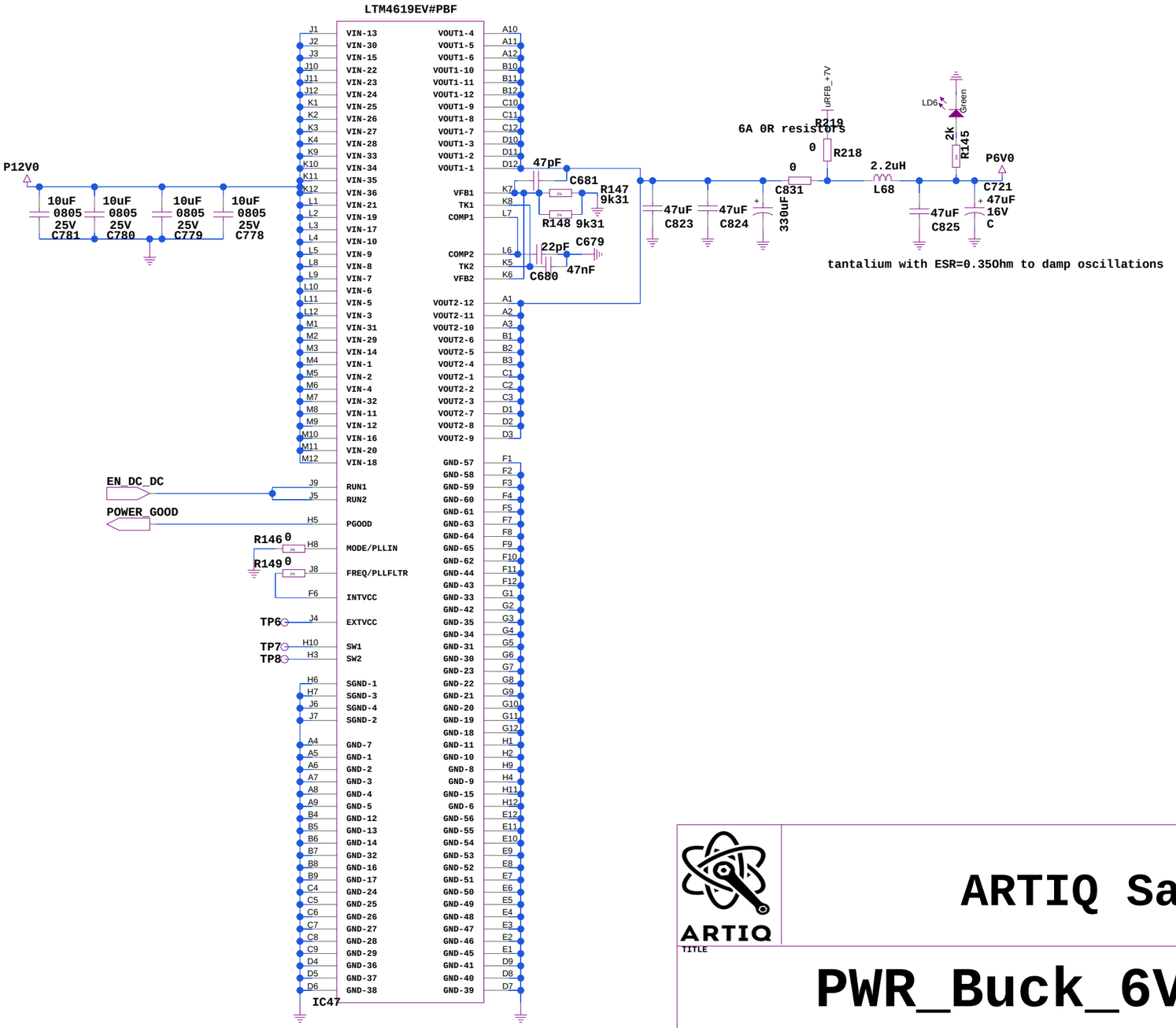
ARTIQ Sayma

TITLE

PWR_Buck_2V_4V_4A

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	17	18	2016/11/07:18:04:02



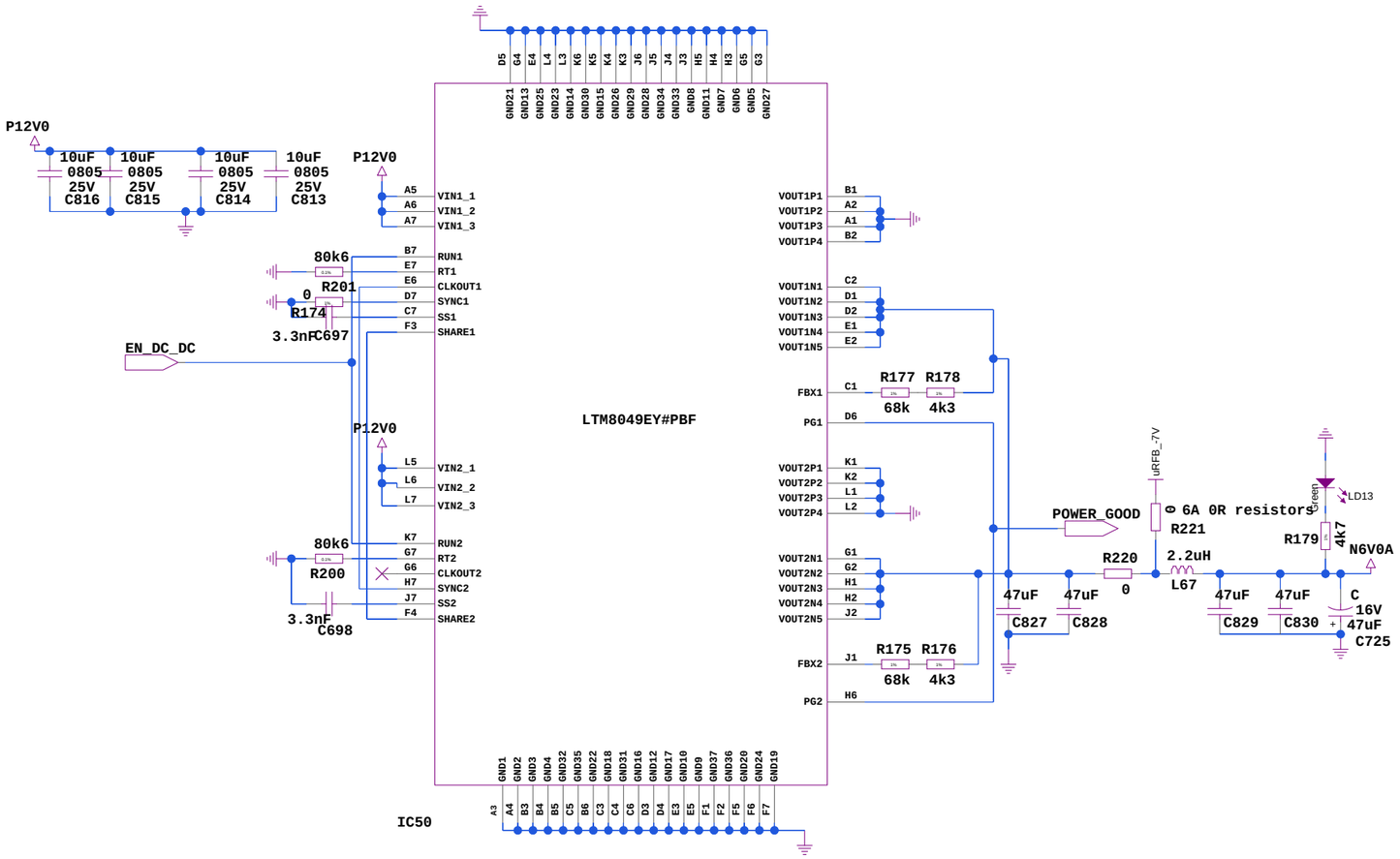
ARTIQ Sayma

TITLE

PWR_Buck_6V_8A

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	18	18	2016/11/07:18:04:02



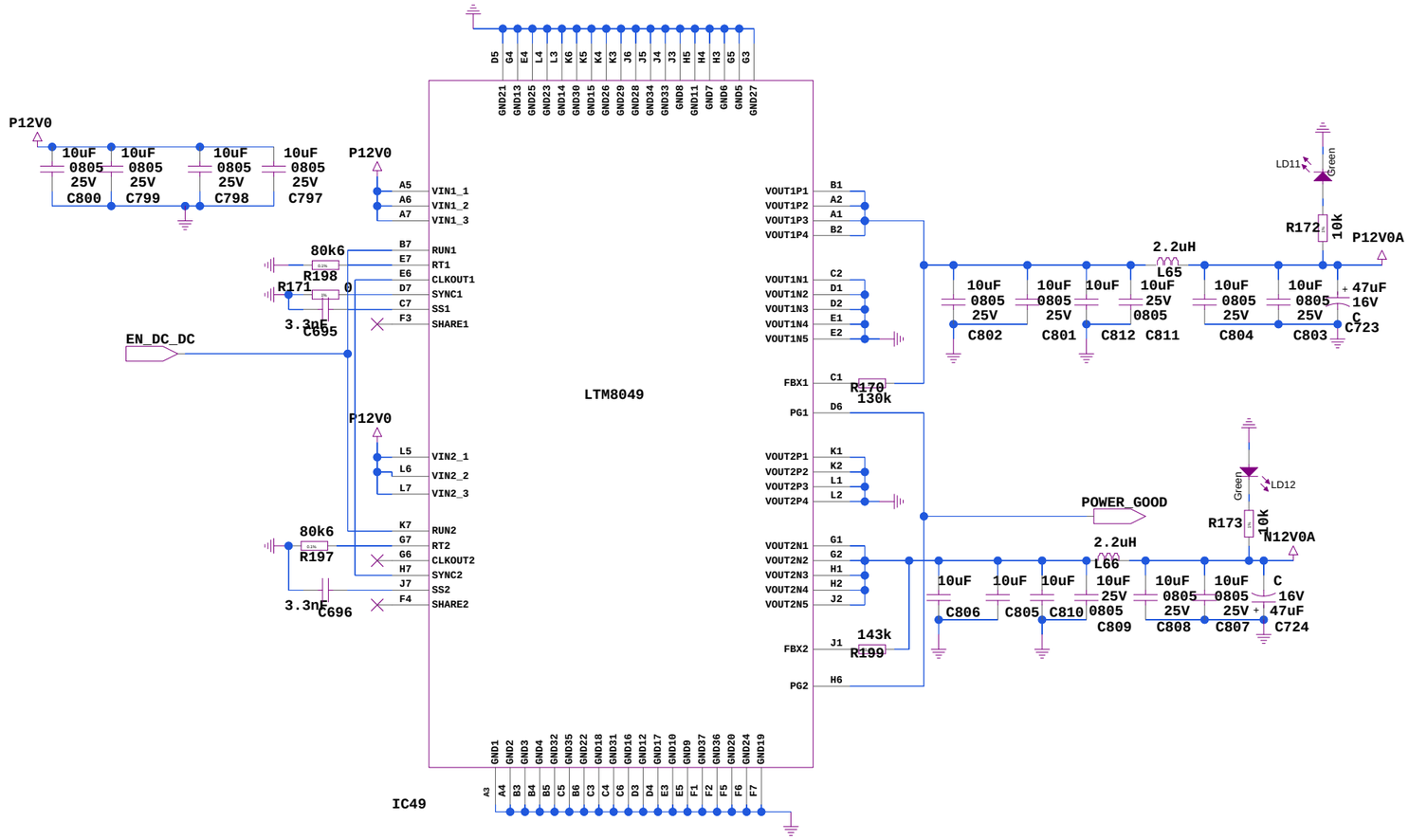
ARTIQ Sayma

TITLE

PWR_SEPIC_N6V

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	19	18	2016/11/07:18:04:03



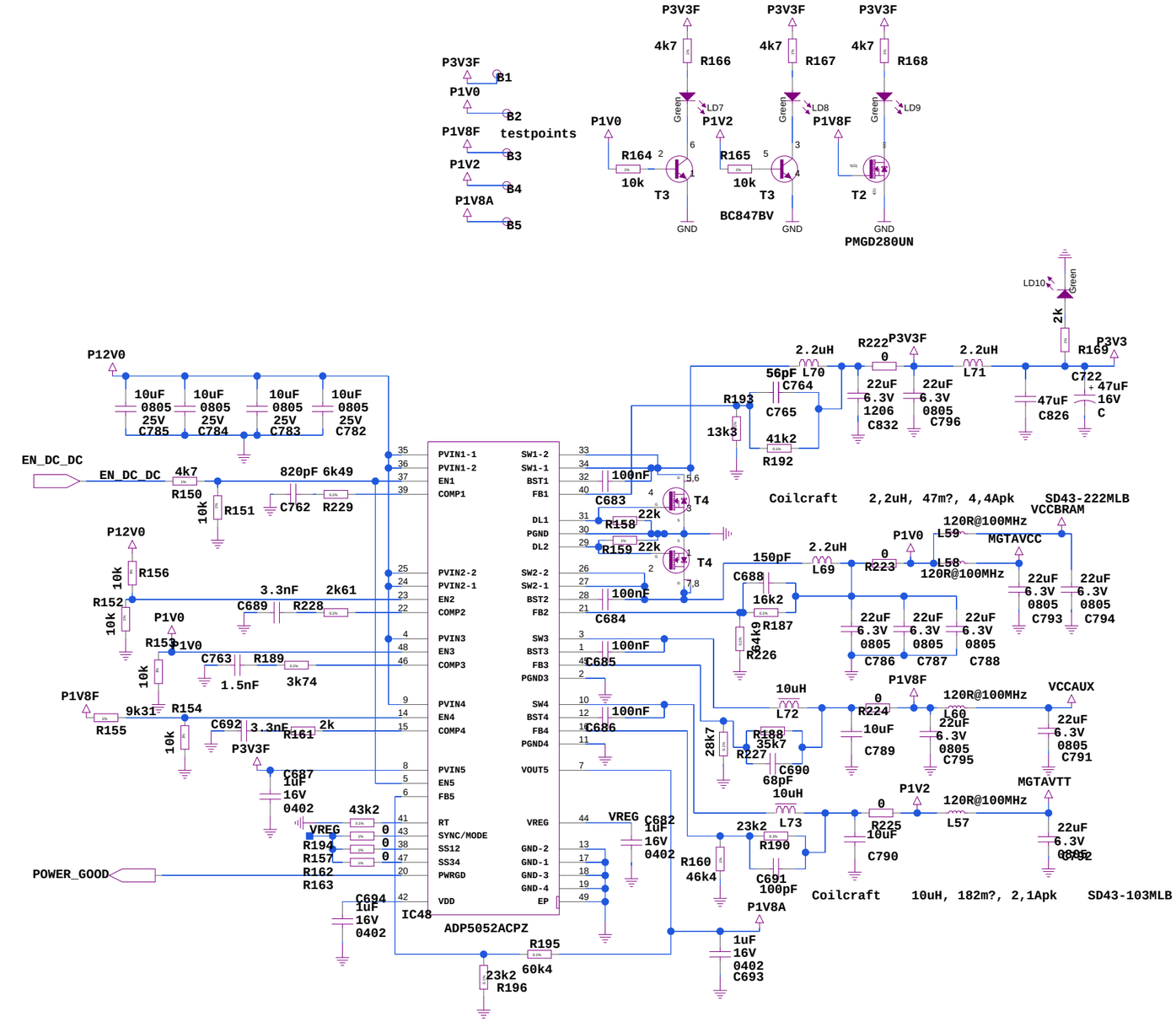
ARTIQ Sayma

TITLE

PWR_SEPIC_P12V_N12V

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	20	18	2016/11/07:18:04:02



ARTIQ

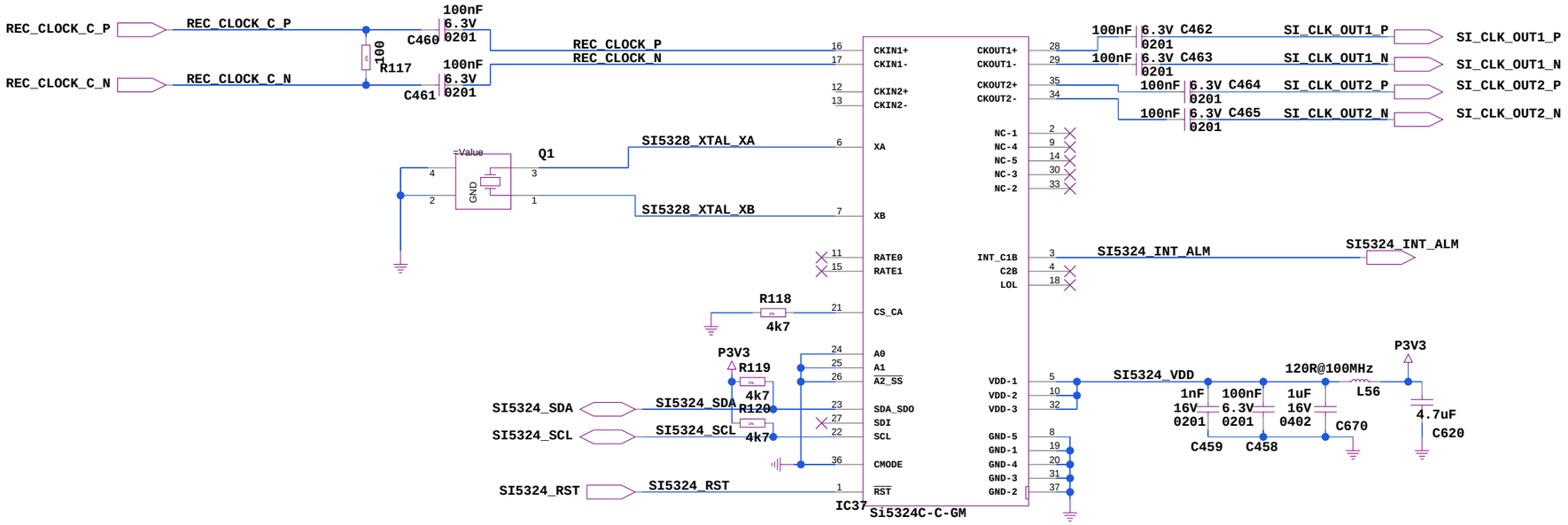
ARTIQ Sayma

TITLE

PWR_buck_FPGA_SUPPLY

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	21	18	2016/11/07:18:04:02



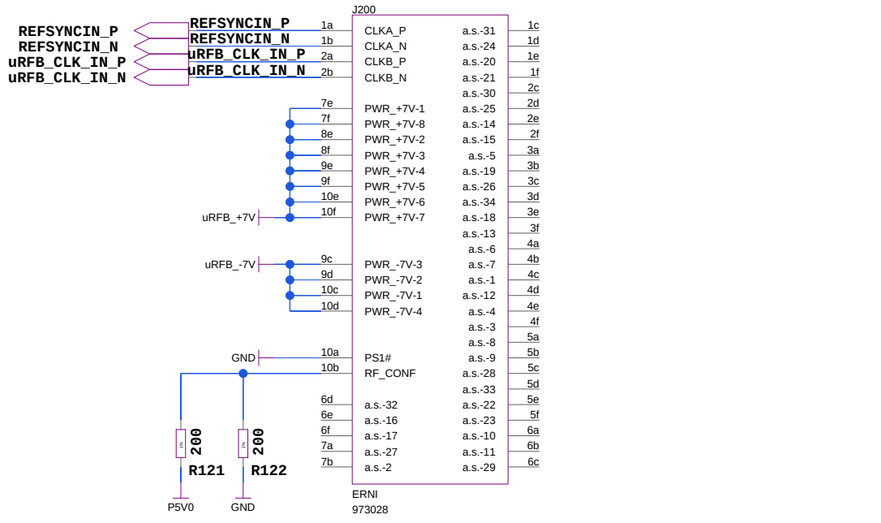
ARTIQ Sayma

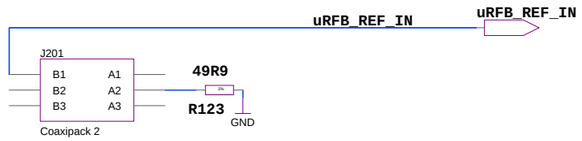
TITLE

SI5324_CLK_RECOVERY

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	22	18	2016/11/07:18:03:56





uRFB_Connectors

ARTIQ

TITLE

ARTIQ Sayma

SIZE	DWG NO	REV
A3		1 v0.9

DRAWN BY	SHEET	of	
G.K.	23	18	2016/11/07:18:03:59