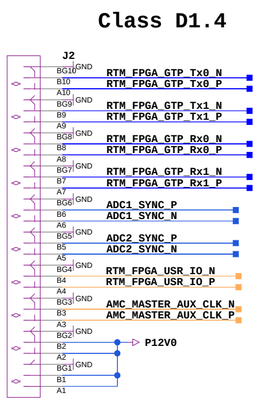
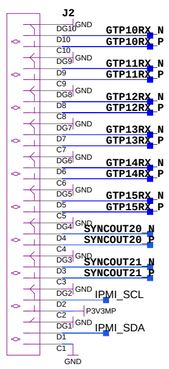
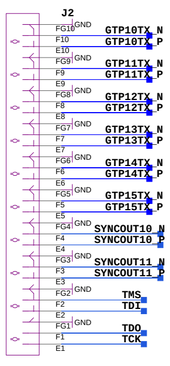
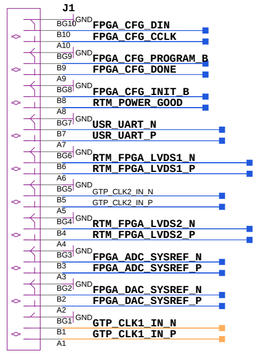
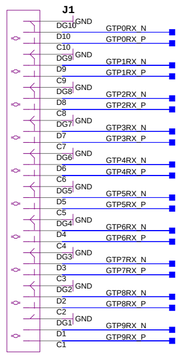
Class D1.4

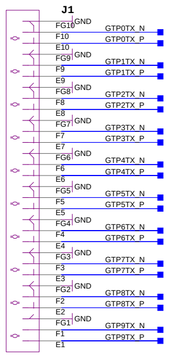


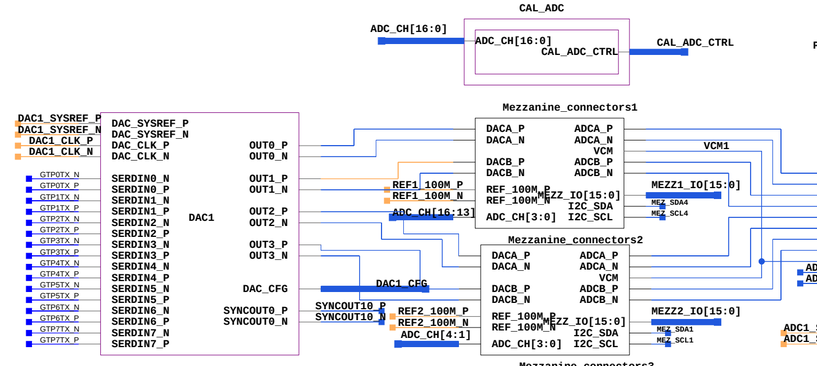


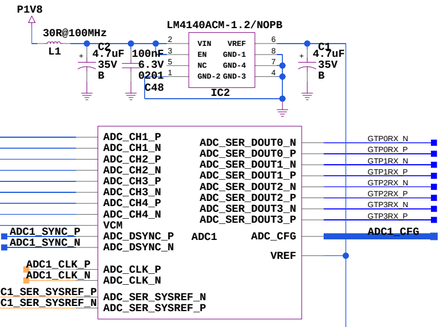


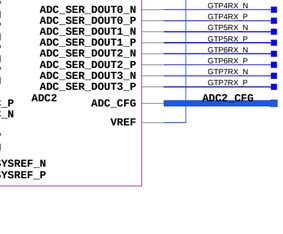


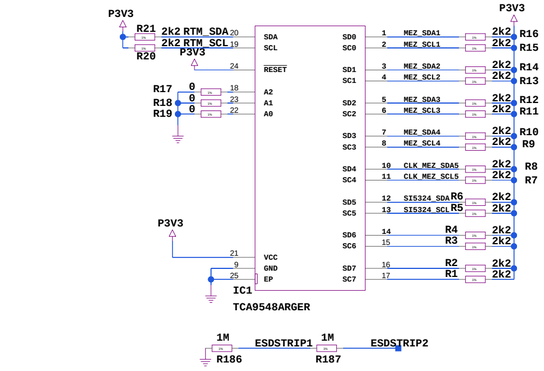


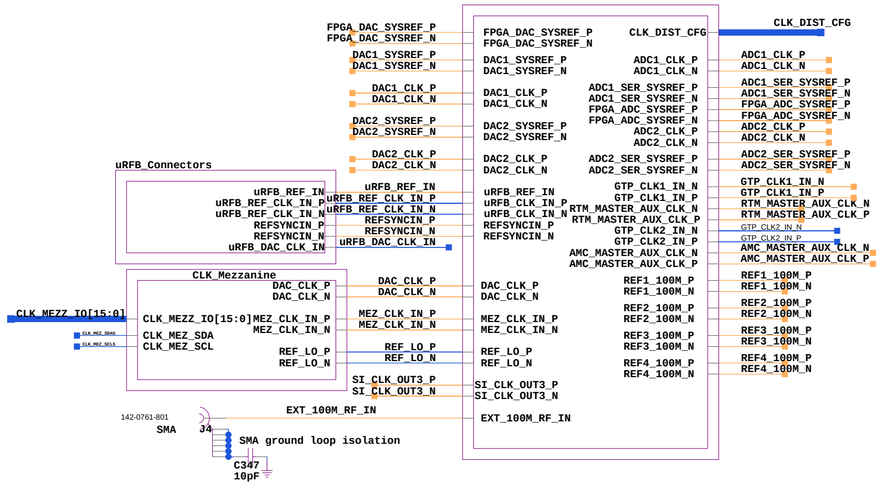


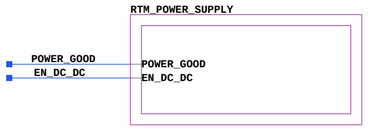


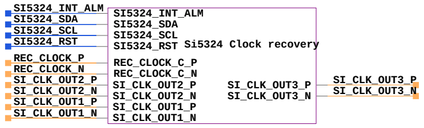


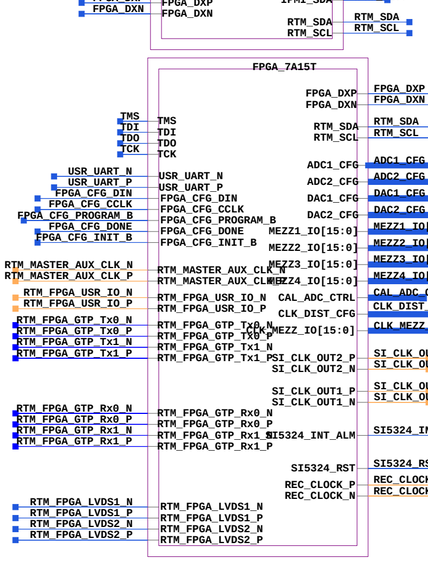












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ARTIQ

TITLE

ARTIQ Sayma

Sayma_RTM

SIZE	DWG NO	REV
A2	1	v0.9

DRAWN BY	SHEET	of	
G.K.	1	18	23/11/2016:22:15

ADC_JESD204B

ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	OF	
G.K.	2	18	23/11/2016:19:38

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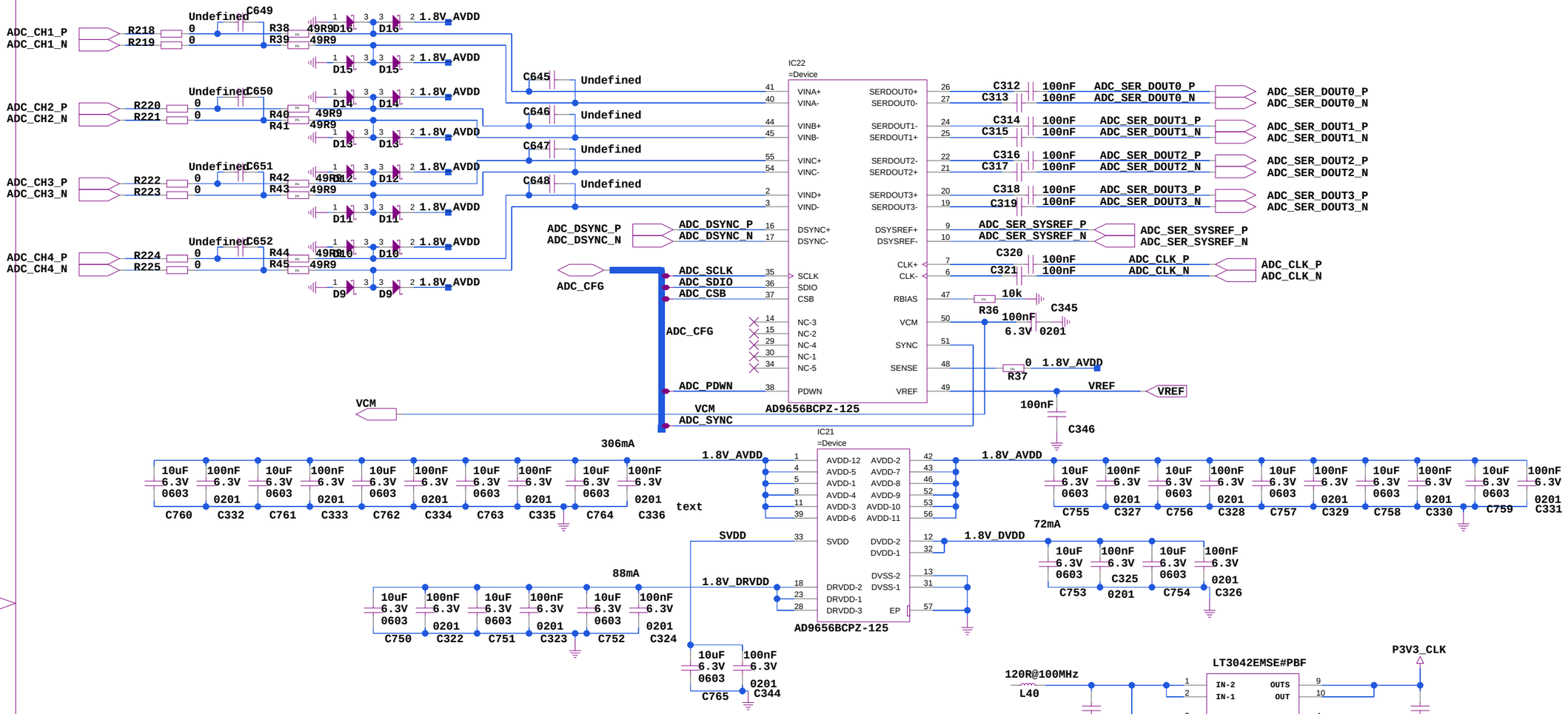

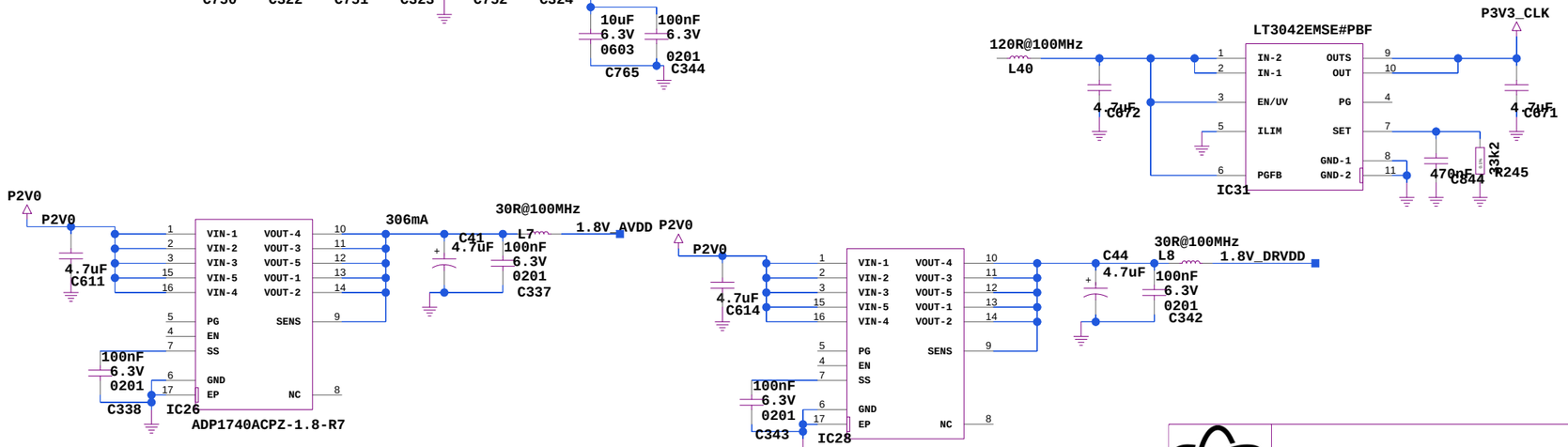

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ARTIQ

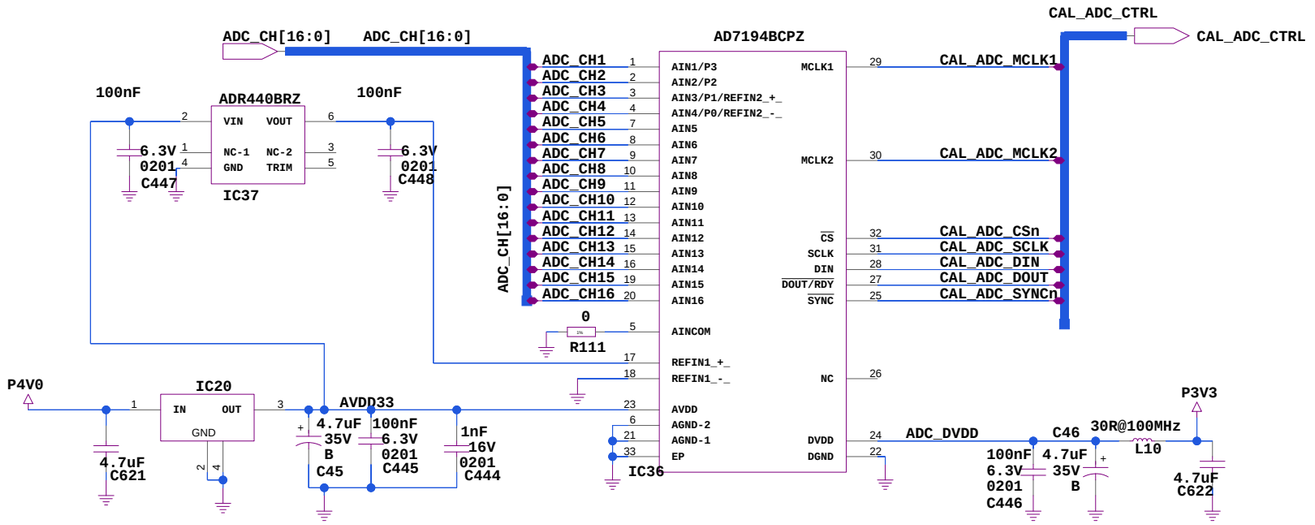
ADC_JESD204B

TITLE

ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET			
G.K.	3	of	18	23/11/2016:19:38



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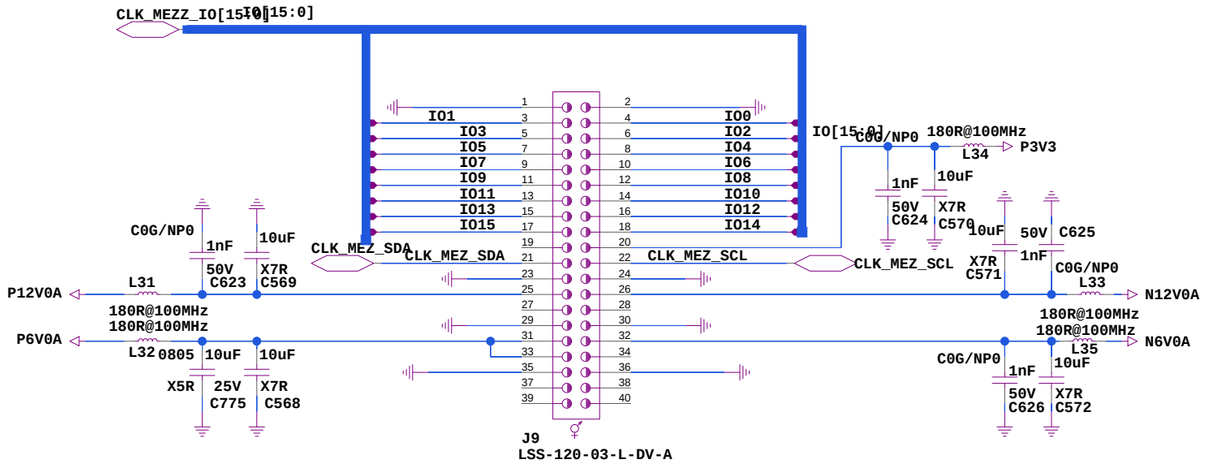
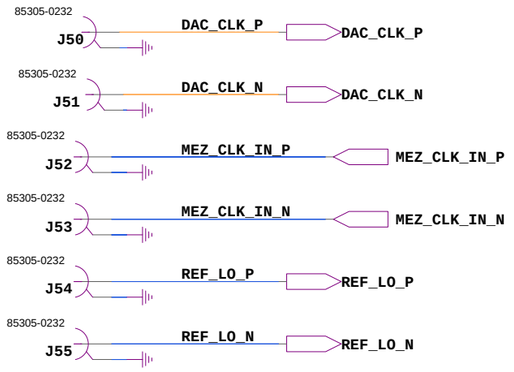
ARTIQ Sayma

TITLE: CAL_ADC

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	4	18	23/11/2016:19:37





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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ARTIQ

TITLE

ARTIQ Sayma

CLK_Mezzanine

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	5	18	23/11/2016:19:37

IOVDD=3.3

SERDIN0_P
SERDIN0_N
SERDIN1_P
SERDIN1_N
SERDIN2_P
SERDIN2_N
SERDIN3_P
SERDIN3_N
SERDIN4_P
SERDIN4_N
SERDIN5_P
SERDIN5_N
SERDIN6_P
SERDIN6_N
SERDIN7_P
SERDIN7_N

C134 6.3V 100nF
C133 6.3V 100nF
C136 6.3V 100nF
C135 6.3V 100nF
C138 6.3V 100nF
C137 6.3V 100nF
C140 6.3V 100nF
C139 6.3V 100nF
C142 6.3V 100nF
C141 6.3V 100nF
C144 6.3V 100nF
C143 6.3V 100nF
C146 6.3V 100nF
C145 6.3V 100nF
C148 6.3V 100nF
C147 6.3V 100nF

15 16 18 19 26 27 29 30 38 37 41 40 49 48 52 51

SERDIN0+ SERDIN0- SERDIN1+ SERDIN1- SERDIN2+ SERDIN2- SERDIN3+ SERDIN3- SERDIN4+ SERDIN4- SERDIN5+ SERDIN5- SERDIN6+ SERDIN6- SERDIN7+ SERDIN7-

DAC_TXEN0 11 TXEN0
DAC_TXEN1 12 TXEN1

DAC_CLK_P 2 CLK+
DAC_CLK_N 3 CLK-

DAC_SPI_SDO 62 SDO
DAC_SPI_SDIO 63 SDIO
DAC_SPI_SCLK 64 SCLK
DAC_SPI_CSn 65 CS

SIOVDD33 35 SIOVDD
IOVDD 66 IOVDD

VTT
1uF 16V 0402 C629
100nF 6.3V 0201 C52
100nF 6.3V 0201 C51
100nF 6.3V 0201 C50
100nF 6.3V 0201 C49
21 25 42 46 VTT-1 VTT-2 VTT-4 VTT-3

AVDD33 80 AVDD33-6
70 AVDD33-8
72 AVDD33-1
75 AVDD33-5
77 AVDD33-3
82 AVDD33-2
85 AVDD33-4
67 AVDD33-7

CVDD12 71 CVDD12-2
76 CVDD12-3
81 CVDD12-4
87 CVDD12-1

DVDD12 13 DVDD12-2
14 DVDD12-1
53 DVDD12-3

IC3 AD9154BCPZ

OUT0+ OUT0- OUT1+ OUT1- OUT2+ OUT2- OUT3+ OUT3-
84 OUT0_P
83 OUT0_N
78 OUT1_P
79 OUT1_N
74 OUT2_P
73 OUT2_N
68 OUT3_P
69 OUT3_N
OUT0_P OUT0_N OUT1_P OUT1_N OUT2_P OUT2_N OUT3_P OUT3_N

SYNCOUT0+ SYNCOUT0- SYNCOUT1+ SYNCOUT1-
23 SYNCOUT0_P
24 SYNCOUT0_N
44
43
SYNCOUT0_P SYNCOUT0_N

PDP_OUT0 59
PDP_OUT1 58

SYSREF+ 5 DAC_SYSREF_P
SYSREF- 6 DAC_SYSREF_N
DAC_SYSREF_P DAC_SYSREF_N

LDO_BYP1 34
LDO_BYP2 88
R23 1 1uF 16V C631
R22 1 0402 C630
1uF 16V 0402

IRQ 60 DAC_IRQn
RESET 61 DAC_RESETn

I120 86 R188 4k02

DNC-1 54
DNC-2 55

DAC_CFG
DAC_IRQn
DAC_RESETn
DAC_SPI_CSn
DAC_SPI_SCLK
DAC_SPI_SDO
DAC_SPI_SDIO
DAC_TXEN0
DAC_TXEN1

Replace with W2L16C473MAT1S

PVDD12 1 57 7 8 9 10 56 4
4.7nF 10V 0201 C71
4.7nF 10V 0201 C72
4.7nF 10V 0201 C70
4.7nF 10V 0201 C69
100nF 6.3V 0201 C68
100nF 6.3V 0201 C67
1nF 16V 0201 C66
1nF 16V 0201 C65
100nF 6.3V 0201 C63
1nF 16V 0201 C64
4.7uF 35V B C4
47uF 16V C C708
100nF 6.3V 0201 C73
100nF 6.3V 0201 C74
100nF 6.3V 0201 C75
1nF 16V 0201 C76
1nF 16V 0201 C77

SVDD12 17 28 45 22 47 39 31 32 33 36 20 50
4.7nF 10V 0201 C84
4.7nF 10V 0201 C85
4.7nF 10V 0201 C83
4.7nF 10V 0201 C82
1nF 16V 0201 C91
1nF 16V 0201 C92
1nF 16V 0201 C81
1nF 16V 0201 C80
100nF 6.3V 0201 C78
1nF 16V 0201 C79
4.7uF 35V B C5
47uF 16V C C709
100nF 6.3V 0201 C86
100nF 6.3V 0201 C87
100nF 6.3V 0201 C88
1nF 16V 0201 C89
1nF 16V 0201 C90

SDVDD12
4.7nF 10V 0201 C121
4.7nF 10V 0201 C122
4.7nF 10V 0201 C120
4.7nF 10V 0201 C119
100nF 6.3V 0201 C118
100nF 6.3V 0201 C117
1nF 16V 0201 C116
1nF 16V 0201 C115
100nF 6.3V 0201 C113
1nF 16V 0201 C114
4.7uF 35V B C8
47uF 16V C C712

XVDD33
4.7uF 35V B C10
47uF 16V C C714

PLLVDD12
1nF 16V 0201 C125
100nF 6.3V 0201 C123
1nF 16V 0201 C124
4.7uF 35V B C9
47uF 16V C C713

SIOVDD33
1nF 16V 0201 C128
100nF 6.3V 0201 C126
1nF 16V 0201 C127
4.7uF 35V B C11
47uF 16V C C715

IOVDD
100nF 6.3V 0201 C132
1nF 16V 0201 C131
100nF 6.3V 0201 C129
1nF 16V 0201 C130
4.7uF 35V B C12
47uF 16V C C716

P1V8
L36 120R@100MHz
C632 1uF 16V 0402
100nF 6.3V 0201 C161
1nF 16V 0201 C162
IOVDD

Replace with W2L16C473MAT1S

P2V0
4.7uF C593
IC5 VIN-1 VIN-2 VIN-3 VIN-5 VIN-4 VOUT-4 VOUT-3 VOUT-5 VOUT-1 VOUT-2 PG EN SS GND EP SENS NC
100nF 6.3V 0201 C150
PVDD12
4.7uF 35V B C13
100nF 6.3V 0201 C149

P2V0
4.7uF C595
IC7
100nF 6.3V 0201 C154
SVDD12
4.7uF 35V B C15
100nF 6.3V 0201 C153

P2V0
4.7uF C594
IC6
100nF 6.3V 0201 C152
DVDD12
4.7uF 35V B C14
100nF 6.3V 0201 C151

P2V0
4.7uF C596
IC8
100nF 6.3V 0201 C156
PLLVDD12
4.7uF 35V B C16
100nF 6.3V 0201 C155

P2V0
4.7uF C597
IC9
100nF 6.3V 0201 C158
CVDD12
4.7uF 35V B C17
100nF 6.3V 0201 C157

P4V0
4.7uF C598
IC15 LT1963AEST-3.3#PBF IN OUT GND
AVDD33
4.7uF 35V B C18
100nF 6.3V 0201 C159

P4V0
4.7uF C599
IC16 IN OUT GND
SIOVDD33
4.7uF 35V B C19
100nF 6.3V 0201 C160

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ARTIQ Sayma

TITLE: DAC_JESD204B

SIZE	DWG NO	REV
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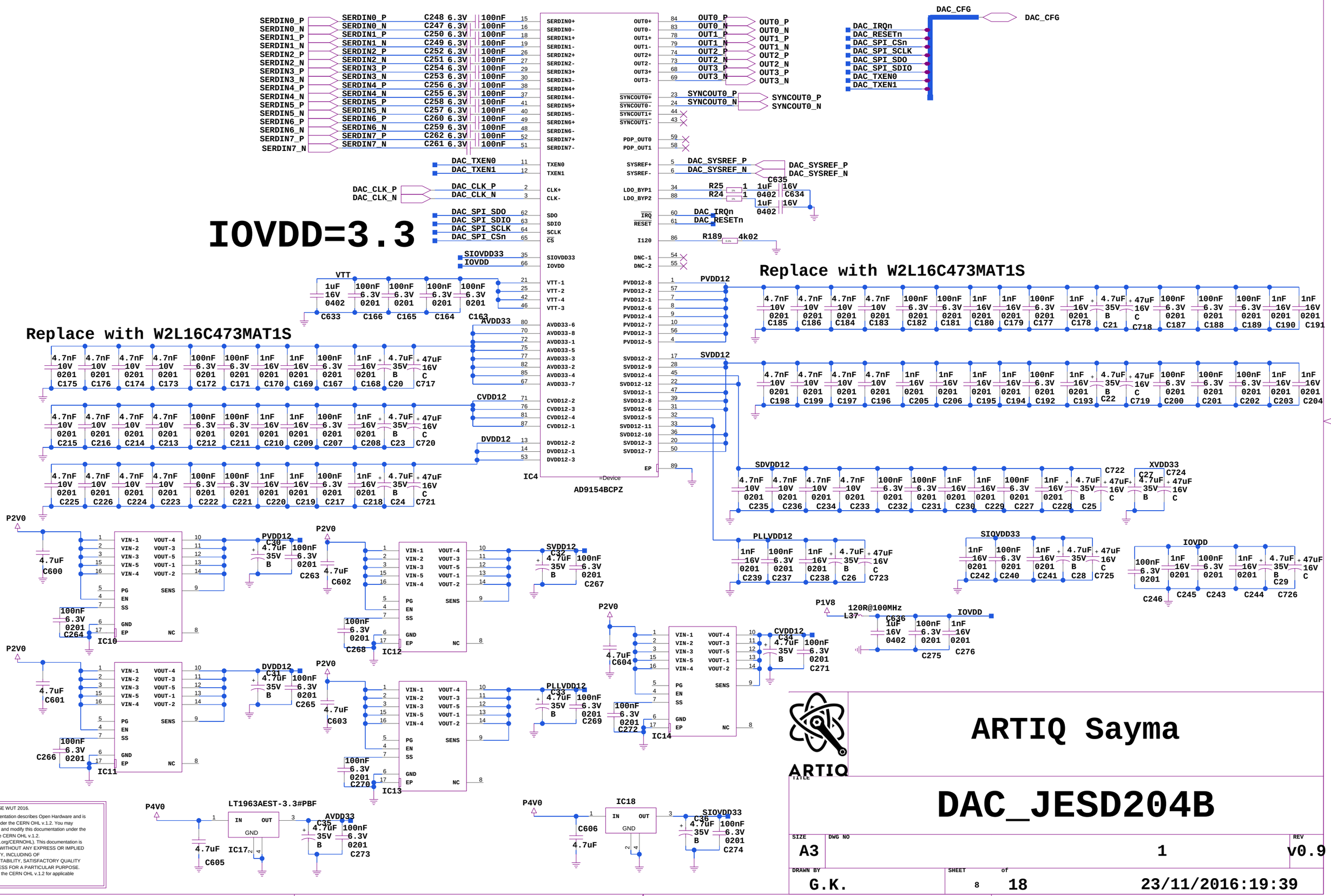
DRAWN BY	SHEET	of	
G.K.	7	18	23/11/2016:19:39



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P3V3F
L78
120R@100MHz
C352
100nF
DNP
OE
NC
VDD
CLK+
CLK-
GND
=Value
RTM_FPGA_GTP_Rx0_N
RTM_FPGA_GTP_Rx0_P
RTM_FPGA_GTP_Rx1_N
RTM_FPGA_GTP_Rx1_P
RTM_FPGA_GTP_CLK_N
RTM_FPGA_GTP_CLK_P
C458
C459
100nF
SI_CLK_OUT1_P
SI_CLK_OUT1_N
RTM_FPGA_GTP_Rx2_N
RTM_FPGA_GTP_Rx2_P
RTM_FPGA_GTP_Rx3_N
RTM_FPGA_GTP_Rx3_P
RTM_FPGA_GTP_Tx0_N
RTM_FPGA_GTP_Tx0_P
RTM_FPGA_GTP_Tx1_N
RTM_FPGA_GTP_Tx1_P
RTM_FPGA_GTP_Tx2_N
RTM_FPGA_GTP_Tx2_P
RTM_FPGA_GTP_Tx3_N
RTM_FPGA_GTP_Tx3_P
XC7A15T-1CSG325_mgt__pcb
XC7A15T-1CSG325
MGTPRXN0_216
MGTPRXP0_216
MGTPRXN1_216
MGTPRXP1_216
MGTREFCLK0P_216
MGTREFCLK0N_216
MGTREFCLK1P_216
MGTREFCLK1N_216
MGTPRXN2_216
MGTPRXP2_216
MGTPRXN3_216
MGTPRXP3_216
MGTPTXN0_216
MGTPTXP0_216
MGTPTXN1_216
MGTPTXP1_216
MGTPTXN2_216
MGTPTXP2_216
MGTPTXN3_216
MGTPTXP3_216
XC7A15T-1CSG325_other_216_pcb
MGTAVTT
100
R113
MGTRREF_216
XC7A15T-1CSG325
MASTER SATA
GND-3
A+_Tx_
A-_Tx_
GND-1
B-_Rx_
B+_Rx_
GND-2
KEY
Tx3_C_P
Tx3_C_N
Rx3_C_N
Rx3_C_P
C450
C451
C452
C453
100nFRTM_FPGA_GTP_Tx3_P
100nFRTM_FPGA_GTP_Tx3_N
100nFRTM_FPGA_GTP_Rx3_N
100nFRTM_FPGA_GTP_Rx3_P
J70
SLAVE SATA
Rx2_C_P
Rx2_C_N
Tx2_C_N
Tx2_C_P
C457
C456
C455
C454
100nFRTM_FPGA_GTP_Rx2_P
100nFRTM_FPGA_GTP_Rx2_N
100nFRTM_FPGA_GTP_Tx2_N
100nFRTM_FPGA_GTP_Tx2_P
J71
FPGA_7A15T_POWER
FPGA_DXP
FPGA_DXN
XC7A15T-1CSG325_0_pcb
R114
FPGA_CFG_CCLK
FPGA_CFG_DONE
FPGA_CFG_INIT_B
R116
R112
FPGA_CFG_PROGRAM_B
TCK
TDI
TDO
TMS
CCLK_0
CFGBVS_0
DONE_0
INIT_B_0
M0_0
M1_0
M2_0
PROGRAM_B_0
TCK_0
TDI_0
TDO_0
TMS_0
3V3 bank
XC7A15T-1CSG325
XC7A15T-1CSG325_14_pcb
ADC1_CFG
ADC2_CFG
DAC1_CFG
ADC1_SDIO
ADC_PDWN
ADC1_CSB
ADC1_SCLK
ADC1_SYNC
ADC2_SDIO
ADC2_CSB
ADC2_SCLK
ADC2_SYNC
DAC1_IRQn
DAC1_SPI_CSn
DAC1_SPI_SCLK
DAC1_SPI_SDO
DAC1_SPI_SDIO
DAC1_TXEN0
DAC1_TXEN1
DAC_RESETn
IO_25_14
IO_L24N_T3_A00_D16_14
IO_L24P_T3_A01_D17_14
IO_L23N_T3_A02_D18_14
IO_L23P_T3_A03_D19_14
IO_L22N_T3_A04_D20_14
IO_L22P_T3_A05_D21_14
IO_L21N_T3_DQS_A06_D22_14
IO_L21P_T3_DQS_14
IO_L20N_T3_A07_D23_14
IO_L20P_T3_A08_D24_14
IO_L19N_T3_A09_D25_VREF_14
IO_L19P_T3_A10_D26_14
IO_L18N_T2_A11_D27_14
IO_L18P_T2_A12_D28_14
IO_L17N_T2_A13_D29_14
IO_L17P_T2_A14_D30_14
IO_L16N_T2_A15_D31_14
IO_L16P_T2_CSI_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L14N_T2_SRCC_14
IO_L14P_T2_SRCC_14
IO_L13N_T2_MRCC_14
IO_L13P_T2_MRCC_14
IO_L12N_T1_MRCC_14
IO_L12P_T1_MRCC_14
IO_L11N_T1_SRCC_14
IO_L11P_T1_SRCC_14
IO_L10N_T1_D15_14
IO_L10P_T1_D14_14
IO_L9N_T1_DQS_D13_14
IO_L9P_T1_DQS_14
IO_L8N_T1_D12_14
IO_L8P_T1_D11_14
IO_L7N_T1_D10_14
IO_L7P_T1_D09_14
IO_L6N_T0_D08_VREF_14
IO_L6P_T0_FCS_B_14
IO_L5N_T0_D07_14
IO_L5P_T0_D06_14
IO_L4N_T0_D05_14
IO_L4P_T0_D04_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L2N_T0_D03_14
IO_L2P_T0_D02_14
IO_L1N_T0_D01_DIN_14
IO_L1P_T0_D00_MOSI_14
IO_0_14
1V8 bank
XC7A15T-1CSG325
REC_CLOCK_N
REC_CLOCK_P
REF_CLK_SRC_SEL_1V8
REF_LO_CLK_SEL_1V8
DAC_CLK_SRC_SEL_1V8
REF_CLK_SRC_EXT_SEL_1V8
DIO0
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
P1V8
J72
MTLW-106-07-L-D-250
FPGA_CFG_DIN
R45
200
CLK_DIST_CFG
P3V3F
OSC1
VCC
OUT
ST
GND
50MHz
100nF
C449
49R9
R115
SI5324_RST
HMC_RESET
USR_UART_N
USR_UART_P
HMC_SPI_SCLK
HMC_SPI_SDATA
HMC7043_SLEN
CLK_MEZZ_IO[15:0]
CAL_ADC_CTRL
CAL_ADC_CSn
CAL_ADC_SYNCn
CAL_ADC_DIN
CAL_ADC_DOUT
CAL_ADC_MCLK1
CAL_ADC_MCLK2
CAL_ADC_SCLK
HMC_SPI_SDO
HMC8830_SPI_SEN
HMC_SPI_GPIO
SI5324_INT_ALM
XC7A15T-1CSG325_15_pcb
MEZZ3_IO[15:0]
IO_25_15
IO_L24N_T3_RS0_15
IO_L24P_T3_RS1_15
IO_L23N_T3_FWE_B_15
IO_L23P_T3_FOE_B_15
IO_L22N_T3_A16_15
IO_L22P_T3_A17_15
IO_L21N_T3_DQS_A18_15
IO_L21P_T3_DQS_15
IO_L20N_T3_A19_15
IO_L20P_T3_A20_15
IO_L19N_T3_A21_VREF_15
IO_L19P_T3_A22_15
IO_L18N_T2_A23_15
IO_L18P_T2_A24_15
IO_L17N_T2_A25_15
IO_L17P_T2_A26_15
IO_L16N_T2_A27_15
IO_L16P_T2_A28_15
IO_L15N_T2_DQS_ADV_B_15
IO_L15P_T2_DQS_15
IO_L14N_T2_SRCC_15
IO_L14P_T2_SRCC_15
IO_L13N_T2_MRCC_15
IO_L13P_T2_MRCC_15
IO_L12N_T1_MRCC_15
IO_L12P_T1_MRCC_15
IO_L11N_T1_SRCC_15
IO_L11P_T1_SRCC_15
IO_L10N_T1_AD11N_15
IO_L10P_T1_AD11P_15
IO_L9N_T1_DQS_AD3N_15
IO_L9P_T1_DQS_AD3P_15
IO_L8N_T1_AD10N_15
IO_L8P_T1_AD10P_15
IO_L7N_T1_AD2N_15
IO_L7P_T1_AD2P_15
IO_L6N_T0_VREF_15
IO_L6P_T0_15
IO_L5N_T0_AD9N_15
IO_L5P_T0_AD9P_15
IO_L4N_T0_15
IO_L4P_T0_15
IO_L3N_T0_DQS_AD1N_15
IO_L3P_T0_DQS_AD1P_15
IO_L2N_T0_AD8N_15
IO_L2P_T0_AD8P_15
IO_L1N_T0_AD0N_15
IO_L1P_T0_AD0P_15
IO_0_15
3V3 bank
XC7A15T-1CSG325
XC7A15T-1CSG325_34_pcb
MEZZ2_IO[15:0]
MEZZ1_IO[15:0]
MEZZ4_IO[15:0]
IO_25_34
IO_L24N_T3_34
IO_L24P_T3_34
IO_L23N_T3_34
IO_L23P_T3_34
IO_L22N_T3_34
IO_L22P_T3_34
IO_L21N_T3_DQS_34
IO_L21P_T3_DQS_34
IO_L20N_T3_34
IO_L20P_T3_34
IO_L19N_T3_VREF_34
IO_L19P_T3_34
IO_L18N_T2_34
IO_L18P_T2_34
IO_L17N_T2_34
IO_L17P_T2_34
IO_L16N_T2_34
IO_L16P_T2_34
IO_L15N_T2_DQS_34
IO_L15P_T2_DQS_34
IO_L14N_T2_SRCC_34
IO_L14P_T2_SRCC_34
IO_L13N_T2_MRCC_34
IO_L13P_T2_MRCC_34
IO_L12N_T1_MRCC_34
IO_L12P_T1_MRCC_34
IO_L11N_T1_SRCC_34
IO_L11P_T1_SRCC_34
IO_L10N_T1_34
IO_L10P_T1_34
IO_L9N_T1_DQS_34
IO_L9P_T1_DQS_34
IO_L8N_T1_34
IO_L8P_T1_34
IO_L7N_T1_34
IO_L7P_T1_34
IO_L6N_T0_VREF_34
IO_L6P_T0_34
IO_L5N_T0_34
IO_L5P_T0_34
IO_L4N_T0_34
IO_L4P_T0_34
IO_L3N_T0_DQS_34
IO_L3P_T0_DQS_34
IO_L2N_T0_34
IO_L2P_T0_34
IO_L1N_T0_34
IO_L1P_T0_34
IO_0_34
RTM_SDA
RTM_SCL
3V3 bank
XC7A15T-1CSG325
REF_CLK_SRC_SEL
REF_LO_CLK_SEL
DAC_CLK_SRC_SEL
REF_CLK_SRC_EXT_SEL
P1V8
P3V3F
IC35
TXB0304RUTR
C350
C351
100nF
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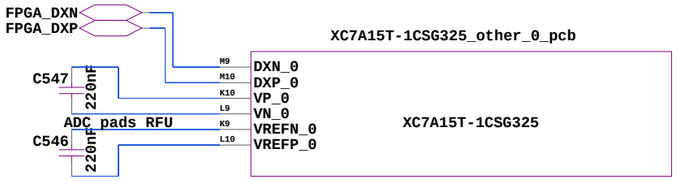
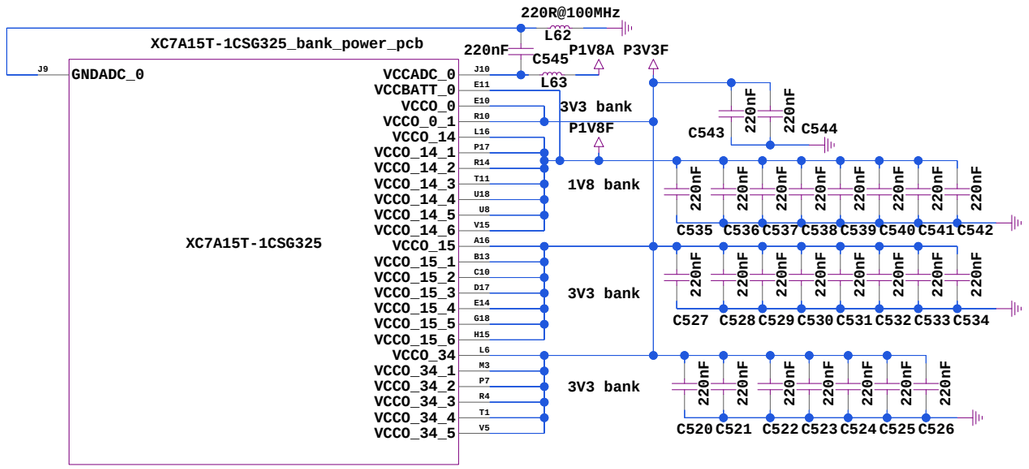
ARTIQ Sayma

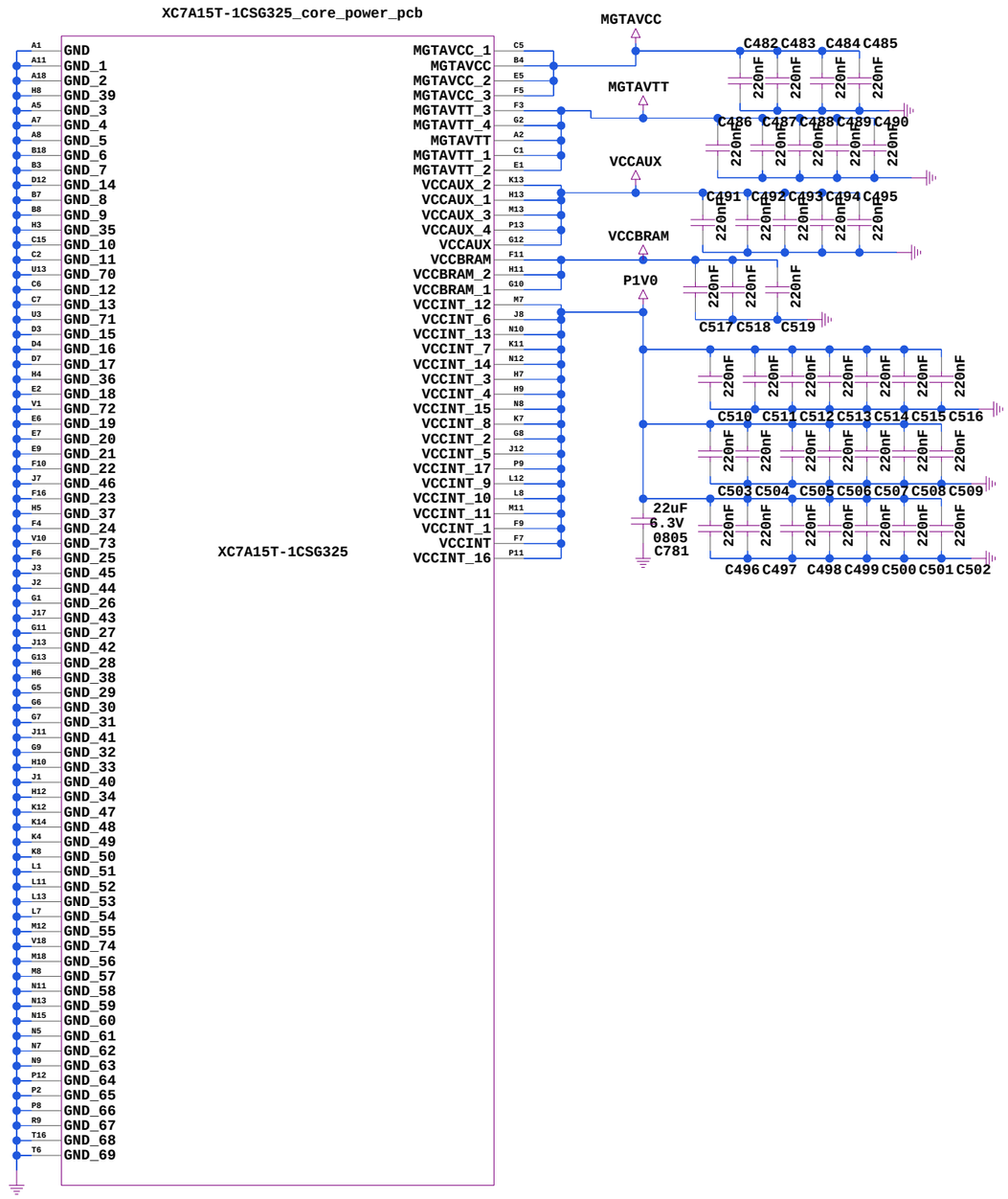
TITLE: FPGA_7A15T

SIZE	DWG NO	REV
A2	1	v0.9

DRAWN BY	SHEET	OF	
G.K.	9	18	23/11/2016:19:39







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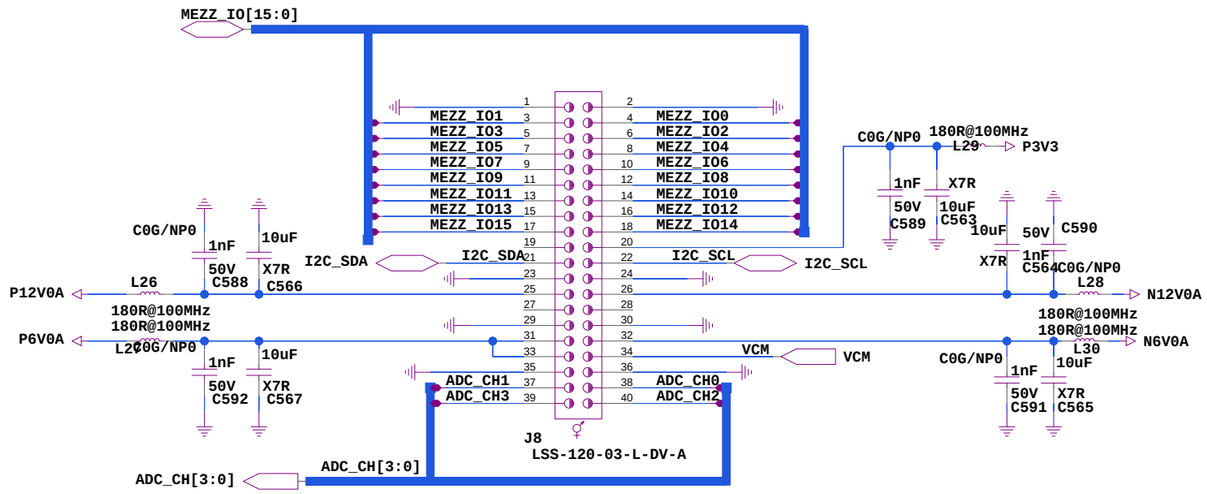
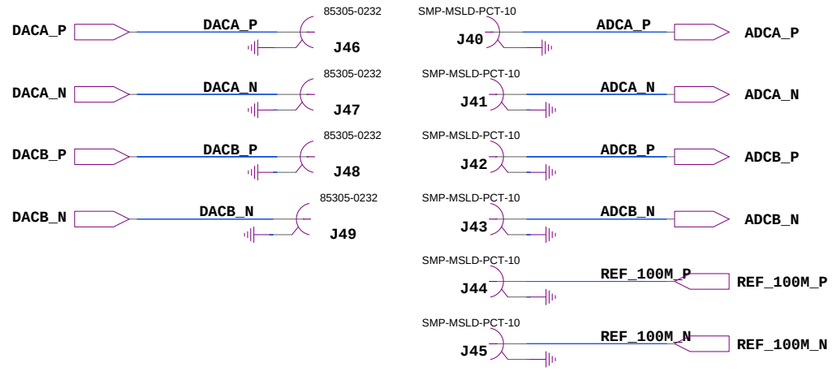
ARTIQ Sayma

TITLE: FPGA_7A15T_POWER

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	10	18	23/11/2016:19:40





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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ARTIQ

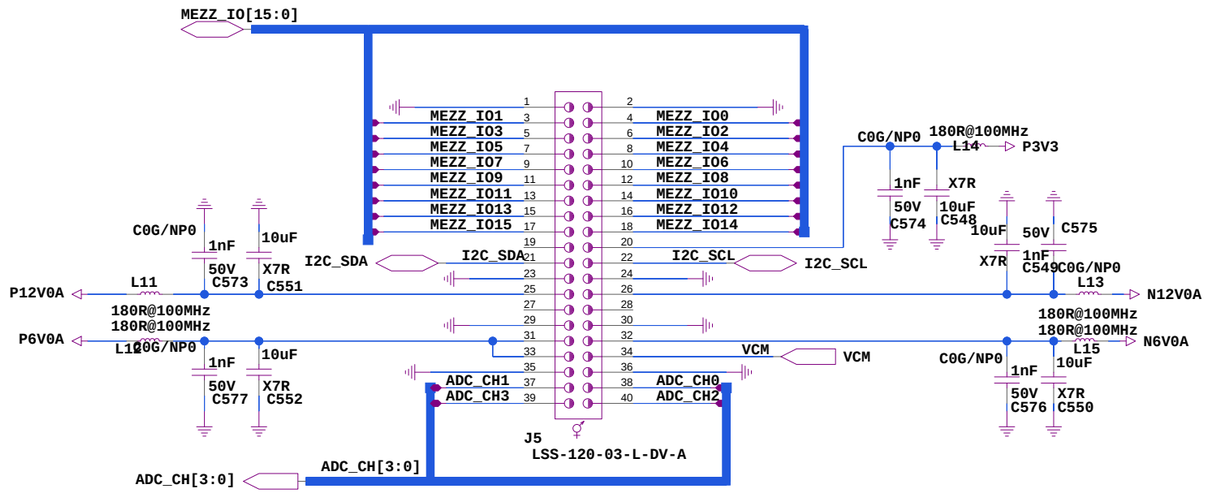
ADC_DAC_AFE_Mezzanine

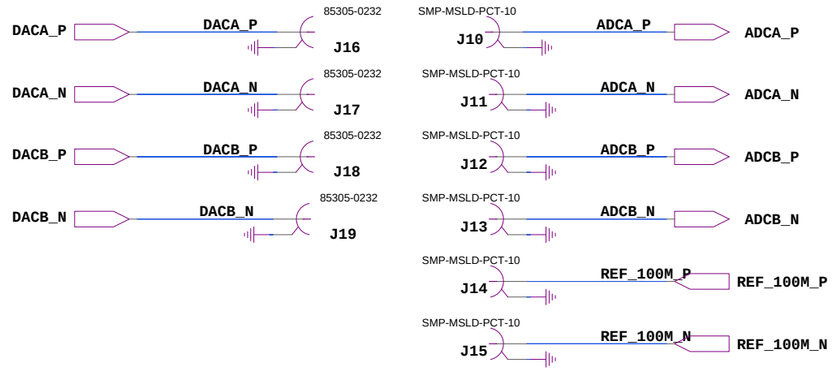
TITLE

ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	11	18	23/11/2016:19:38





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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ARTIQ

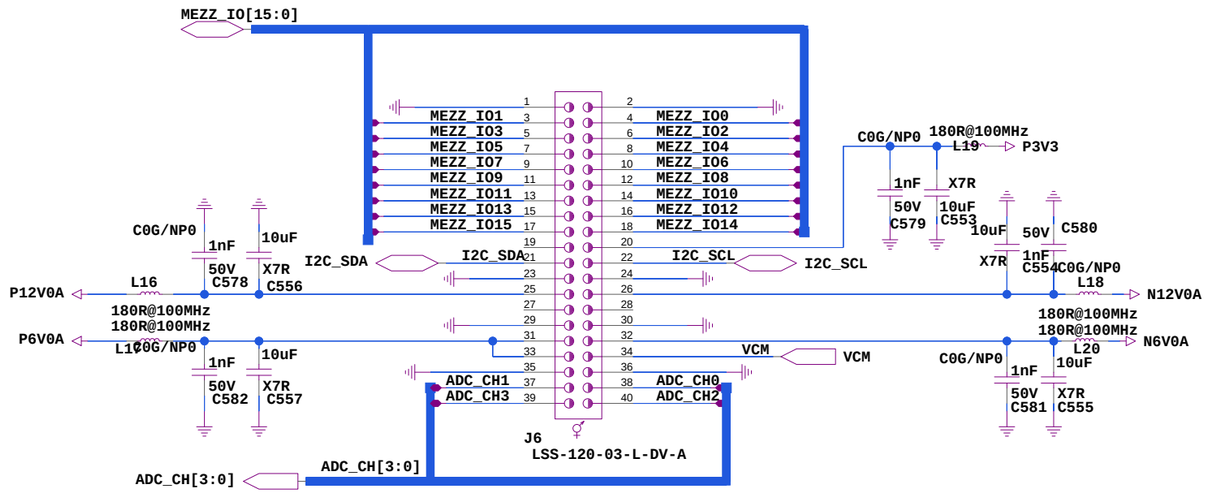
ADC_DAC_AFE_Mezzanine

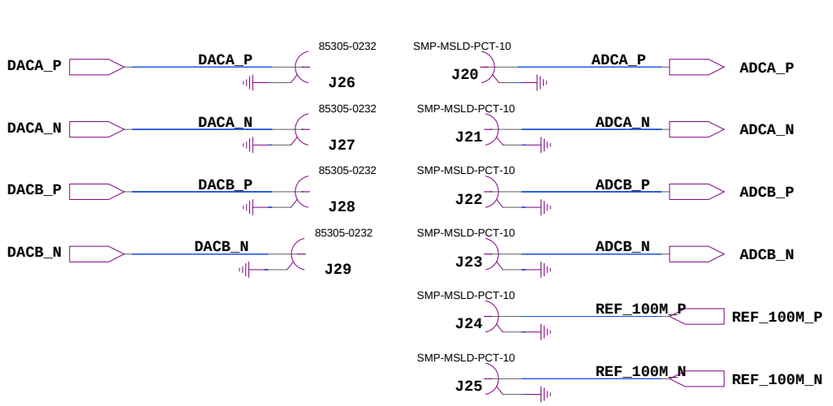
TITLE

ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	12	18	23/11/2016:19:38





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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ARTIQ

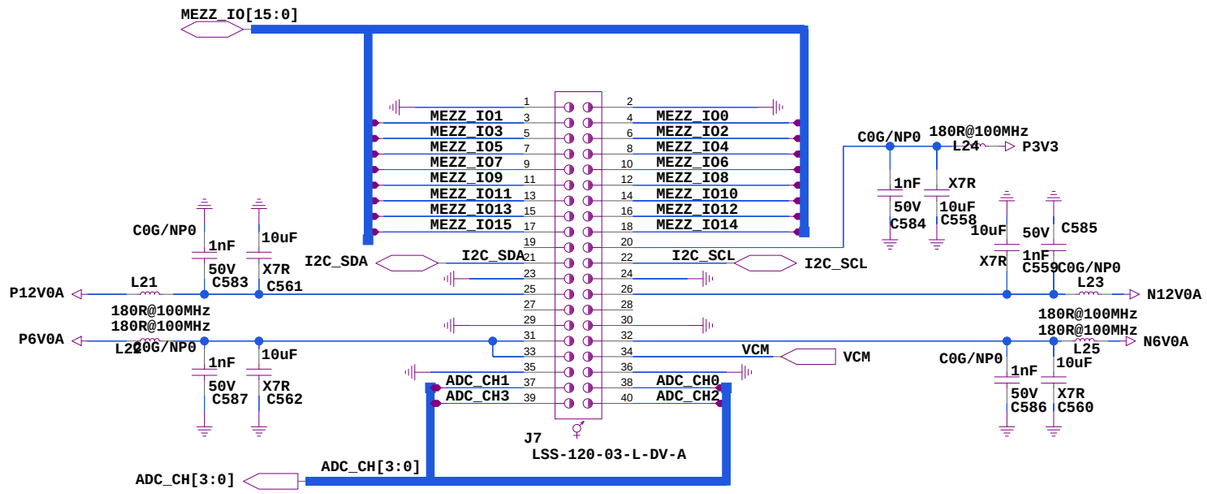
ADC_DAC_AFE_Mezzanine

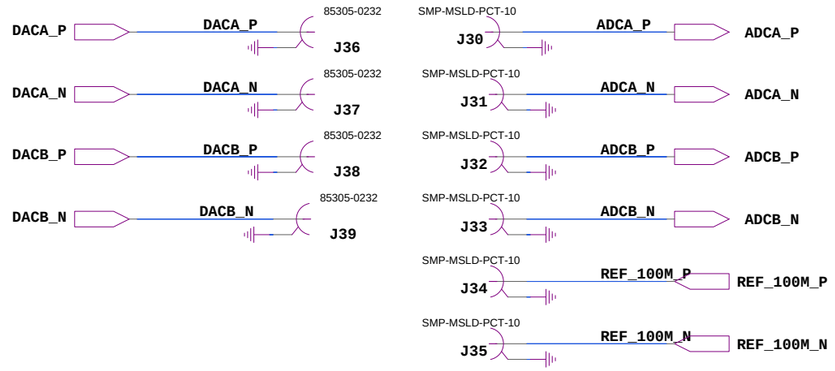
TITLE

ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	13	18	23/11/2016:19:38





+12VDC @ 200 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 50 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 1.5 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 100 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 1 A, max 10 mV p-p noise in 20 Hz-20 MHz

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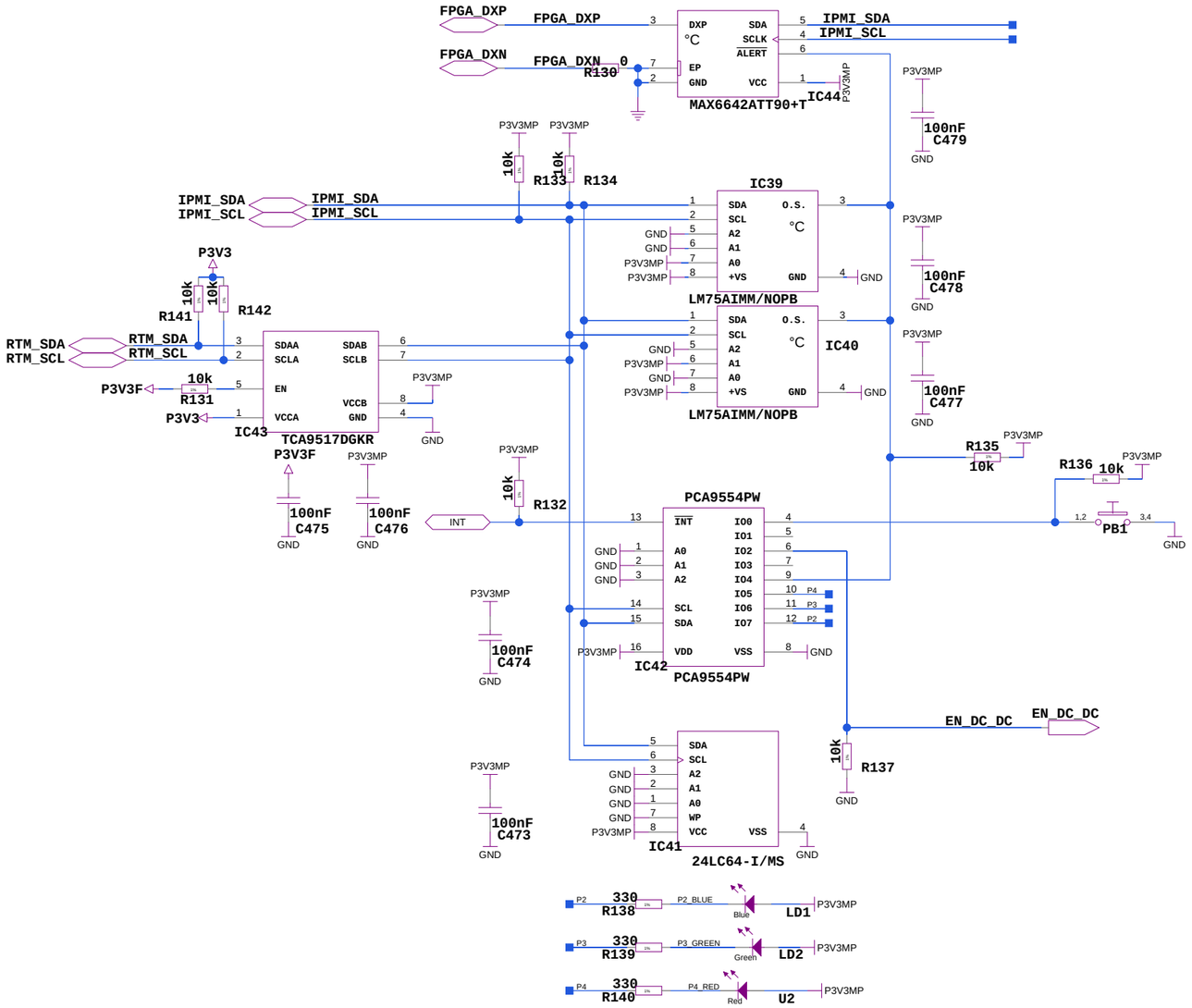
ARTIQ

TITLE: ADC_DAC_AFE_Mezzanine

ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	14	18	23/11/2016:19:38



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ARTIQ

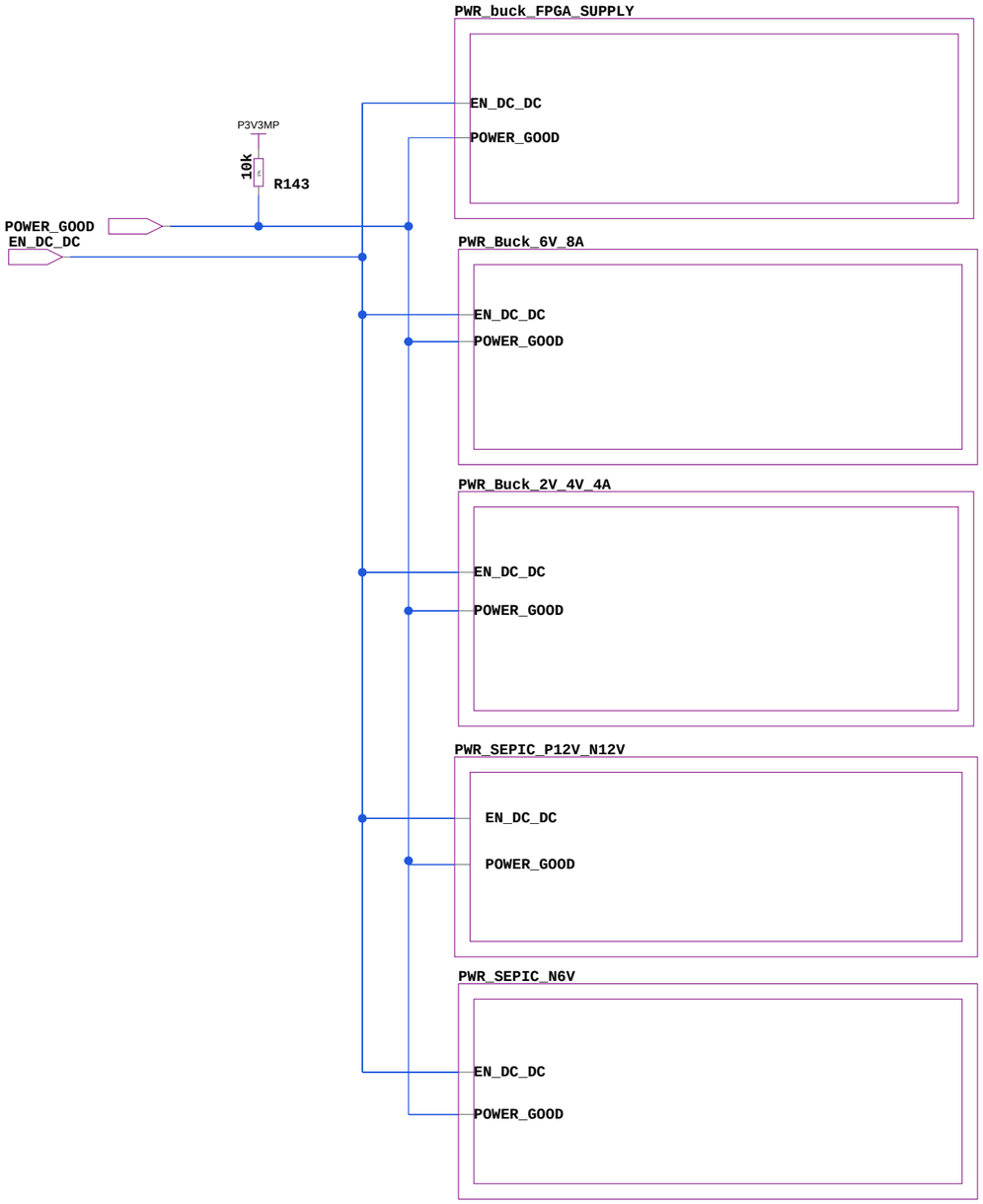
ARTIQ Sayma

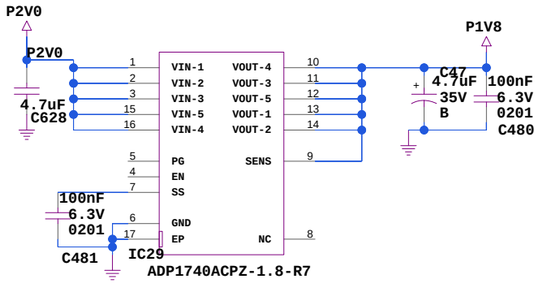
TITLE

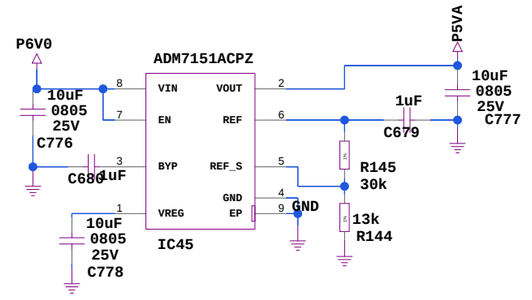
RTM_IPMI

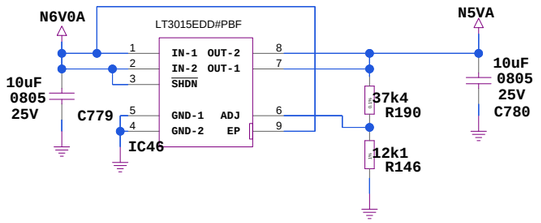
SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	15	18	23/11/2016:19:45









RTM modules power requirements

+12VDC @ 1A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-12VDC @ 250 mA, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+6VDC @ 8 A, max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
-6VDC rail @ 750 mA,max 1 mV p-p noise in 20 Hz-20 MHz bandwidth
+3.3VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

RTM power requirements

+4VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz
+2VDC @ 4 A, max 10 mV p-p noise in 20 Hz-20 MHz

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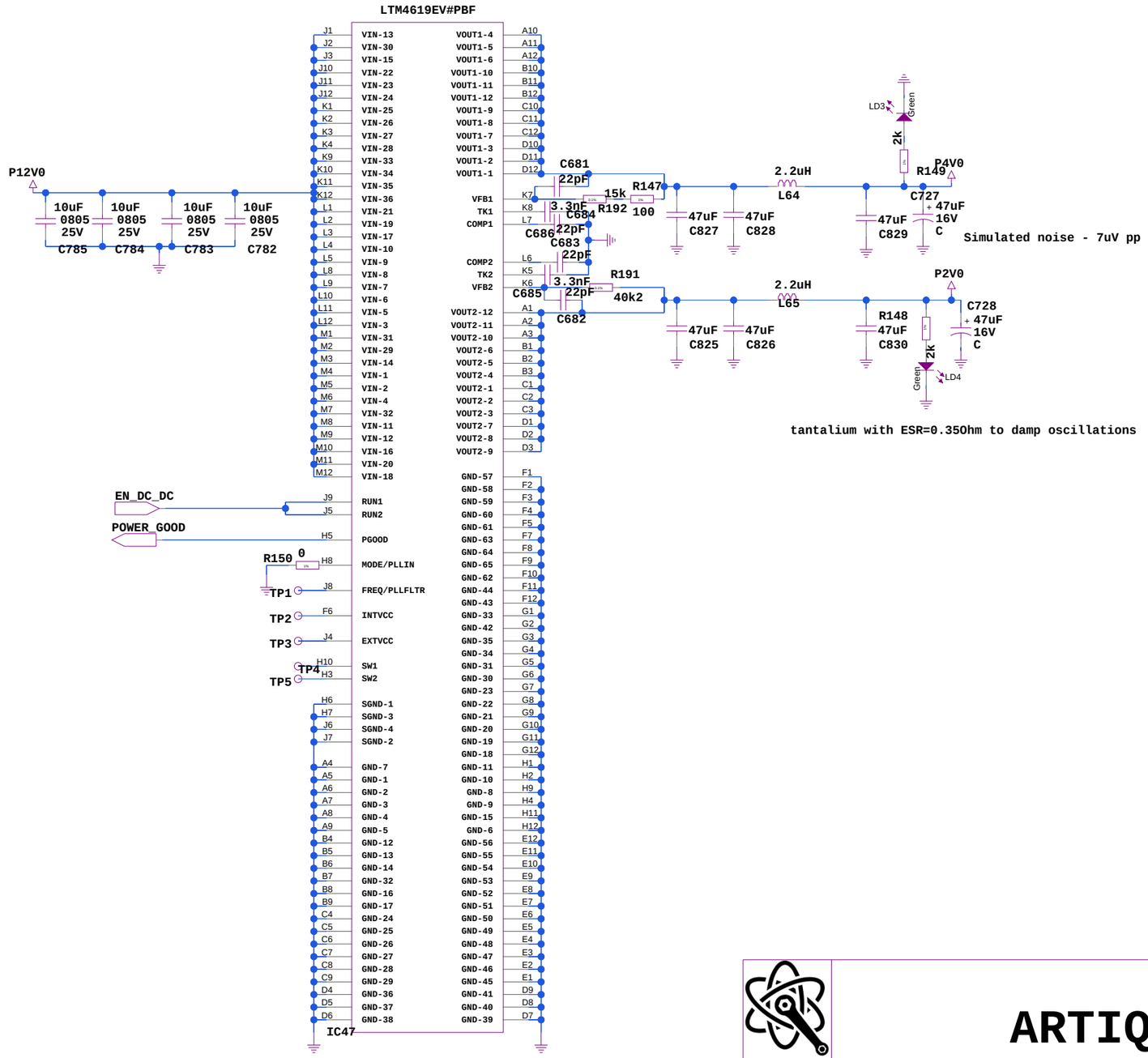
ARTIQ Sayma

TITLE: RTM_POWER_SUPPLY

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	16	18	23/11/2016:19:45



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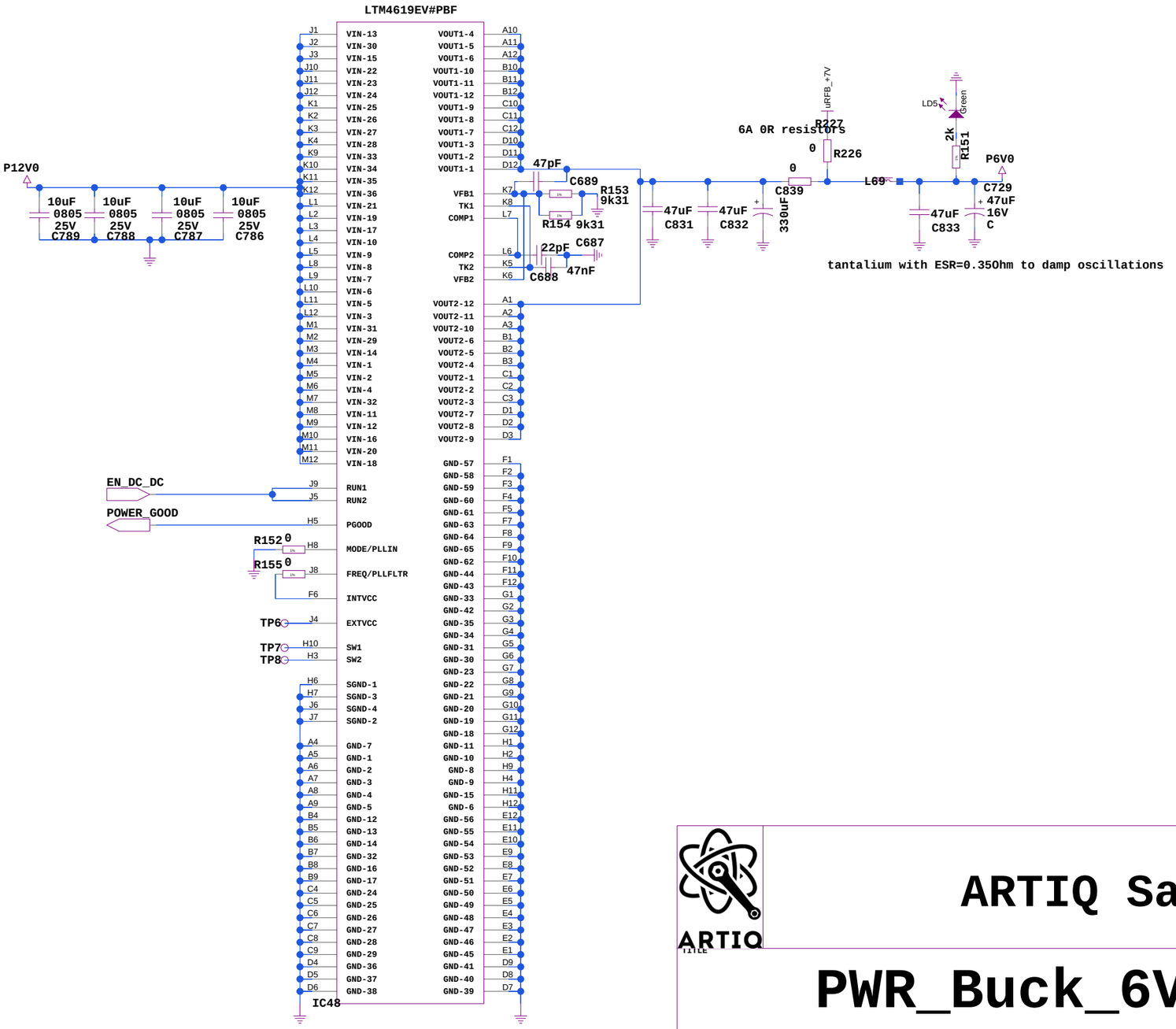
ARTIQ Sayma

TITLE: PWR_Buck_2V_4V_4A

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET			
G.K.	17	of	18	23/11/2016:19:44



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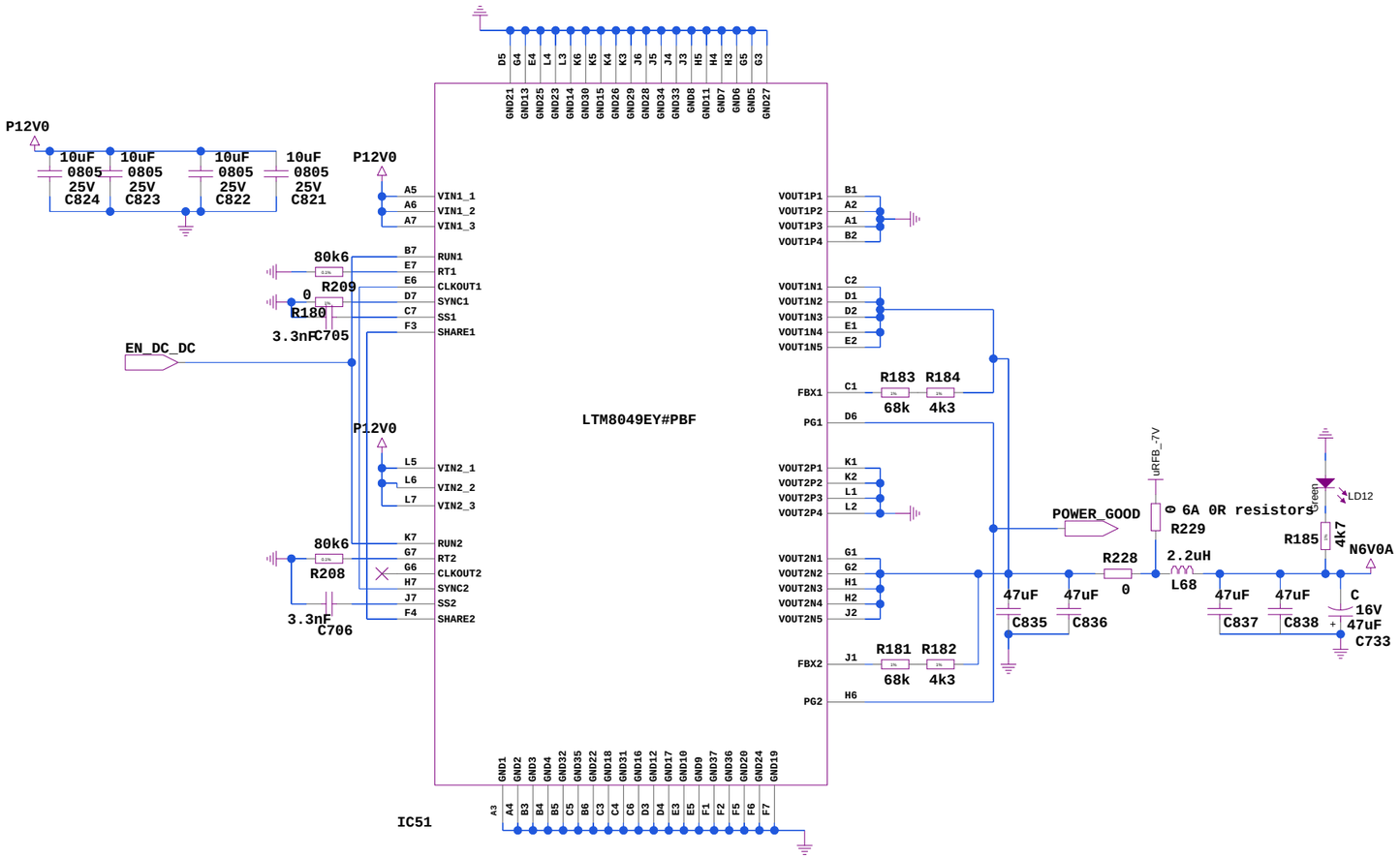
ARTIQ Sayma

TITLE: PWR_Buck_6V_8A

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	18	18	23/11/2016:19:44



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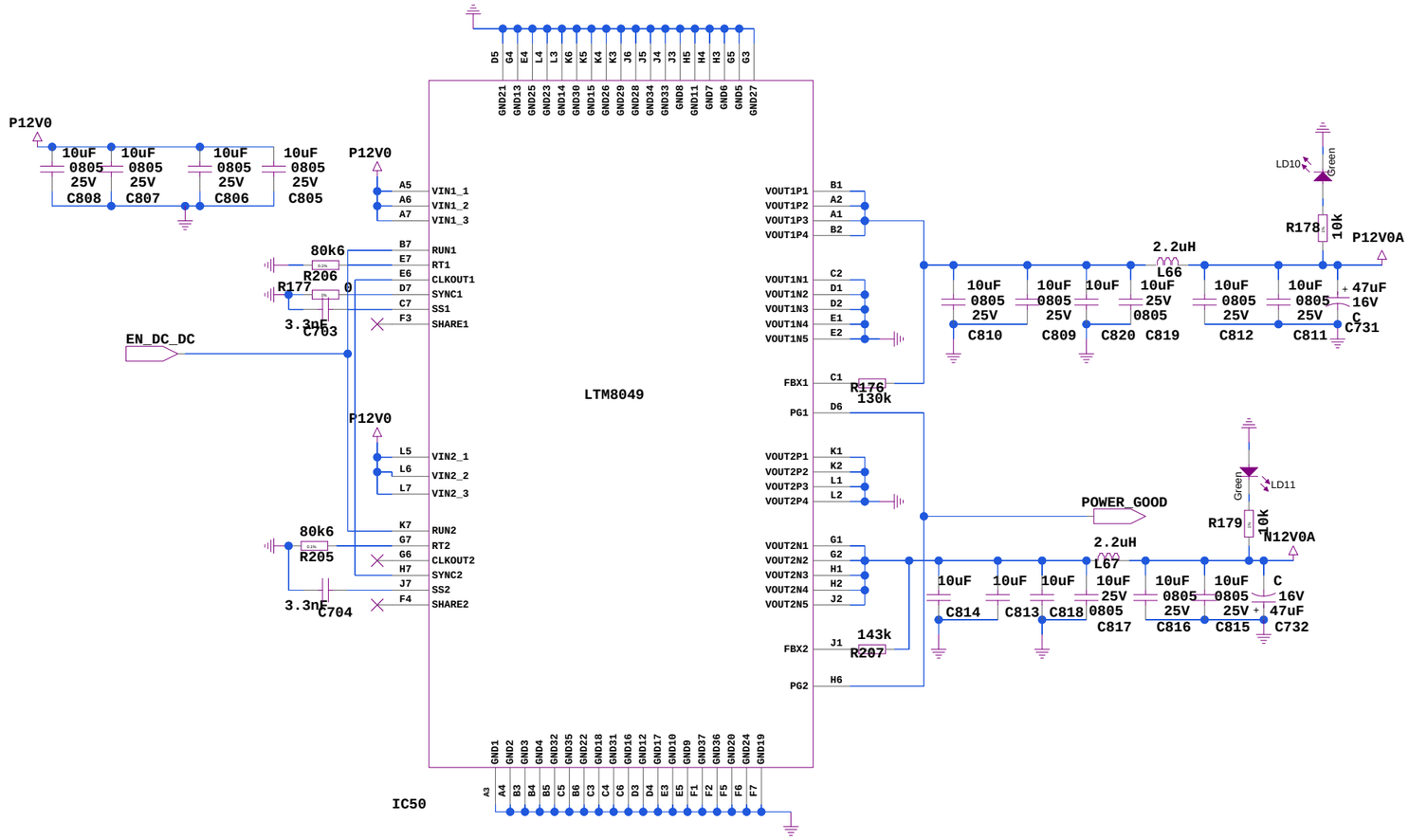
ARTIQ Sayma

TITLE: PWR_SEPIC_N6V

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET		DATE
G.K.	19	of 18	23/11/2016:19:44



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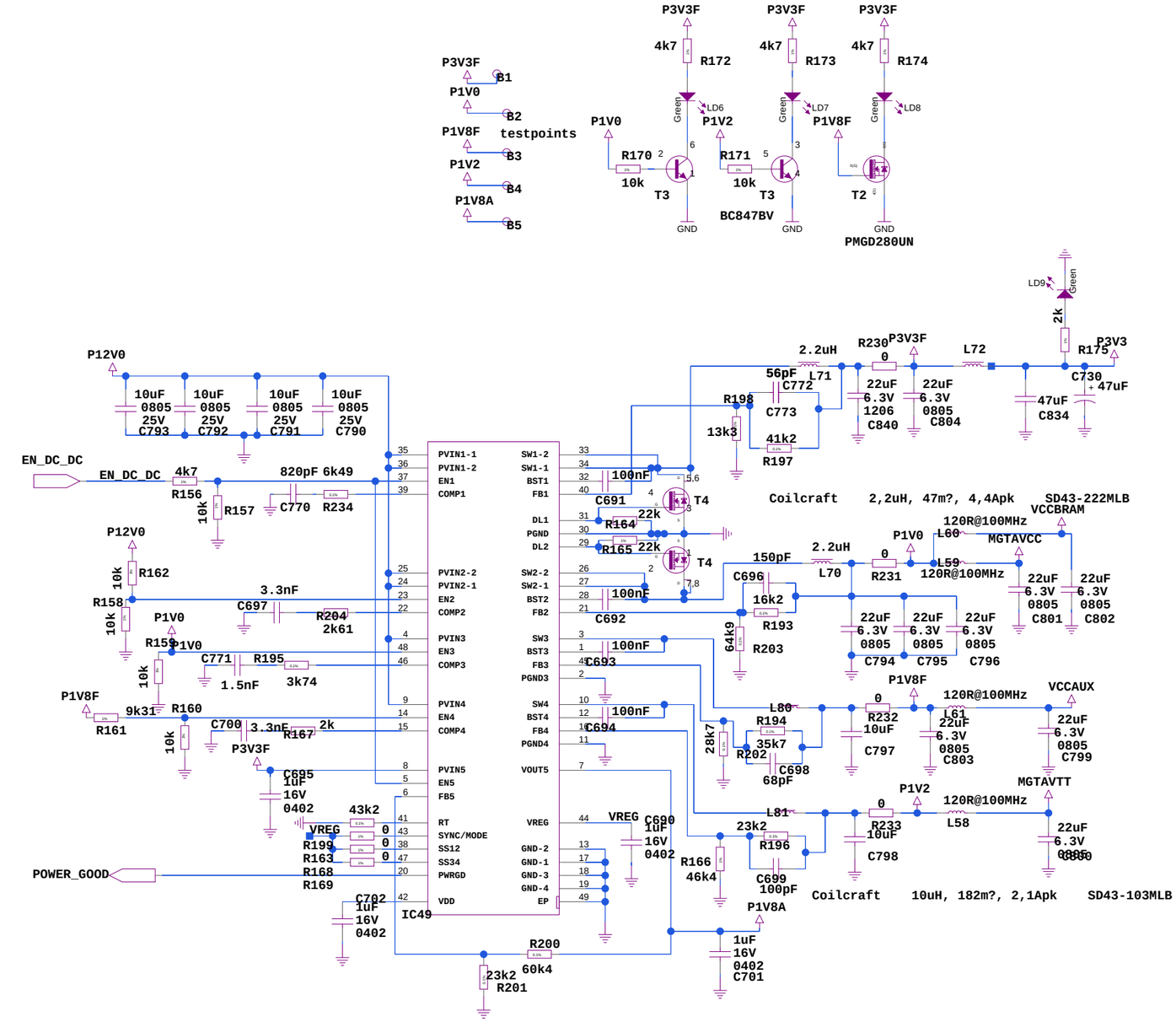
ARTIQ Sayma

PWR_SEPIC_P12V_N12V

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	20	18	23/11/2016:19:44



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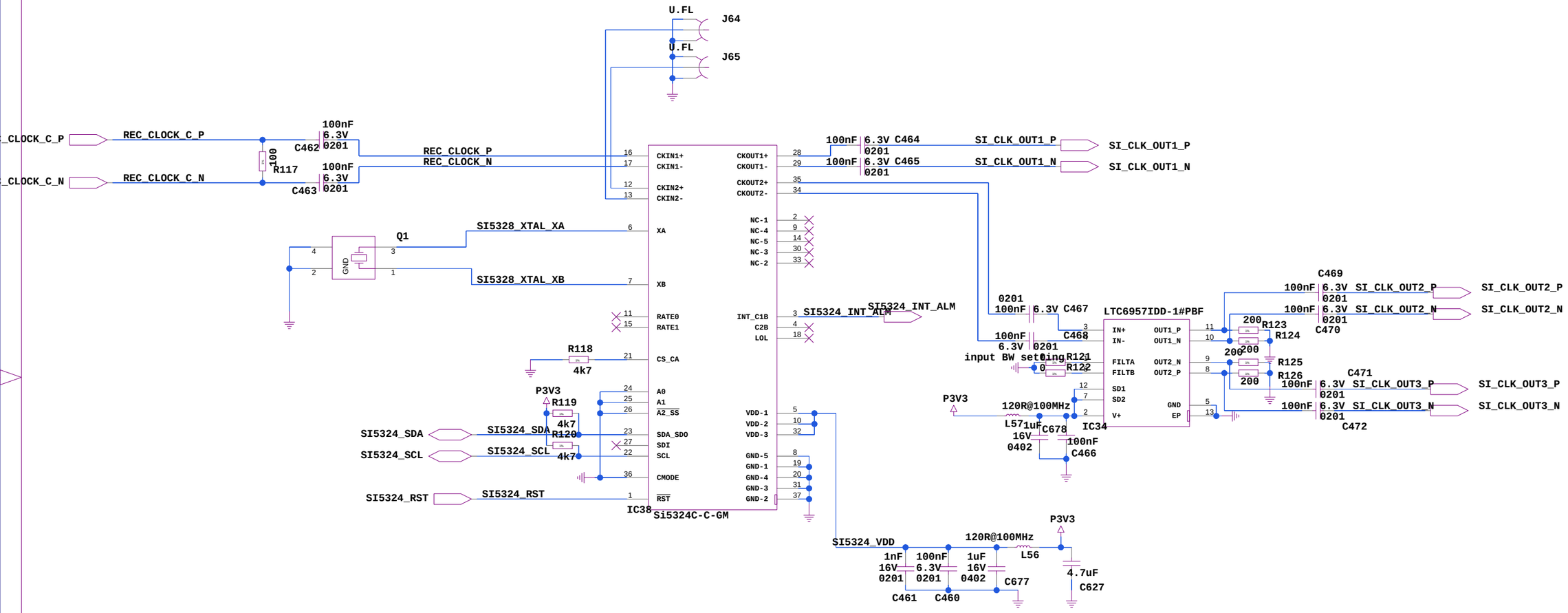
ARTIQ Sayma

TITLE: PWR_buck_FPGA_SUPPLY

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	21	18	23/11/2016:20:03



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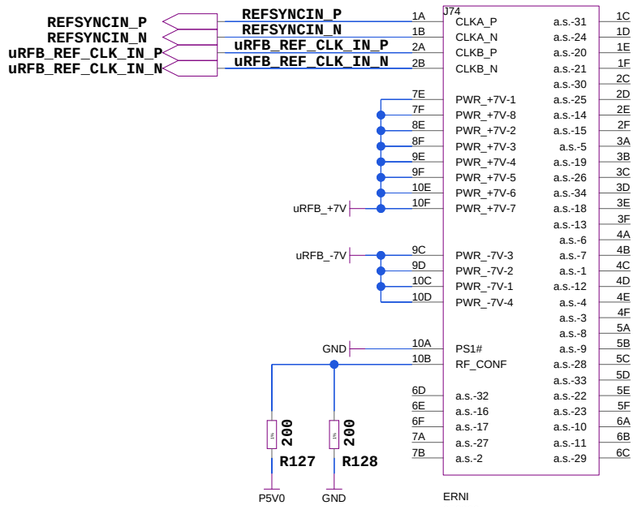
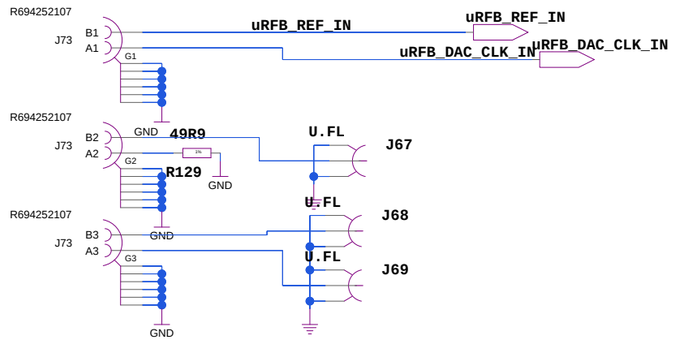
ARTIQ Sayma

TITLE: SI5324_CLK_RECOVERY

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	22	18	23/11/2016:19:45





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uRFB_Connectors

ARTIQ Sayma

SIZE	DWG NO	REV
A3	1	v0.9

DRAWN BY	SHEET	of	
G.K.	23	18	23/11/2016:19:47

uRFB_CLK_IN_P
uRFB_CLK_IN_N
uRFB_REF_IN
EXT_100M_RF_IN
REF_CLK_SRC_EXT_SEL
REF_LO_CLK_SEL
SI_CLK_OUT3_N
SI_CLK_OUT3_P
REF_CLK_SRC_SEL
CLK_DIST_CFG
DAC_CLK_SRC_SEL
P3V3_CLKDIS
P3V3_CLK
P5V0_CLK
P4V0
P6V0A
MEZ_CLK_IN_N
MEZ_CLK_IN_P
REF_LO_P
REF_LO_N
DAC_CLK_P
DAC_CLK_N
HMC_SPI_SCLK
HMC_SPI_SDATA
HMC_SPI_SDO
HMC830_SPI_SEN
HMC_SPI_GPIO
HMC_RESET
REFSYNCIN_P
REFSYNCIN_N
L=CLK0, H-CLK1
To additionally isolate inactive CLK
Shutdown inputs are used
input BW setting
clock module
SYSREF is matched to its CLK (a.k.a. DEVICECLK) to better than 100 ps.
REF1_100M_P
REF1_100M_N
REF2_100M_P
REF2_100M_N
REF3_100M_P
REF3_100M_N
REF4_100M_P
REF4_100M_N
DAC1_CLK_P
DAC1_CLK_N
DAC1_SYSREF_P
DAC1_SYSREF_N
DAC2_CLK_P
DAC2_CLK_N
DAC2_SYSREF_P
DAC2_SYSREF_N
ADC1_CLK_P
ADC1_CLK_N
FPGA_DAC_SYSREF_P
FPGA_DAC_SYSREF_N
ADC2_CLK_P
ADC2_CLK_N
ADC1_SER_SYSREF_P
ADC1_SER_SYSREF_N
ADC2_SER_SYSREF_P
ADC2_SER_SYSREF_N
GTP_CLK2_IN_P
GTP_CLK2_IN_N
FPGA_ADC_SYSREF_P
FPGA_ADC_SYSREF_N
GTP_CLK1_IN_P
GTP_CLK1_IN_N
AMC_MASTER_AUX_CLK_P
AMC_MASTER_AUX_CLK_N
RTM_MASTER_AUX_CLK_N
RTM_MASTER_AUX_CLK_P
IC59 HMC830LP6GE
IC58 HMC7043LP7FE
IC57 ADCLK948BCPZ
IC56 ADCLK948BCPZ
IC55 ADCLK948BCPZ
IC54 ADCLK948BCPZ
IC53 LTC6957IDD-1#PBF
IC52 LTC6957IDD-1#PBF
IC33 LT3042EMSE#PBF
IC32 LT3042EMSE#PBF
IC19 LT1963AEST-3.3#PBF
TR1 TCM2-43X+
TR2 TCM2-43X+
T1 BSS138LT1G

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ARTIQ

TITLE: ARTIQ Sayma

SIZE	DWG NO	REV
A2	Clock_Distribution_PLL 1	v0.9
DRAWN BY	SHEET	
G.K.	1 of 1	23/11/2016:22:17