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# STDP Based Online Learning for a Current-Controlled Memristive Synapse

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***Abstract*—Spike-timing-dependent plasticity (STDP) is a popular approach for online learning that determines synaptic weight updates based on the relative timing of temporal events of pre-synaptic and post-synaptic spikes. Online learning is very effective for fast and low power processing of locally sensed signals. Moreover, the memristor (or "memory resistor") has garnered attention as a key component in emerging synaptic circuits, due in large part to the inherent plasticity of the device. Circuits that leverage metal-oxide memristors, including $HfO_2$, are promising but must be carefully designed to account for the non-idealities of the memristor itself. STDP circuits for memristor-based synapses can be designed based on either voltage- or current-controlled mechanisms. In this paper, a novel current-controlled memristive synapse is presented with an STDP online learning circuit designed for improved reliability. This circuit specifically limits the range of operation to resistance states near the low resistance state (LRS). It utilizes this property to achieve online learning with STDP characteristics. Simulation result are provided that show STDP operation of this circuit, including demonstrations of controlled operation using the more reliable switching characteristics of near-LRS resistance states.**

***Index Terms*—STDP, current-controlled circuit, learning, memristor, synapse, LRS, spiking neural network.**

## I. Introduction

Unsupervised online learning approaches are gaining popularity in machine learning applications including automatic labeling and object detection [1]. One biologically inspired unsupervised online learning technique for spiking neural networks called Spike-Timing-Dependent Plasticity (STDP) uses the timing difference between the output spikes of two connected neurons to adjust the strength of the synapse between them. From the synapse perspective, the pre-neuron spike feeds into the synapse and the post-neuron spike is the subsequent neuron output. If the pre-neuron spike is followed by the post-neuron spike in time, the synapse strength, or weight, is increased or potentiated. If the post-neuron spike occurs before the pre-neuron spike, the weight is decreased or depressed [2]–[5]. The magnitude of weight change is proportional to the amount of time between the two spikes. The closer the spikes are to one another in time, the larger the change in weight. Circuits implementing STDP in a neuromorphic hardware use an adaptable weight storage. One possible solution for analog weight storage that can be used for spiking neural network circuit implementations is the memristor.

Memristors are two terminal devices that show non-volatile analog memory characteristics [6]. Memristors, particularly transition metal-oxide devices, can be integrated alongside transistors in dense arrays. It is suitable to perform analog computation with memristive devices by switching the resistance level. As a switching layer, different materials are utilized such as hafnium oxide ($HfO_2$). Hafnium oxide memristors can vary their resistance levels from few k$\Omega$ to a hundred of k$\Omega$ [7]. A synapse can be constructed with memristors to implement analog weight storage. Reset, set, and read are the important operations for a memristive synapse. Hybrid CMOS/memristor systems can switch into multiple resistance levels using current control [8]. The compliance current sets a limit for the low resistance state. Current control learning helps the memristor to overcome variability and limited resolution [9]. Neural network circuits can implement STDP using transconductance amplifiers and capacitors [10]. Previous work on using these memristors for STDP accounts for the asymmetric switching using voltage control [11].

In this paper, a current-controlled synapse is presented with two PMOS, three NMOS and a memristive device. After forming the device, it enters a low resistance state. A reset operation then increases the resistance value by breaking the filament. Following that, a set operation breaks the filament lowering the resistance value. Low resistance states are programmable and can be set in a range of different resistance values by controlling current compliance. This proposed synapse is current-controlled and uses low resistance levels to achieve reliable functionality. A prior work uses pulse shaping [11]. However, this work is current-controlled and more reliable at low resistance state (LRS) and accounts for the asymmetric characteristics.

## II. Proposed Circuit Design

### A. Current-Controlled Memristive Synapse

The STDP circuit design proposed in this work is intended for a hafnium oxide ($HfO_2$) memristor. The particular properties of this memristor that lead to using this design are the asymmetric switching properties. When decreasing the resistance of the memristor, a positive voltage relative to the formation of the memristor is applied across the device. When increasing the resistance, a negative voltage is applied. Fig. 1 illustrates how the transistors, two PMOS and three NMOS,

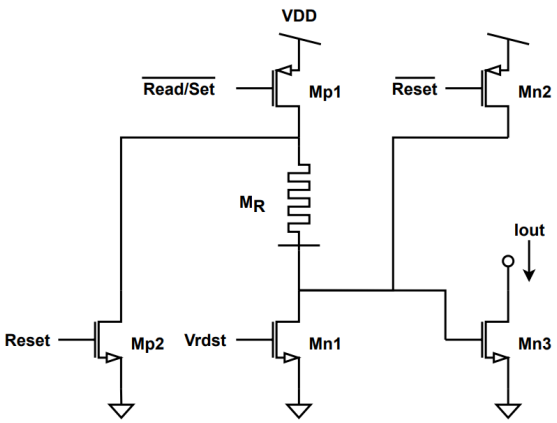


Fig. 1. Current-controlled memristive synapse

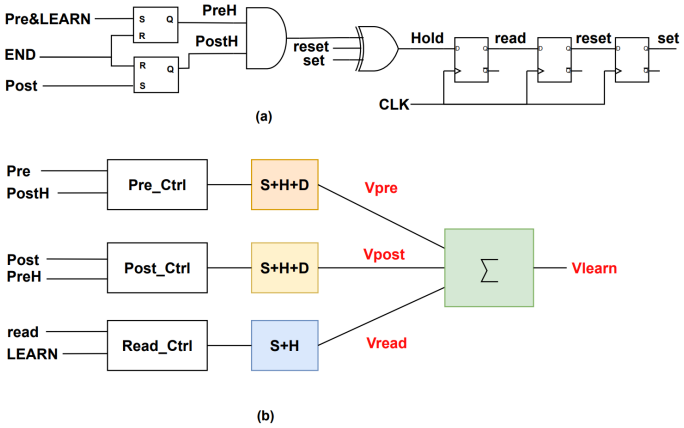


Fig. 2. Block diagram for STDP circuit (a) timing information generator for updating synaptic weight, (b) different functional block (pre, post, read, and summation) of STDP learning circuit

are integrated with the memristor to provide the desired set, reset and read control. The set operation reduces the resistance from the high resistance state (HRS) to a near low resistance state (LRS) using transistors $M_{p1}$ and $M_{n1}$ and voltages $\overline{Set}$ and $V_{rdst}$. The reset operation forces the memristor out of the near-LRS state and resets completely to HRS using $M_{p2}$ and $M_{n2}$ and voltages $Reset$ and $\overline{Reset}$.

To manage memristor switching and achieve incremental adjustments in the resistance (i.e. weight), short reset pulses could be used to gradually increase the resistance [7]. However, equivalent pulses in the positive direction will not achieve equivalent incremental resistance change. The switching process to HRS is inherently current limiting due to the increase in resistance while switching to LRS requires external current control. Without limiting the current in the set process, the device can get stuck in LRS. The low resistance state can be specified by the current limitation created by $M_{n1}$ [8]. The achieved resistance value is proportional to the maximum current through the device during the set operation. When the set operation is applied, the higher the current allowed due to the saturation current of $M_{n1}$, the lower the resistance achieved. An analog gate voltage is applied to control the saturation current during the set operation. This work uses the current controlled low resistance state to implement STDP.

The current control system is also used for the read operation. The transistors $M_{n1}$, $M_{n3}$ and $M_{p1}$ and voltages $\overline{Read}$ and $V_{rdst}$ are used for the read operation. The memristor is current controlled producing a voltage at the gate of $M_{n3}$ that is proportional to the resistance of the device which determines the output current $I_{out}$. The synaptic weight is defined by the memristor's resistance, and the decrease in resistance results in an increase in output current or weight.

### B. Block diagram for STDP circuit

The first challenge with this design is the unidirectional nature of the switching technique. The set operation can only further decrease the resistance value. Due to this, a three step operation is used for implementing the weight change. Fig. 2 (a) shows the timing information generated to update the synaptic weight. The current value of the device is read and temporarily stored, the device is reset, and finally the device is set into its new low resistance value. The new set value is generated by adjusting the previous set current by the proportional time difference between the pre-neuron and post-neuron spikes. Fig. 2 (a) illustrates the circuit includes digital logic to latch the learning process when both spikes occur. Once the process occurs the three operations, read, reset, and set, occur sequentially using a clocked D-Flip-Flop (DFF) system. The final value for the updated set current limitation is a voltage generated by the time difference between the pre-neuron spike, the post-neuron spike and the current memristor value.

In Fig. 2 (b), the circuits used to generate the new current limitation value are shown. The voltage output $V_{learn}$ is generated by combining information from the pre-synaptic neuron spike, post-synaptic neuron spike, and the synapse's current weight. The circuits for timing neuron spike relationship are only needed per neuron and the read and summation circuit are per synapse. While there are three components to sum the current, only two are used at a time. The control circuits in Fig. 2 (b), activate the correct circuits for potentiation or depression. For increasing the resistance of memristor, the voltage $V_{pre}$ and $V_{read}$ are used. On the other hand, decreasing the resistance, the voltages $V_{post}$ and $V_{read}$ are used. The unused transistors are entirely in turn-off mode. This insures a potentiation or depression on the synapse.

### C. Sample, hold, decay and sum circuit.

In order to generate the new resistance value for the memristor, a voltage for the gate of the memristor's current limiting transistor is needed. The voltage $V_{learn}$ is used to generate $V_{rdst}$. This voltage takes information from the previous memristors state, $V_{read}$ and combines it with spike timing information, $V_{pre}$ and $V_{post}$. Fig. 3 shows the blocks from Fig. 2 in greater detail. The spike timing information

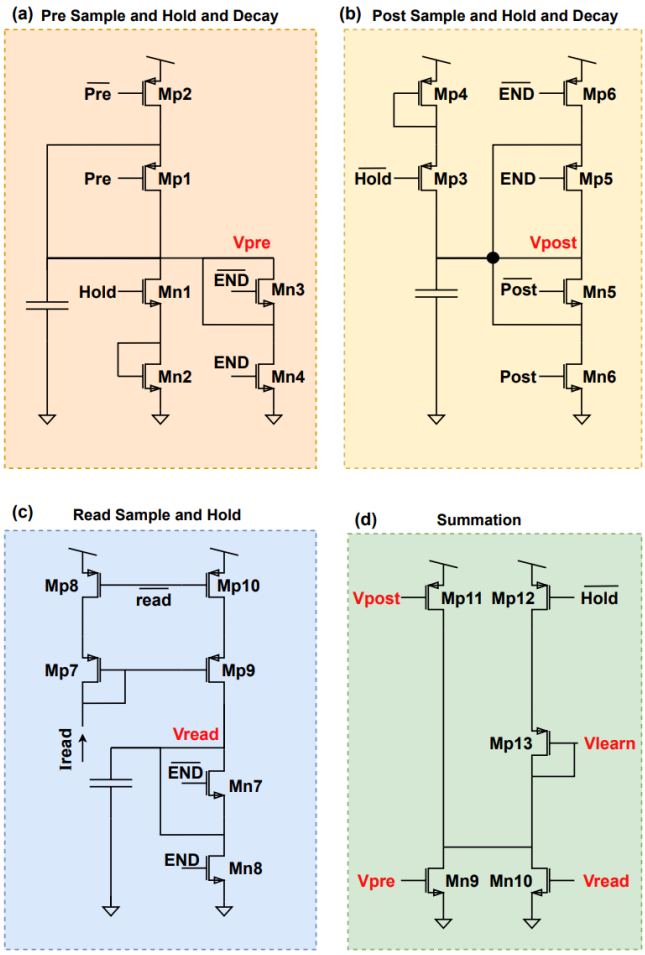


Fig. 3. Sample, hold, decay and sum circuitry, (a) pre: sample, hold and decay (S+H+D), (b) post: sample, hold and decay, (c) read: sample and hold, (d) summation circuit of Vpre, Vpost and Vread to generate Vlearn

is captured by the voltages $V_{pre}$ or $V_{post}$. In Fig. 3 (a), the voltage $V_{pre}$ is charged to 1.2 V when $\overline{Pre}$ is activated by the Pre control circuit in Fig. 2 (b). $V_{pre}$ gradually reduces in voltage through $M_{n4}$ until the post-synaptic spike occurs. Once both spikes have occurred, the voltage $Hold$ activates to stop the leakage of voltage at $V_{pre}$. After the learning process the voltage $V_{pre}$ is reduced to 0 V by the activation of the voltage $END$ and transistor $M_{n4}$. In Fig. 3 (b), the circuit for controlling $V_{post}$ follows the same control strategy except it is using $\overline{Hold}$, $\overline{END}$ and $Post$. When activated the voltage $V_{post}$ is reduced to 0 V and gradually increases through $M_{p4}$. When both spikes occur the voltage is held and after the update process the voltage is brought up to 1.2 V. In Fig. 3 (c), the current resistance of the memristor generates a specific value for $V_{read}$. This system is designed to regenerate the same current limitation used for the previous set operation. In Fig. 3 (d), $V_{learn}$ is generated by the summation of $V_{post}$, $V_{pre}$, and $V_{read}$. For potentiation, $V_{post}$ is at 1.2 V and for depression $V_{pre}$ is at 0 V which do not affect $V_{learn}$. The voltage $V_{learn}$ is converted and applied to $V_{rdst}$ in Fig. 1. The final set operation

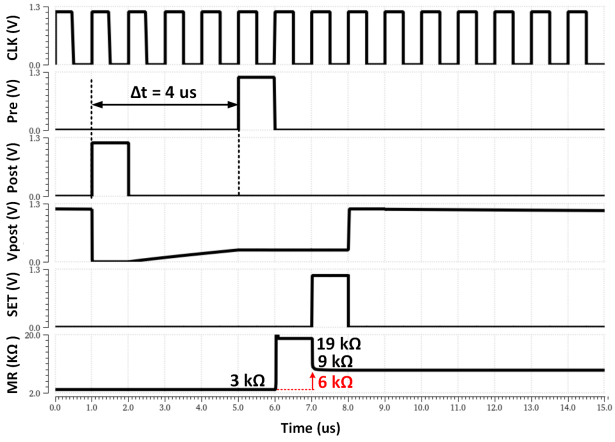


Fig. 4. Timing diagram of depression showing the neuron activity order, post-synaptic then pre-synaptic, the voltage decay of $V_{post}$, and the final change in resistance

in the learning process uses a new voltage value for current limitation to place the memristor in an updated low resistance state.

## III. Results and Discussion

### A. Timing diagram of depression

The resulting change in resistance generated by the STDP circuit requires the digital signals for the pre-synaptic and post-synaptic neuron spikes. After these occur the device value is updated proportional to the length of time and order of spikes. In Fig. 4 the voltages of $CLK$, $Pre$, $Post$, $V_{post}$, $SET$, and the memristor's resistance $MR$ are shown for a depression occurring from a $Pre$ then a $Post$ spike $-4$ µs apart. For depression the device resistance is increasing overall. The bottom wave form, $MR$, shows the device starting at a low resistance state and finishing at a different low resistance state with a reset operation in between that creates a high resistance value. In the learning process, the device is reset, which accounts for the large increase in resistance to a high resistance state and then set into a new low resistance state. The magnitude of the resistance change is determined by the decay of voltage $V_{post}$ which starts when the voltage $Post$ is activated and ends when the voltage $Pre$ is activated. The voltage $V_{pre}$ is held at 0 V and does not adjust the final resistance. For spikes occurring closer together the voltage $V_{post}$ will be larger and have a greater effect on the new low resistance state.

### B. Timing diagram of potentiation

In Fig. 5, the waveforms for increasing the synaptic weight are shown. The potentiation process uses the same control signals but expects the opposite order of pre-synaptic and post-synaptic neuron spikes. The time between $Pre$ and $Post$ is 4 µs. When the pre-synaptic neuron fires, the voltage $V_{pre}$ charges up and decays until the post-synaptic neuron fires. The voltage $V_{post}$ is held at 1.2 V and does not adjust the final resistance. The resistance of the memristor starts in a low

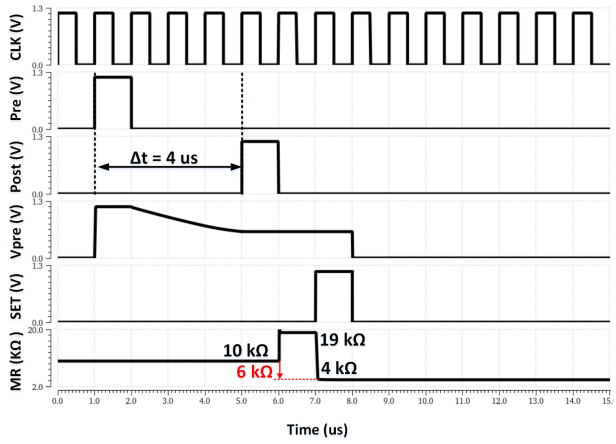


Fig. 5. Timing diagram of potentiation showing the neuron activity order, pre-synaptic then post-synaptic, the voltage decay of $V_{pre}$, and the final change in resistance.

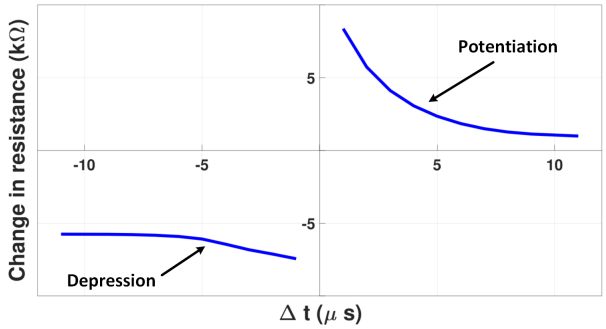


Fig. 6. STDP curve based on synaptic potentiation and depression for varying time between neuron spikes.

resistance state, is reset into a high resistance state, and then set into a new low resistance state that is a lower resistance than the original. The magnitude of resistance change is related to the time between neuron spikes and captured by the decay of $V_{pre}$. For spikes occurring closer together the change in resistance will increase due to a higher voltage $V_{pre}$.

### C. STDP curve

Fig. 6 shows the expected resistance change for different amounts of time between neuron spikes for specific initial resistances. The time difference is the pre-synaptic spike's start time minus the post-synaptic spike's start time as seen in Fig. 4 and 5. Positive time differences indicate potentiation and negative differences result in depression. The change in resistance is greatest the lower the time difference and gradually reduces. The change in resistance is taken as the final resistance minus the initial resistance. Using current limitation to update the low resistance state gives consistent positive and negative resistance changes relative to the spike timing.

## IV. Conclusions

In this work a current-controlled memristive synapse is presented. Low resistance states are utilized for STDP learning. The simulation results based on the proposed circuitry shows the potentiation in pre-post event and depression in post-pre synaptic spike event. The magnitude of resistance change is controlled by the time between spike events. This work shows the reliability of the circuit to switch the device at low resistance states given the asymmetric characteristics. This circuit is being fabricated at the $65\,\mathrm{nm}$ process. Future work will incorporate testing the fabricated circuits, further improving the circuits from these results and expanding the online learning functionality beyond STDP.

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