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Novel designs of spiking neuron circuit and STDP learning circuit based on memristor

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ABSTRACT

The pure circuit implementation of STDP is a worthwhile work. In this study, a novel spiking neuron circuit and STDP learning circuit based on memristors are designed. The proposed spiking neuron circuit, which is based on conventional leaky integrate-and-fire neuron and utilizes the nonlinear variation of memristance, is served to generate spikes. Different release thresholds and amplitudes of the spikes can be obtained through tuning circuit parameters. Extending on the spiking neuron circuit, a STDP learning circuit is built to perform unsupervised learning behaviors. Furthermore, a crossbar array architecture is finally considered to fabricate multi-input multi-output spiking neural network which also perform STDP learning effectively. Circuit simulation results in PSPICE prove the availability of the two proposed circuits.

1. Introduction

Recently, various researches focus on the implementation of brain-inspired systems that imitate biological neural network (BNN). The human brain has the excellent capability to achieve a parallel, efficient, and real-time computation, which is definitely vital for the brain to urge itself to adapt to the constantly changing external environment. This ability relies on the protocol of learning and storage implemented by synapses and neurons in brain. Actually, information from outside the neuron are stored in the form of synaptic weights. By the time the information change, the process of learning occurs, which reflects as the update of synaptic weights, i.e., synaptic plasticity. Spike timing dependent plasticity (STDP) is a promising physiological mechanism when it comes to the modulation of synaptic weights. Importantly, STDP allows unsupervised learning which makes it possible to build a real-time adaptive systems with satisfactory information processing ability inspired by BNN [1–5]. Moreover, the pure circuit implementation of learning rules is also a meaningful work to perform parallel actions in systems as much as possible which is more efficient than software-assistant computing systems.

STDP performs an associative homosynaptic plasticity learning based on the time difference between a pair of spikes that pre- and pos-neuron fire, respectively. This rule determines the synaptic weight modification as either depression or potentiation [6–8]. Thus, these two processes should be well considered when researchers focus on the circuit implementation of STDP. Spike neuron circuit is a critical part that takes the responsibility to generate spikes applied on synapse. In the past studies, a number of pulse generating circuits based on mathematical models were designed, known as spiking neuron models. Some of the most common ones available in studies are mentioned there. The first one based on Hodgkin–Huxley model was proposed in 1991, which described the activity of a neuron in detail but is too complicated to be realized in circuit. After that, a widely used model called integrate and fire neuron model was designed by Culurciello et al. [9] and several improved versions, such as leaky integrate-and-fire neuron and low-power adaptive integrate-and-fire neuron, were proposed in succession. These circuits are simpler than the previous. Nevertheless, because of the minimalism, these circuits can not produce suitable negative wave without additional switch and logical gate. In addition, Eugene Izhikevich presented a neuron model in 2003, i.e., Izhikevich and Wilson model, which is computationally simple compared with HH model but still in the circuit implementation of STDP [9–12].

On the other hand, synaptic circuit also should be well designed. In this connection, Bofillipetit and Murray [13], Indiveri et al. [14,15], Cruzalbrecht et al. [16], Mostafa et al. [17], Jungjin et al. [18], and Azghadi et al. [19] achieved the STDP in circuits. They designed different neuron circuits referring to the integrate-and-fire (I&F) neuron model with different corresponding metallic oxide semiconductor field effect transistor (MOSFET)-based

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synaptic circuits. However, some of these synaptic circuits cannot provide both depression and potentiation in one single design. Besides, some synaptic circuits occupy large area and are too complex to be integrated in crossbar array, which limits their applications in neural network.

Over the past decades, emerging memristor, the fourth circuit element theoretically postulated by Chua in 1971 besides resistor, capacitor, and inductor, has been regarded as a perfect device to the establishment of artificial synapses due to its performance of compact non-volatile memories and the modulation similar to synaptic plasticity. In addition, memristor, as a two terminal passive element with nanoscale, can save area in some possible replacement for silicon circuits. Memeristor initially realized by HP labs in 2008 [20] and since then several compounds became the first batch of materials to be used as memristive synapses. Under this background, Serrano-Gotarredona and Linares-Barranco [21], Lecerf et al. [22], Yu et al. [23], Covi et al. [24], Babacan and Kaçar [25], and Narasimman et al. [26] designed a single synaptic circuit based on memristor to manage the two processes. However, these circuit more or less have additional switches or logical gates and Lecerf et al. [22] adopted current conveyor in his circuits. These circuit integrated elements are not efficient in space saving of array structure. Other researchers like Afifi et al. [27], Zamarreño-ramos et al. [28], Prezioso et al. [29], Shukla et al. [30], and Panwar et al. [31] also used memristor in synaptic circuits and proposed a compact synaptic array frame to perform STDP, but the learning processes partially depended on software which is away from the pure circuit implementation of the STDP. Besides, Azghadi et al. Yu et al. and Covi et al. employed different pre- and pos-spike shapes to behave STDP, which weakened the identity of neuron circuits in array network.

Given the unique features of memristor, especially its nonlinear characteristics, a novel spiking neuron circuit and STDP learning circuit are proposed attempting to solve the above problems especially the circuit implementation of STDP in this paper. Based on traditional leaky integrate-and -fire neuron, we consider the potential evolution of neuron membrane which can be induced by changing the memristance through applying appropriate voltage to it, for which the spiking neuron circuit has the ability to generate spikes. Then with this, the proposed STDP circuit performs unsupervised learning and a two-inputs two-outputs spiking neural network in form of crossbar array are built. We also conduct several circuit simulations to indicate the feasibility of the proposed circuits and discuss the merits of the proposed system in the end.

The remainder of this paper is organized as follows. Section 2 introduces the memristor models and the possibility of the memristor being applied in the synapse and neuron. Section 3 presents the memristor-based spiking neuron circuit. Section 4 discusses the processes of implementing STDP both in learning circuit and neural network. Section 5 analysis the proposed system in some aspects. Section 6 concludes this paper.

2. Memristor models used in neuron circuit and synaptic device

Due to the features of memristor like nano-size, nonvolatile, multiple-state operation, scalability, stackablity, and CMOS compatibility, memristor has the great potential to be used in the next generation nonvolatile memory, logic state operations, neuromorphic computing, and CMOS/memristor hybrid circuits. A variety of materials have been used to stack memristors which bring about their different performances varying in applications [22,27,30]. Two kinds of memristors are employed in CMOS/memristor hybrid circuits of this study.

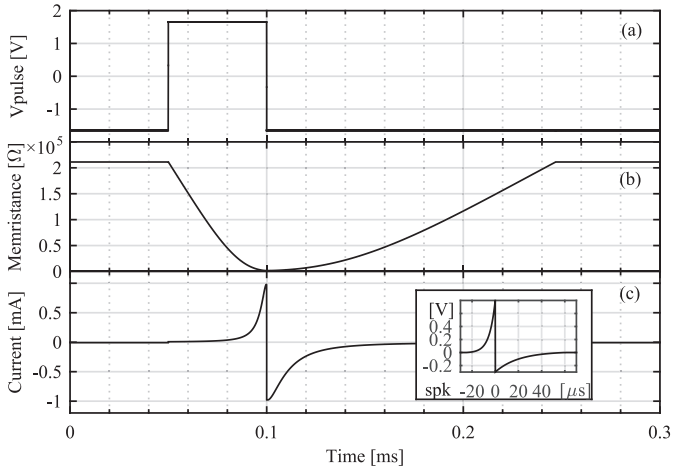

Fig. 1. Characteristics of memristor used in neuron circuit [34]. (a) Applied voltage with ±1.65 V, 5 kHz, and 0.25 duty ratio, (b) change in memristance, and (c) change in current is similar to the *spk* wave in subgraph defined by (1).

2.1. Memristor model for neuron circuit

The potential of cell membrane is related to its permeability for different ions including K^+, Na^+, and Cl^- [10–12,32,33]. The spiking signal released by pre- and pos-neuron determines the modulation of synaptic weights directly. In order to facilitate their research without loss of generality, a number of neuroscience researchers employed simple math models to express the spiking signals in software [28,33]. The change of cytomembrane potential can be considered as a process of exponential nonlinear variation, which can be mathematically defined by:

$$spk(t) = \begin{cases} A^+_{mp}\dfrac{e^{\frac{t}{\tau^+}} - e^{-\frac{t^+_{ail}}{\tau^+}}}{1 - e^{-\frac{t^+_{ail}}{\tau^+}}}, & -t^+_{ail} < t < 0 \\ -A^-_{mp}\dfrac{e^{-\frac{t}{\tau^-}} - e^{-\frac{t^-_{ail}}{\tau^-}}}{1 - e^{-\frac{t^-_{ail}}{\tau^-}}}, & 0 < t < t^-_{ail} \\ 0, & otherwise, \end{cases} \tag{1}$$

where A^+_{mp} and A^-_{mp} represent the positive and negative amplitudes of spiking signal, respectively. τ^+, τ^-, t^+_{ail}, and t^-_{ail} are the time constants. Spike waveform shape is shown in small subgraph of Fig. 1(c).

A voltage-controlled memristor is employed in spiking neuron circuit. Its memristance also changes in an exponential nonlinear way.

The relative mathematical expressions are provided as follows and SPICE codes can be viewed in [34].

$$\frac{dr(V_M,t)}{dt} = \begin{cases} \alpha^- \dfrac{V_M - V_{tl}}{\gamma + |V_M - V_{tl}|}, & V_M < V_{tl} < 0 \\ \beta V_M, & V_{tl} < V_M < V_{tr} \\ \alpha^+ \dfrac{V_M - V_{tr}}{\gamma + |V_M - V_{tr}|}, & 0 < V_{tr} < V_M, \end{cases} \tag{2}$$

$$L(r_{V_M,t}) = L_0\left(1 - \frac{m}{r}\right), \tag{3}$$

$$M(L_{V_M,t}) = f_0\frac{e^{2L}}{L}, \tag{4}$$

where V_M represents applied voltage; V_{tr}, V_{tl} are threshold voltages; L represents tunnel barrier width; M is the memristance; r is state variable; the rest are fitting parameters.

Fig. 1 illustrates the memristance and current as a function of time, respectively, under a pulse voltage as in Fig. 1(a) directly applied to the memristor. Memristance changes in the range $\{R_{ON}, R_{OFF}\} = \{2\,\text{k}\Omega, 200\,\text{k}\Omega\}$ shown in Fig. 1(b). The current through the memristor shown in Fig. 1(c) puts up a similar curve trend compared with the curve in subgraph. Accordingly, we can use this memristor in pulse generating circuit to obtain needed spikes. The finely tuned SPICE parameters are listed as follows: $\alpha^+ = 1 \times 10^7$, $\alpha^- = 3.4 \times 10^6$, $\beta = 0$, $\gamma = 0.1$, $V_{tr} = 1.5\,\text{V}$, $V_{tl} = -1.5\,\text{V}$, $m = 82$, $L_0 = 5$ nm, $f_0 = 310$. Different values between α^+ and α^- help circuit current possess fast evolution in positive direction and slow in opposite. β with a value of 0 avoids the memristance alter when applied voltage is under threshold.

2.2. Memristor model for synaptic device

Synapses play a key role in the transmission of information between two neurons. Several aspects need to be considered when we look for the synaptic device, including synaptic weight storage, adaptive weight modulation in circuit, and the circuit for communication. Definitely, the mechanism of the memristor makes it possible to meet these needs. Memristance records the amount of charges having passed through a memristor in a certain time and then changes by some rules [20]. In this paper, we use a threshold memristor model based on AgInSbTe which is fabricated and characterized in [35,36]. The memristance of this device changes only if the voltage applying to it exceeds the threshold voltage. Above all, the memristance evolution trend is same to the performance in real neural synapse for which we use this memristor as analog. Synaptic weight can be represented by the conductance of memristor, namely the change trend of weight is accordant with conductance but opposite to memristance. The mathematical expressions are

$$f(\omega(t)) = 1 - \left(\frac{2\omega(t)}{D} - 1\right)^{2p}, \tag{5}$$

$$\frac{d\omega(t)}{dt} = \begin{cases} \mu_v \dfrac{R_{ON}}{D} \dfrac{i_{off}}{i(t) - i_0} f(\omega(t)), & 0 < V_{T+} < V_M \\ 0, & V_{T-} < V_M < V_{T+} \\ \mu_v \dfrac{R_{ON}}{D} \dfrac{i(t)}{i_{on}} f(\omega(t)), & V_M < V_{T-} < 0, \end{cases} \tag{6}$$

$$M(t) = R_{ON}\frac{\omega(t)}{D} + R_{OFF}\left(1 - \frac{\omega(t)}{D}\right). \tag{7}$$

In two processes including rise and fall, memristance change fast at first and then goes slow as shown in Fig. 2 what means change rate depends on the initial state of memristance.

3. Designing of spiking neuron circuit

Qualitatively, one biological neuron receives all messages in the form of currents or voltages from its pre-neurons. Then, the sum of the inputs maybe make the neuron membrane potential reach a voltage threshold at a certain moment and a spike will be released immediately in this case. Afterwards, the spiking signal will be sent to its pos-neurons and this neuron will go back to its initial state right away. One cycle of neural firing is finished [32,33].

To acquire the spike patterns above-mentioned, a simple circuit is designed based on LIF neuron model in this section. The whole circuit schematic diagram can be seen in Fig. 3. Circuit constructed by a total of seven MOSFETs, one capacitance, one resistor, and one memristor without any additional switch or logic gate. Capacitor C_m and silicon components P_2, P_3, N_1, N_2 are exactly part of the traditional leaky integrate-and-fire neuron. C_m conducts the current integrate process. The output of inverter made by P_3 and N_1

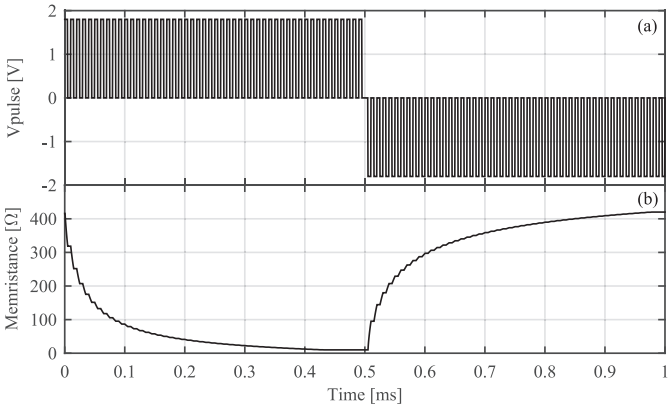

Fig. 2. Characteristics of memristor used as synapse [35]. (a) The voltage applied on the memristor, and (b) change in memristance. Under a periodic pulse voltage, memristance change rate depends on initial memristance (every point on the memristance curve can be regarded as a initial state of memristor, slope represents change rate), namely fast at first and then gradually becomes slow in positive and negative orientation, respectively.

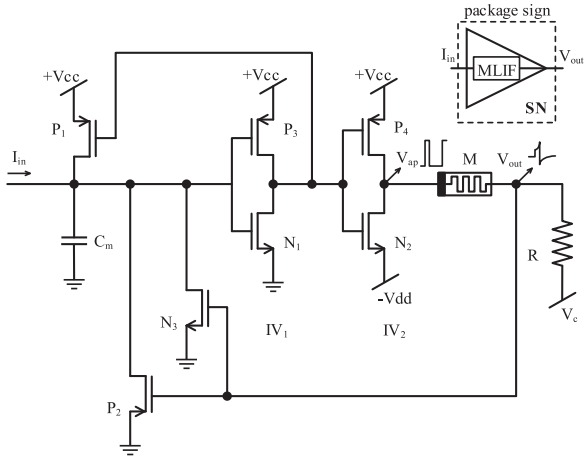

Fig. 3. Circuit structure of Memristor-based Leaky Integrate-and-Fire (MLIF) neuron. I_{in} represents inject current. V_{out} is the output spike signal. Black block is the positive electrode of memristor and the voltage of this end is denoted by V_{ap}. Subgraph is the package symbol that will be used in the following circuits.

(IV_1) is sent back to the grid electrode of P_1 to control hold voltage. Inverter made by P_4 and N_2 (IV_2) exports V_{ap} ($+Vcc$ or $-Vdd$) depending on the output of IV_1. We add a memristor (M) and a resistor (R) in succession to acquire the desired spike V_{out} under the apply voltage V_{ap}, which will connect back to control P_2 and N_3 to release the charges on C_m. V_c provides a translation voltage that moves original V_{out} upward to some extent. We call this circuit Memristor-based Leaky Integrate-and-Fire circuit (MLIF for short).

Circuit behaviors are explained as follows:

The input current (I_{in}) represents the feed coming from all pre-neurons the neuron connects to. C_m acts like the cytomembrane to integrate the inject currents and the potential of it will rise gradually. The initial memristance of M is R_{OFF} and will not change under the applied low voltage ($-Vdd$) that comes from IV_2 (voltage divided by R can be ignored and the V_{out} is almost 0 with the V_c's help). By the time the potential of C_m reaches the turn-on threshold of N_1, IV_1 exports 0 and IV_2 exports $+Vcc$. P_1 turns on first and keeps $V(C_m)$ stable. High voltage applied to M will drag down the memristance to R_{ON}. Since the memristance decreases, the voltage divided by R, namely V_{out}, rises gradually. When voltage V(M) ($V_{ap} - V_{out}$) is lower than the threshold voltage, V_{out} reaches the maximum value in positive direction and

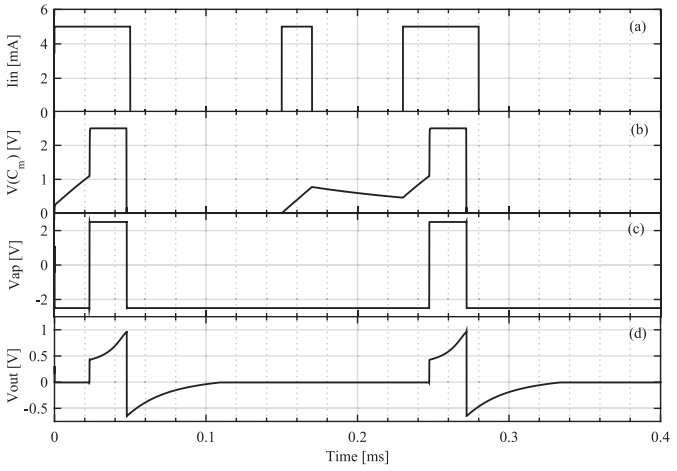

Fig. 4. PSPICE simulation results of SN circuit. (a) Input current I_{in}, (b) voltage change in integrate capacitor C_m, (c) applied voltage V_{ap} derive from IV_2, and (d) divided voltage V_{out} on resistor.

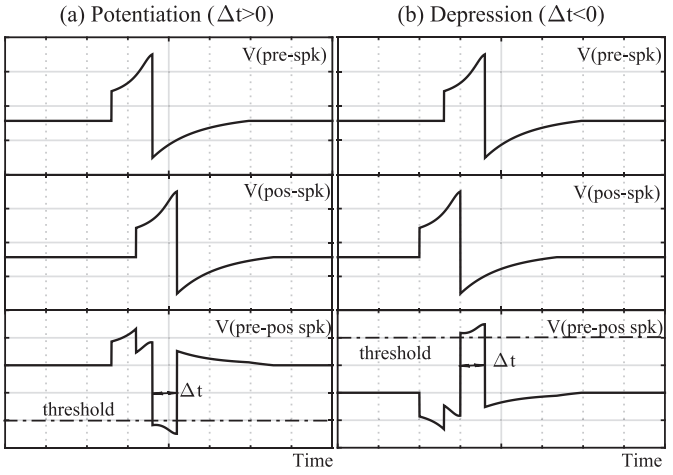

Fig. 5. Spike timing dependent plasticity (STDP). (a) Potentiation process. Pre-spike leads pos; negative voltage applying to negative electrode of memristor can make memristance decrease and thus weight increase. (b) Depression process. Opposed behaviour to (a).

memristance reaches the minimum value. While V_{out} makes N_3 turn on, C_m releases quickly. Then IV_2 outputs reverses and $V(M)$ (actually evolving from $-Vdd-V_{out}$ to near $-Vdd$) drags up memristance to R_{OFF}. Correspondingly, V_{out} evolves from negative maximum value to 0. P_2 turns on and C_m releases. Another function of P_2 is that its parasitic diode leaks charges on C_m slowly whether spike appears or not. When the memristance is back to R_{OFF}, the circuit returns initial state to wait another inject current and one spike signal is complete. Because divided voltage on R cannot come back to 0V when system is static (memristance is R_{OFF}), DC supply V_c added achieves an upward translation. Thus,V_{out} can keep at 0V when no spike is released. V_c and V_{out} can be calculated as

$$V_c = \frac{R}{R_{OFF}+R}Vcc, \tag{8}$$

$$V_{out} = \frac{R}{M+R}V_{ap} + V_c, \tag{9}$$

where the mathematical model of M can be viewed in (4).

Subgraph in Fig. 3 shows a packaged symbol denoted by SN that will be used in the following section.

The circuit parameters are selected as follows: $V_T(N_1) = 1\,\text{V}$, $V_T(N_2) = 3.5\,\text{V}$, $V_T(N_3) = 0.9\,\text{V}$, $V_T(P_1, P_3, P_4) = -1.5\,\text{V}$, $V_T(P_2) = -0.2\,\text{V}$ (V_T is threshold voltage), $C_m = 100\,\text{nF}$, $R = 20\,\text{k}\Omega$, $Vcc = 2.5\,\text{V}$, $Vdd = -2.5\,\text{V}$. The memristor parameters are listed in Section 2-A. V_T can be selected for different spike release thresholds. In the following simulation, we use a N-MOSFET (N_1) with threshold voltage 1 V to decide that when V(C_m) exceeds 1 V, spike appears. If release voltage needs to be 0.8 V, we can choose MOSFETs as $V_T(N_1) = 0.8\,\text{V}$ and $V_T(P_3) = 1.7\,\text{V}$. Moreover, the amplitude of V_{out} also can be changed. We will acquire spike with $+0.95\,\text{V}$ positive maximum value and $-0.65\,\text{V}$ negative minimum value under the above-mentioned parameters. If spike needs to be $+0.5\,\text{V}/-0.15\,\text{V}$, we can choose MOSFETs as $V_T(N_2) = 2.5\,\text{V}$ and $Vcc = 2\,\text{V}$, $Vdd = -2\,\text{V}$. Thus, different release thresholds and amplitudes of the spikes can be obtained for various applications.

The experiments are carried out in PSPICE environment and the results are shown in Fig. 4. In order to simplify our study, input (I_{in}) is a fixed 5 mA nonperiodic current. Obviously, only if the potential of C_m exceeds the threshold voltage $V_T(N_1)$, V(C_m) is kept to 2.5 V and then high voltage $V_{ap} - V_{out}$ (V_{out} is almost 0 at first) is applied to memristor. Spikes appear in the meantime. While V_{out} reach the positive maximum value, C_m releases quickly. If the input current is not enough to make V(C_m) exceed $V_T(N_1)$, charges on C_m will release slowly through the parasitic diode of P_2. Any input can

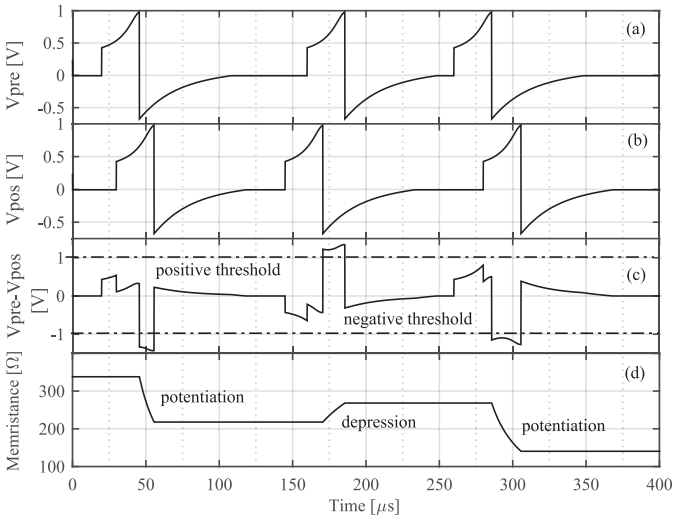

Fig. 6. Circuit simulation results of STDP. (a) Pre voltage spikes, (b) pos voltage spikes, (c) pre-pos voltage, and (d) evolution of memristance. Memristance's performance is consist with the mechanism introduced in Fig. 5.

still be accepted to fire another spike in this stage just like the circuit performance during the second spike period. Fig. 4(b) reveals the integrate process and Fig. 4(d) reveals the fire process.

4. Designs of STDP learning circuit and crossbar array structure for spiking neural network

In this section, the STDP learning circuit is built in Section 4.1. One single memristor (mentioned in Section 2.2) is regarded as a synaptic device. The design of crossbar array structure for spiking neural network is presented in Section 4.2.

4.1. Design of STDP learning circuit

Based on the Memristor-based Leaky Integrate-and-Fire circuit designed in Section 3, a circuit is established to perform the two processes of STDP, i.e., potentiation and depression defined in Fig. 5 [7,25]. A simple validation in PSPICE environment through applying different pre- and pos- voltage spikes to memristor is shown in Fig. 6. STDP learning circuit structure is shown in Fig. 7.

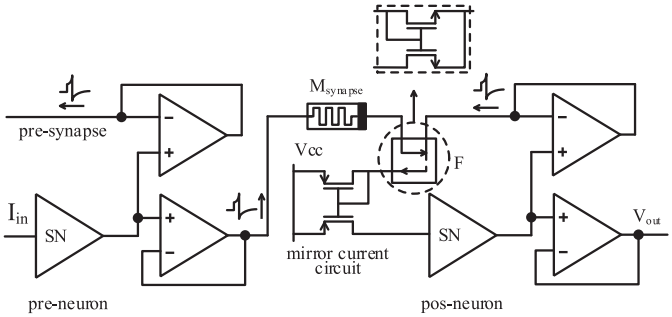

Fig. 7. STDP learning circuit. Two voltage followers behind every neuron (SN) play a role of isolation and transmission forward as well as backward. Mirror current circuit copy current that flows memristor-based synapse to pos-neuron and prevent the resistor-effect of pos-neuron.

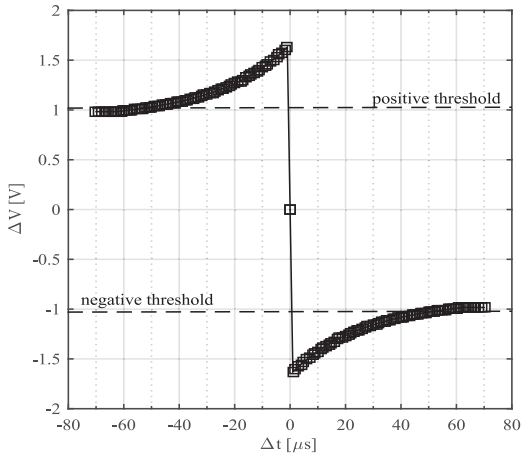

Fig. 8. The maximum absolute voltage applied to memristor ($\triangle V = \pm \max|V_{pre} - V_{pos}|$) is the function of $\triangle t$. Approximately when $|\triangle t| > 70\,\mu s$, $|\triangle V|$ is lower than threshold voltage and memristance will not change under this condition.

The pre-neuron accepts input current and fires spike when neural threshold voltage is reached (t_{pre}). We place two voltage followers that can separate neuron from pre- and pos-synapse, respectively, at the export of every MLIF neuron. Pre-spike signal passes the memristor-based synapse to be weighted thus current signal is acquired which will be injected to the post-neuron through a mirror current circuit. Mirror current circuit is used to copy same current as in memristor and avoid its influence on neurons (include pre- and pos-neuron). Pos-neuron obtains input from mirror current circuit. When neural threshold is reached (t_{pos}), the pos-neuron fires identical to the pre-neuron. The pos-signal will access to the other side of synaptic device, namely, memristor. Accordingly, there is a time difference ($\triangle t = t_{pre} - t_{pos}$) between the pre- and pos-spike signals. Further, the voltage $\triangle V$ ($V_{pre} - V_{pos}$) applied to memristor-based synapse is a function of $\triangle t$. Fig. 8 reveals the relationship between the biggest $\triangle V$ and $\triangle t$. When the absolute time difference $|\triangle t|$ increases gradually, the absolute biggest $\triangle V$ decreases in the mean time. $\triangle V$ exceeding threshold can lead to learning behaviour, namely, synaptic weight updates. Approximately $|\triangle t| > 70\,\mu s$, $\triangle V$ falls below synaptic threshold set as 1 V and learning disappear. The variation of synaptic weight ($\triangle G$) denoted by memristor conductance is the function of $\triangle V$ and related to its initial conductance (G_0). Therefore, $\triangle G$ does have to do with $\triangle t$, indirectly. This is exactly spike timing dependent plasticity. $\triangle G$ can be calculated as:

$$\triangle G = \frac{G_u - G_0}{G_0} \times 100\%, \tag{10}$$

where G_u is the conductance after update.

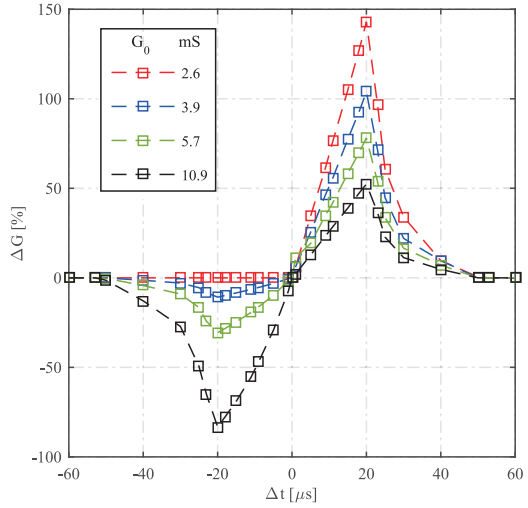

Fig. 9. Influence of G_0 on the resulting STDP memristor weight update function $\triangle G(\triangle t)$.

Serval sets of circuit simulation results under different G_0 are displayed in Fig. 9, which indicates that the synaptic plasticity is related to its initial state indeed. This property is consistent with the feature of the memristor introduced in Fig. 2, namely, memristance change rate depends on its initial value. This is what biological neuron synapse behave according to the experiments data [18,19,22]. Concretely, when negative voltage is applied, conductance decreases and the higher it is, the faster it falls; when positive voltage is applied, conductance increases and the lower it is, the faster it rises. For a fixed G_0, $\triangle G$ is relate to $\triangle t$ behaving as STDP $\triangle G(\triangle t)$. Thus, STDP is achieved in circuit.

4.2. Design of crossbar array structure for spiking neural network

Crossbar array structure saves circuit areas effectively for circuit implementation of multi-input multi-output neural network. This architecture fabricates simply and has fault-tolerance to a certain degree [15,19,21,23,26–28]. A feasible crossbar framework for two-inputs two-outputs spiking neural network is designed in Fig. 10. In order to simplify study, pre-neuron SN_1 is fed by current source (5 mA) for 50 μs per 200 μs. After 15 μs, pre-neuron SN_2 accesses the same current input. Different time that pre-neurons accesses supply is to obtain lead and lag performance among pre- and pos-neurons, for which we can observe learning manner on memristors. In order to get results easy to watch, M_{13}, M_{14}, M_{23}, M_{24} are initialized to 215 Ω, 420 Ω, 294 Ω, 380 Ω, respectively. The public part of mirror current circuit is only needed one per neuron which gathers currents come form all pre-neurons its connect to and then send the sum current signal to the post-neuron. The rest part is needed one per memristor-based synapse.

Intuitively, pos-neuron SN_3 and SN_4 will fire at different moments depending on the weighted input currents form two pre-neurons. Simulation results are analysed below.

The input currents are shown in Fig. 11(a), the output spikes of four *SN*s are shown in Fig. 11(b), the memristance updates of four memristors are shown in Fig. 11(c). As illustrated by the graph, during first spike period, SN_1 fires first followed by SN_3, SN_2, and SN_4 in turn. Therefore, referring to STDP rules exhibited in Fig. 5, M_{13}, M_{14}, and M_{24} get potentiation; M_{23} gets depression. We can think that both SN_1 and SN_2 play a part in SN_4's fire but only SN_1 makes efforts to SN_1's fire. Because M_{13} and M_{23} change in the opposite direction, during second spike period the weighted input currents from two pre-neurons to SN_3 barely changes. Thus the time that SN_3 fires after SN_1 remains in the first period value.

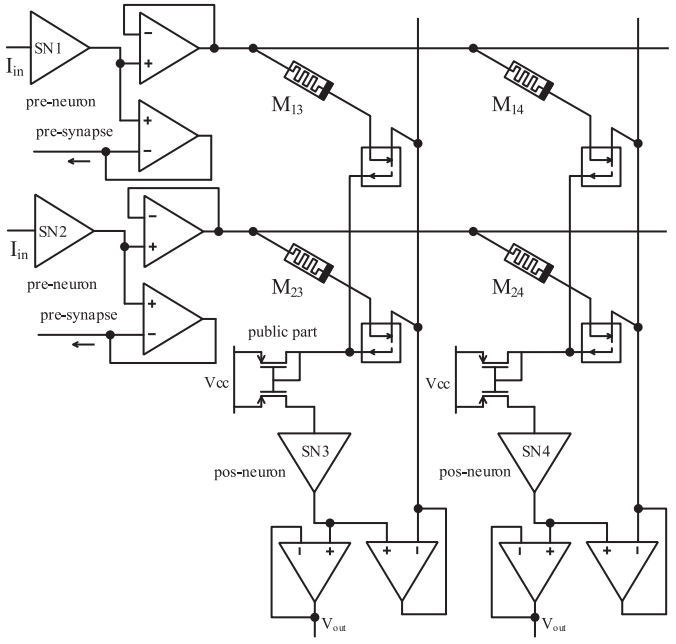

Fig. 10. Crossbar array for spiking neural network. The public part of mirror current circuit used to gathers currents is assembled for every neuron and the rest is needed for every synapse.

On the contrary, since both M_{14} and M_{24} get potentiation, the time SN_4 fires will advance SN_2 in second period. After that, M_{24} gets depression different form its first behave while others act like previous time. In the end, SN_2 does not have anything to do with the SN_4's fire anymore. Weights of M_{13} and M_{14} have increased to the point that only SN_1's expert is enough to make two pos-neurons fire. Accordingly, STDP also works normally in crossbar array.

5. Analysis for merits and insufficient of the proposed circuits.

The proposed MLIF uses 7 transistors and 1 memristor which can generate spikes in microsecond level just like in the real biological neuron [32,33]. No additional switch and logic gate circuits is needed for which the neuron circuit structure is greatly simplified. Moreover, we use identical spikes for both pre- and pos-synaptic signals which benefits the following network topology design. In STDP learning circuit, one memristor is served as synaptic device for its unique property so that there is no need to design complex synaptic circuits. Voltage followers and mirror current circuit are used to conduct circuit isolation to make network stable as much as possible. With the relatively simple network design, STDP rules is implemented in wether learning circuit or crossbar network without any soft control or computing. Unsupervised learning rules' implementation in pure circuit is a worthwhile work for which spiking neural network does not need to design additional supervisory feedback control circuit.

We do efforts to the large scale integration of the neural network. However, problems exactly exist. A spike needs about 90 μs (period) and this time scale depends on the evolution property of memristor used in MLIF, namely, the evolution velocity of memristance. The power dissipation per spike can be calculated as

$$I(t) = \frac{V_{ap} - V_c}{R + M(t)}, \tag{11}$$

$$P_{spike} = \int_{period} V_{ap} I(t) dt, \tag{12}$$

where $I(t)$ represents the current flowing past memristor used in MLIF. The last calculated value of P_{spike} per spike is about $4nJ$. This

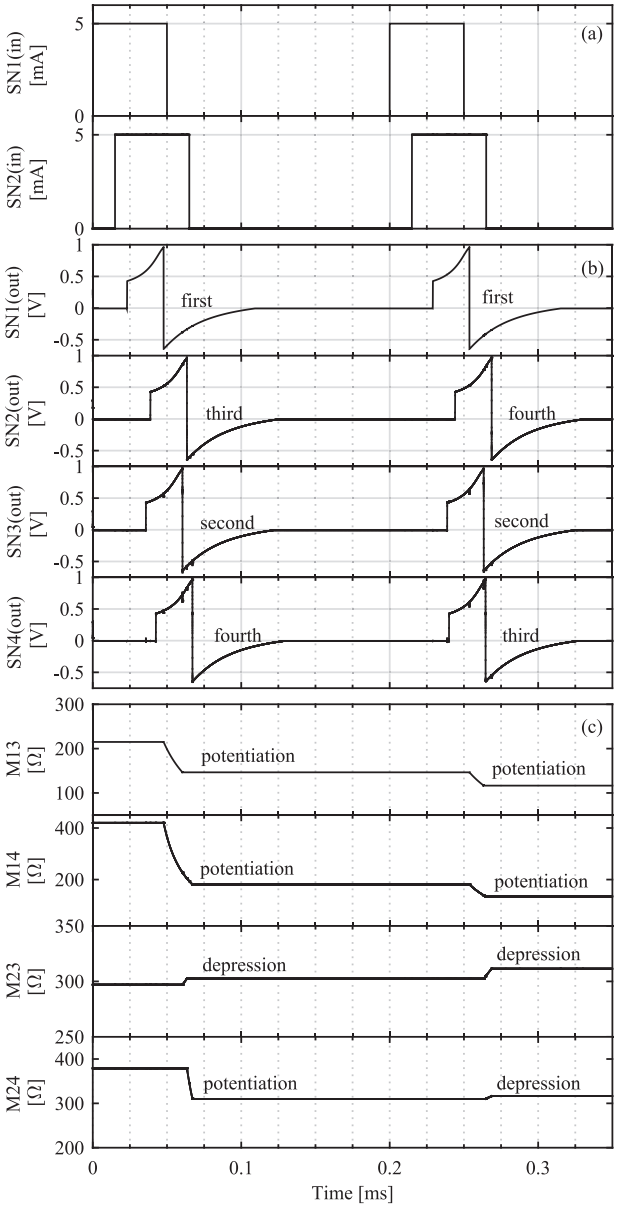

Fig. 11. PSPICE simulation results of crossbar array circuit. (a) Input currents I_{in}, (b) output spikes of four SNs. Two spike periods are recorded; The fire order of SN_2 and SN_4 alters because of the first synaptic weights' update. (c) the memristance evolution of four memristors. M_{24} behaves different in two spike periods depending on the spike fire order.

is a some big value. Comparison with other STDP circuit is displayed in Table 1. Leaky integrate-and-fire is abbreviated as LIF. Integrate-and-fire is abbreviated as IF. Negative potential is abbreviated as NP. T represents transistor. M represents memristor. In the six aspects listed in Table 1, the performance of system we design is good. Only seven transistors and one memristor can complete the task to generate spike like biological pulse. No comparator needs. No logical gate needs. Learning process does not require software assistance. For all that, the proposed MLIF is a considerable candidate for VLSI because of the simple circuit structure. One solution for insufficient in dissipation could be searching a memristor with more fast evolution in memristance to reduce spike's period. We will pay close attention to the newest memristor materials in the future.

Table 1
Comparison of different STDP circuits in studies.

STDP circuit	In [13]	In [14]	In [16]	In [15]	In [17]	In [21]	in [22]	in [23]	in [24,27,29,31]	proposed
Neuron model and number of transistors used in neuron circuit	LIF, 22T+	IF, 22T	LIF, 19T	LIF	IF	LIF, 17T+, comparator	LIF, current conveyer	LIF, comparator, multiplier	LIF	MLIF, 7T
Identity of pre-and post-spike shapes	Yes, square wave without NP	Yes	Yes, without NP	Yes	Yes	Yes	Yes	No	No	Yes
Complexity in synaptic circuit	High, 18T	High, 12T	High, transconductance amplifier	High, 6T1C	High, 21T, operational transconductance amplifier	Low, 1M	Low, 1M	High, 1M with switches	Low, 1M	Low, 1M2T
Additional switches or logical gates used in system	Yes, D-trigger	No	Yes	No	No	Yes, switch	No	Yes	Yes, switch	No
Learning without program	Available	Available	Unavailable	Available	Available	Unavailable	Available	Unavailable	Unavailable	Available
Feasible scheme in crossbar array	Hard	Hard	Hard	Easy	Hard	Hard	Easy	Hard	Hard	Easy

6. Conclusion

A memristor-based spiking neuron circuit is constructed for the pure circuit implementation of STDP. The spiking neuron circuit fires spikes taking advantage of the memristor features and can be regarded as a improvement on the conventional Leaky Integrate-and-Fire neuron model. No comparator or logical gate is used in neuron circuit which benefit to the network integration. Then, basing on the designed spiking neuron circuit, a STDP learning circuit is built to implement adaptive-learning of synaptic weights. Memristor's conductance represents synaptic weight. STDP works well in learning circuit. Further, a simple 2-input 2-output spiking neural network framework in form of crossbar array is designed. STDP learning rules also work efficiently in network. PSPICE simulation results validate the practicability of the spiking neuron circuit and STDP learning circuit. The proposed system possesses a relatively simple circuits structure that is propitious to the VLSI's implementation of spiking neural network. Problem also exists and the possible solution in future work are put forward. In the mean time, we will explore the possibility of the proposed circuits in some practical applications such as image recognition and associative memory.

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