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Unsupervised learning in hexagonal boron nitride memristor-based spiking neural networks

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Unsupervised learning in hexagonal boron nitride memristor-based spiking neural networks

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CrossMark

Abstract

Resistive random access memory (RRAM) is an emerging non-volatile memory technology that
can be used in neuromorphic computing hardware to exceed the limitations of traditional von
Neumann architectures by merging processing and memory units. Two-dimensional (2D)
materials with non-volatile switching behavior can be used as the switching layer of RRAMs,
exhibiting superior behavior compared to conventional oxide-based devices. In this study, we
investigate the electrical performance of 2D hexagonal boron nitride (h-BN) memristors towards
their implementation in spiking neural networks (SNN). Based on experimental behavior of the
h-BN memristors as artificial synapses, we simulate the implementation of unsupervised learning
in SNN for image classification on the Modified National Institute of Standards and Technology
dataset. Additionally, we propose a simple spike-timing-dependent-plasticity (STDP)-based
dropout technique to enhance the recognition rate in h-BN memristor-based SNN. Our results
demonstrate the viability of using 2D-material-based memristors as artificial synapses to perform
unsupervised learning in SNN using hardware-friendly methods for online learning.

Keywords: resistive random access memory, spiking neural network, two-dimensional
memristors, spike-timing-dependent-plasticity

(Some figures may appear in colour only in the online journal)

1. Introduction

Artificial neural networks (ANN) offer an approximate
simulation of the human brain and can be realized with highly
interconnected processing units in neuromorphic computing
hardware. Despite remarkable advancements in neuromorphic
computing hardware, biological neural networks continue to
outperform ANNs in terms of energy efficiency and cap-
abilities for online learning. To better emulate biological
neural networks and to bridge the gap between neuroscience
and machine learning, spiking neural networks (SNN) exploit
event-based spikes for data transfer and processing [1, 2].
SNNs employ processing units and biologically plausible

learning models (e.g. spike-timing-dependent-plasticity or
STDP) that closely mimic the human brain [3]. SNN-based
neuromorphic computing systems are noteworthy and pro-
mising solution to improve energy efficiency as demonstrated
with TrueNorth, a neuromorphic complementary metal-oxide
semiconductor (CMOS) integrated circuit produced by IBM
[4], and Loihi, a neuromorphic processor with on-chip
learning from Intel [5]. While not a direct comparison,
TrueNorth can produce 400 billion SOPS (synaptic operations
per second) per watt for networks with high spike rates and a
high number of active synapses, compared to one of the most
energy-efficient supercomputers at the time that only mana-
ged 4.5 billion FLOPS (floating-point operations per second)
per watt [4]. Another comparison can be made between Loihi
and a 1.67-GHz Atom CPU to solve L1-minimization.

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Table 1. Comparison between this work and previous approaches on recognition rate during single training epoch of MNIST dataset.

Work	Method	Technology	# of output neurons	Recognition rate
[31]	STDP-based unsupervised learning	Au/h-BN/Ti	800	64%
[33]	Unsupervised learning with aligned CNT+CMOS	Carbon nanotube	40	76%
This work	Unsupervised learning (simplified STDP)	Au/h-BN/Ti	40	67.5%
This work	Unsupervised learning (STDP-based weight dropout)	Au/h-BN/Ti	40	80.2%

Results showed that Loihi is $2.58\times$, $8.08\times$ and $48.74\times$ more energy efficient depending on the number of unknowns [5].

Furthermore, non-volatile memory technology such as resistive random access memory (RRAM) offers an energy-efficient implementation of neural networks through in-memory computing (IMC). In this approach, processing and memory units are combined to alleviate bottlenecks associated with the movement of data. RRAM facilitates improvements to neuromorphic hardware due to several notable characteristics, including scalability, non-volatility, fast switching speeds, low power dissipation, and compatibility with CMOS [6–11]. The storage element in RRAM has a programmable resistance and is often referred to as a memristor. The resistance of a memristor is adjusted with the application of an external stimulus (e.g. a voltage across its two terminals). Moreover, the change in resistance can also be tuned by the amplitude, direction, or duration of the applied voltage [11, 12]. Its resistive state depends on the history of the external stimulus as it introduces a non-volatile effect. However, conventional memristor technologies present challenges such as a limited conductance range [13], asymmetric potentiation and depression characteristics, non-linearity, and variability [14]. These non-idealities can affect neuromorphic system performance and efficiency [15–19].

Recently, two-dimensional (2D) materials such as transition metal dichalcogenides [20], hexagonal boron nitride (h-BN) [21–23], black phosphorus [24, 25], and graphene [26, 27], were shown to exhibit non-volatile resistive-switching behavior. These 2D memristors can help alleviate some of the non-idealities of oxide-based RRAM [28] towards more efficient and better performing SNNs. For example, the layered structure of 2D materials could help minimize variation in resistive switching layer thickness to provide a more robust implementation of STDP [29]. Moreover, compared to oxide-based RRAM, synaptic plasticity (long-term potentiation and depression) can be better controlled in chemical vapor deposition (CVD)-grown h-BN memristors as filament formation/dissolution occurs in confined and chemically stable defects surrounded by crystalline h-BN [28]. Other factors that can further help enhance the energy efficiency of SNN are the low programming voltages [30] and fast switching speeds [31, 32] of 2D-material-based memristors.

Previous works provide detailed characterization of CVD-grown 2D h-BN memristors [23]. Here, we fabricate stable CVD-grown Au/Ti/h-BN/Au memristors and further study their experimental properties in anticipation for their use in SNN. We develop a recursive mathematical model which follows the experimental pulsing behavior of the h-BN memristor [33] to simulate an energy-efficient, CMOS-compatible, and hardware-friendly SNN for pattern classification. We then propose a novel STDP-based weight dropout technique to improve classification accuracy. Previous studies have shown the feasibility of SNN implementation utilizing non-2D material memristors as synaptic devices [33, 34]. A recent study used an empirically extracted STDP learning rule to examine the viability of Au/Ti/h-BN/Au memristors as synapses in a SNN [35]. Compared to this previous work, our method achieves similar classification accuracy with fewer leaky integrate and fire (LIF) output neurons. In addition, our proposed implementation complies to the experimental potentiation/depression characteristics of h-BN memristor resulting from pulses of fixed amplitude and same width. This makes our method hardware-friendly as it eliminates the need for complicated pulses with different shapes/width. Finally, we show that the proposed STDP-based weight dropout strategy considerably enhances the outcomes by 12%, making our SNN more computationally efficient as well as more hardware- and power-friendly. Table 1 presents a comparison between the methods proposed in this study and those from previous reports in terms of recognition rate for a single training epoch of the modified national institute of standards and technology (MNIST) dataset. Our study demonstrates the viability of training an adaptable SNN with memristors based on 2D materials.

2. Results

2.1. Physical characteristics of h-BN memristor devices

This work uses 2D h-BN memristors with non-volatile and multi-state resistive switching characteristics. The detailed fabrication methods for these devices are found elsewhere [23]. Here, we investigate the physical and electrical properties of the device towards their application as artificial synapses in SNN. Figure 1(a) shows a picture of 2D h-BN memristor arrays fabricated on a SiO_2/Si wafer. A schematic of the memristor arrays is shown on the left side of figure 1(b). The Au bottom electrode is shared by 10 devices in a row, each device having separate Ti/Au top electrode. The right side of figure 1(b) depicts the design of a single Au/Ti/h-BN/Au memristor. The top electrode (TE) is Ti (30 nm) capped with Au (30 nm) to prevent oxidization. The resistive-switching medium is multilayer h-BN, and the bottom electrode (BE) is Au. The thickness of the multilayer h-BN is identified by atomic force microscope (AFM) as indicated in figure 1(c) and is approximately 10 nm. The CVD-grown multilayer h-BN film is further characterized by its Raman spectrum plotted in figure 1(d) (blue line), which shows a peak position around $1368\,cm^{-1}$ and full width at half maximum (FWHM) of approximately $45\,cm^{-1}$. For comparison,
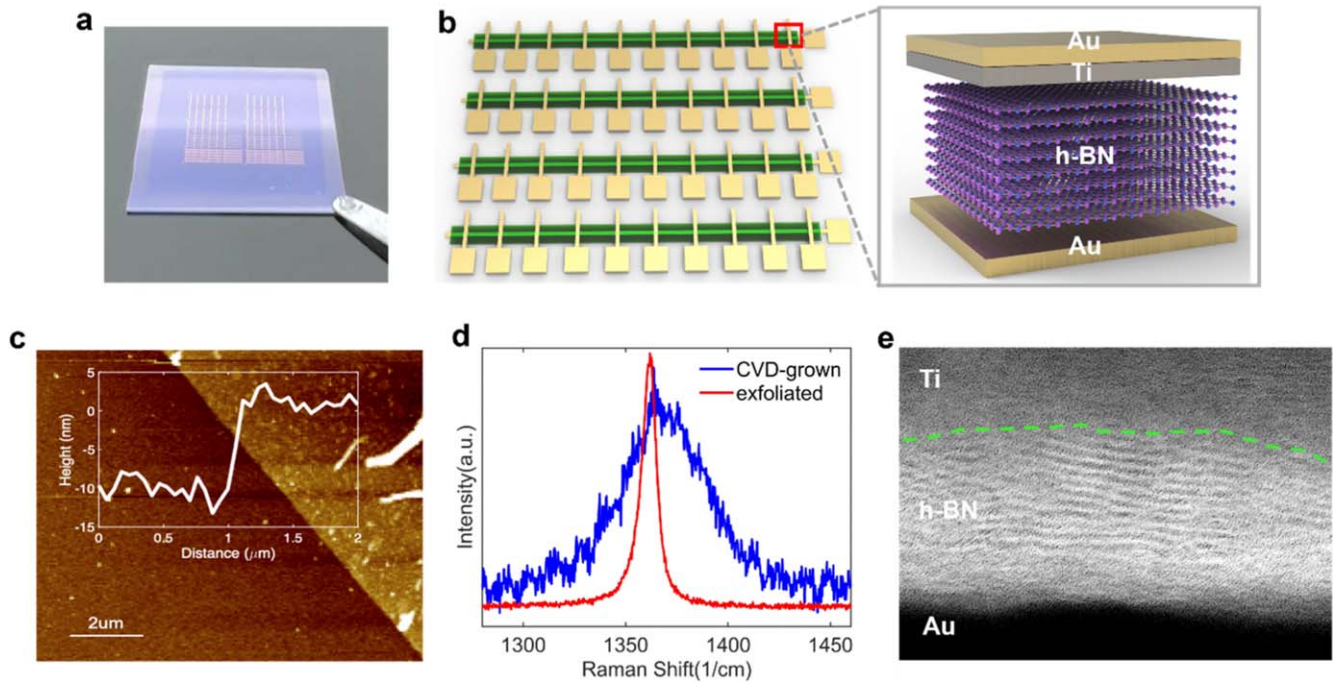
Figure 1. (a) The Au/h-BN/Ti memristor arrays on 90 nm SiO2/Si wafer. (b) Schematic of the Au/h-BN/Ti memristor arrays (on left) and graphical design of a single Au/h-BN/Ti memristor (on right). (c) Atomic force microscope of the h-BN memristor. (d) Raman spectrum of CVD-grown multilayer h-BN shown in blue color versus exfoliated crystalline h-BN shown in red color. (e) Cross-sectional TEM image of Au/h-BN/Ti memristor.

an exfoliated h-BN sample is also characterized by its Raman spectrum and plotted in figure 1(d) (red line). For the exfoliated h-BN sample, the approximate peak position and FWHM are respectively $1362 \, cm^{-1}$ and $10 \, cm^{-1}$. CVD-grown samples reveal a broadened FWHM compared to exfoliated crystalline flakes because of random defects generated during the CVD process.

A cross-sectional transmission electron microscopy (TEM) image is shown in figure 1(e) identifying the multi-layered h-BN structure (approximately 15–20 layers) and revealing defects (blurred darker regions) associated with filamentary formation of conductive paths. As reported earlier, grain boundaries (GBs) in CVD-grown h-BN films act as percolation paths for metallic penetration and filamentary resistive-switching effects [32]. This is true for devices with active metal electrodes (in this work Ti), where the application of a positive bias leads to metallic ion penetration preferentially along the GBs [36–38]. We note that metallic penetration may also initiate during TE contact deposition because of the damage from the bombardment of atoms [36]. For devices with both electrochemically inter electrodes (e.g. Pt, Au, etc) intrinsic h-BN species (e.g. boron vacancies) play a more significant role in the resistive-switching behavior. These can migrate from lattice defects (GBs) under the application of electric fields to form interlayer bridges (bonds) that modifying the electronic properties and conductance along the sites of the defects [36, 39]. Theoretical and experimental work have identified the migration of boron vacancies as more energetically favorable (lower activation energy) compared to nitrogen [40, 41].

2.2. Electrical behavior of h-BN memristor devices

Figure 2(a) plots the experimental current–voltage (*I–V*) measurements of a device with a $3 \, \mu m \times 3 \, \mu m$ active area over 50 consecutive cycles. The data shows a transition in resistance from high resistance state (HRS) to low resistance state (LRS) and the arrows label the direction of the voltage sweep and *I–V* characteristics. These *I–V* measurements were obtained by applying a sweeping voltage on the top electrode (bottom electrode grounded) while measuring current to reveal the resistive-switching effect (hysteresis in *I–V* curves). Here, a compliance of 10^{-3} and 10^{-2} A were activated for positive and negative applied voltages, respectively. Figure 2(b) plots the cumulative distribution of resistance (HRS and LRS) at a read voltage of 0.1 V for all 50 cycles. Figure 2(c) shows histograms of the set and reset voltages (V_{set} and V_{reset}) corresponding to transitions between HRS and LRS as extracted from the 50 cycles of DC *I–V* measurements. Figure 2(d) illustrates the retention (non-volatile) properties of the h-BN memristors by measurements of current as a function of time up to 10^4 s with negligible drift in HRS and LRS. This is consistent with previous works that reported stable retention for over a week at room temperature ($\sim 10^6$ s) [32], as well as good retention and stability over multiple conductive states [23].

In addition to DC *I–V*, we perform pulsed voltage experiments to capture gradual changes in conductance and verify the feasibility of using h-BN memristors to emulate synaptic functions (i.e. long-term potentiation and depression). Figure 2(e) shows the pulsed programming of the h-BN memristor. By delivering a succession of positive/negative
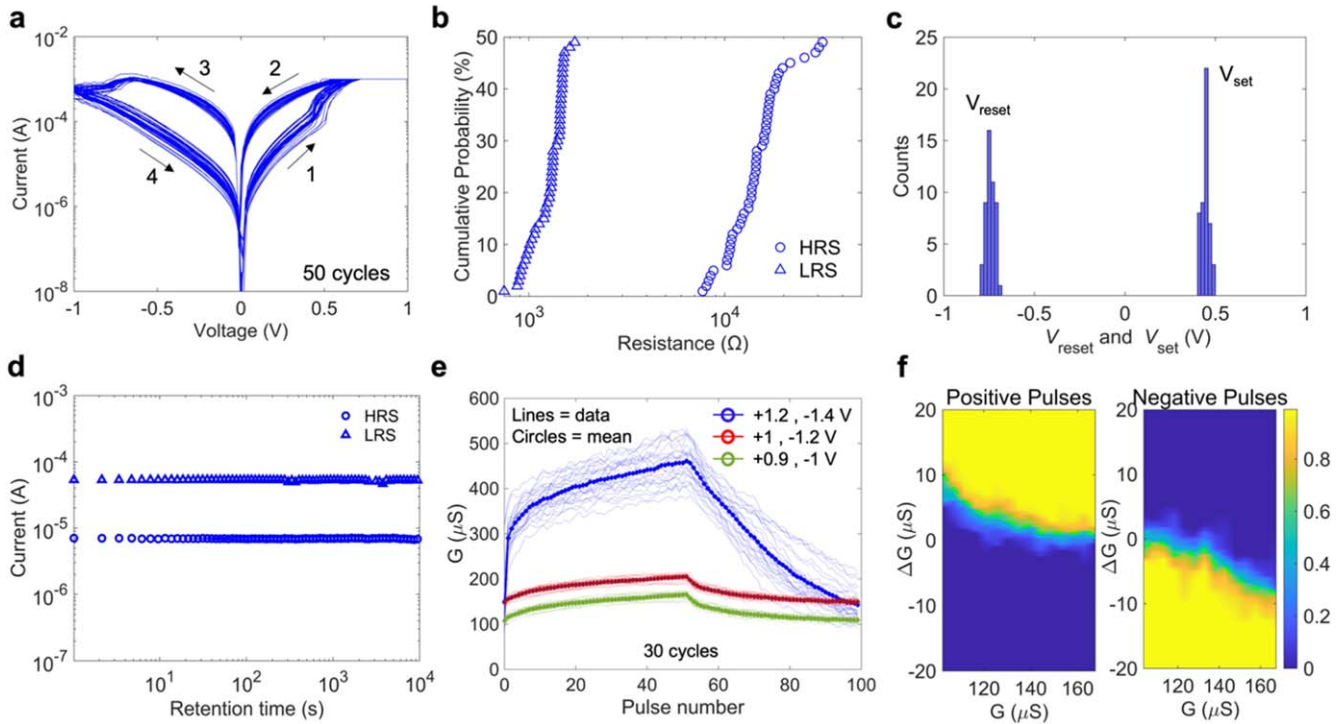
Figure 2. (a) Measured current–voltage (*I–V*) characteristics of the h-BN memristor over 50 cycles. (b) HRS and LRS cumulative probability distribution (read voltage at 0.1 V). (c) histogram of set and reset voltages. (d) Retention tests measured for 10 000 s for LRS and HRS using a read voltage of 0.1 V. (e) Pulse measurement of the h-BN device conductance for three different pulse amplitudes (fixed pulse width), each case is the average over 30 consecutive cycles. There are 50 positive pulses followed by 50 negative pulses. (f) CDF plot for the green case in (e) showing the variability and non-abrupt (linear) response of ΔG versus pulse programming for positive and negative pulses over 30 cycles.

voltage pulses, we reveal analog conductance characteristics compatible with the emulation of synaptic plasticity (i.e. changes in the strength of neuron connections). We used 50 positive pulses followed by 50 negative pulses with fixed width of 100 ns and varying pulse amplitudes of +1.2 and −1.4 V for case 1 (blue line), +1 and −1.2 V for case 2 (red line), and +0.9 and −1 V for case 3 (green line) over 30 consecutive cycles each. After each pulse, a voltage of 0.1 V is applied to read current and obtain conductance. The results reveal a gradual change in conductance with each programming pulse, indicating applicability of h-BN devices as artificial synapses. Moreover, increasing the pulse amplitudes achieves larges update in conductance (ΔG) suggesting advanced synaptic functionality (e.g. tunable synaptic plasticity).

By observing the distribution of conductance updates (ΔG) as a function of conductance (*G*) form multiple programming/erase cycles we can better identify the variability and linearity of the pulse update scheme. This is shown in figure 2(f) as contours of the cumulative distribution function (CDF) of ΔG versus *G* over 30 cycles (for positive and negative pulses). Note that the CDF plots correspond to the data in figure 2(e) (green) for pulse amplitudes of +0.9 and −1 V. In figure 2(f), the green dashed line traces the midpoint in the distribution (i.e. the value of 0.5). For a perfectly linear device, the midpoint line should remain constant as a function of *G*, and the transition through the midpoint would be abrupt in the absence of variation. Here we observe a minor change in the distribution midpoint with *G* indicating good linearity for both positive (potentiation) and negative (depression)

pulses. Moreover, we verify that cycle-to-cycle variability is small, as illustrated by a short range in the distribution of ΔG transitioning through the midpoint (abrupt change in contour plot). Our initial results also indicate a yield of ~90% (most devices from same wafer exhibit reasonable resistive switching behavior) [23], as well as similar resistive-switching characteristics (both *I–V* and pulsed) for different devices [42]. However, a comprehensive and quantitative device-to-device variability study is not reported here and is beyond the scope of this work. Nonetheless, device-to-device variability remains a general challenge for memristors based on 2D layered materials [43–45], but could be mitigated with optimized methods for synthesis and transfer of critical 2D active layers [45], as well as by optimized methods for contact deposition [36].

2.3. Spiking neural network based on h-BN memristors

A synapse is a junction of two neurons through which they communicate by mean of electrical or chemical signals. In electrical synapses, a source neuron (pre-synaptic neuron) sends a signal to a target neuron (post-synaptic neuron) by means of the synapse in the form of an electrical impulse (action potential). Figure 3(a) shows a simplified overview of biological neural system. The transmission of electrical signals is made possible by the synapse, which connects the axon of one neuron (pre-synaptic neuron) to the dendrite of another neuron (post-synaptic neuron). In this work, each pre-synaptic (input) neuron is connected to all post-synaptic
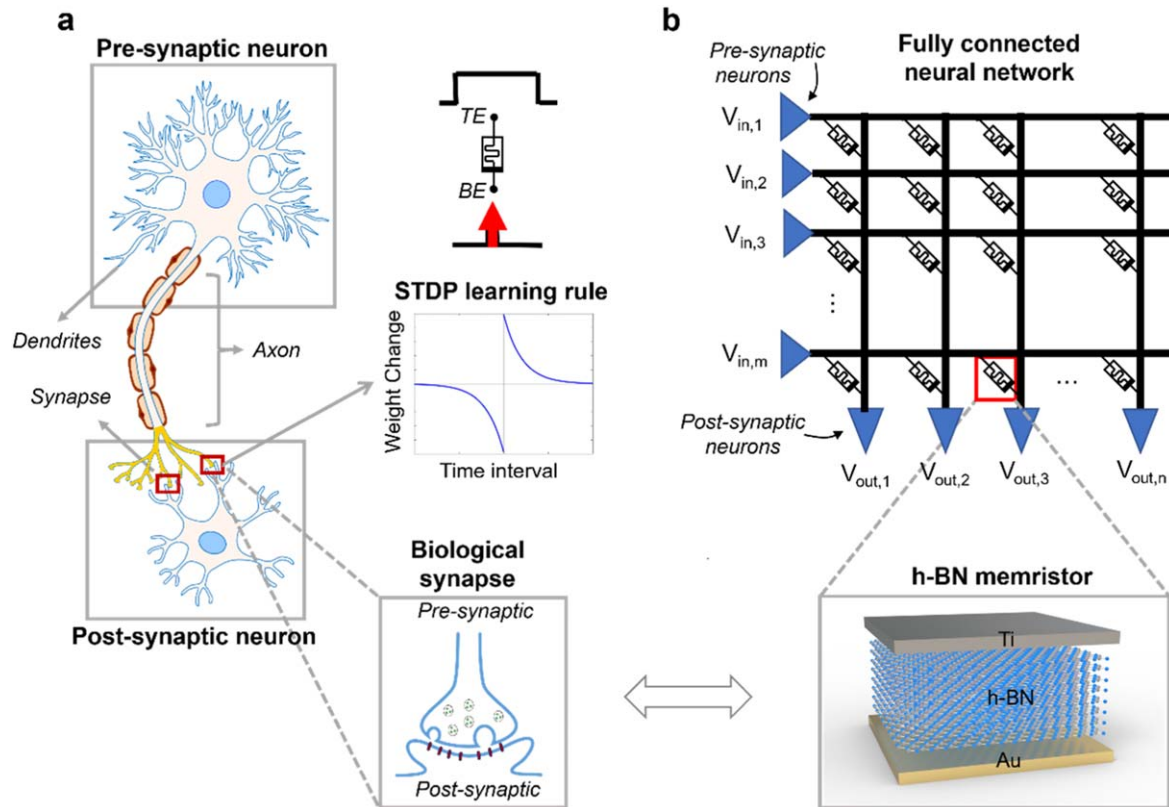
Figure 3. (a) An illustration of a biological neurons consisting of pre-synaptic and post-synaptic neurons, axon, and biological synapse. (b) A fully connected memristor-based artificial neural network utilizing 2-terminal h-BN memristor device as an artificial synapse.

(output) neurons with varying strengths (weights). STDP is a learning scheme for SNN in which the sign and magnitude of changes in synaptic strength are influenced by the temporal correlation of pre- and post-synaptic spikes [46, 47]. Figure 3(b) illustrates the fully-connected SNN used in this study. Here, h-BN devices are used as artificial synapses to implement the SNN. The biological synapse and the 2-terminal artificial synapse (i.e. the multi-layer 2D h-BN memristor) are contrasted at the bottom of figure 3.

2.4. Implementation of unsupervised h-BN memristor-based spiking neural network

This section describes the implementation of our SNN model based on experimental data from individual h-BN memristors. The SNN architecture consists of two fully-connected layers: 784 input neurons and 40 output neurons. For the output neurons, we consider a commonly used spiking neuron model: the LIF model [48] . In a circuit implementation of the LIF model, an RC circuit with a threshold acting as integrator of synaptic signal inputs [49]. The accumulated (integrated) signal is compared against a threshold reference and will activate an output spike production circuit if the threshold is achieved. Figure 4(a) shows a flowchart for the simulated crossbar implementation of the SNN. The simulation conducts unsupervised learning to classify the MNIST handwritten digit dataset. This dataset consists of 60 000 training images of handwritten digits and 10 000 separate testing images.

The SNN implementation is based on feedforward and feedback modes, validated with h-BN memristor data, to simulate accumulated charge at the output neurons (Ohm's law and Kirchhoff's law) as well as updates in synaptic weights (pulsed conductance updates). The experimental data is used to fit synaptic plasticity mathematical models that used in the SNN simulation. This way, the simulation captures the realistic behavior and non-idealities of an h-BN memristor implementation. The model considers the averaged experimental data across 30 cycles (see figure 2(e)), and cycle-to-cycle and device-to-device variability are excluded from the simulation. Variability can affect the performance of the SNN, but we expect significant robustness as similar demonstrations on conventional memristor technologies have shown [50]. Further investigation on the impact of cycle-to-cycle and device-to-device variability on ANN implementations should be conducted as h-BN memristor technology advances in maturity and more data on variability and stability (retention) becomes available. Nonetheless, promising preliminary results for 2D-material implementations indicate high accuracy in ANN-based image recognition with less variation compared to other materials [51]. However, experimental verification remains a challenge as reliable methods for large-scale integration of 2D electronics with conventional technology (i.e. silicon CMOS) needs further efforts.

Phase 1: Feedforward mode (current and charge integration.

Initially, the pixel intensities of two-dimensional grayscale input training images (28-by-28 pixels) are translated to
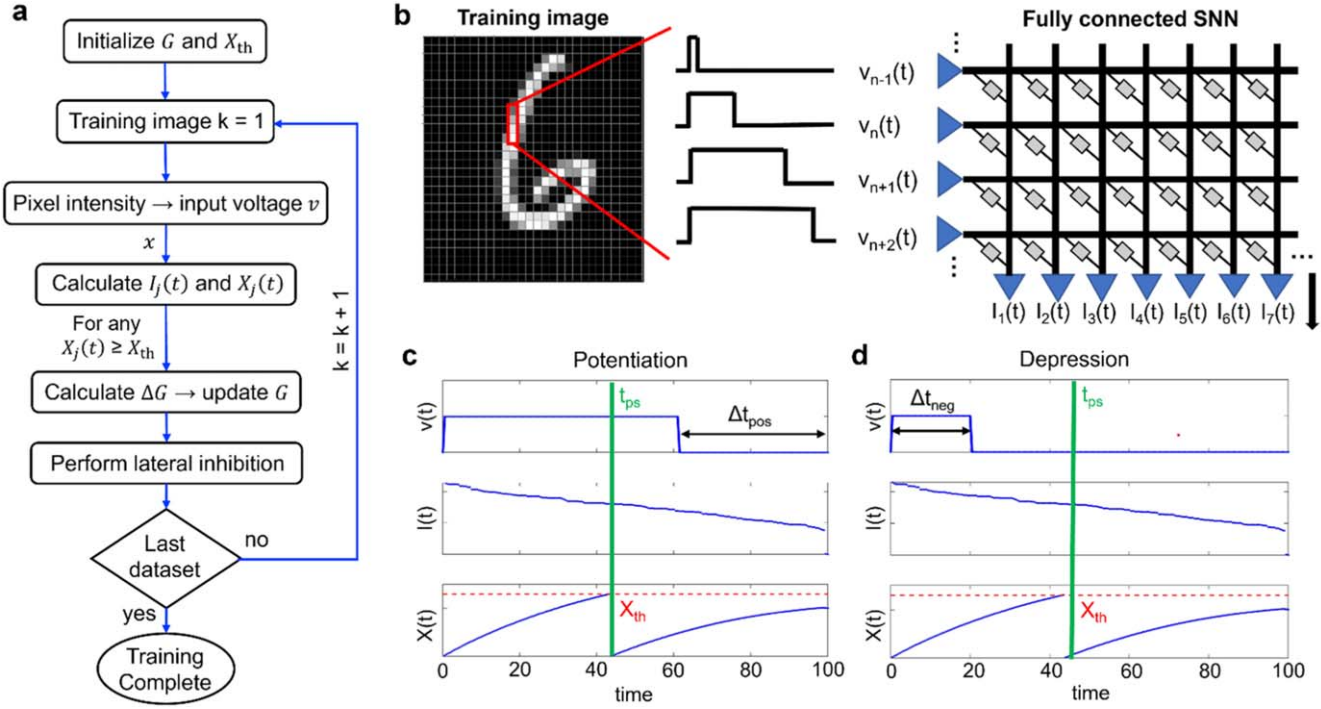
Figure 4. (a) Flow chart of implementation of spiking neural network for pattern classification on a h-BN memristor crossbar. (b) Demonstration of two-layer spiking neural network implementation with h-BN synaptic devices to accomplish unsupervised learning for MNIST dataset classification: The input layer transform input image pixels into input voltages (spikes). The synapses fully connect the input neurons and the output neurons. The synapses receive generated voltages (pre-spikes), perform the dot-product, and send accumulated output current to the output layer. The output layer's LIF neurons process accumulated current and produce output spikes. (c) Output current accumulation and charge integration for an input voltage width (t_{width}) larger than post-synaptic spike time ((t_{ps}). (d) Current accumulation and charge integration when $t_{\text{width}} < t_{ps}$.

one-dimensional temporal voltages (784 input voltage pulses). Each voltage pulse has fixed amplitude of $V_r = 0.1$ V and different widths (t_{width}) ranging between 0 and 100 ms corresponding to pixel intensity. A black pixel corresponds to a voltage pulse with minimum t_{width} (minimum intensity), a white pixel corresponds to $t_{\text{width}} = 100$ ms (maximum intensity), and any other pixel intensity translates to pulse widths between 0 and 100 ms. The input voltages, $v_i(t)$, are applied to the h-BN memristor crossbar and the accumulated currents at the bottom electrodes are calculated at every time step. Figure 4(b) depicts this procedure graphically. The postsynaptic currents at each column (indexed with j) are obtained based on Kirchhoff's law as $I_j(t) = \sum_i v_i(t)G_{ij}$, where G_{ij} are the adjustable h-BN memristor conductances and $v_i(t)$ are the input voltages at each row in the crossbar. Mathematically, the output current vector results from the multiplication of the input voltage vector and the matrix of memristor conductances (vector-matrix multiplication or VMM). In the crossbar architecture, VMM can be computed with a single read operation (parallel computation). The SNN simulation follows with the calculation of accumulated charge at the output LIF neurons based on

$$\tau_{RC} \frac{\mathrm{d}X_j(t)}{\mathrm{d}t} - X_j(t) = I_j(t). \tag{1}$$

In [1], $I_j(t)$ is the current in neuron j at time t and $X_j(t)$ is the accumulated charge. Here, τ_{RC} is the time constant associated

with the LIF circuit. Reaching a predetermined threshold ($X_{th} = 10$ mC) at any of the output neuron will trigger the firing of a post-synaptic spike. In figures 4(c) and (d), t_{ps} denotes the triggering time of the post-synaptic spike. Through lateral inhibition pathways, the output spike propagates among other LIF output neurons to prevent them from firing at the same time. In our implementation, following a post-synaptic spike, the charge at every output neuron is reset to an initial condition ($X_i = 0$) and held there for a fixed time ($t_{inh} = 10$ ms) except for the neuron that recently fired which can immediately return to accumulating charge. This competitive learning model where neurons can inhibit each other is known as winner-takes-all (WTA) [52, 53]. WTA is thought to be a basic component of cognitive tasks including attention and object recognition [54, 55]. All synaptic connections to the neuron that fired will be adjusted. In hardware, this means updating the conductance of memristors from a specific column connected to the neuron that fired. We must consider two cases of synaptic plasticity: (1) strengthening the connection (potentiation) to inputs that contribute to the firing (inputs that were active at the time of the post-synaptic spike, $t_{\text{width}} > t_{ps}$); (2) weakening the connection (depression) for inputs that contribute less (inputs that were inactive at the time of the post-synaptic spike, $t_{\text{width}} < t_{ps}$). Figures 4(c) and (d) respectively illustrate examples of potentiation and depression with plots of input voltage (top), output current at the post-synaptic neuron (middle), and accumulated charge
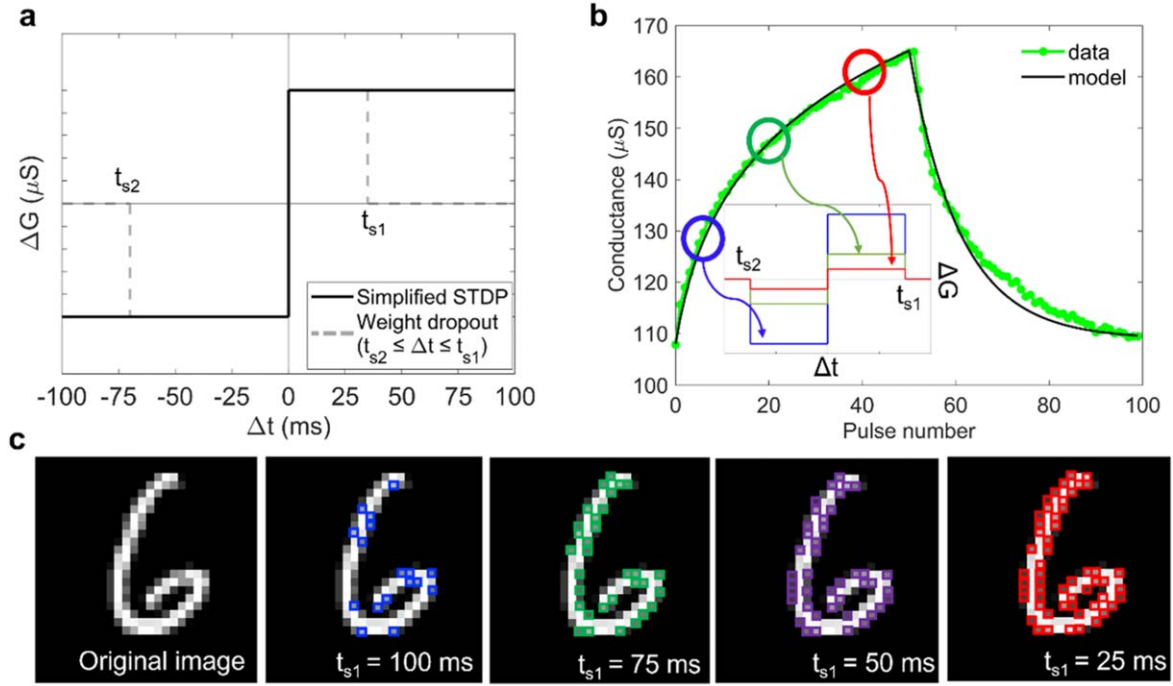
Figure 5. (a) Simplified STDP rule (solid black line) versus STDP-based weight dropout rule (dashed gray line). (b) Mathematical model (black solid line) fit to experimental pulsed h-BN memristor data with 100 ns pulses and amplitudes of 0.9 and -1 versus (c) Updates performed during learning for STDP-based weight dropout rule with different positive time filters (t_{s1}): the colored pixels are the ones that do not update at each iteration for each STDP-based weight dropout case. In all the weight dropout cases, the negative time filter (t_{s2}) is fixed at -70 ms.

(bottom) during a 100 ms timeframe (single training step). Synaptic weight update is discussed next.

Phase 2: Feedback mode (synapse update)

We use a simplified learning rule to update synapse weights which follows the experimental pulsing behavior of h-BN memristor. As previously reported, memristors are compatible with the implementation of STDP learning rules [56–63]. In our simplified hardware-friendly STDP implementation, ΔG will be either positive or negative based on the temporal correlation of corresponding input voltage pulse widths (t_{width}) and post-synaptic spikes (t_{ps}), and the magnitude will be modeled to simulate h-BN memristor pulsed characteristics (see figure 5(a)). In other words, a single or set of consecutive positive (negative) voltage pulses are applied to memristors that require potentiation (depression). The change in h-BN memristor conductance follows an experimentally-verified recursive model given by

$$\Delta G = a_p + b_p e^{-c_p \frac{G - G_{\min}}{G_{\max} - G_{\min}}}, \text{ Potentiation} \quad (2a)$$

$$\Delta G = a_d + b_d e^{-c_d \frac{G_{\max} - G}{G_{\max} - G_{\min}}}, \text{ Depression} \quad (2b)$$

where a_p, a_d, b_p, b_d, c_p, c_d are fitting parameters and $G_{\max}$, $G_{\min}$ correspond to the maximum and minimum experimental conductances respectively [33]. Figure 5(b) shows the model fit to experimental data with fitting parameters values of 10^{-10}, 10^{-4}, 5×10^{-6}, -10^{-4}, 2.5, 0.05 for a_p, a_d, b_p, b_d, c_p and c_d respectively. The conductance is bounded to $G_{\min}$ and $G_{\max}$ which are measured at 108 and 165 μS for the h-BN memristor with a 3×3 μm active area. The inset in figure 5(b) emphasizes how the simplified STDP approach

introduces non-ideal (non-linear) h-BN memristor behavior into our SNN simulation. For example, when G is in the lower end, the change in conductance with the application of a single pulse (positive or negative) is larger compared to when G is in towards the upper end. In addition, the simulation incorporates homeostatic regulation to maintain similar firing rates for all neurons by making small adjustments to the firing thresholds as given by $\Delta X_{\text{th}} = \gamma (f_r - 1/N)$. Here, γ is a threshold update fitting factor (set to 5 μ C), f_r is the firing rate, and N is the number of output neurons. By adjusting γ, recognition and convergence rate changes. It is important to adjust X_{th} and δ to maintain reasonable firing rates and to avoid overfitting in the learning SNN unsupervised learning process.

3. Discussion

To improve the effectiveness of neural transmissions, excess neurons and synaptic connections are removed through a process known as synaptic weight dropout. Synapses connecting neurons with high spiking correlation are preserved, while synapses with poor or uncorrelated spiking activity are pruned [64]. Weight dropout also mitigates overfitting in neural networks trained with large size data sets by preventing unwanted specialization towards details and noise in the training data and allowing better generalization [65].

We demonstrate an STDP-compatible technique to prune (remove) insignificant weights for an improved network performance in terms of classification accuracy. This
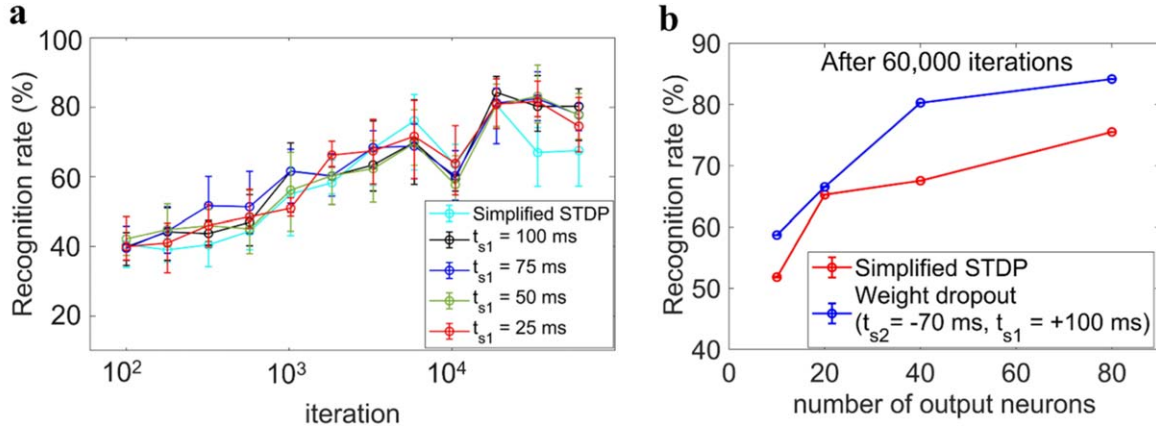
Figure 6. (a) Comparison of recognition rate as a function of iteration for simplified STDP rule versus STDP-based weight dropout rule with 4 different positive time filter over 5 cycles with different initial conductance states. (b) Comparison of recognition rate as a function of number of output neurons for simplified STDP rule (blue plot) vs. STDP-based weight dropout rule with $t_{s2} = -70$ ms and $t_{s1} = +100$ ms (red plot). Plots are the mean over 5 consecutive cycles.

technique applies a time filter on the temporal correlation between input voltage pulse widths and post-synaptic spikes (i.e., Δt), to limit the number of conductances that will be updated in the feedback phase. The process is as follows. First, Δt is calculated as

$$\Delta t_{\mathrm{neg}} = t_{\mathrm{width}}(ms) - 0(ms), \text{ for } t_{\mathrm{width}} < t_{ps} \qquad (4a)$$

$$\Delta t_{\mathrm{pos}} = 100(ms) - t_{\mathrm{width}}(ms), \text{ for } t_{\mathrm{width}} \geqslant t_{ps} \qquad (4b)$$

where t_{width} denotes the input DC voltage width, t_{ps} denotes the post-spike time (see figures 4(c), (d)). Next, the calculated Δt is normalized to fall within the STDP range $(+/- 100$ ms$)$. As shown in figure 5(a), we define t_{s1} as the positive (potentiation) time filter and t_{s2} as the negative (depression) time filter. All the synapses with Δt between t_{s2} and t_{s1} are subject to a conductance update determined by the experimentally-verified recursive model in equation (2). We have performed simulations for $t_{s2} = -70$ ms and $t_{s1} = 100, 75, 50$ and 25 ms. In figure 5(c), the same grayscale MNIST image (out of 60 000 training images) is shown with colored pixel outlines indicating the synapses that were dropped (not updated) with various values of the time filters ($t_{s2} = -70$ ms and $t_{s1} = 100, 75, 50$ and 25 ms). Evidently, the number of pruned (dropped) conductances is largest for $t_{s2} = -70$ ms and $t_{s1} = 25$ ms. Also, the figure labeled 'original image' represents the case without weight dropout. This implies that in simplified STDP learning approach no weight is eliminated, and during each iteration all the corresponding synapses are updated.

Figure 6 summarizes the results from the SNN simulations using simplified STDP as well as STDP-based weight dropout learning schemes. In figure 6(a), the recognition rate for arrays with 40 output neurons is plotted as a function of training number for both cases (different time filters shown for weight dropout). For each case, the simulation is conducted five times, and the mean value is plotted with the length of error bars indicating the standard deviation. Since the labels of training images are not known to the network (training is unsupervised), recognition rate is based on the spiking activity for all 10 000 test images of MNIST dataset.

Each neuron is assigned to the handwritten digit for which it spiked the most, and the ratio of spikes on the assigned digit to the total number of spikes is calculated as the recognition rate. The recognition rate shown in figure 6(a) is the average of all the handwritten digits in MNIST dataset. As observed in figure 6(a), the final recognition rate (after 60 000 training steps) for the STDP-based weight dropout rule of $t_{s2} = -70$ ms and $t_{s1} = 100$ ms (in solid black line) has improved by 12% for 40 output neurons reaching 80.2% compared to the simplified STDP method recognition rate of 67.5%. Figure 6(b) shows the results of the simulations for 10, 20, 40 and 80 output neurons when trained with recursive model-based simplified STDP (red line) and STDP-based weight dropout with time filters of $t_{s2} = -70$ ms and $t_{s1} = 100$ ms (blue line). Plots are the average over five simulation cycles for each case. The results shown for each number of output neurons are the recognition rate after training with one single epoch (i.e. 60 000 training images). Improved recognition rate is observed when the proposed STDP-based weight dropout technique is applied. The improvement is attributed to alleviating overfitting in the SNN, as the improvement appears more significantly towards the end of the training epoch.

4. Conclusions

We have reported the synaptic characteristics of 2D Au/h-BN/Ti memristors for spiking neural network neuromorphic application. The devices exhibit advanced synaptic functionality such as larger dynamic range with increased pulse amplitude, good linearity for both potentiation and depression, and small cycle-to-cycle variability. Simulation results for MNIST pattern classification based on Au/h-BN/Ti memristive SNN hardware following the experimental pulsing behaviour of memristor reaches satisfactory recognition rate of 67.5% for 40 output neurons. The recognition rate improved as we increased the number of output neurons. We then proposed a STDP-based pruning technique to improve

the recognition rate to 80% for 40 output neurons by improving the overfitting issue observed in our system. Our work is a step towards the deployment of real 2D materials in SNN hardware for training and inference applications.

Acknowledgments

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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