



Integration, the VLSI Journal

journal homepage: www.elsevier.com/locate/vlsi



Circuit implementation of on-chip trainable spiking neural network using CMOS based memristive STDP synapses and LIF neurons

Sahibia Kaur Vohra ^{*}, Sherin A. Thomas, Mahendra Sakare, Devarshi Mrinal Das

Department of Electrical Engineering, Indian Institute of Technology Ropar, Rupnagar 140001, India

ARTICLE INFO

Keywords:

Spiking neural networks
Spike-timing dependent plasticity (STDP)
Memristor crossbar
On-chip training
Pattern recognition

ABSTRACT

Computation on a large volume of data at high speed and low power requires energy-efficient architectures for edge computing applications. As a result, scientists focus on memristive circuits and systems for area and energy efficiency. Spiking neural network (SNN) with bio-inspired spike-timing-dependent plasticity learning (STDP) is a promising solution for energy-efficient neuromorphic systems than conventional artificial neural network (ANN). Previous works on SNN with STDP learning primarily use memristor macro models, which are software-based and cannot give complete insight into circuit implementation challenges. Some reported works on SNN use memristive devices, which require additional fabrication steps. This article presents a full circuit-level implementation of the SNN system featuring on-chip training and classification using memristive STDP synapse in standard CMOS technology. A new learning rule using the modified STDP is implemented to simplify the weight modification process. It does not involve FPGAs, CPUs, or GPUs to train the neural network. The approach used in this paper to modify the weights does not require any additional combinational or digital circuits attached to the memristive synapse resulting in less consumption of area, energy and time. We demonstrated the complete circuit-level design, implementation and simulation of SNN with on-chip training and pattern classification using 180 nm CMOS technology. A comprehensive comparison of the proposed SNN circuit with the previous related work is also presented. To demonstrate the versatility of the CMOS synapse circuit for application scenarios requiring rate-based learning, we have tuned the pair-based STDP circuit to obtain Bienenstock–Cooper–Munro (BCM) characteristics and applied it to heart rate classification.

1. Introduction

Spiking neural network (SNN) is the third generation artificial neural network that provides a promising solution for replacing area and power-hungry hardware for neuromorphic computing. The brain's superior energy efficiency for decision-making cognitive tasks made scientists to focus their efforts on building non-Von Neumann computer systems that imitate the biological brain. Neurons process information as asynchronous event-driven spikes and retain memories as synaptic strengths of their connection in the brain. In this regard, a spiking neural network (SNN) is more bio-plausible than other neural networks that can pave a new way for future intelligent devices for low-power computing applications [1,2].

Spiking neuromorphic computing architecture as shown in Fig. 1, processes information in the form of spikes. Therefore, input sensory analog signal should be converted to spikes which can be performed by various neuron models [3]. Out of all the neuron models, the LIF neuron model gives a good balance between accuracy and ease of hardware implementation, and also it resembles much of biological

neurons [3,4]. The other important block of the SNN is the synapse circuit that stores the synaptic weight and defines the strength of the connection between the neurons. Memristor proves to be the most suitable candidate for emulating a synapse as it provides the tunable and non-volatile storage of synaptic weights [5]. Memristive neuromorphic systems outperform Von-Neumann systems in power efficiency and learning capabilities [6].

The learning mechanism used for updating the synaptic weights is a crucial aspect of the neural network. The training algorithm such as backpropagation used in literature [7,8] is widely established but needs extensive hardware resources and is hard to be fully implemented in analog circuits [9]. Many works have shown the training of memristive neural network using the ex-situ method [10,11] where an external circuit or computational platform is required for weight calculation. In work [12], training is implemented by mapping the values of the obtained weight using learning algorithms in software to the neural crossbar. Some make use of GPUs, FPGAs or microcontrollers, which increases the complexity and power consumption [12,13]. Another

* Corresponding author.

E-mail address: sahibia.19eez0002@iitrpr.ac.in (S.K. Vohra).

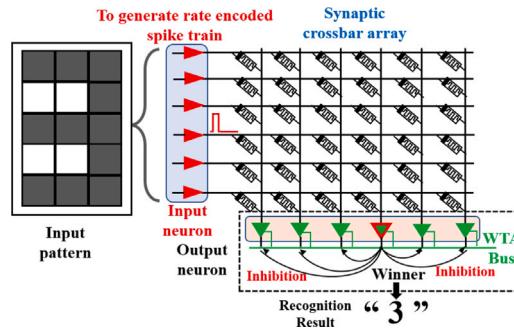


Fig. 1. The simplified architecture of SNN for pattern recognition comprising input layer LIF neurons, memristive crossbar and output layer LIF neurons with WTA mechanism.

approach is training the non-SNN first and then converting it to an SNN, which has several limitations in terms of accuracy loss and large inference latency [14]. The more efficient way is to do both training and classification in SNN hardware. As a result, doing the training on the implemented hardware for SNN (known as in-situ training) is the more power-efficient way. In view of this, a bio-plausible learning mechanism, spike-timing-dependent plasticity (STDP) can be used. It has been proved that STDP can be used to train the SNN in-situ without compromising parallelism [15,16]. Unlike gradient-descent based algorithms, in STDP, the weight updating information is provided to the synapse locally, thus eliminating the need of routing the information to the synapse through wires which consumes a significant amount of area on a chip [17].

The realization of neuromorphic circuits with memristive synapse have shown wider applications for low power and energy and area-efficient computing neuromorphic system-on-a-chip (NeuSoc) implementation. Many works [11,18,19] show the SNN architecture for pattern recognition applications using the SPICE model of the memristor, which cannot be used for real hardware implementation. Some works [20–22] have shown the hardware implementation of SNN using STDP learning. However, they have employed memristive devices, which require additional fabrication steps [23], making it difficult to integrate with standard CMOS circuit components in the same die. Thus, it requires extra chip-to-chip or die-to-die interconnects for connecting the separate RRAM ICs which induces more parasitics [24]. In contrast, we have used a CMOS-based memristor emulator exhibiting STDP characteristics that can be easily integrated with CMOS circuits in the same die. The varying threshold of the memristive devices, stochastic switching and variable resistance states put challenges on the memristive devices [25]. Also, these devices require long duration or high amplitude set-reset pulses for desired conductance change [26]. The low ON resistance (few k Ω s), which necessitates the power-hungry driver circuits and leads to high energy consumption by the synapses, is the major concern from the circuit design perspective [25,27]. In addition, unlike CMOS-based circuit components, memristive devices are yet not popular in standard CMOS technology PDK. Physical memristors as circuit components are not readily available for researchers in many domains except few commercial memristors with limited capability and stability [28]. As a result, while memristive device technology matures, CMOS-based memristive synapse circuits can be investigated for real-time hardware implementation of neuromorphic circuits. This helps bridge the gap between the concepts to the chip-scale realization of prototyping neuromorphic chips surpassing the challenges of the memristor device. CMOS implementation of neuromorphic circuits is shown in some works [29,30] where the weights are calculated on-chip. However, it requires additional digital circuits for complete weight processing, necessitating the complex interconnection to implement one synapse. Thus, losing the benefit of in-memory computation. In comparison, we have employed a much simpler CMOS memristor

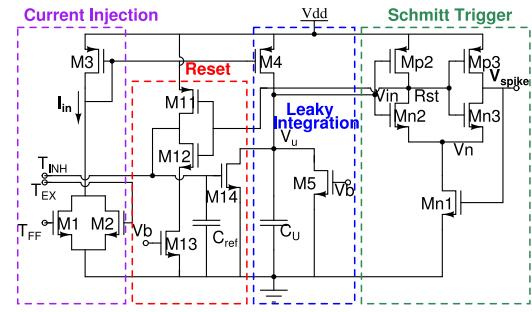


Fig. 2. CMOS circuit of LIF neuron. It comprises various sections for current injection, leaky integration, Schmitt trigger for firing and reset [2].

emulator circuit as a synapse in a crossbar that does not need any digital circuit for weight computation and storage. These challenges and limitations motivated us to design an SNN system with CMOS memristor emulators to get full insight into the circuit implementation challenges for memristive SNN based neuromorphic computing (NMC) system. Some latest research works have employed the CMOS based memristive synapses [24,28,31–33].

The main contributions of this work are:

1. A complete CMOS realized analog SNN system for pattern recognition is designed, integrating spiking LIF neurons and memristor crossbar array. Unlike many prior works which have used software-based memristor models, the proposed system employs a CMOS memristor emulator circuit with STDP characteristics in a crossbar.
2. The CMOS STDP synapse circuit is adapted to implement the modified STDP learning. The weight training method used in the proposed system does not involve the use of FPGAs, CPUs or GPUs. Also, it does not require any additional combinational or digital circuit attached to the synapse for programming and storing the synaptic weights.
3. The proposed system features the in-situ training and classification at CMOS transistor level, which is validated for pattern recognition of six images.
4. To demonstrate the versatility of the CMOS memristive synapse circuit, we have tuned the CMOS based STDP circuit by exploiting the rate-based Bienenstock–Cooper–Munro (BCM) learning characteristics for the heart rate classification.

The rest of the paper is organized as follows. Section 2 gives the detail of the LIF neuron circuit for converting the input pixel of an image into a spike train. Section 3 explains the STDP learning obtained using CMOS memristive STDP circuit. Section 4 explains the proposed CMOS based SNN system. Section 5 discusses the simulation, robustness and comparison with the other works. Section 6 contains the prospect for the used STDP circuit for heart rate classification application. The conclusion is drawn in Section 7.

2. LIF neuron circuit

In our SNN system, the low-power, low-complexity neuron circuit proposed in [18] is employed as a presynaptic and postsynaptic neuron. It contains a lateral inhibition interface, which is used for implementing the winner-take-all (WTA) mechanism (refer to Fig. 1) in SNN. In Fig. 2 input current I_{in} , (controlled by voltage given at input terminals T_{EX} and T_{FF}) is injected into the current integration section via the current mirror, which charges the capacitor C_u . When membrane voltage V_u reaches the neuron's threshold, the spike is generated with the help of the Schmitt trigger, and simultaneously Rst will be low, which turns on $M11$ and resets the voltage V_u through C_{ref} and $M14$. The circuit can also get reset through external pin T_{INH} . The switching voltage (V_{SV})

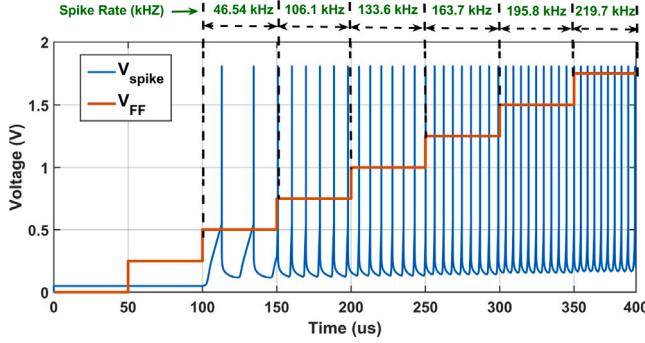


Fig. 3. Response of spiking LIF neuron to different input step voltages. Rate of spiking is increasing with each step of input voltage V_{FF} .

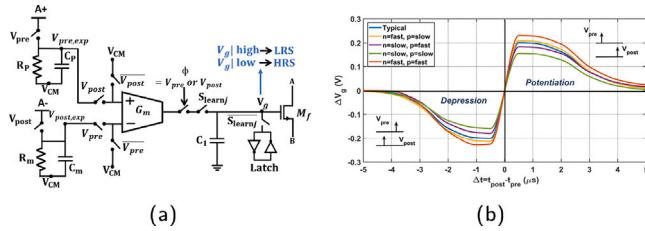


Fig. 4. (a) CMOS circuit of memristive STDP learning synapse. (b) STDP characteristic curve obtained from the synapse circuit for all process corners with parameters listed in Table 1.

of the Schmitt trigger [34] is the neuron's firing threshold, which can be calculated as

$$I_{Dn2} = \beta_{n2}(V_{SV} - V_n - V_{TH})^2 \quad (1)$$

$$I_{Dp2} = \beta_{p2}(V_{DD} - V_{SV} - |V_{tp}|)^2 \quad (2)$$

where $I_{Dn,p}$ is the drain current and $\beta_{n,p}$ represents the transconductance of transistor $M_{n,p}$. Now, equating (1) and (2), we get

$$V_{SW} = V_n + \frac{V_{DD} + V_T(1 - R) - V_n}{R + 1} \quad (3)$$

$$I_{Dn1} = \beta_{n1}(V_n - V_{TH})^2 \quad (4)$$

Equating (1) and (4), we get

$$V_n = \frac{V_{HL}}{R_n + 1} + V_{TH} \frac{R_n - 1}{R_n + 1} \quad (5)$$

After substituting (5) in (3), V_{SV} is given as

$$V_{SV} = V_{DD} \frac{R_n + 1}{R_n(R + 1) + 1} + V_{TH} \frac{R_n(2R - 1) - 1}{R_n(R - 1) + 1} \quad (6)$$

where $R = \sqrt{\frac{\beta_{n2}}{\beta_{p2}}}$; $R_n = \sqrt{\frac{\beta_{n1}}{\beta_{p2}}}$. Whenever the neuron's membrane voltage (V_u) reaches the switching voltage V_{SV} , neuron outputs a spike. The width of the spike can be controlled by the switching voltage of the Schmitt trigger given by (6).

Further, we have adapted this circuit to meet the desired requirements of our proposed CMOS based SNN system. The simulation result of the LIF circuit is shown in Fig. 3. It can be observed that the neuron will not generate spikes for input voltage $V_{FF} < 500$ mV (given at T_{FF}) and spiking rate is proportional to the input voltage for $V_{FF} > 500$ mV. This property is used to convert the input signal into rate encoded spike train.

3. Memristive synapse circuit featuring STDP learning mechanism

The phenomenon of STDP learning depends on the spike timing of presynaptic and postsynaptic neuron. It strengthens (weakens) the

Table 1
Circuit components and parameter values of STDP synapse.

Name	Values	Name	Values
$R_{p,m}$	10 MΩ	HRS	1.6 MΩ
$C_{p,m}, C_1$	0.1 pF, 0.6 pF	LRS	114 kΩ
A_+, A_-	1.8 V	G_m	18 μA/V
V_{CM}	900 mV	W/L_{M_f}	0.42/10 μ

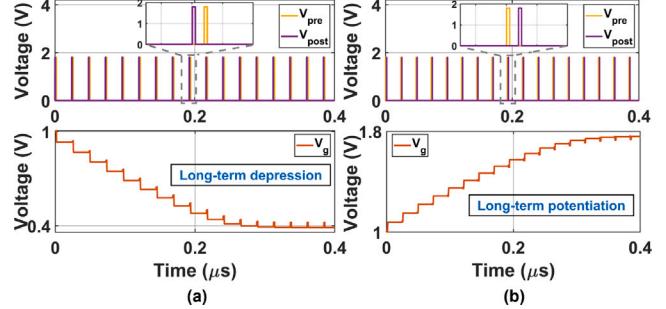


Fig. 5. Transient simulation of a single STDP synapse for (a) Long-term depression (LTD) and (b) long-term potentiation (LTP).

synaptic weight between two neurons if the presynaptic neuron fires earlier (later) than the postsynaptic neuron. Fig. 4(a) shows the compact memristive STDP learning circuit given in [33] which is used as a synapse for our proposed CMOS SNN system. The R_p , C_p and R_m , C_m shown in Fig. 4 implements the two exponential decay circuits (EDCs) for pre spike and post spike respectively. The post spike (pre spike) samples the $V_{pre,exp}$ ($V_{post,exp}$) trace and update the voltage at the positive (negative) terminal of the operational transconductance amplifier (OTA). The exponential traces are translated to the current through transconductance G_m , which will charge the capacitor C_1 when the switches (controlled by ϕ , S_{learnj}) are closed. The voltage V_g across C_1 is the state of the synapse and models the synaptic weight (W_s) by controlling the conductance (G) of transistor M_f as given by (7), (8)

$$G = K_n \frac{W}{L} (V_g - V_{CM} - V_{THn}) \quad (7)$$

$$W_s = G(V_g) \quad (8)$$

The synapse circuit is implemented in 180 nm CMOS technology with parameters given in Table 1. The values of $R_{p,m}$, $C_{p,m}$ have to be selected according to the spiking frequency of neurons so that it can show the synaptic plasticity for the frequency range of the LIF neurons. The simulated result of the synapse circuit shown in Fig. 4(b) verifies that the STDP learning curve is retained in all process corners. All postsynaptic spikes preceding (succeeding) presynaptic spikes with the delay $|\Delta t| < t_{max,pot}$ ($|\Delta t| < t_{max,dep}$) result in long-term potentiation (LTP) (Long-term depression (LTD)) as shown in Fig. 5. $t_{max,pot}$ and $|t_{max,dep}|$ are the maximum timing difference between presynaptic and postsynaptic spikes after which net change in weight (ΔW) is 0 for potentiation and depression respectively. LTP and LTD lead to the low resistance state (LRS) and high resistance state (HRS) of the STDP memristive synapse, respectively. Though the switches ϕ and S_{learnj} are opened after training to hold the capacitor stored charge, there will be leakage through the transistor and the charge over the capacitor will leak away with time. Therefore, latch (as shown in Fig. 4(a)) is used for long-term bistability of the synapse and weight quantization for binary states HRS and LRS [33].

In this paper, we have adapted this memristive synapse circuit for achieving the modified STDP learning [13]. In this modified learning rule, the change of the state depends on the rate of the input spike instead of the timing difference. The proposed circuit modification at the system level to achieve this learning is explained in Section 4.

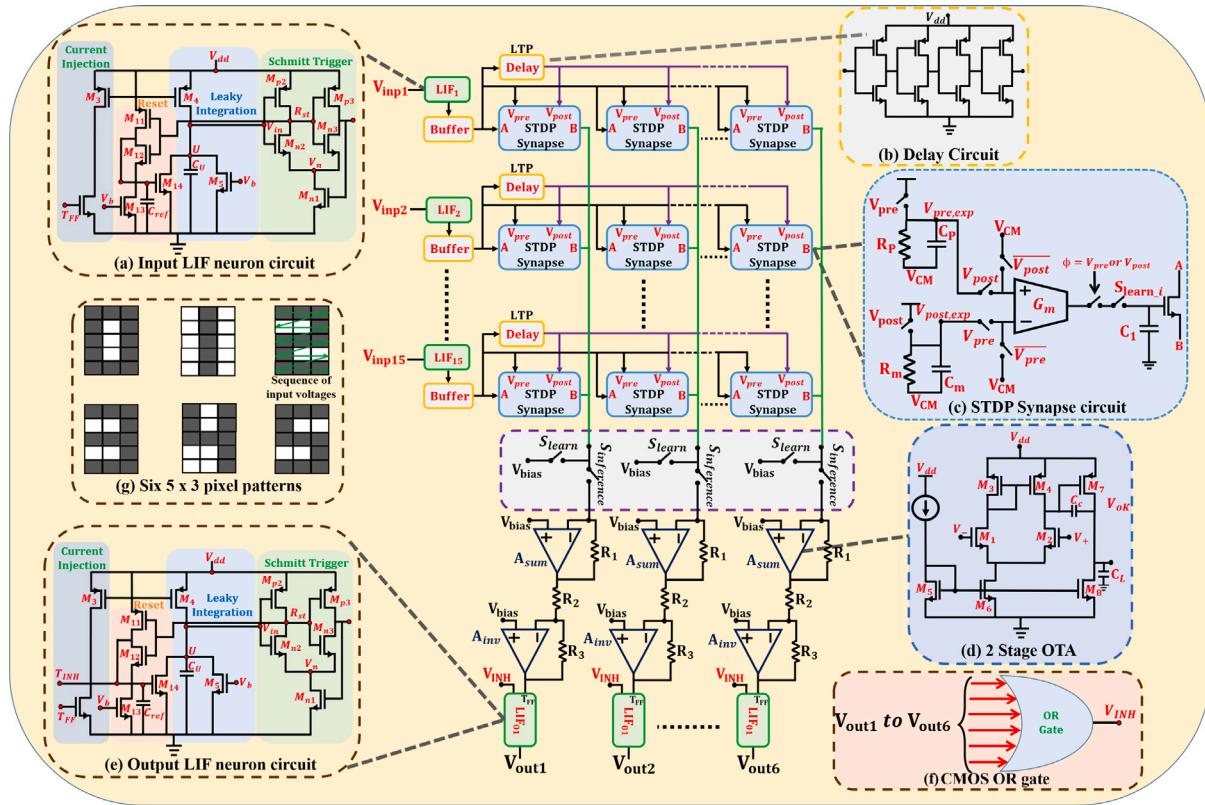


Fig. 6. The proposed CMOS based SNN system architecture combining 15 input LIF neurons, 15*6 memristive crossbar array and 6 output LIF neurons. (a) Input LIF neuron circuit. (b) Delay circuit designed for the delay of 1 μ s. (c) CMOS memristive STDP synapse circuit (d) 2-stage OTA used for summing the synaptic currents. (e) Output LIF neuron circuit with inhibitory interface. (f) OR gate for sending the inhibitory signal to output neurons. (g) six 5 X 3 pixels patterns for recognition.

4.1. The proposed circuit design for the modified STDP learning

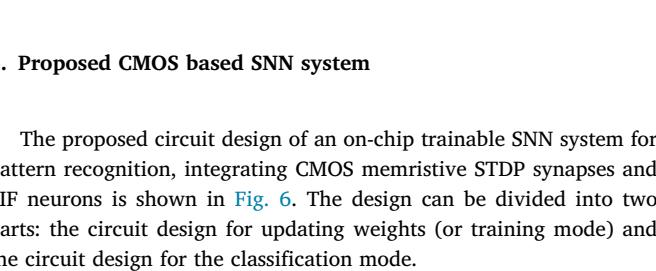
The long-term potentiation (LTP) obtained using the memristive STDP circuit is used to update the synaptic weights according to the input. During the training mode, switch $S_{inference}$ is open and switch S_{learn} is closed. Thus the output layer is disconnected from the synaptic crossbar resulting in the equivalent circuit shown in Fig. 7(a). The B terminal of each STDP synapse is biased at a constant voltage. Each STDP circuit in the crossbar will receive presynaptic spikes from the input layer LIF neuron. The postsynaptic spikes to the STDP circuit will be a delayed version of the presynaptic spikes given from the input LIF neuron. Initially, all the synaptic weights are set as slow or at HRS. As the modified STDP learning, the process of updating weight based on the input can be divided into two different situations

1. For a high value of the input (corresponding to a black pixel or a value greater than the threshold voltage of LIF neurons), spikes will be generated by the input LIF neuron. These spikes will act as presynaptic spikes to the STDP circuit. The delay unit will deliver these spikes to the STDP circuit's postsynaptic terminal with the delay Δt . Each postsynaptic spike will occur Δt seconds after the presynaptic spike. As a result, the weight change will increase monotonically with each postsynaptic spike that leads to LTP.
2. For a low value of the input (corresponding to a white pixel or a value less than the threshold voltage of the LIF neuron), no spike is generated from the input LIF neuron and the weight will remain unchanged or in HRS.

In the proposed training process using the modified STDP, a delay unit is added after each input neuron which ensures that whenever there is a positive rate presynaptic spikes, each postsynaptic spike occurs at a delay to the presynaptic spike. Hence, the weight increases and the state changes from HRS to LRS. This is the scenario shown in Fig. 5(b).

4. Proposed CMOS based SNN system

The proposed circuit design of an on-chip trainable SNN system for pattern recognition, integrating CMOS memristive STDP synapses and LIF neurons is shown in Fig. 6. The design can be divided into two parts: the circuit design for updating weights (or training mode) and the circuit design for the classification mode.



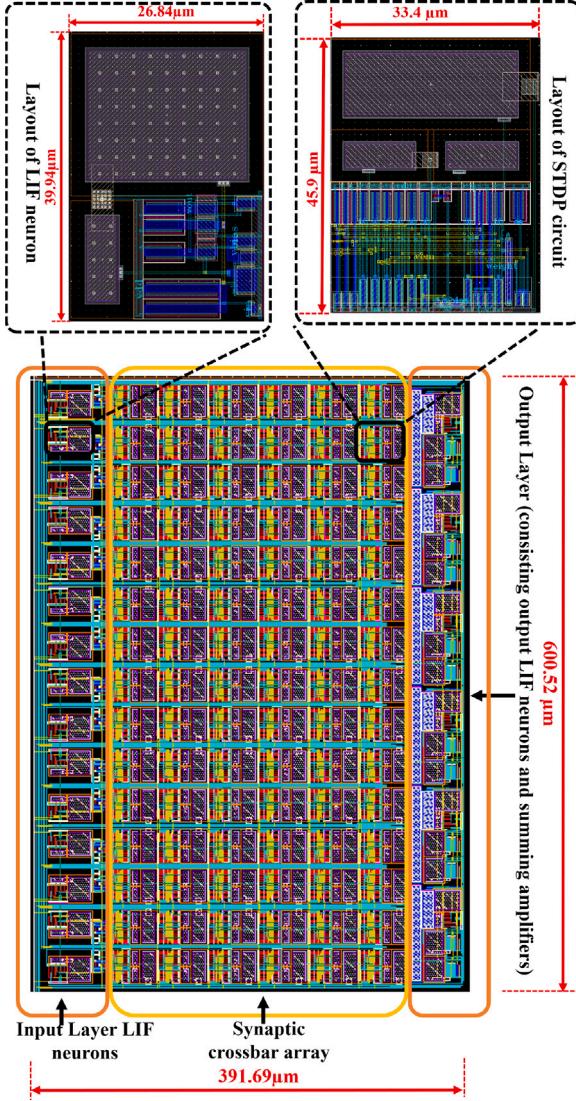


Fig. 8. Layout of the proposed CMOS based SNN system.

4.2. Circuit design of classification mode

During the inference Mode, switch $S_{inference}$ is closed and switch S_{learn} is open. The input layer is thus fully connected to the output layer through the synaptic crossbar, as shown in Fig. 7(b). The input corresponding to a pattern is given at the input neurons and processed with the synaptic crossbar. The weighted currents are summed column-wise and converted to a voltage using a summing amplifier (A_{sum}) and an inverter amplifier (A_{inv}). The output LIF neuron (i.e. the winner neuron) with the highest summed current will fire first and inhibit other neurons from firing. Unlike input layer LIF neurons, inhibitory interface (using V_{INH}) is required in output LIF neurons for implementing the winner-take-all (WTA) mechanism. Whenever a winner neuron fires, the output of an OR gate turns high which resets other neurons through inhibitory terminals (V_{INH}).

5. Simulation results

This section presents the post-layout simulation results of the proposed CMOS based SNN system for the training and classification mode. To validate the working of the proposed SNN circuit for pattern recognition, we have performed the image classification of six patterns

Table 2

Recognition rate for various noisy patterns.

Noise (%)	Total noisy patterns	Expected recognition rate from analytical results(%)	Recognition rate from circuit simulation(%)
0	$1 \times 6 = 6$	100	100
6.67	$15 \times 6 = 90$	77.8	77.8
13.3	$105 \times 6 = 630$	55.4	55.4
20.0	$455 \times 6 = 2730$	46.2	46.2

(‘0’, ‘1’, ‘2’, ‘3’, ‘4’, ‘5’) shown in Fig. 6(g). The layout of the complete system is shown in Fig. 8, which occupies area of $392 \times 600 \mu\text{m}^2$. Each pattern is a binary image of 5×3 pixels, requiring 15 input LIF neurons, 6 output LIF neurons, and the crossbar of 90 STDP synapse circuits for classification.

5.1. Training mode

The network is trained for each pattern sequentially and is in a configuration shown in Fig. 7(a). Initially, all the STDP synapses are in the high resistance state (HRS). The control signals applied during the training mode is shown in Fig. 9(a). All the synapses in the j th column will be trained in the j th learning cycle ($S_{learn-j}$, $j = 1$ to 6). As an example shown in Fig. 9(a), during high input of $S_{learn-3}$ if input pattern ‘2’ is given in the sequence (shown in Fig. 6(g)), the synaptic state of the STDP circuit in 1st row, 3rd column ($V_{g1,3}$) will increase according to STDP learning. Simultaneously, all other synaptic states of 3rd column will be updated ($V_{gi,3}$, $i = 1$ to 15) as illustrated in Fig. 9(b). The synaptic states ($V_{g1,3}$, $V_{g2,3}$, $V_{g3,3}$, $V_{g6,3}$, $V_{g7,3}$, $V_{g8,3}$, $V_{g9,3}$, $V_{g10,3}$, $V_{g13,3}$, $V_{g14,3}$, $V_{g15,3}$) emulated by the gate voltage of the floating transistor of the STDP circuit (refer to Fig. 4) increases (or the synaptic resistance decreases to LRS) while remaining states are in their initial HRS. The change in the synaptic states of other columns in j th learning cycle corresponding to the given pattern is also shown in Fig. 9(b). All the synapses in j th column will be trained in j th learning cycle parallelly, irrespective of the size of the image, and the number of learning cycles is equal to the number of output classes. Therefore, the training time will be the same for any size of image, but it will increase with the number of output classes.

5.2. Classification mode

After training the network for all patterns, each synaptic crossbar column ($j = 1$ to 6) will store the weights according to the corresponding pattern (0 to 5). Each pattern is presented to the network for $10 \mu\text{s}$. Only the winner neuron will fire when its corresponding pattern is given at the input while inhibiting the other neurons. Fig. 10 shows the firing response of the output LIF neurons, which confirms that each output neuron is able to recognize the corresponding pattern.

5.3. Robustness

In order to analyse the robustness of the proposed SNN system for pattern recognition of digits (‘0’, ‘1’, ‘2’, ‘3’, ‘4’, ‘5’), we have evaluated the recognition rate of the circuit for different noisy patterns. Also, we have considered the limitations of CMOS fabrication technology by adding process and temperature variations of all the circuit components in the architecture. The noise is added by inverting the pixel of the original pattern from 0 to 1 and vice versa in the percentage of 6.67%, 13.3% and 20% as done in [12]. We have tested all possible combinations of noisy patterns listed in Table 2. Taking the case of 13.3% noise patterns, i.e. change of 2 pixels in 5×3 pixel image, there are 105 cases of noisy patterns for one digit patterns and 630 cases for six digit patterns. Analytical results represent the ideal recognition rate in response to the noisy patterns. The recognition rate from the

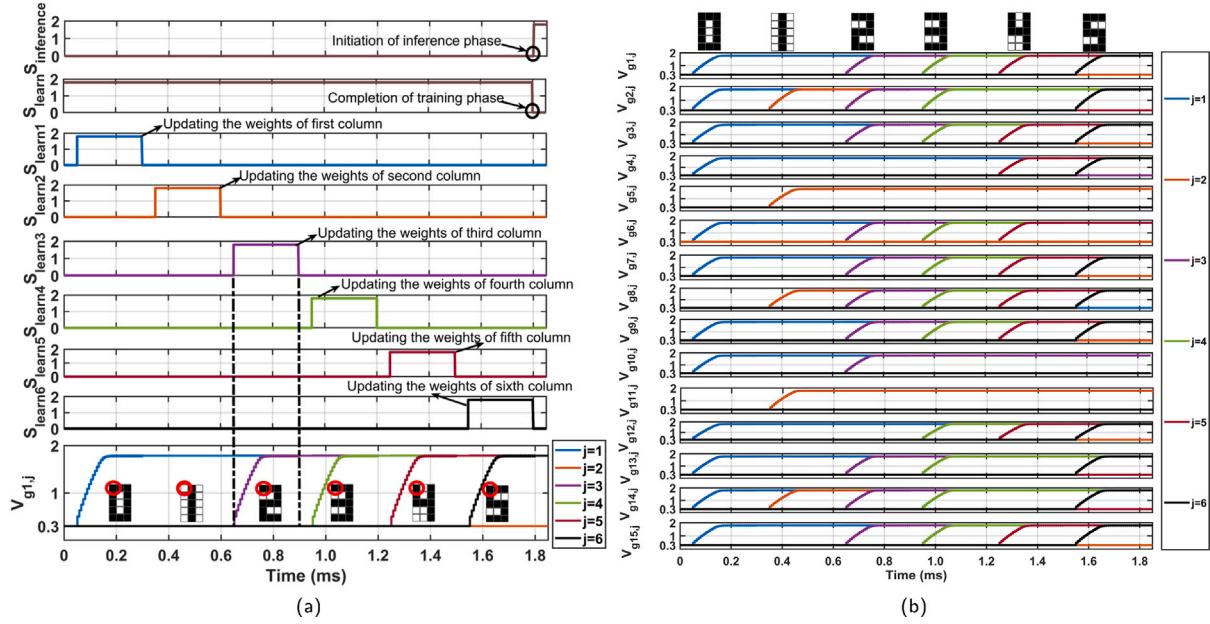


Fig. 9. Simulation results of training mode (a) Control signals for training each column's synapses sequentially. (b) Synaptic state change of all STDP memristors corresponding to the input pattern.

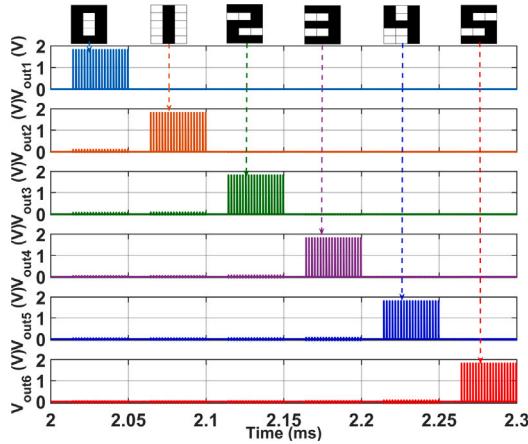


Fig. 10. Simulation result of classification mode.

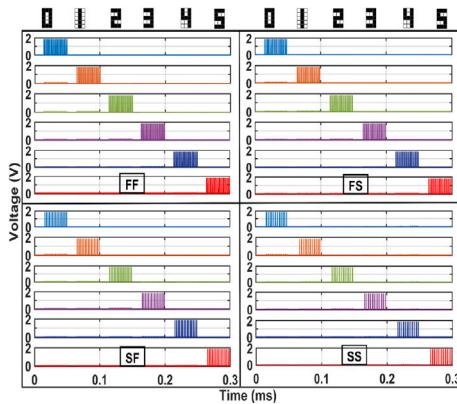


Fig. 11. Response of the system (i.e. firing of the output neurons) in classification mode for all extreme process corners at temperature = 27 °C.

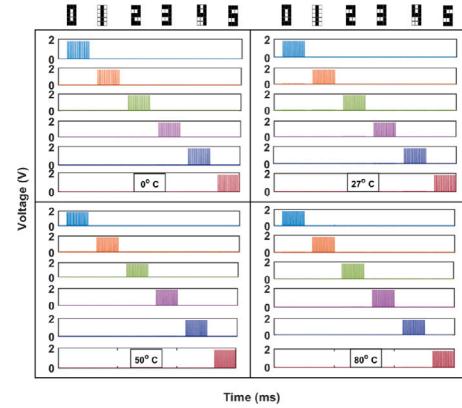


Fig. 12. Response of the output neurons in classification mode across different temperatures.

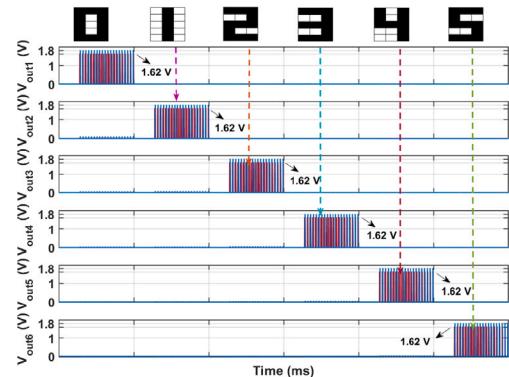


Fig. 13. Response of the system showing the robust firing of the output neurons with 10% variations in vdd (shown with red spikes) and $vdd = 1.8$ V (shown with blue spikes).

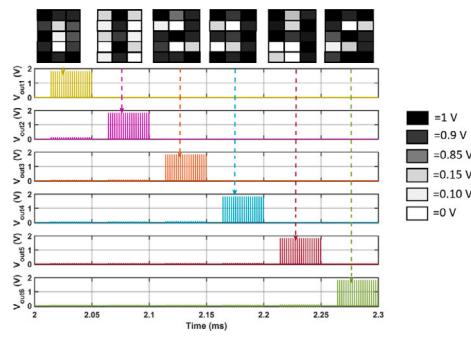


Fig. 14. Response of the system (i.e. firing of the output neurons) in classification mode for grey images of digit patterns.

simulation results incorporates all the non-idealities and challenges of the CMOS circuit design. Simulation results matching with recognition rate obtained from analytical results verify that despite all the CMOS non-idealities, the proposed CMOS-based SNN system is robust enough to match the analytical results and does not produce any additional error. Response of output neuron in classification mode shown in Fig. 11 verifies the correctness of the circuit under extreme process corners. Fig. 12 shows the firing response of the neurons for different temperatures, which validates the robustness of the complete system to recognize the patterns for different temperatures. The complete system was tested for 10% variations in the supply voltage. The response of the output neurons will remain unaffected only the magnitude of the spikes will change by 10% as shown in Fig. 13. Therefore, the system behaves accurately even in the presence of the supply voltage variations. The proposed CMOS-based SNN system is trained to bimodal weighted values, i.e. HRS and LRS. However, the trained system can not only recognize the 0-and-1 (black-and-white) binary images but can also recognize grey images having sufficient value differences in dark (black, black-grey) and light pixels (white, white-grey). As shown in Fig. 14, when the grey pattern is input to the binary-trained SNN system, the corresponding neuron is able to fire correctly. Each case of noisy pattern is also tested for process corners (SS, SF, FS, FF, TT) and different temperatures ($0\text{ }^{\circ}\text{C}$, $27\text{ }^{\circ}\text{C}$, $50\text{ }^{\circ}\text{C}$, $80\text{ }^{\circ}\text{C}$). The circuit is robust for process and temperature variations and also for the mismatches of the circuit components of the system (STDP synapses, output LIF neurons and op-amp), which is verified by Monte Carlo simulation. During the classification mode, the weighted sum input to the output LIF neurons decides the firing of the correct neuron. If there are mismatches in the output LIF neurons, and for the worst case, if there is a difference of only one pixel in the images of the trained crossbar, then there is a possibility that a wrong LIF neuron fires. In order to avoid that, we can scale the minimum difference of the input voltages (sum of weighted inputs) of the winner neuron and the other neuron (corresponding to the worst case of one pixel difference) by tuning the values of R_1 , R_2 and R_3 in Fig. 6. In our proposed system, we have kept it around 100 mV. As shown in Table 2, the recognition rate of the circuit-based simulations matches closely with the analytical results using MATLAB. This depicts the robustness of the circuit for noisy patterns in the presence of process and temperature variation. The results prove the robustness of the circuit for PVT variations, mismatches and noisy images.

5.4. MNIST data recognition

In order to check the proposed SNN system for practical data set, we have downscaled the MNIST greyscale images to binarised 14×14 pixel size images in MATLAB as shown in Fig. 15. While the MATLAB was used to fetch the MNIST data and downscaling it to lower pixel size, all the training and inference simulations are performed on the

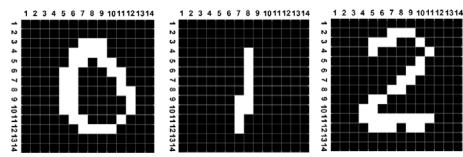


Fig. 15. MNIST downscaled binarised images of 14×14 pixels.

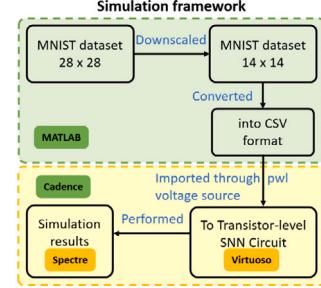


Fig. 16. Flowchart of the simulation framework adopted for MNIST classification.

designed full CMOS circuit of SNN using Cadence tool as shown in Fig. 16. Ten images corresponding to each digit pattern '0', '1', and '2' are used to train the synaptic weights of the 196×3 crossbar array. The weights will eventually stabilize to the desired binary states after several training data. The system's accuracy evaluated for thirty testing images was estimated to be 91%. The reduced accuracy is due to the smaller crossbar size and limited data set used to train the crossbar array. The smaller data set is taken because of the computational resource and time restriction on circuit-level simulations.

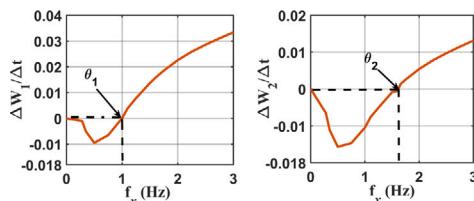
5.5. Comparison and discussion

This paper presents the full CMOS-based transistor level implementation of SNN for pattern recognition with memristive STDP synapses which makes it different from other existing literature listed in Table 3. Authors in [18] have proposed the hardware architecture using spiking LIF neurons and synaptic circuits. However, they have used the SPICE model of the memristor in their simulations. Also, the weights were calculated in an ex-situ fashion and were mapped to the memristive crossbar using digital pulses. This makes the use of an extra circuit to read/write a weight value from/to a synaptic circuit. In view of this, our work implements in-situ learning avoiding the use of any additional circuit overhead. In paper [19,33], SNN is designed for digit recognition using in-situ STDP learning which requires a teacher signal for each output neuron. However, in our designed SNN circuit for digit recognition, no involvement of an external signal is required. The WTA mechanism implemented in [19,33] requires a bus interface circuit made of digital gates and D-FFs. In contrast, the employment of LIF neurons [18] in the output layer, which have an inhibitory interface, has aided in achieving the WTA mechanism discussed in section 4.2 in a more straightforward manner. Our system uses only a CMOS OR gate with output neurons to perform the inhibition. In [33], CMOS based memristor circuit with STDP learning is proposed but simulated using memristive synapse and WTA neuron macro models using brian2 libraries in Python. In [13], instead of taking any SPICE model of the memristor, a fabricated PCMO based memristive device is used. However, full SNN hardware was not implemented in one chip. Also, it requires the use of FPGA as a controlling unit. In comparison, our proposed work does not require FPGA and gives the on-chip design of SNN for pattern recognition that can be integrated in one chip on the same die. For the same patterns taken in [12], the total energy consumed by the CMOS memristive STDP synapses is 56.49 pJ which is significantly less than the work [12]. The reason lies in the low R_{ON}

Table 3

Comparison of Circuit Implementation of Different Memristive Crossbar-Based Neural Network Circuits.

	Shamshi et al. TVLSI, 2018 [18]	X. Wu et al. JETCAS, 2015 [19]	V. Saxena et al. ISCAS, 2018 [33]	M. Chu et al. TIE, 2015 [13]	C. Pan et al. TCAD, 2021 [35]	Y. Jiang et al. TCAS I, 2018 [12]	This work
Type of memristor	Yakopcic SPICE model	Yakopcic SPICE model	STDP synapse circuit	Fabricated memristive device	Memristor model	Fabricated RRAM array	CMOS STDP synapse circuit
Training type	STDP, ex-situ	STDP, in-situ	STDP, in-situ	Modified STDP learning	Hebbian, ex-situ	ex-situ	Modified STDP, in-situ
Type of data for updating memristor weight	Programming memristor using digital pulses	Spikes	Spikes	Digital pulses of ± 3 V	Set and reset pulses	Set and reset pulses	Spikes
WTA mechanism	–	Bus interface circuit made of digital gates and D-FF	Bus interface circuit made of digital gates and D-FF	Control logic	–	A threshold controller circuit	Using a CMOS OR gate
Image size/no. of patterns	$(5 \times 5)/4$	$(8 \times 8)/10$	$(8 \times 8)/10$	$(5 \times 6)/10$	$(3 \times 3)/3$	$(5 \times 3)/6$	$(5 \times 3)/6$
No. of synapse in crossbar	100	640	640	300	27	90	90
Average energy consumed by synapses	–	–	–	–	–	$0.31 \mu\text{J}$	56.49 pJ
Training time for one pattern	5 s	7 ms	–	–	0.49 s	2 μs	100 μs
Full CMOS transistor level circuit implementation	Not implemented (used memristor model)	Not implemented (used memristor model)	Not implemented (simulated using memristive synapse and WTA neuron macro-models using Brian2 libraries in python)	Hardware implementation using memristor crossbar array in one chip, FPGA and LIF neurons integrated in another chip	Not implemented (used memristor model), used MATLAB for training	Hardware implementation using memristor crossbar array in one chip, FPGA and LIF neurons integrated in another chip	Full CMOS transistor level circuit implementation of system

**Fig. 17.** BCM learning curve of the nearest-neighbour pair-based STDP circuit with different thresholds ($\theta_1 = 1$ Hz, $\theta_2 = 1.667$ Hz).

resistance and longer inference time required in the RRAM synapses than in the CMOS memristive synapses. Furthermore, the training time needed to adjust the weights corresponding to a single pattern is significantly less than the works tabulated in [Table 3](#) for on-chip training.

6. Prospect

Although the proposed CMOS SNN system is used for pattern recognition of six digits, it can also be used for visual pattern recognition. The complete neuromorphic system for visual pattern recognition will contain CMOS photoreceptor which converts optical data into a spike train. The generated spike train will be input to the memristive neural network for recognition.

In view of the CMOS STDP circuit used in this paper, we have also applied it to demonstrate the heart rate classification. We have explored this circuit to obtain Beinenstock–Cooper–Munro (BCM) characteristics for rate-based learning other than timing based learning. Unlike spike-timing (STDP) based learning, BCM learning modifies the synaptic weights based on pre and postsynaptic spike frequencies. It has been

Table 4

Parameters Used for Different Threshold BCM Learning.

Parameter	θ_1 (For 60 BPM)	θ_2 (For 120 BPM)
A_+	0.267	0.19
τ_+	0.7	0.7
A_-	0.175	0.138
τ_-	1.7	1.7

reported that by limiting the interaction of pre and postsynaptic spikes to the nearest-neighbour spike interaction only, BCM learning can be replicated from pair-based STDP learning circuit [36,37]. The synaptic weight change is determined by the threshold frequency θ , if postsynaptic firing rate $f_x < \theta$, depression occurs (change in synaptic weight is negative), if firing rate $f_x > \theta$, potentiation occurs (change in synaptic weight is positive). The threshold frequency between potentiation and depression (at which the rate change of the synaptic weight is zero) is given by (9), where A_+, A_-, τ_+, τ_- are the parameters of the STDP curve [36];

$$\theta = -\frac{A_+/\tau_+ + A_-/\tau_-}{A_+ + A_-} \quad (9)$$

In rested condition, the lower and the upper safe limits of heart rate (in beats per minute) are 60 bpm and 100 bpm, which corresponds to 1 Hz and 1.667 Hz respectively. The two BCM curves corresponding to θ_1, θ_2 are shown in [Fig. 17](#), which are obtained by optimizing the two STDP circuits for parameters listed in [Table 4](#). The classifier (containing two BCM learning enabled STDP circuits) has been tested with ECG data sets taken from PhysioBank ATM. $\Delta W_1, \Delta W_2$ correspond to the weight change observed in STDP circuit tuned for $\theta_1 = 1$ Hz and $\theta_2 = 1.667$ Hz respectively. The input spike data is generated in MATLAB by detecting the Q peaks from the ECG signal. Based on the rate of weight change

Table 5
Heart Rate Classification output for ECG Database.

S. No.	Actual Heart Rate (bpm)	Δw_1 (For 60 bpm)	Δw_2 (For 100 bpm)	Classifier output
1	70.36	5.783×10^{-3}	-6.416×10^{-3}	NORMAL
2	82.15	1.073×10^{-2}	-2.966×10^{-3}	NORMAL
3	87.42	1.275×10^{-2}	-1.546×10^{-3}	NORMAL
4	96.84	1.601×10^{-2}	-7.544×10^{-4}	NORMAL
5	56.00	-1.642×10^{-3}	-1.154×10^{-2}	LOW
6	43.06	-7.143×10^{-3}	-1.501×10^{-2}	LOW
7	134.87	2.582×10^{-2}	7.722×10^{-3}	HIGH
9	108.42	1.952×10^{-2}	3.239×10^{-3}	HIGH
1	106.72	1.903×10^{-2}	2.895×10^{-3}	HIGH
10	51.2	-3.708×10^{-3}	-1.288×10^{-2}	LOW

the proposed heart rate classifier correctly classifies the ECG database (present on PhysioBank ATM) as shown in **Table 5**. The classified rate is normal if potentiation is seen in ΔW_1 (positive value of ΔW_1) and depression in ΔW_2 (negative value of ΔW_2).

7. Conclusion

This paper presents the complete CMOS based transistor-level implementation of SNN for pattern recognition. It integrates 15 input CMOS LIF neurons, a crossbar array of 90 CMOS memristive synapse circuits and 6 output LIF neurons for classification of six 5×3 pixel images. This system embeds on-chip training and classification using modified STDP mechanism and WTA property. The designed CMOS based SNN system is validated with the post-layout simulation results for the training and classification of six patterns. The proposed circuit is shown to be robust for PVT variations and mismatches. Moreover, the recognition rate obtained from the circuit simulation under noisy patterns matches the analytical results, proving the accuracy of the proposed CMOS-based SNN circuit. Other than the timing based STDP learning, rate-based learning is also explored using the same pair-based STDP circuit and shown its application for heart rate classification by obtaining the BCM characteristics of the STDP circuit.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

Acknowledgements

The authors thank Ministry of Education (MoE), India, MeitY, India and SERB, India, India for providing institute fellowship, availing the tools through SMDP-C2S project Grant no. :CRG/2021/007283 and project funding, respectively.

References

- [1] A. Basu, L. Deng, C. Frenkel, X. Zhang, Spiking neural network integrated circuits: a review of trends and future directions, in: 2022 IEEE Custom Integrated Circuits Conference, CICC, IEEE, 2022, pp. 1–8.
- [2] J. Shamsi, K. Mohammadi, S.B. Shokouhi, Columnar-organized memory (COM): Brain-inspired associative memory with large capacity and robust retrieval, Biol. Inspired Cognit. Archit. 20 (2017) 39–46.
- [3] C. Zhao, Y. Yi, J. Li, X. Fu, L. Liu, Interspike-interval-based analog spike-time-dependent encoder for neuromorphic processors, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 25 (8) (2017) 2193–2205.
- [4] O. Krestinskaya, A.P. James, L.O. Chua, Neuromemristive circuits for edge computing: A review, IEEE Trans. Neural Netw. Learn. Syst. 31 (1) (2019) 4–23.
- [5] B. Rajendran, F. Alibart, Neuromorphic computing based on emerging memory technologies, IEEE J. Emerg. Sel. Top. Circuits Syst. 6 (2) (2016) 198–211.
- [6] B. Rajendran, A. Sebastian, M. Schmuker, N. Srinivasa, E. Eleftheriou, Low-power neuromorphic hardware for signal processing applications: A review of architectural and system-level design approaches, IEEE Signal Process. Mag. 36 (6) (2019) 97–110.
- [7] D. Negrov, I. Karandashev, V. Shakirov, Y. Matveyev, W. Dunin-Barkowski, A. Zenkevich, An approximate backpropagation learning rule for memristor based neural networks using synaptic plasticity, Neurocomputing 237 (2017) 193–199.
- [8] Y. Zhang, X. Wang, E.G. Friedman, Memristor-based circuit design for multilayer neural networks, IEEE Trans. Circuits Syst. I. Regul. Pap. 65 (2) (2017) 677–686.
- [9] J. Shi, Z. Zeng, Design of in-situ learning bidirectional associative memory neural network circuit with memristor synapse, IEEE Trans. Emerg. Top. Comput. Intell. 5 (5) (2020) 743–754.
- [10] F. Alibart, E. Zamanidoost, D.B. Strukov, Pattern classification by memristive crossbar circuits using ex situ and in situ training, Nat. Commun. 4 (1) (2013) 2072.
- [11] C. Yakopcic, R. Hasan, T.M. Taha, Memristor based neuromorphic circuit for ex-situ training of multi-layer neural network algorithms, in: 2015 International Joint Conference on Neural Networks, IJCNN, IEEE, 2015, pp. 1–7.
- [12] Y. Jiang, P. Huang, D. Zhu, Z. Zhou, R. Han, L. Liu, X. Liu, J. Kang, Design and hardware implementation of neuromorphic systems with RRAM synapses and threshold-controlled neurons for pattern recognition, IEEE Trans. Circuits Syst. I. Regul. Pap. 65 (9) (2018) 2726–2738.
- [13] M. Chu, B. Kim, S. Park, H. Hwang, M. Jeon, B.H. Lee, B.G. Lee, Neuromorphic hardware system for visual pattern recognition with memristor array and CMOS neuron, IEEE Trans. Ind. Electron. 62 (4) (2014) 2410–2419.
- [14] P.U. Diehl, D. Neil, J. Binas, M. Cook, S.C. Liu, M. Pfeiffer, Fast-classifying, high-accuracy spiking deep networks through weight and threshold balancing, 2015 International Joint Conference on Neural Networks, IJCNN, IEEE, 2015, pp. 1–8.
- [15] P.U. Diehl, M. Cook, Unsupervised learning of digit recognition using spike-timing-dependent plasticity, Front. Comput. Neurosci. 9 (2015) 99.
- [16] B. Nessler, M. Pfeiffer, L. Buesing, W. Maass, Bayesian computation emerges in generic cortical microcircuits through spike-timing-dependent plasticity, PLoS Comput. Biol. 9 (4) (2013) e1003037.
- [17] E. Covi, E. Donati, X. Liang, D. Kappel, H. Heidari, M. Payvand, W. Wang, Adaptive extreme edge computing for wearable devices, Front. Neurosci. 15 (2021) 611300.
- [18] J. Shamsi, K. Mohammadi, S.B. Shokouhi, A hardware architecture for columnar-organized memory based on CMOS neuron and memristor crossbar arrays, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 26 (12) (2018) 2795–2805.
- [19] X. Wu, V. Saxena, K. Zhu, Homogeneous spiking neuromorphic system for real-world pattern recognition, IEEE J. Emerg. Sel. Top. Circuits Syst. 5 (2) (2015) 254–266.
- [20] G. Pedretti, V. Milo, S. Ambrogio, R. Carboni, S. Bianchi, A. Calderoni, N. Ramaswamy, A.S. Spinelli, D. Ielmini, Memristive neural network for on-line learning and tracking with brain-inspired spike timing dependent plasticity, Sci. Rep. 7 (1) (2017) 1–10.
- [21] I. Boybat, M. Le Gallo, S.R. Nandakumar, T. Moraitis, T. Parnell, T. Tuma, B. Rajendran, Y. Leblebici, A. Sebastian, E. Eleftheriou, Neuromorphic computing with multi-memristive synapses, Nat. Commun. 9 (1) (2018) 2514.
- [22] L. Zhao, Q. Hong, X. Wang, Novel designs of spiking neuron circuit and STDP learning circuit based on memristor, Neurocomputing 314 (2018) 207–214.
- [23] N. Dey, J. Sharda, U. Saxena, D. Kaushik, U. Singh, D. Bhowmik, On-chip learning in a conventional silicon MOSFET based analog hardware neural network, in: 2019 IEEE Biomedical Circuits and Systems Conference, BioCAS, IEEE, 2019, pp. 1–4.
- [24] S.A. Thomas, S.K. Vohra, R. Kumar, R. Sharma, D.M. Das, Analysis of parasitics on CMOS based memristor crossbar array for neuromorphic systems, in: 2021 IEEE International Midwest Symposium on Circuits and Systems, MWSCAS, IEEE, 2021, pp. 309–312.
- [25] V. Saxena, High LRS-resistance CMOS memristive synapses for energy-efficient neuromorphic SoCs, in: 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems, MWSCAS, IEEE, 2019, pp. 1143–1146.

- [26] V. Milo, E. Chicca, D. Ielmini, Brain-inspired recurrent neural network with plastic RRAM synapses, in: 2018 IEEE International Symposium on Circuits and Systems, ISCAS, IEEE, 2018, pp. 1–5.
- [27] C. Mohan, L.A. Camuñas-Mesa, M. José, E. Vianello, T. Serrano-Gotarredona, B. Linares-Barranco, Neuromorphic low-power inference on memristive crossbars with on-chip offset calibration, *IEEE Access* 9 (2021) 38043–38061.
- [28] C. Yang, S.P. Adhikari, H. Kim, On learning with nonlinear memristor-based neural network and its replication, *IEEE Trans. Circuits Syst. I. Regul. Pap.* 66 (10) (2019) 3906–3916.
- [29] N. Qiao, H. Mostafa, F. Corradi, M. Osswald, F. Stefanini, D. Sumislawski, G. Indiveri, A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128K synapses, *Front. Neurosci.* 9 (2015) 141.
- [30] G. Indiveri, B. Linares-Barranco, T.J. Hamilton, A.V. Schaik, R. Etienne-Cummings, T. Delbrück, S.C. Liu, P. Dudek, P. Häfliger, S. Renaud, J. Schemmel, Neuromorphic silicon neuron circuits, *Front. Neurosci.* 5 (2011) 73.
- [31] V. Saxena, A compact CMOS memristor emulator circuit and its applications, in: 2018 IEEE 61st International Midwest Symposium on Circuits and Systems, MWSCAS, IEEE, 2018, pp. 190–193.
- [32] S.K. Vohra, S. Thomas, M. Sakare, D.M. Das, Full CMOS implementation of bidirectional associative memory neural network with analog memristive synapse, in: 2021 IEEE International Midwest Symposium on Circuits and Systems, MWSCAS, IEEE, 2021, pp. 445–448.
- [33] V. Saxena, X. Wu, K. Zhu, Energy-efficient CMOS memristive synapses for mixed-signal neuromorphic system-on-a-chip, in: 2018 IEEE International Symposium on Circuits and Systems, ISCAS, IEEE, 2018, pp. 1–5.
- [34] S.F. Al-Sarawi, Low power schmitt trigger circuit, *Electron. Lett.* 38 (18) (2002) 1.
- [35] C. Pan, Q. Hong, X. Wang, A novel memristive chaotic neuron circuit and its application in chaotic neural networks for associative memory, *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* 40 (3) (2020) 521–532.
- [36] E.M. Izhikevich, N.S. Desai, Relating stdp to bcm, *Neural Comput.* 15 (7) (2003) 1511–1523.
- [37] M.R. Azghadi, S. Al-Sarawi, N. Iannella, D. Abbott, Design and implementation of BCM rule based on spike-timing dependent plasticity, in: The 2012 International Joint Conference on Neural Networks, IJCNN, IEEE, 2012, pp. 1–7.