Neuromorphic Hardware System for Visual Pattern Recognition With Memristor Array and CMOS Neuron

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***Abstract*—This paper presents a neuromorphic system for visual pattern recognition realized in hardware. A new learning rule based on modified spike-timing-dependent plasticity is also presented and implemented with passive synaptic devices. The system includes an artificial photoreceptor, a $Pr_{0.7}Ca_{0.3}MnO_3$-based memristor array, and CMOS neurons. The artificial photoreceptor consisting of a CMOS image sensor and a field-programmable gate array converts an image into spike signals, and the memristor array is used to adjust the synaptic weights between the input and output neurons according to the learning rule. A leaky integrate-and-fire model is used for the output neuron that is built together with the image sensor on a single chip. The system has 30 input neurons that are interconnected to 10 output neurons through 300 memristors. Each input neuron corresponding to a pixel in a 5 × 6 pixel image generates voltage pulses according to the pixel value. The voltage pulses are then weighted and integrated by the memristors and the output neurons, respectively, to be compared with a certain threshold voltage above which an output neuron fires. The system has been successfully demonstrated by training and recognizing number images from 0 to 9.**

***Index Terms*—Complimentary metal–oxide–semiconductor (CMOS) image sensor, leaky integrate-and-fire (I–F) neurons, memristor, neural network, neuromorphic, pattern recognition, spike-timing-dependent plasticity (STDP).**

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I. Introduction

An artificial neural network (ANN) is a computational model inspired by the neocortex of human brain that is capable of solving a variety of problems in recognition, prediction, optimization, and control [1]–[4]. It can be also described as a network of synaptically connected neurons that can create, modify, and preserve information through sequential learning procedures. The hardware implementation of spiking neural networks has been an active research field, and recent publications [5]–[8] have proven the feasibility of applying neural networks for some industrial applications such as the signal processing of complex data sets.

Recent developments in CMOS technology allow the large-scale integration of integrate-and-fire (I&F) neurons on a single chip [9]–[12]. However, the CMOS implementation of synaptic circuits requires a large number of transistors and a considerable amount of power consumption [13]–[15]. A lot of efforts have been made to develop a passive device that behaves similar to a synapse, and recently, such a device, which is called a memristor (memory + resistor), has been invented and successfully used as a synapse [16]–[19]. In [16], a synaptic device consisting of a memristor bridge and transistors is proposed, and the work in [17] explains a multilayer neural network employing the synaptic device in [16]. In [18] and [19], a weight change rule based on an average firing rate of prespike and postspike is proposed and simulated with a simple I&F neuron and memristor. However, most of the neuromorphic systems utilizing the memristor, including [16]–[19], have been implemented in software and only verified with simulations. For example, instead of using a physical memristor device, a TiO_2 memristor model proposed by Hewlett-Packard Company [20] was used in [16] and [17], and a simple variable resistor model was used in [18] and [19].

The motivation of this paper is suggesting the possibility of implementing a neuromorphic hardware system employing a physical memristor device by utilizing the proposed learning rule. Shown in Fig. 1 is the proposed neuromorphic system for visual pattern recognition that is implemented on hardware with a CMOS image sensor (CIS), a signal processing unit (SPU), a memristor array, and CMOS neurons. An image is taken by the CIS, and the image data are processed to generate a spike signal by the SPU, which is implemented in a field-programmable gate array. The spike signal is used to either strengthen or weaken

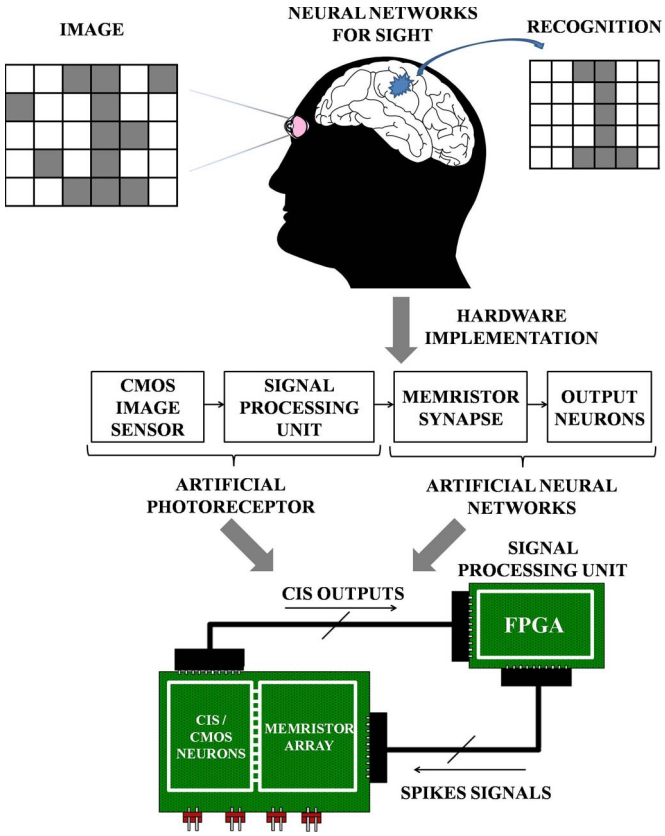

Fig. 1. Proposed neuromorphic system for visual pattern recognition.

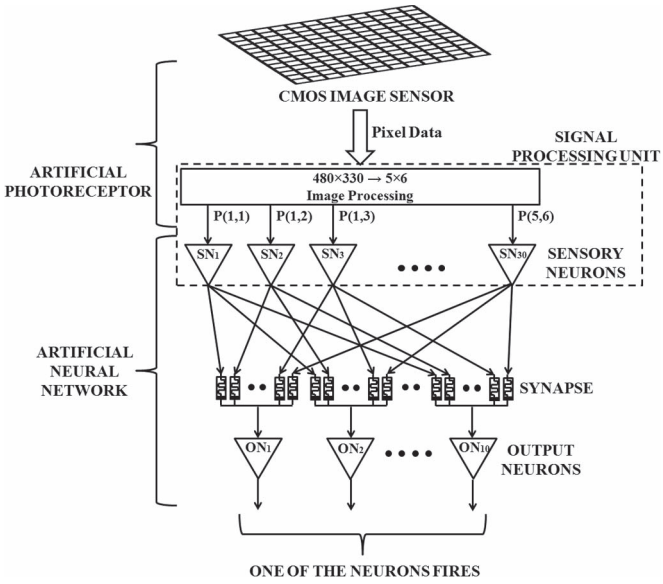

Fig. 2. Block diagram of the neuromorphic system.

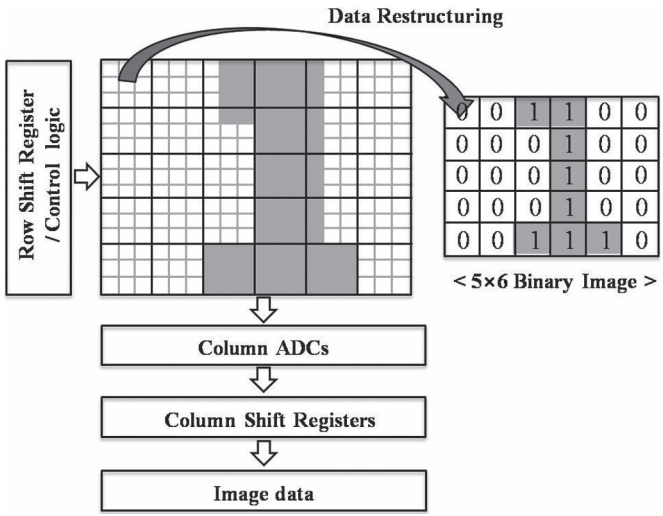

Fig. 3. Block diagram of the CIS and image restructuring process.

the synaptic connections between sensory (or input) and output neurons according to the proposed learning rule. Synapses are implemented with a memristor array [21], and a leaky I&F neuron model is used for the output neuron, which is implemented with CMOS circuits. As a demonstration, the system was tested with number images from 0 to 9.

The rest of this paper is organized as follows. Section II introduces the proposed system with detailed explanations of important building blocks in the system. The system's operation and proposed learning rule are explained in Section III. Experimental results are presented in Section IV, and conclusions have been drawn in Section V.

II. Proposed System

As shown in Fig. 2, the system can be divided into two main functional blocks. The first block consisting of the CIS and the SPU works as an artificial photoreceptor, and the second block is a single-layer ANN including 10 output neurons and 300 memristors for the synaptic interconnections between the sensory and output neurons. In the following sections, the artificial photoreceptor, the memristor, and the output neuron will be discussed in detail.

A. Artificial Photoreceptor

A photoreceptor is a special neuron that can convert light into a spike signal. The CIS and the SPU work together as an artificial photoreceptor in the system. As shown in Fig. 3, the CIS contains a 480 × 330 pixel array, analog-to-digital converters (ADCs), control logic, and row and column shift registers. Each pixel consisting of a photo diode and four transistors generates an analog signal whose amplitude is proportional to the light intensity, and the analog signal gets converted into a 10-b digital code by the column ADC. The SPU restructures a 480 × 330 pixel image out of the CIS into a 5 × 6 pixel binary image by mapping 96 × 55 neighborhood pixels into one pixel in the binary image. The SPU calculates the local average of 96 × 55 pixels' digital output and compares it with the global average of the entire pixel. If the local average is greater than the global average, the corresponding pixel value in the binary image is set to "1"; otherwise, it is set to "0." With a pixel value of 1, the SPU, which is also working as a sensor neuron, will generate spikes, and no spike will be generated with 0.

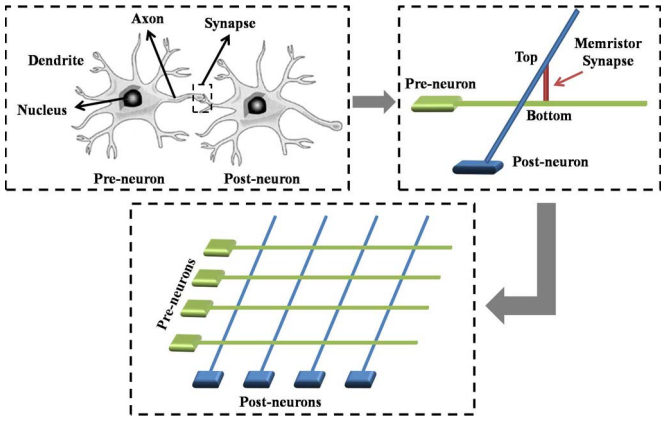

Fig. 4. Memristor array for synaptic connections.

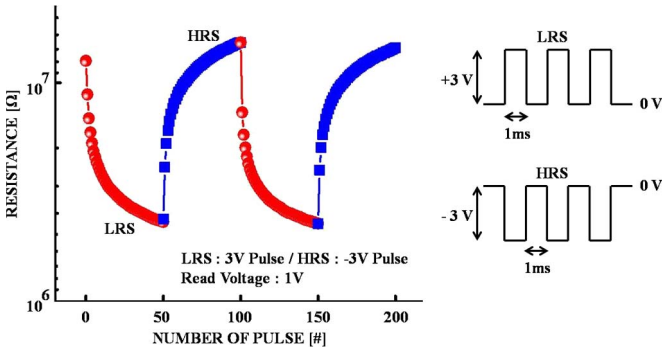

Fig. 5. Memristance versus pulse counts.

B. Memristor as Synapse

A memristor is a two-terminal passive device that modifies or retains its resistance according to the time integral of the current flowing through it [22]. It has been shown that a synaptic weight can be modeled with the memristor's resistance (memristance), and various types of memristors have been reported recently [23].

In this paper, as shown in Fig. 4, synapses are implemented with a crossbar array of $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO)-based memristors. The memristor, which is formed in each cross point of the array, is built with multiple layers of Pt/TiN$_x$/PCMO/Pt. Pt is used to generate both top and bottom electrodes, and a thin layer of TiON, which is generated between TiN$_x$ and PCMO, changes its oxidation rate according to the bias voltage across the top and bottom electrodes, causing the memristance change. The memristor only changes its memristance if a voltage pulse whose amplitude is greater than a certain threshold voltage is applied to it. The threshold voltage, which is controlled by the thickness of the PCMO layer, was set to about 1.2 V. Fig. 5 shows the measured memristance versus pulse counts. With positive pulses (+3 V), the memristance abruptly drops at the first couple of pulses and then gradually decreases until it is saturated to a minimum value or a low-resistance state (LRS). The memristance increases in a similar way with negative pulses (−3 V) and reaches its maximum called the high-resistance state (HRS).

Spike-timing-dependent plasticity (STDP) has been modified and applied to update the memristance. In STDP [24], as shown in Fig. 6, the synaptic weight exponentially changes according to the arrival time difference between the presynaptic and postsynaptic spikes (Δt). The weight change function, i.e., ΔW, can be given as follows:

$$\Delta W(\Delta t) = \begin{cases} W_+ e^{\frac{\Delta t}{\tau_+}} & (\Delta t < 0) \\ -W_- e^{-\frac{\Delta t}{\tau_-}} & (\Delta t > 0) \end{cases} \quad (1)$$

where W_+ and W_- are the maximum and minimum values, respectively, of ΔW; and τ_+ and τ_- are the time windows determining the weight update rate for long-term depression and long-term potentiation, respectively. If the presynaptic spike arrives before the postsynaptic spike, the synaptic weight increases; otherwise, it decreases. In this paper, instead of a spike time difference, the memristor changes its state based on a pulse rate. If a positive pulse is continuously applied to the memristor

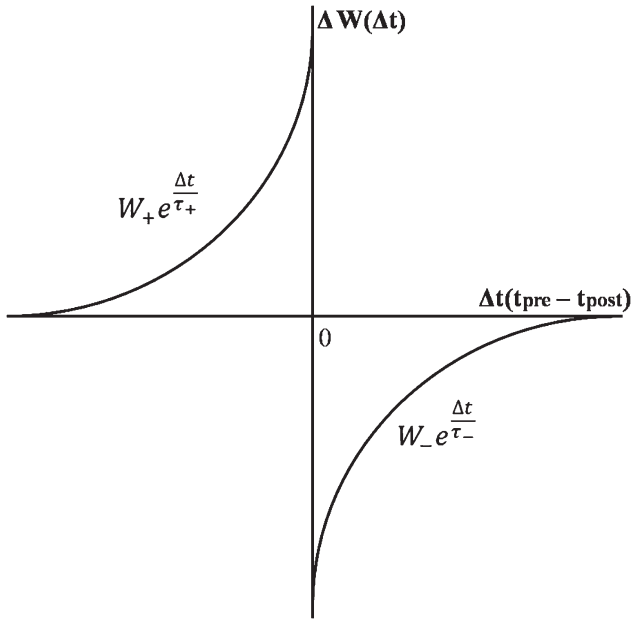

Fig. 6. Synaptic weight change in the STDP.

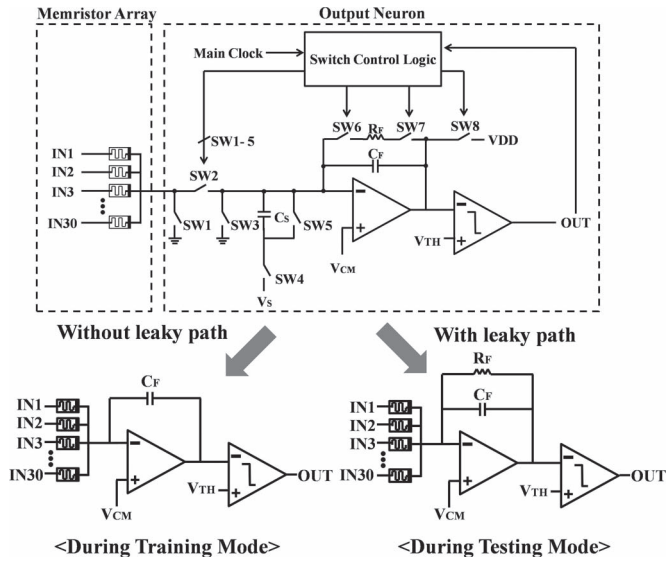

Fig. 7. Schematics of the output neuron in each operational mode.

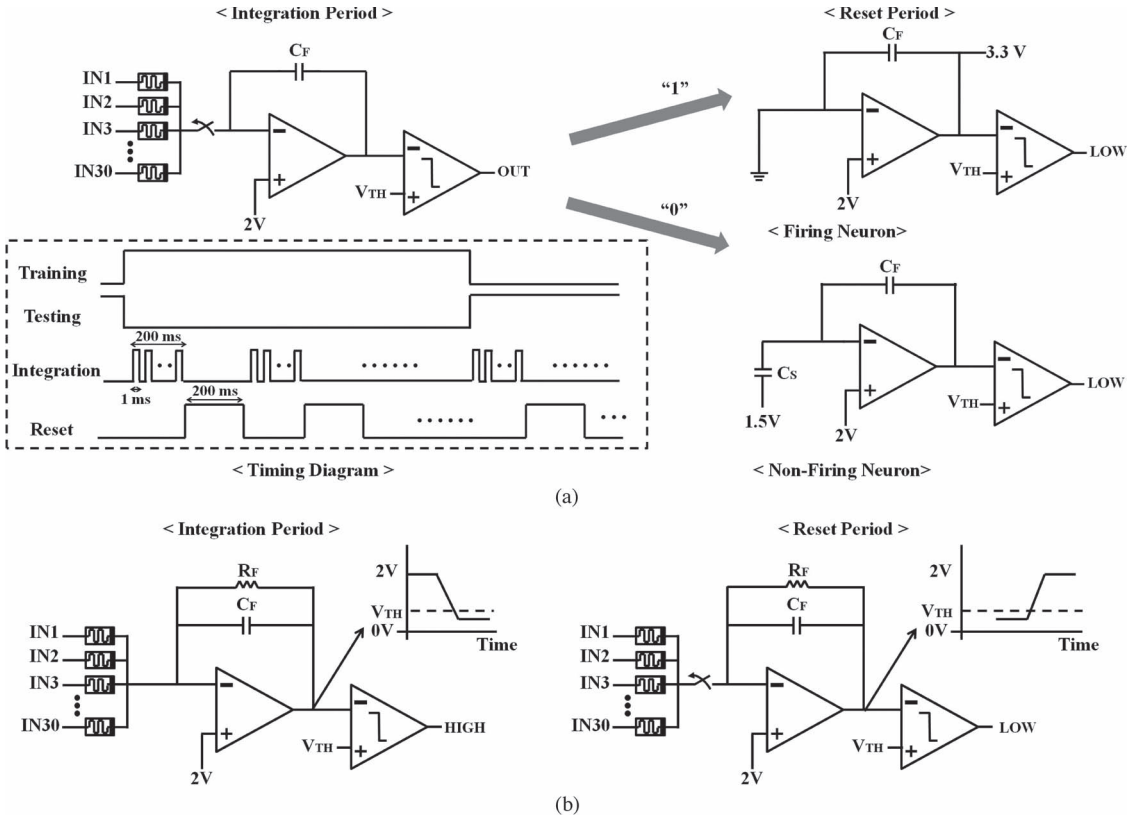

Fig. 8. Circuit diagrams for (a) training and (b) testing.

for a certain amount of time after which a neuron fires, its state changes from the HRS to the LRS, which corresponds to increasing the synaptic weight.

Note that, although the memristor has a bidirectional characteristic of changing its state, the system only utilizes one-directional change from the HRS to the LRS due to the nonsymmetrical behavior of the memristor being used in this paper. In general, the existing learning rules require symmetrical weight changes for positive and negative weights. In order to accommodate nonsymmetrical memristance change, a new learning rule, which will be explained in Section III, is introduced in this paper. With the help of the learning rule, the system achieves acceptable recognition accuracy even for noisy images.

C. Output Neuron

A leaky I&F neuron is used as an output neuron. As shown in Fig. 7, it is implemented with an integrator, a comparator, switches, and control logic. The integrator has an inverting output; hence, the output decreases as the current flowing through the memristor is accumulated on C_F. The smaller the memristance, the larger the amplitude of the current and the faster the output voltage drops. As soon as the integrator output goes down below a certain threshold voltage (V_{TH}), the comparator output goes high (logic "1"), and this is recognized by the control logic as the neuron has fired. Note that the neuron operates in two different modes, i.e., training and testing, and a leaky path formed by a feedback resistor R_F is only activated in the testing mode. The proposed learning rule, which will be explained later, requires that the charge on C_F be held by disconnecting the leaky path and leaving C_F floating until the end of the training mode, and this helps in making sure that only one neuron fires for a given training image during the training mode. On the other hand, in the testing mode, the neuron goes through a refractory period, which is determined by an RC $(R_F \cdot C_F)$ time constant of the integrator after a neuron fires. During this period, the charge on C_F needs to be fully discharged through the leaky path in order for the neuron to start over with the next test image.

The details of the system operation and the learning rule will be discussed in the following section.

III. System Operation

This section explains the overall system operation followed by the proposed unsupervised learning rule and its hardware implementation.

A. Overall System Operation

The system works in two different operating modes, i.e., training and testing. In the training mode, training images are sequentially applied, and a training process for each image is performed in two steps, i.e., integration and reset. The circuit diagram for training is shown in Fig. 8(a). During the integration period, the neuron integrates input currents and fires if V_T has been reached. Once one neuron fires, it makes all the neurons stop integration and hold their integrator output. In the reset period, the integrator output of the firing neuron is reset to 3.3 V by forcing the operational amplifier input and output to ground

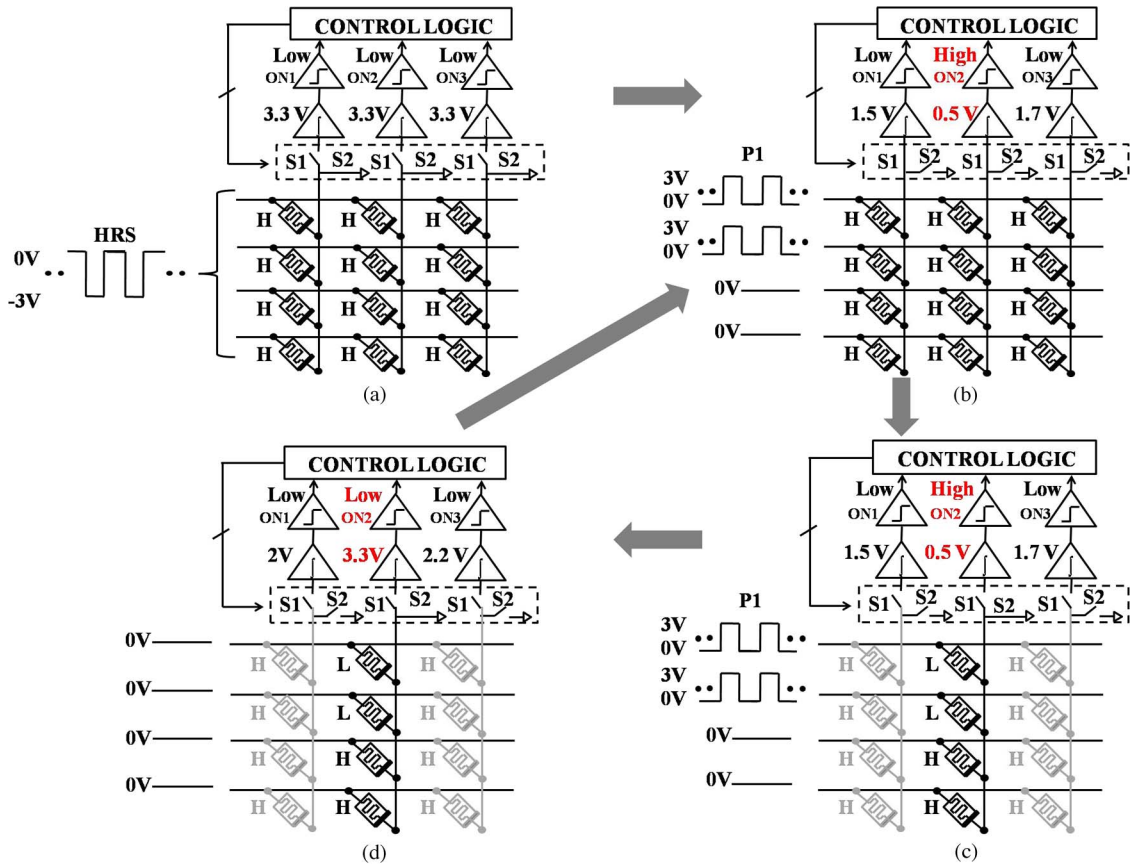

Fig. 9. (a)–(d) Learning procedure.

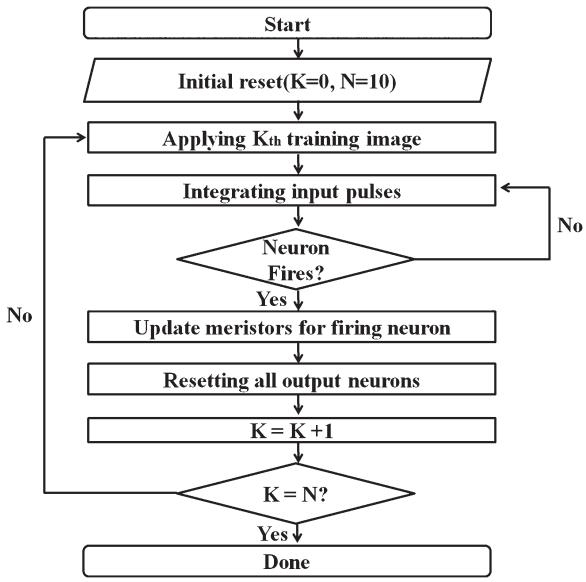

Fig. 10. Flowchart for the system's learning.

and 3.3 V, respectively, and the outputs of the other neurons are shifted up by 0.5 V. To shift the output voltage while keeping a charge stored on C_F, a series capacitor (C_S) has been added to transfer a charge for a 0.5-V direct-current shift from C_S to C_F.

In the testing mode, the neurons fire one by one as they recognize the test images based on what they have learned. As shown in Fig. 8(b), an image recognition, just like the training

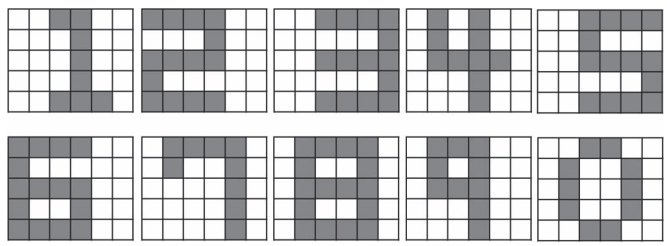

Fig. 11. Training images.

process, also requires two operational periods, i.e., integration and reset. In the integration period, the integrators generate the output that will be compared with V_{TH}, and the time it will take for the integrators to reach V_{TH} for a given test image varies depending on the memristance of their corresponding memristors. The neuron that fires first sends out an inhibitory signal, which freezes all the neurons' operation. During the reset period, all the memristors are disconnected from the neurons, and the outputs of the integrators settle to a common-mode voltage (2 V) as C_F is slowly discharged through the leaky path. In the next integration period, the integration is reinitiated with the next test image.

B. Proposed Learning Rule

As modified STDP, the proposed learning rule requires two operational periods, i.e., integration and reset. The output neuron that has the strongest correlation with a given input pattern is found during the integration period. Then, the associated

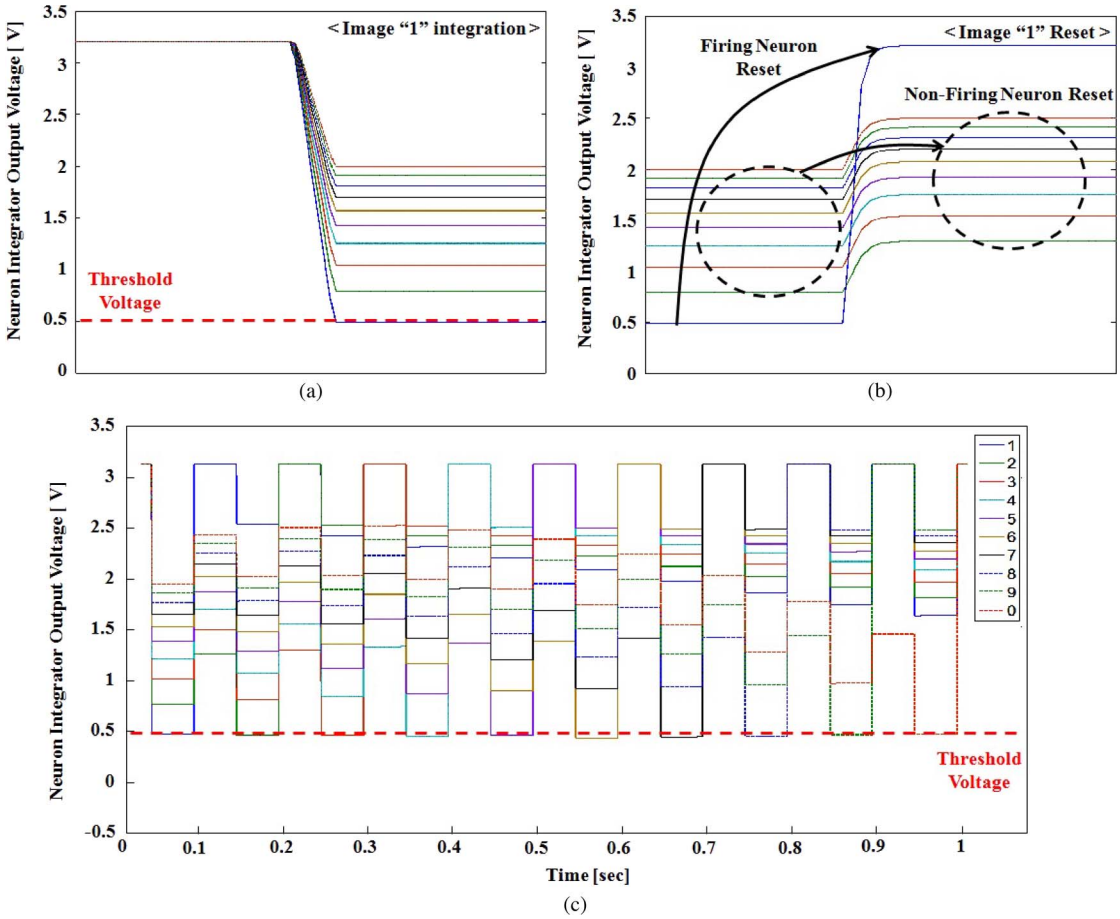

Fig. 12. Simulation results of the system's training: the outputs of ten integrators for image "1" (a) during the integration period and (b) during the reset period. (c) Integrators' outputs for all training images.

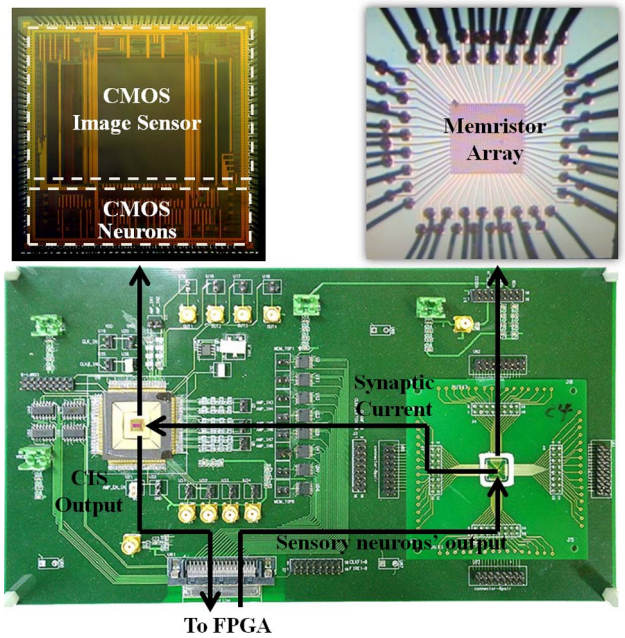

Fig. 13. System implementation.

memristors are trained, and the integrators' outputs are reset for the next input pattern in the reset period. This process is repeated until all the memristors are trained for all training images. As shown in Fig. 9, it can be easily explained with

Fig. 14. Training images taken by the CIS.

a simple four-input and three-output network. The learning procedure is as follows.

1) Initially, all the memristors are reset to the HRS by applying −3-V pulses, and all the integrators' outputs are reset to 3.3 V, as shown in Fig. 9(a).
2) As shown in Fig. 9(b), the input pulses representing image pattern P1 are applied, and the currents flowing through the memristors are integrated during the integration period. Note that, in the presence of process variation, none of the memristors have the same memristance even after the initial reset; hence, one of the integrators will reach V_T earlier than others. Since the firing neuron for a certain training image is not predetermined but rather determined by random process variation, this method can be considered an "unsupervised learning."
3) As soon as the control logic senses "1" from the neuron firing first [the neuron in the middle in Fig. 9(c)], the

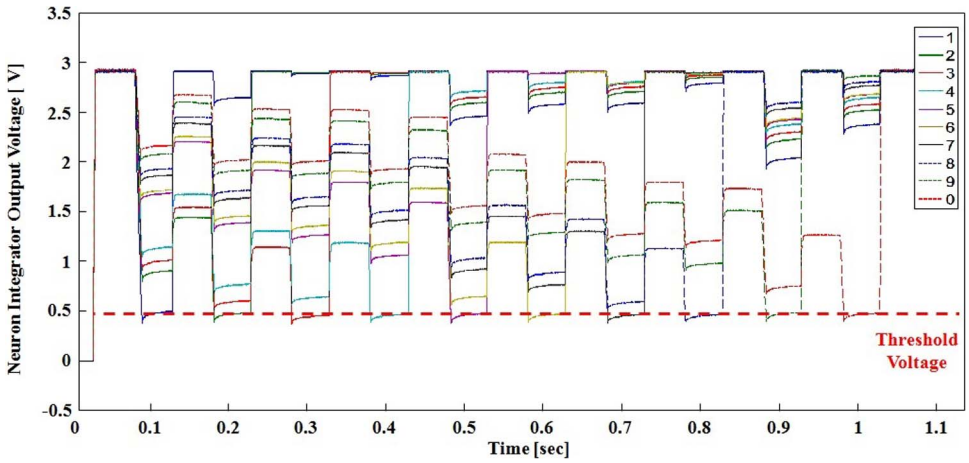

Fig. 15. Measured outputs of all integrators during training.

associated memristors' states are changed to the LRS, and the others are left unchanged by turning off all S1 switches and only turning on the S2 switch in the firing neuron.

4) After finishing updates, the integrator of the firing neuron is reset to 3.3 V, and the other two are shifted up by 0.5 V; then, all S1 switches turn back on, and S2 turns off. With the next training pattern (P2), the integration continues until one of the other two neurons fires. Note that a level-up voltage for the nonfiring neurons should be carefully chosen through simulations to allow the neurons to fire just once during training. The corresponding circuit diagram is shown in Fig. 9(d).
5) Steps 2–4 are repeated until the memristors are trained for all training images.

A flowchart of this procedure is also given in Fig. 10.

C. SPICE Simulation Result of Learning

The learning rule has been verified with Simulation Program with Integrated Circuit Emphasis (SPICE) simulations. The memristor is modeled with Verilog using the measured memristance data, and the output neurons are designed with CMOS transistors. The 5×6 pixel training images of 0–9 are shown in Fig. 11.

Simulation results are shown in Fig. 12. The outputs of ten integrators for image "1" are plotted in Fig. 12(a). As expected, the integrators' outputs almost linearly fall at different rates after an initial reset. Once one of them reaches V_T, the integration stops, and the outputs are held for the rest of the integration period. Then, as shown in Fig. 12(b), the integrator's output of the firing neuron is reset to 3.3 V, and the others are shifted up by 0.5 V until the end of the reset period. Fig. 12(c) shows the simulation result for all number patterns. Note that only one neuron fires in each integration period, which means one neuron and its associated memristors are trained at a time, as expected.

IV. Experimental Results

Fig. 13 shows the implemented pattern recognition system on a printed circuit board. The CIS and the neurons are built on a single chip, which was fabricated in the 0.18-μm CIS process, and the memristor array is fabricated through an in-house laboratory of our research group.

The training images taken by the CIS and the measurement results are shown in Figs. 14 and 15, respectively. The measured outputs of all the integrators are well matched to those of the simulations in Fig. 12, and this indicates that the system's training has been performed as expected. After training, the system has been tested with the training images for which the system was trained. As shown in Fig. 16, all the integrators' outputs are reset to 2 V during the reset period, and then, they drop at different rates until the control logic senses a firing neuron. This process is repeated for all test images. A detailed test result for image "1" is shown in Fig. 16(b). The neuron that was trained for "1" fires and makes all the neurons hold their internal states until the next reset. Note that the system has a limitation in recognizing images that have similar pixel values. For example, the images of "3" and "5" only have one pixel difference in their patterns; hence, as shown in Fig. 16(c), the neuron that was trained for "5" could have a similar integrator output to that of the neuron trained for "3." The system could be easily confused and make a wrong decision in the presence of various circuit noise levels. This issue could be relaxed by adding more pixels representing the image, but it will increase the system's complexity as much. The system was also tested with noisy images. As shown in Fig. 17, random noise patterns are added on top of the training images before they are applied to the system for recognition. Table I summarizes the measured recognition rates for various noise levels. The recognition rate rapidly drops as the noise level increases. For example, the recognition rate is reduced to 55% with a noise level of 16%. The main reason for incorrect recognition is the nonuniformity of memristance due to memristor process variation. With the memristance variation and high noise, the total memristance value of the memristors that are not trained for the input image can be smaller than that of the trained memristors. As a result, the current flowing into an irrelevant neuron increases, resulting in erroneous recognition. As aforementioned, the system would be much more tolerable to pattern noise or circuit noise if it has more sensory neurons and memristors. Using a memristor that has a symmetric behavior in increasing and decreasing

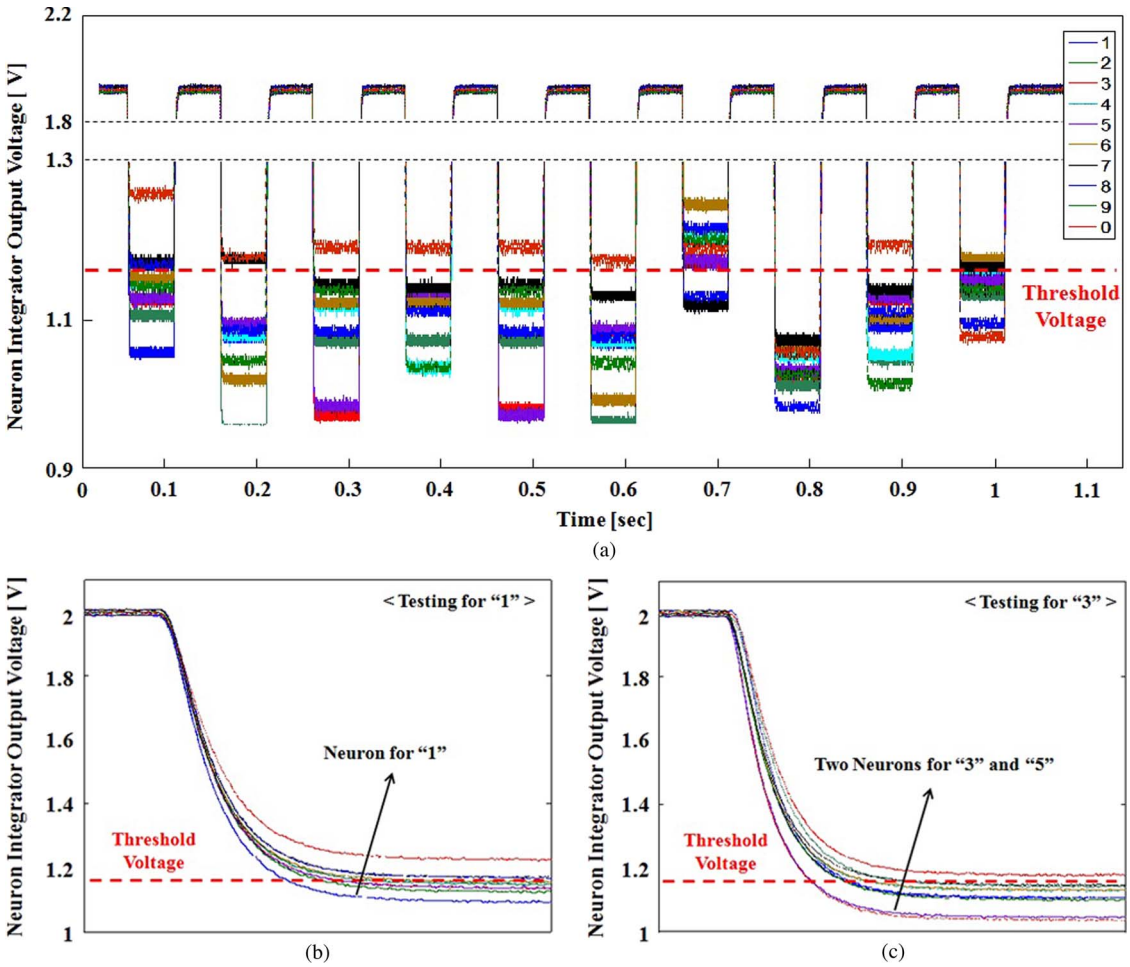

Fig. 16. Measurement results during the testing mode. (a) Outputs of all integrators. The integrator output of the neuron trained for (b) (b) image "1" and (c) image "3" during the integration period.

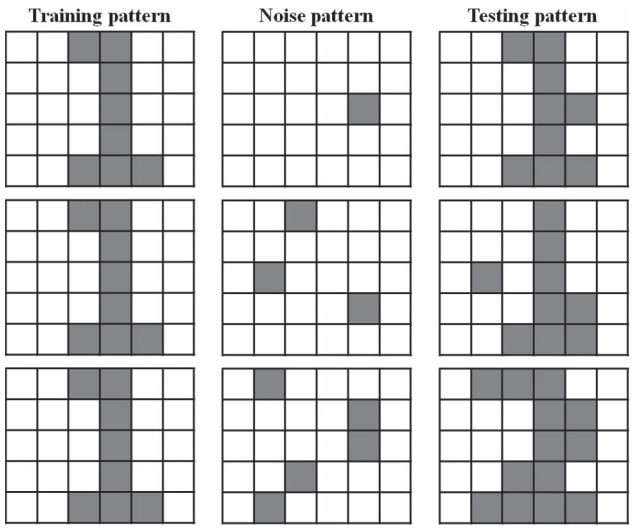

Fig. 17. Noisy patterns used for the recognition test.

memristance is another way of improving the recognition rate. As an ongoing research in our group, the symmetric memristance change makes it possible to utilize both the positive and negative weight updates for the system's training. This will also allow the system to be applied to a wide range of applications.

TABLE I
RECOGNITION RATES FOR VARIOUS NOISY PATTERNS

Noise level (# of noise pixel /30)	Correct recognition rate
0%	100%
3%	95%
10%	85%
16%	55%

V. CONCLUSION

A neuromorphic system employing new learning has been presented. It contains an artificial photoreceptor, which converts an image into voltage pulses, a memristor array for synaptic connections, and leaky I&F neurons as output neurons. Modified STDP has been proposed to accordingly adjust the memristors' state or synaptic weights during the system's training. In testing, one of the output neurons fires as it integrates currents flowing through the memristors and reaches a certain threshold earlier than others. Then, the firing neuron sends out an inhibitory signal that freezes all neurons and resets their internal states to start over the recognition process with the next test image. Implementation details are also presented with test results.

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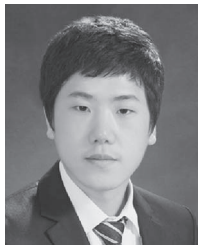

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