

Analysing Mismatch effect of CMOS Neurons in Spiking Neural Network with Winner-take-all Mechanism

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Abstract—The aim of designing the energy-efficient high-density spiking neural network (SNN) is not possible without channelising the efforts to design the basic repeating blocks of Neuromorphic Computing (NMC), i.e., neurons and synapses. The investigation done to replace synapses in the last years has created memristors as the most prominent solution for high-density SNN. CMOS-memristive integrated circuits are widely adopted to realise brain-inspired neuromorphic circuits. While the challenges of the memristors have been highlighted and resolved in various literature, much attention is not given to designing robust CMOS neurons and its challenges for achieving high-density integration in neuromorphic chips. Process-induced variations must be analysed for the robustness of the CMOS neurons. Apart from the process and temperature variations of CMOS neuron, which is mostly analysed in previous works, mismatches are critical for the SNN with a winner-take-all (WTA) mechanism where output neurons compete to win the competition. In this paper, we have shown that the SNN with WTA mechanism is robust to PVT variations but is sensitive to mismatch variations of CMOS neurons. We have also proposed an approach to mitigate the mismatch effect. The observations are validated with the post-layout simulation results of the SNN circuit designed in 180 nm CMOS technology.

Index Terms—Spiking neural networks, CMOS neuron, Memristor, Winner-take-all, Neuromorphic computing.

I. INTRODUCTION

Spiking neural network (SNN), the third-generation neural network, has emerged as the most viable alternative to realise the energy-efficient neuromorphic system-on-a-chip because of its event-driven nature and close resemblance to brain dynamics. Fig. 1 shows the architecture of SNN with the winner-take-all (WTA) mechanism implemented in our recent work [1], where the information is processed in the form of spikes. Thus, requiring to convert the input analogue sensory signal into spikes, which may be done using several neural models [2]. The LIF neuron model offers the best compromise between accuracy and simplicity of hardware implementation, and it also closely matches the biological neurons [2], [3]. WTA is incorporated in SNN architectures to increase sparsity and data storage [4] as only one output neuron that receives maximum input current is activated to spike.

CMOS-RRAM integrated circuits for implementing neuromorphic systems are widely adopted to provide area- and

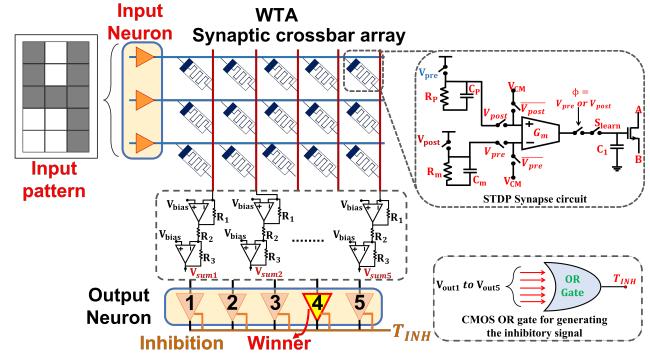


Fig. 1. The simplified CMOS architecture of SNN with WTA mechanism for pattern recognition.

energy-efficient bioinspired computing hardware. Various non-idealities and challenges of nano memristor devices, such as variability of resistance states and threshold voltages, resistive loading due to low ON resistance of RRAMs, nonlinearity and low endurance, have been addressed in various literature [5]. However, not much attention is given to the other important component of SNN, i.e. CMOS neuron. Various works [6], [7] focus on area- and energy efficiency while designing the CMOS neuron for achieving high-density integrated SNN. For low-power operation, CMOS neurons work in low current and low voltage; the variability in the CMOS process can affect the overall operation of the SNN. Since there is a competition between the output neurons in spiking WTA, besides the PVT immune neuron design discussed in works [5], [8], the other non-idealities, such as mismatches and noise, are also crucial for analysing the robustness of the complete network.

Unlike many other works [5]–[8], this paper analysed the effect of mismatches of CMOS neurons on the accuracy and robustness of the CMOS spiking WTA for pattern recognition. The entire system was designed using CMOS memristive synapse and LIF neuron, same as our earlier works [1], [9]–[11]. With post-layout simulation results and observations, we have shown that the impact of mismatches is more significant than PVT variations of CMOS neurons on the overall accuracy and robustness of the SNN system. We have also proposed an approach to mitigate the mismatch effect, which can be applied to any type of neuron implemented in SNN with the

WTA mechanism.

This paper is structured as follows. Section II describes the CMOS LIF neuron used in our designed spiking WTA. Section III explains the proposed CMOS spiking WTA for pattern recognition along with the process-induced variations and proposed mitigation technique. Simulation results are discussed in section III. The paper's conclusion is drawn in section IV.

II. CMOS LEAKY INTEGRATE-AND-FIRE (LIF) NEURON

The low-power, low-complexity neuron circuit suggested in [13] is used as a presynaptic and postsynaptic neuron in our on-chip trainable SNN system. In order to implement the winner-take-all (WTA) mechanism in SNN (see Fig. 1), it has a lateral inhibition interface. In Fig. 2, input current I_{in} is injected into the current integration section through the current mirror, charging the capacitor C_u , and is regulated by the voltage provided at input terminals T_{EX} and T_{FF} . With the aid of the Schmitt trigger, a spike is produced when the membrane voltage V_u approaches the threshold of a neuron. At the same time, R_{st} will be low, turning on M_{11} and resetting V_u through C_{ref} and M_{14} . The external pin T_{INH} can also be used to reset the circuit. The neuron's firing threshold, which is determined by the switching voltage (V_{SV}) of the Schmitt trigger, can be computed as

$$I_{Dn2} = \beta_{n2}(V_{SV} - V_n - V_{TH})^2 \quad (1)$$

$$I_{Dp2} = \beta_{p2}(V_{DD} - V_{SV} - |V_{tp}|)^2 \quad (2)$$

where $I_{Dn,pi}$ is the drain current and $\beta_{n,pi}$ represents the transconductance of transistor $M_{n,pi}$. Now, equating (1) and (2), we get

$$V_{SV} = V_n + \frac{V_{DD} + V_T(1 - R) - V_n}{R + 1} \quad (3)$$

$$I_{Dn1} = \beta_{n1}(V_n - V_{TH})^2 \quad (4)$$

Equating (1) and (4), we get

$$V_n = \frac{V_{HL}}{R_n + 1} + V_{TH} \frac{R_n - 1}{R_n + 1} \quad (5)$$

After substituting (5) in (3), V_{SV} is given as

$$V_{SV} = V_{DD} \frac{R_n + 1}{R_n(R + 1) + 1} + V_{TH} \frac{R_n(2R - 1) - 1}{R_n(R - 1) + 1} \quad (6)$$

where $R = \sqrt{\frac{\beta_{n2}}{\beta_{p2}}}$; $R_n = \sqrt{\frac{\beta_{n1}}{\beta_{n2}}}$. A spike is produced whenever the neuron's membrane voltage (V_u) exceeds the switching voltage V_{SV} . The Schmitt trigger's switching voltage, which is provided by (6), may be used to modify the spike's width.

Additionally, we modified this circuit to fit the needs of our suggested CMOS-based SNN system. Fig. 3 presents the results of the LIF circuit simulation. The neuron will not produce spikes for input voltages $V_{FF} < 500mV$ (applied at input node T_{FF}), and the rate of spiking increases with increasing input voltage for $V_{FF} > 500mV$. The input signal is transformed into a rate-encoded spike train using this feature.

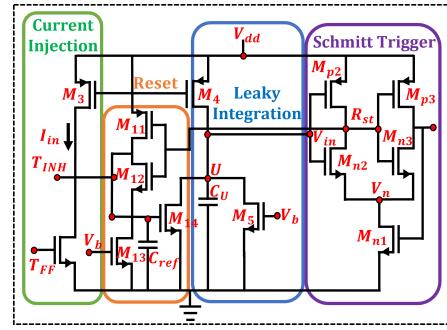


Fig. 2. The CMOS circuit of Leaky Integrate-and-Fire (LIF) neuron.

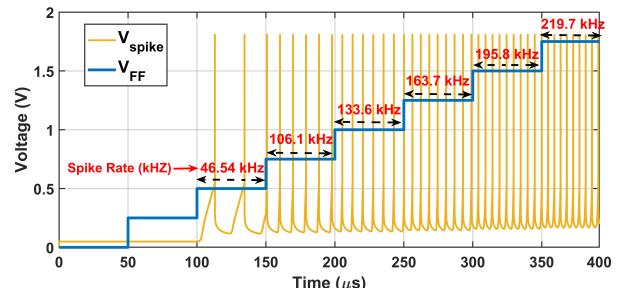


Fig. 3. Spiking LIF neuron response to varied step voltage inputs. Spiking frequency increases with each step of input voltage V_{FF} .

III. CMOS SPIKING WTA FOR PATTERN RECOGNITION

This section briefs the working of the implemented on-chip trainable SNN architecture with the WTA mechanism. Process-induced variations, including PVT and mismatches, and the proposed mitigation technique are also explained.

A. Working

We have used the architecture of on-chip trainable SNN implemented in our recent work [1] (shown in Fig. 1) for pattern recognition. The CMOS memristive synapse circuit that shows the STDP mechanism is used as a synapse in the crossbar. The working is more elaborated in [1].

During the training mode, the output layer neurons are disconnected from the crossbar (shown in Fig. 4(a)), and each synapse in column j will be trained according to the pattern given during j^{th} learning cycle (S_{learn_j}). All the synapses are initially at a high resistance state (HRS). The synaptic state will change from HRS to a low resistance state (LRS) corresponding to a black pixel and remain in HRS in response to a white pixel.

During the inference mode shown in Fig. 4(b), each column j will perform the sum of product computation according to (7), where g_{ij} is the conductance of the synapse in i^{th} row and j^{th} column. The current of each row is summed and converted to voltage V_{sum} at the output of each column using a summing amplifier (A_{sum}) and an inverting amplifier (A_{inv}). The summed voltage at each column will be modeled as

$$i_{sum_j} = \Sigma(V_{in_i} - V_{bias}) * g_{ij} \quad (7)$$

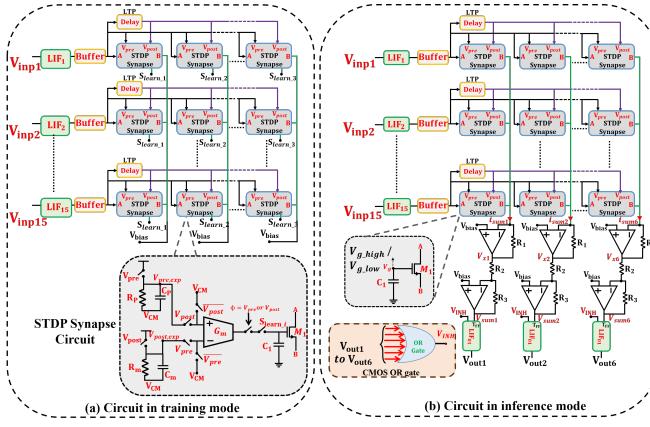


Fig. 4. The equivalent circuit of SNN with WTA mechanism in training and inference mode.

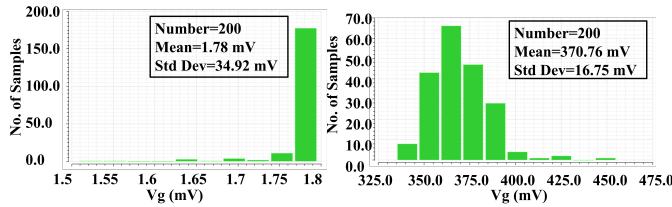


Fig. 5. Monte Carlo simulation results showing variation in the (a) LRS corresponding to maximum V_g (b) HRS corresponding to minimum V_g , incorporating process variation and mismatch of all components.

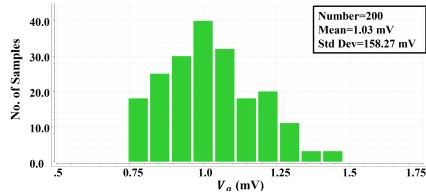


Fig. 6. Monte Carlo simulation result showing variation in the intermediate state V_g incorporating process variation and mismatch of all components.

$$V_{x_j} = V_{bias} - i_{sum_j} * R_1 \quad (8)$$

$$V_{sum_j} = V_{bias} + \frac{R_3}{R_2} (V_{bias} - V_x) \quad (9)$$

$$V_{sum_j} = V_{bias} + \frac{R_3 R_1}{R_2} i_{sum_j} \quad (10)$$

$$V_{sum_j} = V_{bias} + \frac{R_3 R_1}{R_2} \Sigma (V_{in_i} - V_{bias}) * g_{ij} \quad (11)$$

The output neuron (LIF_{Oj}) in column j which will have the highest summed voltage will fire first and will inhibit the other neurons to elicit spikes by sending the inhibitory high signal through an OR gate shown in Fig. 4(b) thus exhibiting the winner-take-all mechanism.

B. PVT Induced Variations

The STDP synapses of the SNN are trained to extreme values, i.e. HRS and LRS (modelled by the resistance and

controlled by the gate voltage (V_g) of transistor M_1 (biased in deep triode region) of the STDP memristive synapse circuit shown in Fig. 4). The accuracy of the training phase of the binary-weighted SNN will not be affected by the process variations across extreme corners (SS, FF, SF, FS). The binary-weighted SNN is least affected by the process variations compared to the analog state neural network since the difference in the analog states is much less than the room between the extreme binary states. Therefore the analog states are much more likely to drift from their values than binary states. This can also be seen from the Monte Carlo simulation of the synapse trained for binary states shown in Fig. 5, the deviation in the achieved binary state is less than the analog state depicted in Fig. 6. Thus, the PVT will not affect the training accuracy of the binary-weighted SNN.

The inference phase critically evaluates the accuracy of the binary-weighted WTA spiking neural network. Under process and temperature variations, the correct neuron is expected to fire first and inhibit the other neurons. In view of this, SNN with WTA mechanism is robust to PVT variations as the winner neuron will remain the winner in all process corners and temperature ranges. The change in the neuron's firing frequency (Δf) due to process and temperature variations will be the same for all the output neurons. Therefore the winning neuron wins the competition of firing first in all the process corners and temperatures.

In conclusion, PVT variations will neither effect the training of binary weighted SNN nor the inference phase of SNN with the WTA mechanism.

C. Mismatches induced variations

Mismatches variations are more critical than the PVT variations for determining the accuracy of the correct firing of the output neuron in SNN with the WTA mechanism. The current flowing through the synapse in the LRS state is given by (12), where R_{LRS} is the low resistance (or ON resistance) of the synapse. From the circuit design perspective, having a high value of R_{LRS} (100s of k Ω) is preferable to a few Ω s for energy-efficient and low power SNN. Therefore the low value of currents will flow through the synapse, making the mismatches even more critical while designing the network.

$$i_{syn} = \frac{V_{syn}}{R_{LRS}} \quad (12)$$

Now, consider the case where there is a one-pixel difference in the trained images of two columns of the crossbar. Due to mismatches between the output neurons, the neuron, even with lower input summed voltage, may fire at a higher frequency and become the winning neuron. This results in the wrong firing of the neuron leading to inaccurate pattern recognition of similar patterns (or the patterns with low pixel difference).

In conclusion, mismatch variations will not effect the training of binary weighted SNN (shown in Fig. 5, Fig. 6) as in our case, output neurons are not involved in the training process, and synapses are trained to binary states. Also, in most cases, training involves a teacher signal or self-correcting

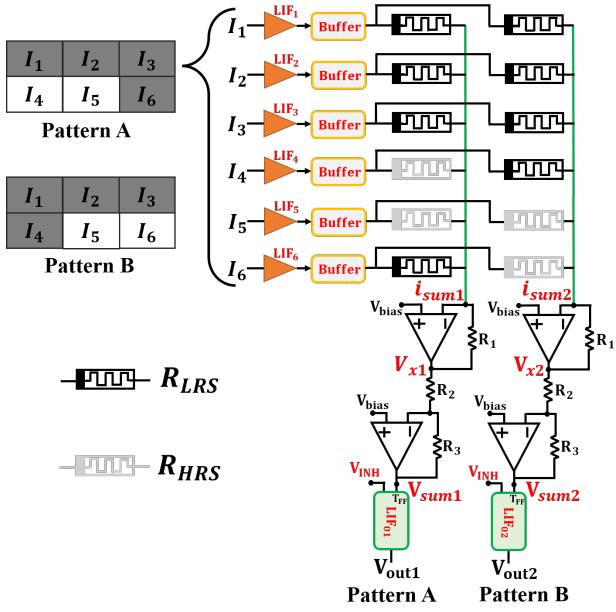


Fig. 7. Schematic of spiking WTA for pattern recognition of two patterns with one pixel value difference.

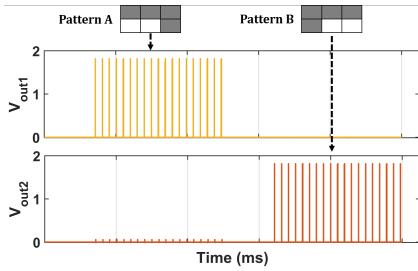


Fig. 8. Firing of the output neurons in response to Pattern A and Pattern B without including mismatches.

loop, making training inherently robust to mismatch variations. However, mismatch variations can effect the inference phase of SNN with the WTA mechanism.

D. Proposed Mitigation Technique

To mitigate the mismatch variations, it is important to identify the root cause of the problem. Given this, we run the Monte Carlo simulations to check the robustness of the spiking WTA. We have taken the elements for mismatch variations one by one, tabulated in Table I, to evaluate the accuracy of SNN. The accuracy was affected when the mismatch variations of the output LIF neurons were included. This concludes that the robustness of the spiking WTA is sensitive to the mismatch variation of the output LIF neurons.

Mismatches for low-current and low-power spiking WTA can be highlighted by the test case in Fig. 7. Where column 1 and column 2 are trained for patterns A and B, respectively, shown in Fig. 7. V_{sum1} is the summed voltage for pattern A, and the output weighted summed voltage for pattern B is modelled as V_{sum2} . Without including mismatches in the

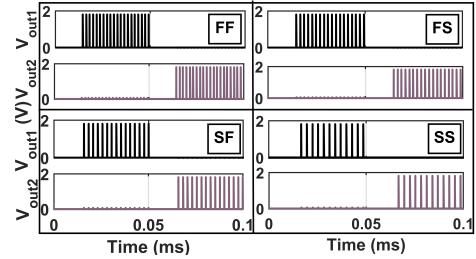


Fig. 9. Firing of the output neurons in response to Pattern A and Pattern B in all process corners.

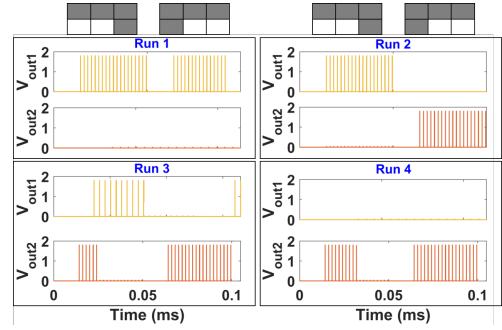


Fig. 10. Monte Carlo simulation of the firing of output LIF neurons (including the mismatches of the neurons) for 4 runs.

output LIF neurons, LIF_{O1} should spike when pattern A is input to the WTA and LIF_{O2} spikes in response to pattern B. This is the case shown in Fig. 8. PVT variations will also not effect the correct firing of LIF neurons as shown in Fig. 9 (process and temperature will have a similar effect on the firing frequency of neurons). However, including the mismatches of the output LIF neurons results in the wrong firing of LIF neurons shown in the Monte Carlo simulation for 4 runs in Fig. 10.

To overcome this we have modeled the maximum frequency deviation in the LIF neuron corresponding to the mismatch variations as below.

When pattern A is input to the spiking WTA, using eq. (11),

$$V_{sum1} = V_{bias} + \frac{R_3 R_1}{R_2} [4(V_{inH} - V_{bias}) * \frac{1}{R_{LRS}} + 2(V_{inL} - V_{bias}) * \frac{1}{R_{HRS}}] \quad (13)$$

$$V_{sum2} = V_{bias} + \frac{R_3 R_1}{R_2} [3(V_{inH} - V_{bias}) * \frac{1}{R_{LRS}} + 1(V_{inL} - V_{bias}) * \frac{1}{R_{LRS}} + 1(V_{inL} - V_{bias}) * \frac{1}{R_{HRS}} + 1(V_{inL} - V_{bias}) * \frac{1}{R_{HRS}}] \quad (14)$$

where V_{inH} and V_{inL} are the high and the low input to the crossbar generated by the input LIF neurons corresponding to the black and white pixel respectively.

TABLE I
EVALUATING THE ROBUSTNESS OF SPIKING WTA FOR MISMATCH VARIATIONS IN DIFFERENT CASES OF IDEAL AND NON-IDEAL COMPONENTS OF

	Input LIF neurons	CMOS synapses	Opamp	Output LIF Neurons	Is Design Robust?
1.	Ideal	Ideal	Ideal	Ideal	Yes
2.	Non-ideal	Ideal	Ideal	Ideal	Yes
3.	Ideal	Non-ideal	Ideal	Ideal	Yes
4.	Ideal	Ideal	Non-ideal	Ideal	Yes
5.	Ideal	Ideal	Ideal	Non-ideal	No

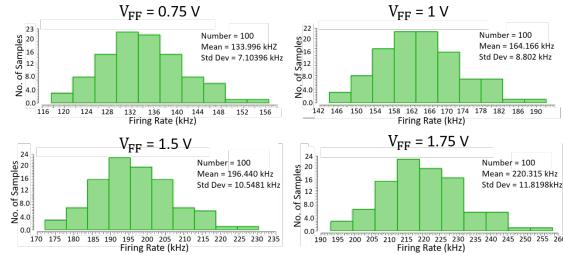


Fig. 11. Monte Carlo simulation results of LIF firing frequency at a DC input of 0.75 V, 1 V, 1.5 V, and 1.75 V, incorporating process variations and mismatches of all components.

Considering $V_{inH} = V_H + V_{bias}$, $V_{inL} = V_{bias}$ and ignoring the negligible current flowing through the R_{HRS} , V_{sum1} and V_{sum2} can be represented as

$$V_{sum1} = V_{bias} + \frac{R_3 R_1}{R_2} [4(V_H) * \frac{1}{R_{LRS}}] \quad (15)$$

$$V_{sum2} = V_{bias} + \frac{R_3 R_1}{R_2} [3(V_H) * \frac{1}{R_{LRS}}] \quad (16)$$

$$\Delta V = \frac{R_3 R_1}{R_2} [(V_H) * \frac{1}{R_{LRS}}] \quad (17)$$

Comparing (15) and (16), $V_{sum1} > V_{sum2}$ and hence LIF_{O1} should win the competition to fire first. However, if the difference (ΔV given by (17)) between the V_{sum1} and V_{sum2} is very less (corresponding to one pixel difference), then there is a possibility that a wrong LIF neuron fires. In order to avoid that, R_1, R_2, R_3 can be chosen such that the ΔV increases and accommodates the maximum variation in the frequency. Monte Carlo simulation of the LIF neuron's firing frequency at different input voltages shown in Fig. 11 shows the maximum deviation ($\pm 3\sigma$) of 12 KHz. This maximum deviation in the spiking frequency corresponds to a 65 mV variation in the input voltage of LIF neuron. Thus, ΔV should be kept greater than 65 mV to accommodate the maximum deviation in the neuron's firing frequency (ΔV is kept 100 mV in our implemented SNN system).

IV. RESULTS AND DISCUSSION

In this section post-layout simulation results of the full CMOS SNN with WTA mechanism (architecture shown in

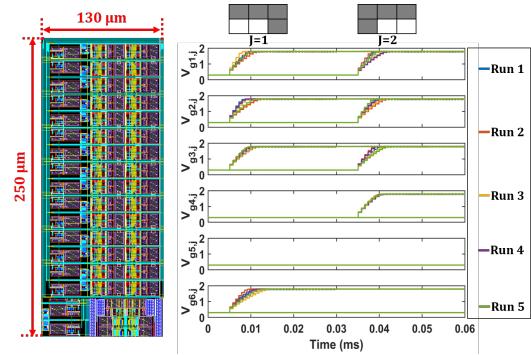


Fig. 12. (Left) Layout of the implemented SNN with WTA mechanism for pattern recognition of two patterns and (Right) Monte Carlo simulation for the training phase of the SNN for 5 runs.

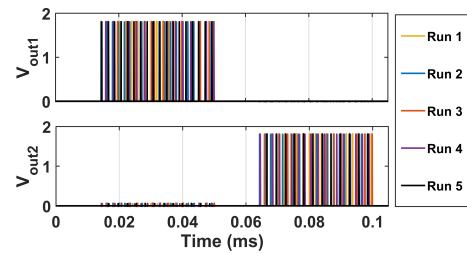


Fig. 13. Monte Carlo simulation (for 5 runs) of the firing of the output neurons (with applied mitigation technique) in response to Pattern A and Pattern B.

Fig. 1 and the layout is shown in Fig. 12 for pattern recognition of two 6-pixel binary images are discussed. The architecture and working of the SNN with WTA mechanism is same as implemented in our recent work [1], where each synapse is implemented using CMOS STDP memristive synapse circuit.

A. Simulation Results of Training Phase

Column 1 and column 2 of SNN with WTA mechanism is trained for pattern A and pattern B respectively. Fig. 12 shows the Monte Carlo simulation for the training phase of the SNN for 5 runs. Initially all the synapses are at HRS corresponding to $V_g|low$ of the transistor M_1 of the STDP synapse (refer to Fig. 4 and working details can be found in [1]). It can be observed that the state of all the STDP synapses reaches their desired state (LRS corresponding to $V_g|high$) in response to the black pixel of the input pattern in all the 5 runs. Thus, training of the synapses to binary states is robust to PVT and mismatch variations.

B. Simulation Results of Inference Phase

The firing of only the correct output neuron in response to the trained input image under process and mismatch variations decides the robustness of the SNN system. When $\Delta V < 100$ mV, Monte Carlo simulation of LIF's firing frequency was not correct as shown in Fig. 10. After adjusting R_1, R_2, R_3 for $\Delta V = 100$ mV, output neurons were able to fire correctly in all the 5 runs of the Monte Carlo simulation shown in Fig. 13.

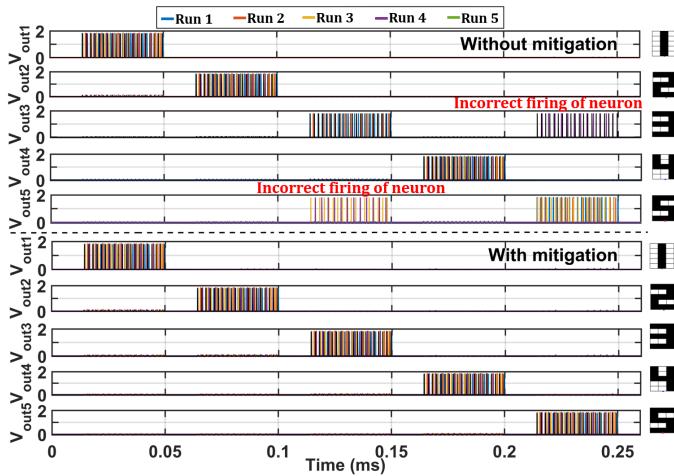


Fig. 14. Monte Carlo simulation of the inference results for digit pattern recognition with and without proposed mitigation technique.

C. Accuracy with and without Mitigation Technique

We have also implemented the same architecture of SNN with the WTA mechanism for pattern recognition of digit patterns ‘1’, ‘2’, ‘3’, ‘4’, ‘5’ shown in Fig. 14. The neurons trained for patterns ‘1’, ‘2’, ‘4’ can fire correctly in all five runs. However, without the mismatch mitigation technique, the neurons for 3 and 5 are not firing correctly for all five runs of the Monte Carlo simulation because of only a 1-pixel difference, resulting in reduced accuracy. The other way to overcome this is to increase the number of pixels in the image, but it increases the circuit complexity. For a practical demonstration of the proposed mitigation technique, we have also taken the 30 samples of each digit pattern ‘1’, ‘2’, ‘3’, ‘4’, ‘5’ in MNIST handwritten dataset. The images were downsampled into 8×8 binarised images. The accuracy evaluated was 94.1% and 89% with and without mitigation technique, respectively. Thus, the proposed technique improves the accuracy, robustness and precision of the SNN system with WTA mechanism.

D. Comparison

Table II compares the state-of-the-art works for CMOS neuron circuits based on analysing the robustness test of the LIF neuron for the accuracy of the SNN. Work [7] proposes the energy-efficient LIF neuron circuit but doesn’t analyse its robustness for its implementation in SNN. Process corners invariant digitally controlled LIF neuron is proposed in [8], however mismatch variations were not considered and robustness of the complete SNN was not evaluated. A novel LIF neuron circuit was also proposed in [6] but robustness was not analysed for process and mismatch variations. In [5] robustness against process variations of LIF neurons were discussed but its mitigation techniques were only applied to Op-amp based neuron circuits. In comparison to above, our work presents the analysis of the PVT and mismatch variations of LIF neuron for the robustness of the SNN system with WTA mechanism. The mitigation technique proposed in our work

TABLE II
COMPARISON OF STATE-OF-THE-ART LIF NEURON CIRCUITS FOR SNN IMPLEMENTATION

Work	Tech.	PVT Test	Mismatch Test	Energy/spike/synapse	Mitigation technique
ISCAS, 2020 [5]	180 nm	✓	✗	40 fJ	✗
TCAS I, 2022 [6]	28 nm	✗	✗	9.43 pJ	✗
TCAS II, 2021 [7]	180 nm	✓	✗	0.135 fJ	✗
ISCAS, 2018 [8]	65 nm	✓	✗	-	✗
This work	180 nm	✓	✓	0.28 pJ	✓

can be implemented to any type of neuron circuit applied in the SNN with WTA mechanism.

V. CONCLUSION

This work analyses the mismatch effect of the CMOS neurons for evaluating the overall accuracy and robustness of the full CMOS SNN with the WTA mechanism. It is shown that the binary-weighted SNN is inherently robust to PVT variations as the winner neuron will remain the first neuron to spike in all the process corners and temperature ranges. Also, PVT variation will not effect the training accuracy of the memristive STDP synapses to HRS and LRS states. The inference phase, where the correct neuron should fire in response to the input pattern, determines the pattern recognition accuracy of the SNN with WTA mechanism. Since there is internal competition between the output neurons to fire first, mismatches are critical for the inference phase. This work also proposes a mitigation approach to overcome the mismatch effect of the output neurons for the robust implementation of SNN. The proposed technique can be implemented for any type of neuron applied to SNN with the WTA mechanism. The results are validated with the post-layout simulation of the full CMOS SNN with the WTA mechanism for pattern recognition application.

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