

Pin Planner C:/Users/ASUS/Downloads/EXPORT-20220115T222527Z-001/EXPORT/RAM/PROYECTOSDII - PROYECTOSDII

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GRUPO 4 ADRIANA PONCE Y RICARDO MUÑOZ PARALELO 102 PROF. ALLISON CONSTANTINE

Report

Report not available

Groups Report

Tasks

Early Pin Planning

Early Pin Planning...

Run I/O Assignment

Export Pin Assignment

Pin Finder...

Highlight Pins

I/O Banks

VREF Groups

Edges

Clock Pins

Clock

Pin 1 / Pin 1 Input

Top View - Wire Bond

Cyclone IV E - EP4CE15F23C6

Pin Legend

Symbol Pin Type

User I/O

User assign...

Filter assign...

Unbonded ...

Reserved pin

Other confi...

DEV_OE

DEV_CLR

DIFF_n

DIFF_p

DQ

DQS

CLK_n

CLK_p

Other PLL

Other dual ...

MSEL0

MSEL1

MSEL2

MSEL3

CONF_DONE

nCE

nCONFIG

TDI

TCK

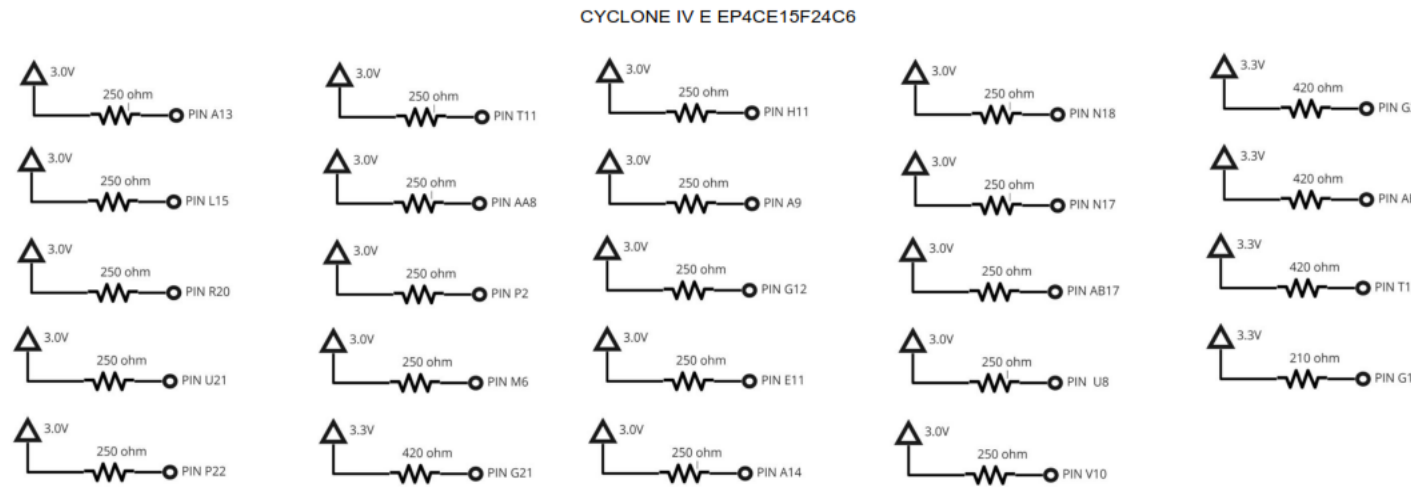
TMS

TDO

Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Filter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	ict Pre
Dat[0]	Output	PIN_H11	8	B8_NO	PIN_H11	3.0-V LVTTTL		12ma	2 (default)		
Dat[4]	Output	PIN_A9	8	B8_NO	PIN_A9	3.0-V LVTTTL		12ma	2 (default)		
Dat[9]	Output	PIN_G12	7	B7_N1	PIN_G12	3.0-V LVTTTL		12ma	2 (default)		
Dat[11]	Output	PIN_E11	7	B7_N1	PIN_E11	3.0-V LVTTTL		12ma	2 (default)		
Dat[5]	Output	PIN_A14	7	B7_N1	PIN_A14	3.0-V LVTTTL		12ma	2 (default)		
Dat[2]	Output	PIN_A13	7	B7_N1	PIN_A13	3.0-V LVTTTL		12ma	2 (default)		
Dat[3]	Output	PIN_L15	6	B6_N1	PIN_L15	3.0-V LVTTTL		12ma	2 (default)		
start	Input	PIN_G21	6	B6_N1	PIN_G21	3.3-V LVTTTL		8ma			
Dat[15]	Output	PIN_R20	5	B5_N1	PIN_R20	3.0-V LVTTTL		12ma	2 (default)		
Dat[6]	Output	PIN_U21	5	B5_NO	PIN_U21	3.0-V LVTTTL		12ma	2 (default)		
Dat[8]	Output	PIN_P22	5	B5_NO	PIN_P22	3.0-V LVTTTL		12ma	2 (default)		
Dat[11]	Output	PIN_N18	5	B5_NO	PIN_N18	3.0-V LVTTTL		12ma	2 (default)		
Dat[13]	Output	PIN_N17	5	B5_NO	PIN_N17	3.0-V LVTTTL		12ma	2 (default)		
Dat[12]	Output	PIN_AB17	4	B4_N1	PIN_AB17	3.0-V LVTTTL		12ma	2 (default)		
done	Output	PIN_T12	4	B4_N1	PIN_T12	3.3-V LVTTTL		8ma	2 (default)		
show	Input	PIN_AB16	4	B4_N1	PIN_AB16	3.3-V LVTTTL		8ma			
Dat[16]	Output	PIN_U8	3	B3_N1	PIN_U8	3.0-V LVTTTL		12ma	2 (default)		
Dat[18]	Output	PIN_V10	3	B3_NO	PIN_V10	3.0-V LVTTTL		12ma	2 (default)		
Dat[17]	Output	PIN_T11	3	B3_NO	PIN_T11	3.0-V LVTTTL		12ma	2 (default)		
Dat[7]	Output	PIN_AA8	3	B3_NO	PIN_AA8	3.0-V LVTTTL		12ma	2 (default)		
Dat[14]	Output	PIN_P2	2	B2_NO	PIN_P2	3.0-V LVTTTL		12ma	2 (default)		
Dat[10]	Output	PIN_M6	2	B2_NO	PIN_M6	3.0-V LVTTTL		12ma	2 (default)		
resetn	Input	PIN_T2	2	B2_NO	PIN_T2	3.3-V LVTTTL		8ma			
clk	Input	PIN_G1	1	B1_N1	PIN_G1	3.3-V LVTTTL		16ma			

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- Las entradas y salidas operan a 8mA
- Los datos de la RAM operan a 12mA
- La frecuencia de reloj opera a 16mA