Fei Song

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Research Interests

My research interests lie in **power electronics (PE)** and **power management (PM)**. I focus on the design and improvement of monolithic hybrid switched-capacitor topologies, low power delivery with a large conversion ratio, and energy harvesting power supplies.

Work Experience

Tsinghua University — Beijing, P.R.China
Full-time Research Assistant — *June 2025 – now*

Education Experience

University of Macau — Macau SAR, P.R.China
Master of Philosophy (M.Phil.) of Microelectronics, GPA: 3.56/4.0 — *Aug. 2022 – June 2025*

University of Electronic Science and Technology of China — Chengdu, Sichuan, P.R.China
Bachelor of Optoelectronic Information Science and Engineering, GPA: 3.67/4.0 — *Sep. 2018 – June 2022*

Publications

[1] S. Han, **F. Song**, Z. Zhu, X. Wu, H. Jiang, T. Ren, and Y. Lu, "A lego-like easy-stacking step-up sc converter with ultra-high and wide vcr using all input-stress-only devices," in *2025 IEEE Custom Integrated Circuits Conference (CICC)*, 2025, pp. 1–3.

[2] **F. Song**, S. Han, R. P. Martins, and Y. Lu, "An 85-to-230vac to 3.3-to-4.6vdc 1.52w capacitor-drop sigma-floating-sc ac-dc converter with 81.3% peak efficiency," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 68, 2025, pp. 1–3.

[3] **F. Song**, Y. Zhang, and J. Zhang, "Optimization of cnn-based garbage classification model," in *Proceedings of the 4th International Conference on Computer Science and Application Engineering*, ser. CSAE '20. New York, NY, USA: Association for Computing Machinery, 2020. [Online]. Available: https://doi.org/10.1145/3424978.3425089

Project Experience

An 85-230VAC input and 3.3-4.6VDC output AC-DC converter — *Oct. 2023 - Oct. 2024*

- A Sigma-Floating-SC topology is proposed to achieve 81.3% peak efficiency and 1.52W maximum output power.
- Up to 10% increased efficiency over a large load current range, compared with prior works.
- The design is fabricated in a 180nmBCD process and the manuscript has been accepted by ISSCC 2025.

Ultra-Light-Weight Multi-Chip Easy-Stacking Step-Up SC DC-DC Converter — *Oct. 2023 - Oct. 2024*

- The design is proposed to convert 5V voltage to 30V, 70V, and 150V to drive electrostatic and piezoelectric (PZT) actuators.
- The proposed topology combines local drivers and level-shifters together without bootstrap capacitors to reduce the driver loss.
- The design is fabricated in a 180nmBCD process and the manuscript has been accepted by CICC 2025.

A fast-transient response single-input-multiple-output DC-DC converter — *Sep. 2022 - Oct. 2023*

- The design utilize an auxiliary capacitor stacked with the input power source to increase the inductor charging speed and thereby improve the transient response.
- Collaborated with 3Peak INCORPORATED.

Low-power, high transient response LDO design without off-chip capacitors — *Nov. 2020 - Aug. 2021*

- Developed a bandgap with 1.2V voltage reference and 50nA current reference, whose power consumption was less than 200nW, in the temprature variation range of -40 to 125 degrees celsius.
- Developed a circuit of super positive feedback and self-bias amplifier, with static power consumption of 3-7uA and high bandwidth of 80M-160MHz.

- Won the first prize of National University Student Integrated Circuit Innovation and Entrepreneurship Competition in Southwest Devision (2021).

Smartphone-based Analysis of Non-destructive Apple Brix Measurement *Apr. 2021 - Aug. 2021*

- Designed an optical system using Zemax OpticStudio to achieve Czerny-Turner Spectroscope structure using a positive (converging) lens, two spherical mirrors, a blazed grating and a linear CCD.
- Designed a CCD driver board including a Xilinx FPGA, a Toshiba linear CCD, a high-speed and high-precision ADC and so on to capture light spectra and transmit digital spectra data to smart phones.
- Programmed verilog HDL codes on Xilinx FPGA to drive CCD and ADC, besides communicating with smart phones by USB protocol.
- Won the second prize of National University Student's Opt-Sci-Tech Competition (2021).

Intelligent Biological Microscope *Apr. 2020 - July. 2020*

- Designed a multi-method of resizing and merging limited images under microscope to make up a full cell image.
- Migrated M2Det algorithm to suit the blood cell recognizing, segmentation and counting.
- Developed a dataset of blood cells with five classification including neutrophils, lymphocytes, moncytes, eosinophils and basophils.
- Won the fisrt prize of National University Student's Opt-Sci-Tech Competition (2020) and the first prize of China-U.S. Young Maker Competition in Chengdu Division (2020).

Intelligent Device to Protect Children left in Cars *Apr. 2019 - July. 2019*

- Designed a multi-model network merged by AgeNet and Yolo-v2 to detect children left in cars.
- Used sensors such as temperature and humidity sensor, Oxygen sensor and AIoT to send data to private servers.
- Programmed a mobile app to receive warnings sent by servers to remind children's guardians of the states in cars about their children.
- Won the third prize of National University Student's Opt-Sci-Tech Competition (2019).

Honors & Awards

- First Prize of National University Student Integrated Circuit Innovation and Entrepreneurship Competition in Southwest Devision, 2021.
- Second Prize of National University Student's Opt-Sci-Tech Competition, 2021.
- First Prize of National University Student's Opt-Sci-Tech Competition, 2020.
- First Prize of China-U.S. Young Maker Competition in Chengdu Division, 2020.
- Third Prize of National University Student's Opt-Sci-Tech Competition, 2019.
- Third Prize of National Undergraduate Engineering Training Integration Ability Competition in Sichuan Province Division, 2019.

Work Experience

Excellent President of Application Electronics Association *Sep. 2019 – Sep. 2021*

Organized lectures and competitions about electronic design and program.

Member of UESTC Linux User Group *July 2020 – July 2021*

Technical Skills

Circuit Design: Printed Circuit Design, Integrated Circuit Design
Programming Languages: Verilog HDL, C for Embedded System, Python, Rust, High-Level Synthesis (HLS)
Developer Tools: Cadence (eg. Virtuoso, Capture CIS, Allegro), FPGA IDE (eg. Vivado, Diamond, Quartus,), MDK-ARM, STM32CubeIDE, CCS