	reg dist	reg write	ALU src	ALU op	Branch	Jump	Mem read	Mem write	Mem to Reg
Add	1	1	0	0	0	0	0	0	1
AddU	1	1	0	0	0	0	0	0	1
Sub	1	1	0	0	0	0	0	0	1
SubU	1	1	0	0	0	0	0	0	1
AddI	0	0	0	10	0	0	0	0	0
AddIU	0	0	0	10	0	0	0	0	0
AND	1	1	0	0	0	0	0	0	1
ANDI	0	0	0	10	0	0	0	0	0
OR	1	1	0	0	0	0	0	0	1
ORI	0	0	0	10	0	0	0	0	0
XOR	1	1	0	0	0	0	0	0	1
XORI	0	0	0	10	0	0	0	0	0
NOR	1	1	0	0	0	0	0	0	1
SLT	1	1	0		0	0	0	0	1
SLTU	1	1	0	0	0	0	0	0	1
SLTI	1	1	0	10	0	0	0	0	1
SLTIU	1	1	0	0	0	0	0	0	1
CLO	1	1	0	0	0	0	0	0	1
CLZ	1	1	0	0	0	0	0	0	1
SLL	1	1	0	0	0	0	0	0	1
SLLV	1	1	0	0	0	0	0	0	1
SRA	1	1	0	0	0	0	0	0	1
SRAV	1	1	0	0	0	0	0	0	1
SRL	1	1	0	0	0	0	0	0	1
SRLV	1	1	0	0	0	0	0	0	1
MOVN	1	1	0	0	0	0	0	0	1
MOVZ	1	1	0	0	0	0	0	0	1
LUI load upper	0	0	0	10	0	0	0	0	0
LW load word	0	1	1	10	0	0	1	0	0
LB load byte	0	1	1	10	0	0	1	0	0
LBU	0	1	1	10	0	0	1	0	0
SD	0	1	1	10	0	0	0	1	0
SW store word	0	1	1	10	0	0	0	1	0

SH store half	0	1	1	10	0	0	0	1	0
SB stored byte	0	1	1	10	0	0	0	1	0
BEQ	0	0	0	0	1	0	0	0	0
BGEZ	0	0	0	0	1	0	0	0	0
BGTZ	0	0	0	0	1	0	0	0	0
BLEZ	0	0	0	0	1	0	0	0	0
BLTZ	0	0	0	0	1	0	0	0	0
BLTZAL	0	0	0	0	1	0	0	0	0
BNE	0	0	0	0	1	0	0	0	0
J	0	0	0	0	0	1	0	0	0
JAL	0	0	0	0	0	1	0	0	0
JALR	0	0	0	0	0	1	0	0	0
JR	0	0	0	0	0	1	0	0	0