UNIMORE
UNIVERSITÀ DEGLI STUDI DI MODENA E REGGIO EMILIA

Dipartimento di Scienze Fisiche, Informatiche e Matematiche

3. Prestazioni dei Computer

Architettura dei calcolatori [MN1-1143]

Corso di Laurea in INFORMATICA
(D.M.270/04) [16-215]
Anno accademico 2022/2023

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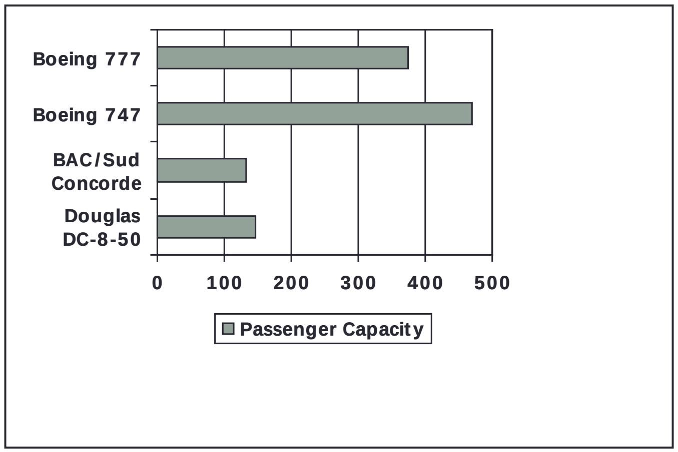
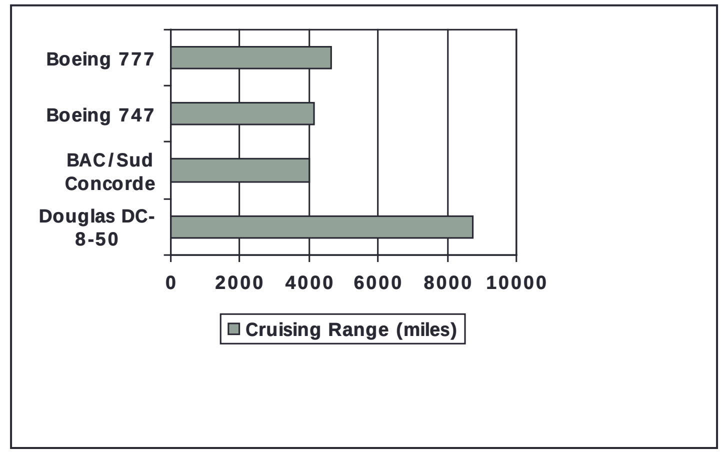
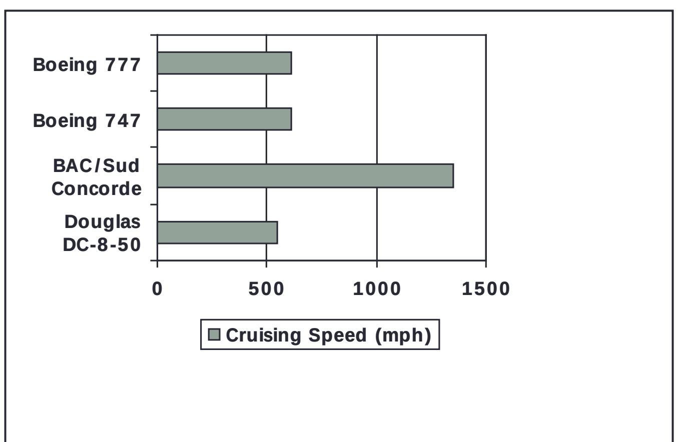
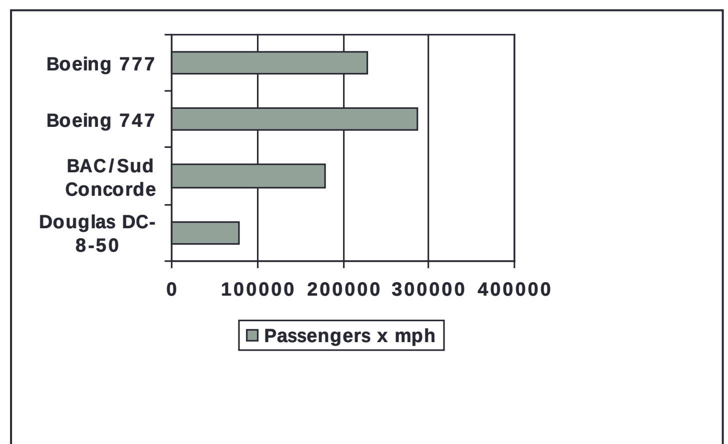
Defining Performance

- Which airplane has the best performance?









Response Time and Throughput

- **Response time (latency, execution time)**
  - How long it takes to do a task
- **Throughput**
  - Total work done per unit time
    - e.g., tasks/transactions/… per hour
- How are response time and throughput affected by
  - Replacing the processor with a faster version?
  - Adding more processors?
- We’ll focus on response time for now…

Understanding Computer Performance

What determines the performance of a program?

- Algorithm
  - Determines number of operations executed

```
ALGORITHM 1

BEGIN:
        ISTR1
        ISTR2
        ISTR3
        ISTR4
        ...
        ISTR20
END
```

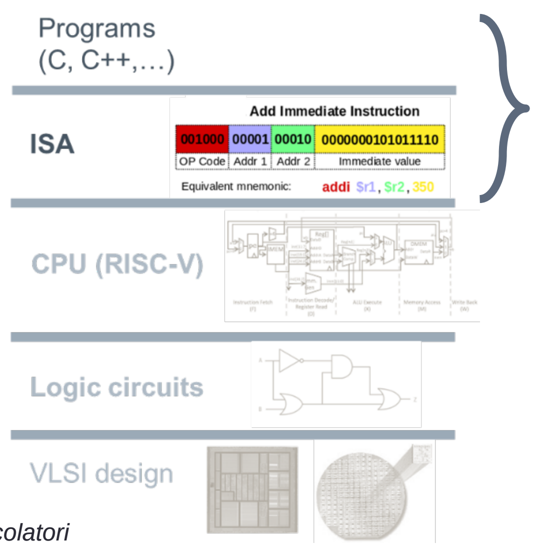
```
ALGORITHM 2

BEGIN:
        ISTR1
        ISTR2
        ISTR3
        ISTR4
        ...
        ISTR15
END
```

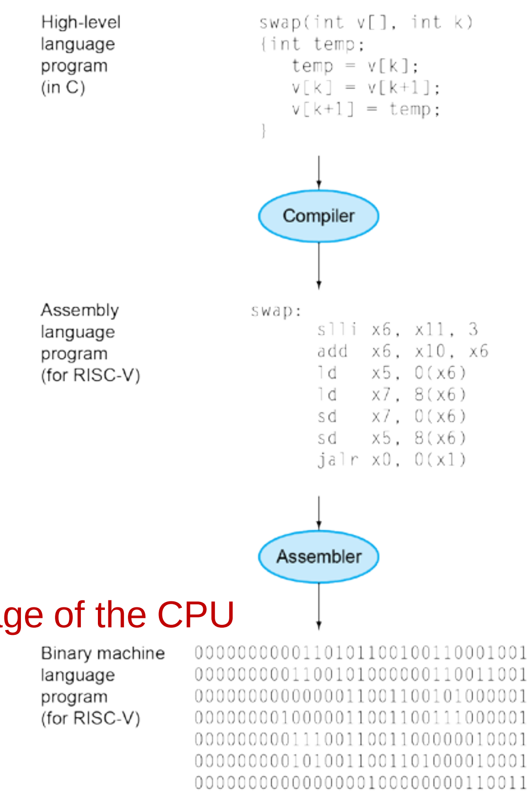
Understanding Computer Performance

What determines the performance of a program?

- Algorithm
  - Determines number of operations executed

- Programming language, compiler, architecture
  - Determine number of machine instructions executed per operation





language of the CPU

The HW/SW interface

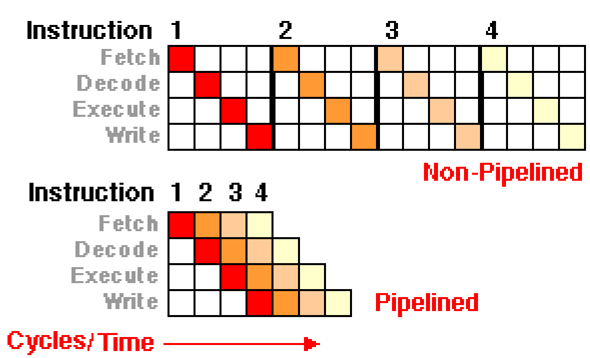
ISA

001000	00001	00010	0000000101011110
OP Code	Addr 1	Addr 2	Immediate value

Understanding Computer Performance

What determines the performance of a program?

- Algorithm
  - Determines number of **operations** executed
- Programming language, compiler, architecture
  - Determine number of **machine instructions** executed per operation
- Processor and memory system
  - Determine how **fast** instructions are executed



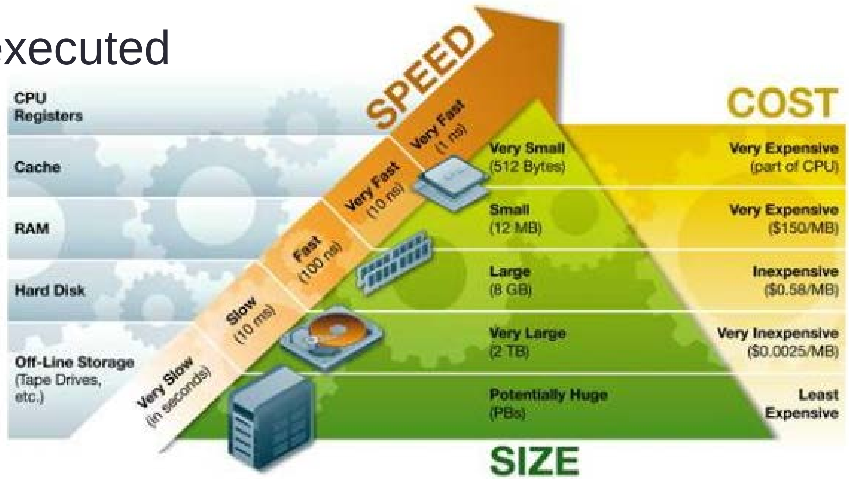
Understanding Computer Performance

What determines the performance of a program?

- Algorithm
  - Determines number of **operations** executed
- Programming language, compiler, architecture
  - Determine number of **machine instructions** executed per operation

The HW/SW interface

- Processor and memory system
  - Determine how **fast** instructions are executed
- I/O system (including OS)
  - Determines how fast I/O operations are executed



Relative Performance

- Define **Performance = 1/Execution Time**
- "X is n time faster than Y"

$$\text{Performance}_X / \text{Performance}_Y$$
$$= \text{Execution time}_Y / \text{Execution time}_X = n$$

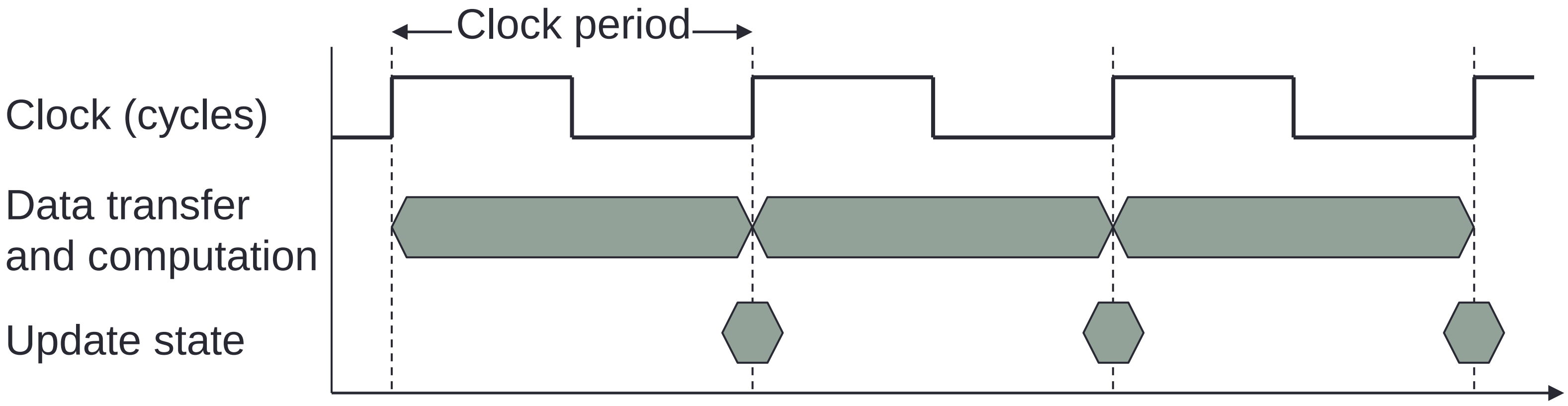
- **Example**: time taken to run a program
  - 10s on A, 15s on B
  - Execution Time_B / Execution Time_A
    = 15s / 10s = 1.5
  - So A is 1.5 times faster than B

Measuring Execution Time

- **Elapsed time**
  - Total response time, including all aspects
    - Processing, I/O, OS overhead, idle time
  - Determines system performance
- **CPU time**
  - Time spent processing a given job
    - Discounts I/O time, other jobs' shares
  - Comprises user CPU time and system CPU time
  - Different programs are affected differently by CPU and system performance

CPU Clocking

- Operation of digital hardware governed by a constant-rate clock



- **Clock period**: duration of a clock cycle
  - e.g., 250ps = 0.25ns = 250×10^{-12}s
- **Clock frequency (rate)**: cycles per second
  - e.g., 4.0GHz = 4000MHz = 4.0×10^{9}Hz

CPU Time

$$\text{CPU Time} = \text{CPU Clock Cycles} \times \text{Clock Cycle Time}$$

$$= \frac{\text{CPU Clock Cycles}}{\text{Clock Rate}}$$

- Performance improved by
  - Reducing number of clock cycles
  - Increasing clock rate
  - Hardware designer must often trade off clock rate against cycle count

CPU Time Example

- Computer A: 2GHz clock, 10s CPU time
- Designing Computer B
  - Aim for 6s CPU time
  - Can do faster clock, but causes 1.2 × clock cycles
- How fast must Computer B clock be?

$$\text{Clock Rate}_B$$

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$$= 10s \times 2GHz = 20 \times 10^9$$

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$$\text{Clock Rate}_B = \frac{1.2 \times 20 \times 10^9}{6s} = \frac{24 \times 10^9}{6s} = 4\text{GHz}$$

Instruction Count and CPI

$$\text{Clock Cycles} = \text{Instruction Count} \times \text{Cycles per Instruction}$$

$$\text{CPU Time} = \text{Instruction Count} \times \text{CPI} \times \text{Clock Cycle Time}$$

$$= \frac{\text{Instruction Count} \times \text{CPI}}{\text{Clock Rate}}$$

- **Instruction Count** for a program
  - Determined by program, ISA and compiler

- Average **cycles per instruction (CPI)**
  - Determined by CPU hardware
  - If different instructions have different *CPI*
    - Average CPI affected by instruction mix

CPI Example

- Computer A: Cycle Time = 250ps, CPI = 2.0
- Computer B: Cycle Time = 500ps, CPI = 1.2
- Same ISA
- Which is faster, and by how much?

$$\text{CPU Time}_A$$

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$$

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A is faster…

$$\text{CPU Time}_B = \text{Instruction Count} \times \text{CPI}_B \times \text{Cycle Time}_B$$

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$$

A is faster…

$$
\frac{\text{CPU Time}_B}{\text{CPU Time}_A}
$$

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$$\frac{\text{CPU Time}_B}{\text{CPU Time}_A} = \frac{I \times 600\text{ps}}{I \times 500\text{ps}} = 1.2$$

…by this much

CPI in More Detail

- If different instruction classes take different numbers of cycles

$$\text{Clock Cycles} = \sum_{i=1}^{n} (\text{CPI}_i \times \text{Instruction Count}_i)$$

- Weighted average CPI

$$\text{CPI} = \frac{\text{Clock Cycles}}{\text{Instruction Count}} = \sum_{i=1}^{n} \left(\text{CPI}_i \times \underbrace{\frac{\text{Instruction Count}_i}{\text{Instruction Count}}}_{\text{Relative frequency}} \right)$$

CPI Example

- Alternative compiled code sequences using instructions in classes A, B, C

Class	A	B	C
CPI for class	1	2	3
IC in sequence 1	2	1	2
IC in sequence 2	4	1	1

- Sequence 1: IC = 5
  - Clock Cycles $= 2\times1 + 1\times2 + 2\times3 = 10$
  - Avg. CPI = 10/5 = 2.0
- Sequence 2: IC = 6
  - Clock Cycles $= 4\times1 + 1\times2 + 1\times3 = 9$
  - Avg. CPI = 9/6 = 1.5

Other performance metrics

- IPC – Instructions Per Cycle
  - How many instruction (on average) can a processor retire per cycle?

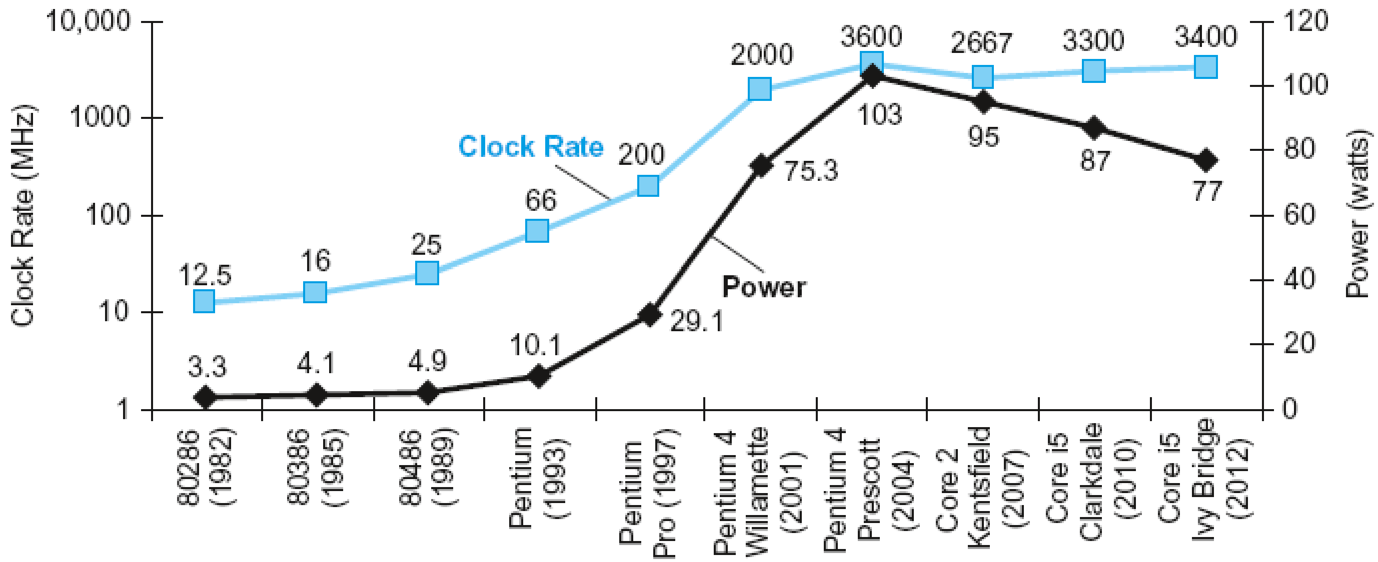
$$\mathrm{IPC} = \frac{\text{Instruction Count}}{\text{Clock Cycles}} = \frac{1}{\text{CPI}}$$

Performance Summary

$$\text{CPU Time} = \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Clock cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Clock cycle}}$$

- Performance depends on
  - **Algorithm**: affects IC, possibly CPI
  - **Programming language**: affects IC, CPI
  - **Compiler**: affects IC, CPI
  - **Instruction set architecture (ISA)**: affects IC, CPI, T_c

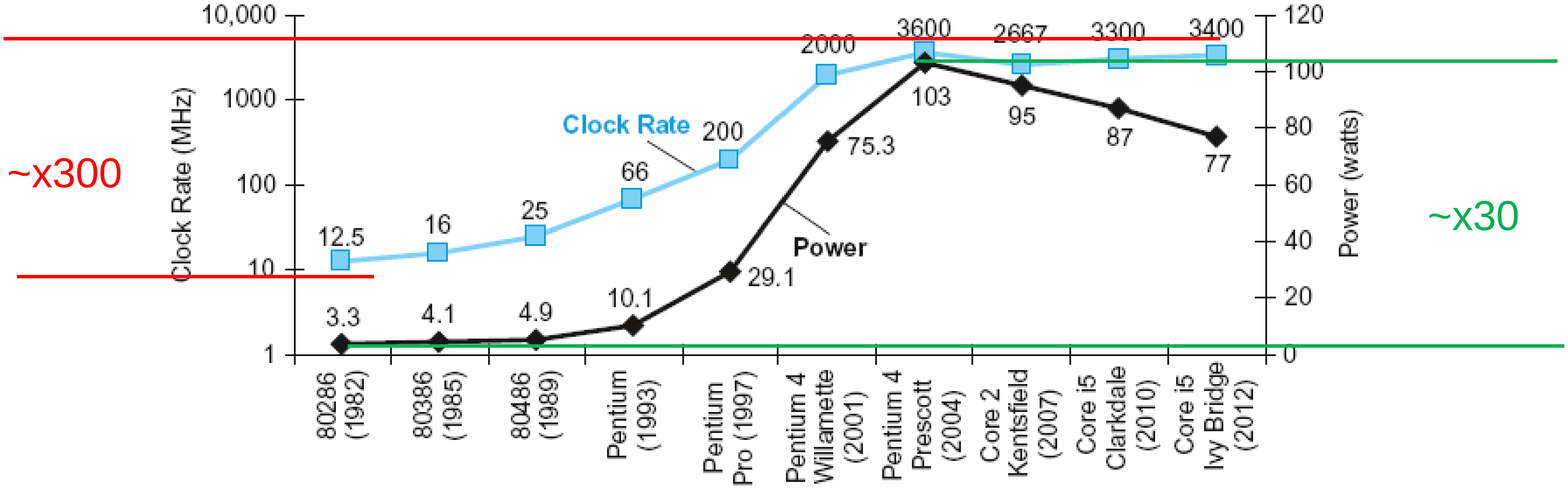
Power Trends



- In CMOS IC technology

$$\text{Power} = \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency}$$

Power Trends



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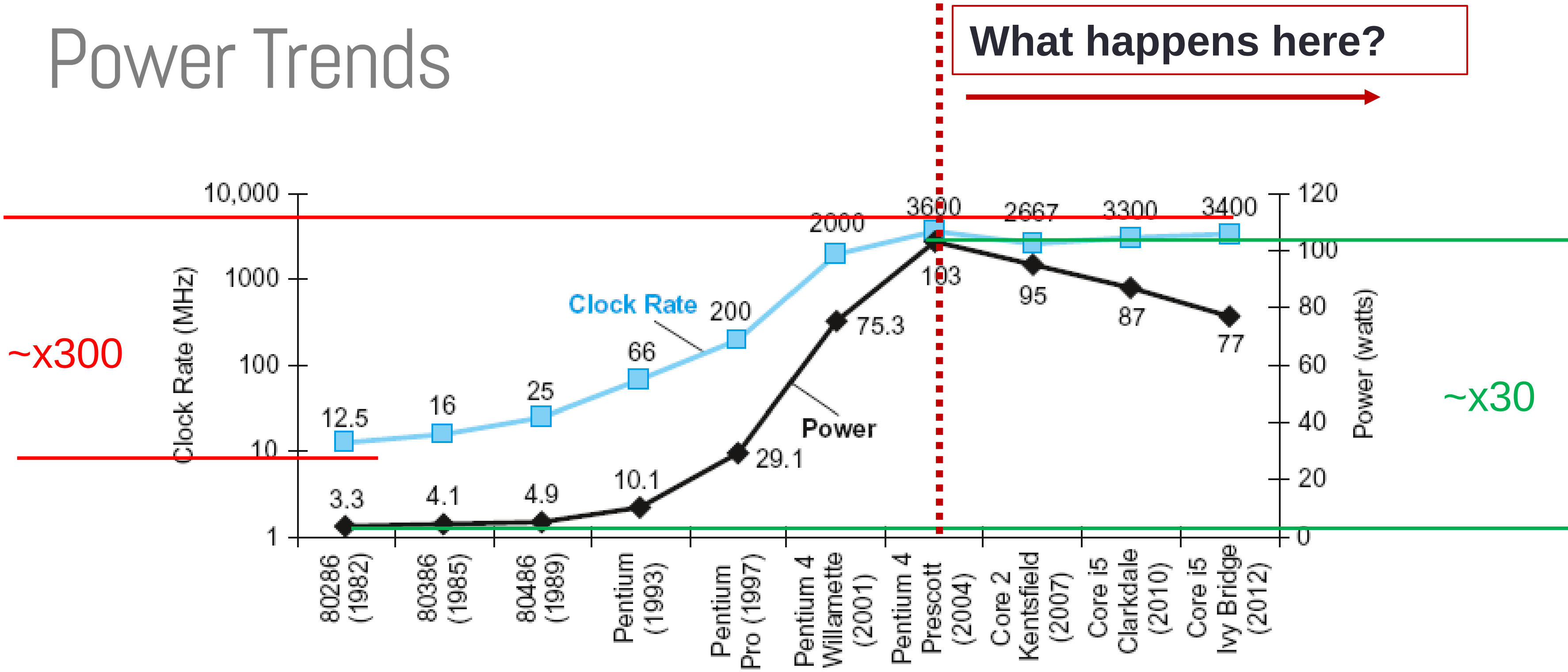
×30

5V → 1V

×1000

Power Trends



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×30

5V → 1V

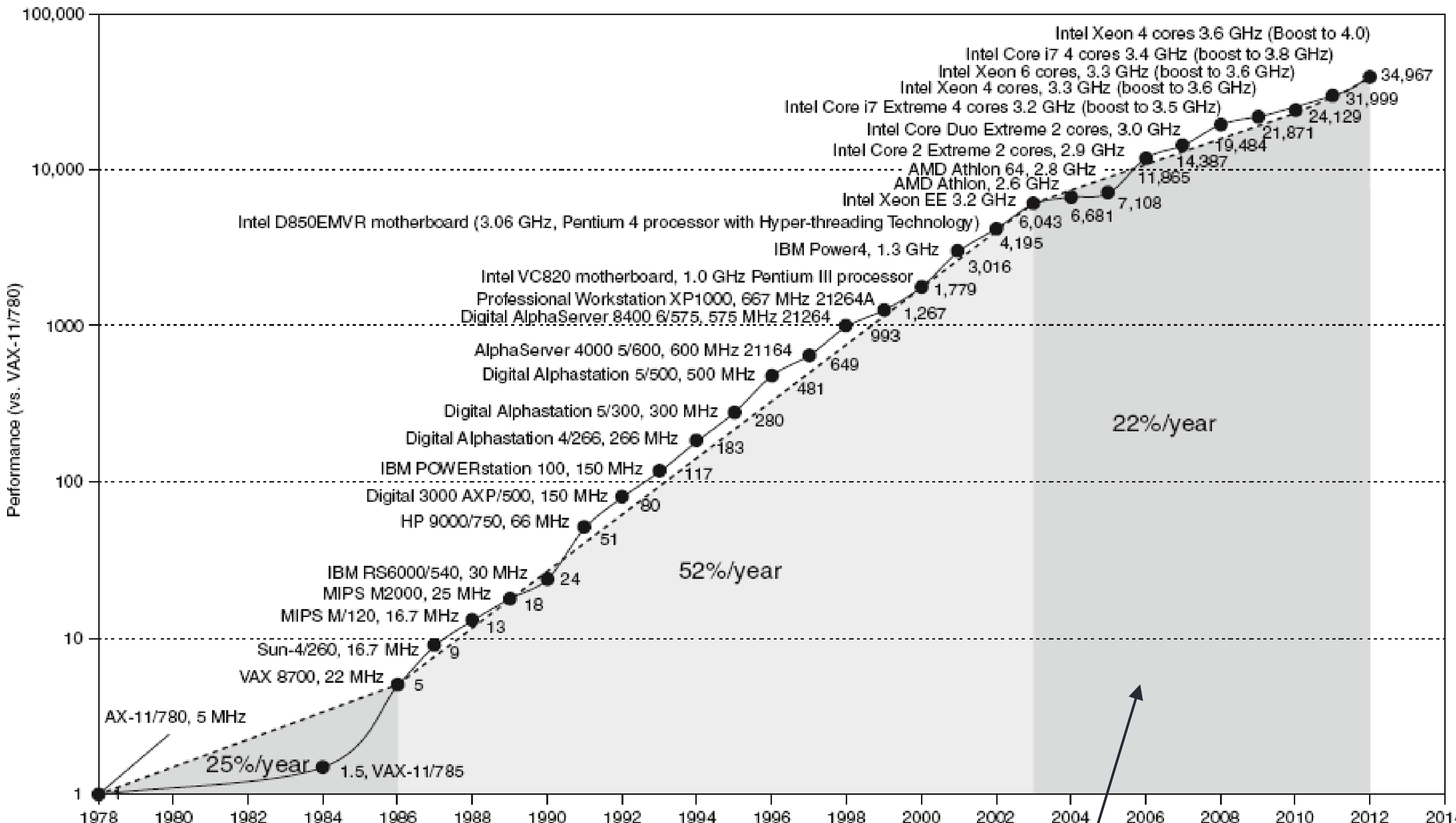
×1000

Reducing Power

- The power wall *(around 2004…)*
  - We can’t reduce voltage further
  - We can’t remove more heat

- How else can we improve performance?

Uniprocessor Performance

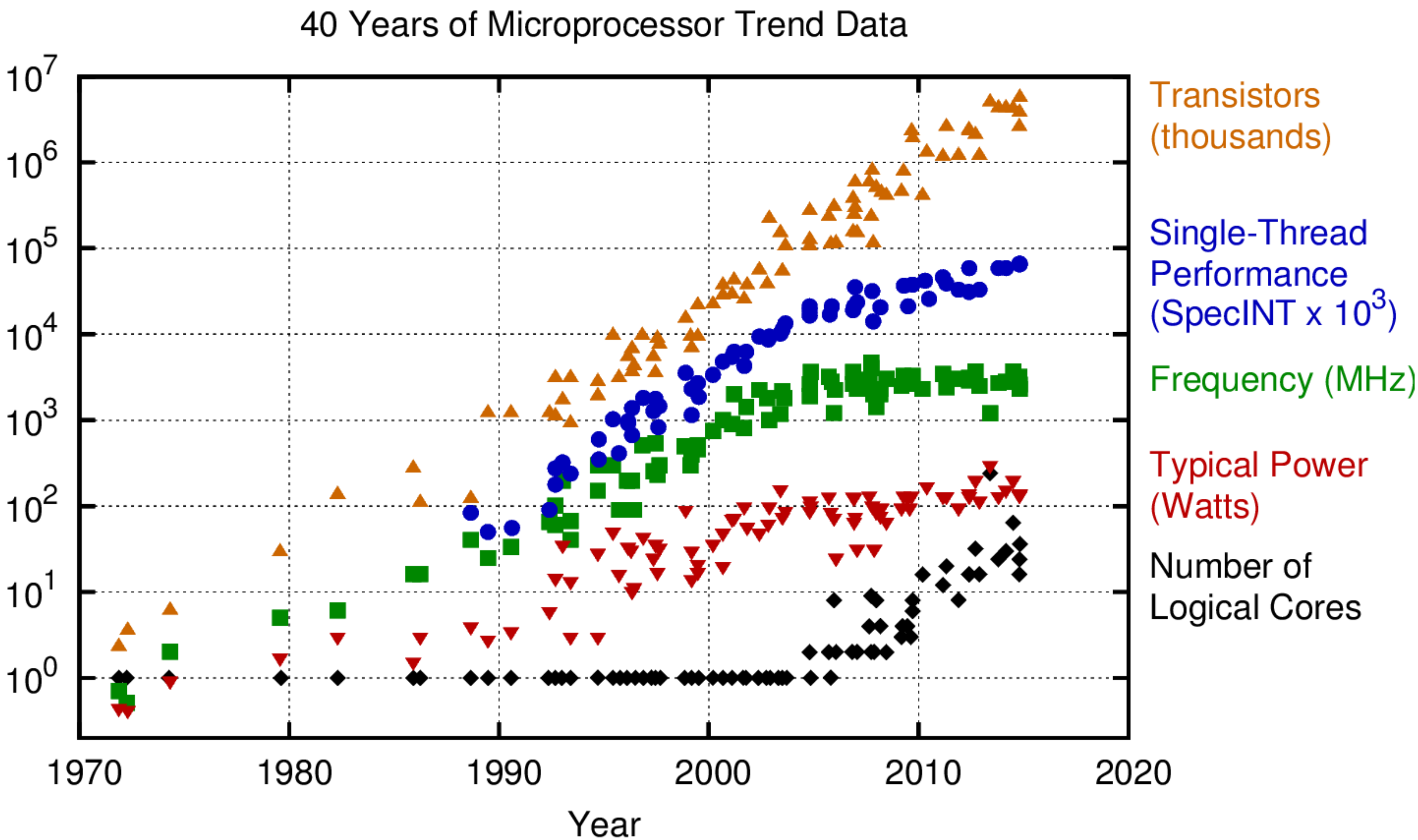


Constrained by power, instruction-level parallelism, memory latency

Multiprocessors

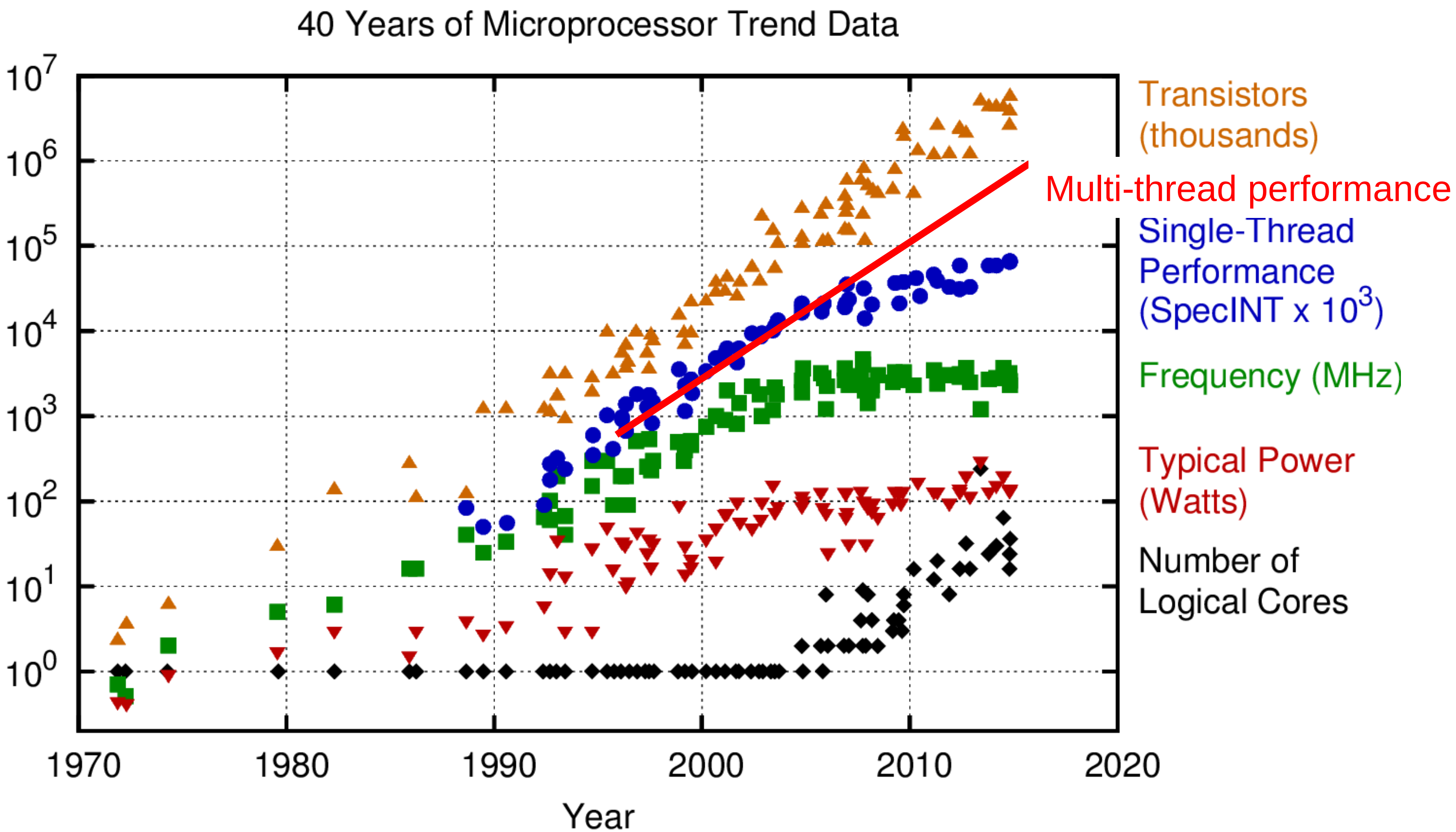
- Multicore microprocessors
  - More than one processor per chip

The multicore revolution



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2015 by K. Rupp

The multicore revolution



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Multiprocessors

- Multicore microprocessors
  - More than one processor per chip
- Requires explicitly parallel programming
  - Compare with instruction level parallelism
    - Hardware executes multiple instructions at once
    - Hidden from the programmer
  - Hard to do
    - Programming for performance
    - Load balancing
    - Optimizing communication and synchronization

Il contenuto del corso di High Performance Computing alla magistrale

Relative Performance – **Speedup**

- "X is n time faster than Y"

$$\text{Performance}_X / \text{Performance}_Y = \text{Execution time}_Y / \text{Execution time}_X = n$$

- **Speedup** is the relative performance of a "new" or *improved* system compared to an "old" system

Execution time of the "new" (**improved**) system

- **Speedup = T_{old}/T_{new}**

Execution time of the "old" system

Pitfall: **Amdahl's Law**

- Improving an aspect of a computer and expecting a proportional improvement in overall performance

$$\mathrm{T_{improved}} = \frac{\mathrm{T_{affected}}}{\text{improvement factor}} + \mathrm{T_{unaffected}}$$

- Example: multiply accounts for 80s/100s
  - How much improvement in multiply performance to get Speedup=5?

$$T_{old} = 100 = T_{affected} + T_{unaffected} = 80 + 20$$

$$T_{new} = T_{improved} = \frac{80}{n} + 20$$

$$Speedup = \frac{T_{old}}{T_{new}} = 5 \rightarrow \frac{T_{old}}{5} = T_{new} \rightarrow \frac{100}{5} = \frac{80}{n} + 20 = 20$$

Can't be done!

Other performance metrics

- MIPS: Millions of Instructions Per Second
  - Doesn't account for
    - Differences in ISAs between computers
    - Differences in complexity between instructions

$$\text{MIPS} = \frac{\text{Instruction count}}{\text{Execution time} \times 10^6}$$

$$= \frac{\text{Instruction count}}{\dfrac{\text{Instruction count} \times \text{CPI}}{\text{Clock rate}} \times 10^6} = \frac{\text{Clock rate}}{\text{CPI} \times 10^6}$$

› CPI varies between programs on a given CPU

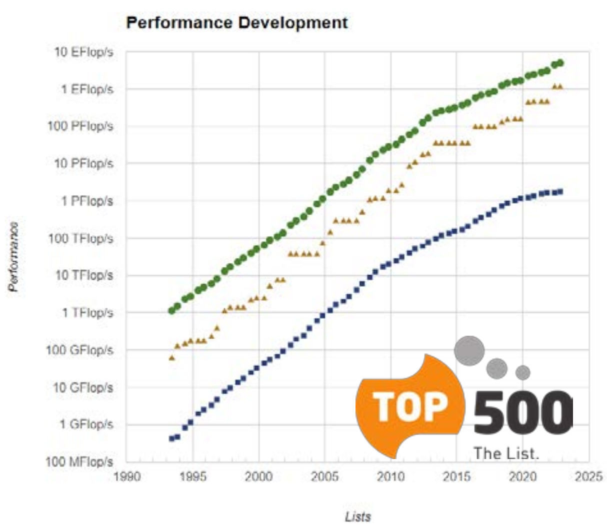
Many more…

- Single Precision Floating Point Operations per seconds (FLOPs/s)

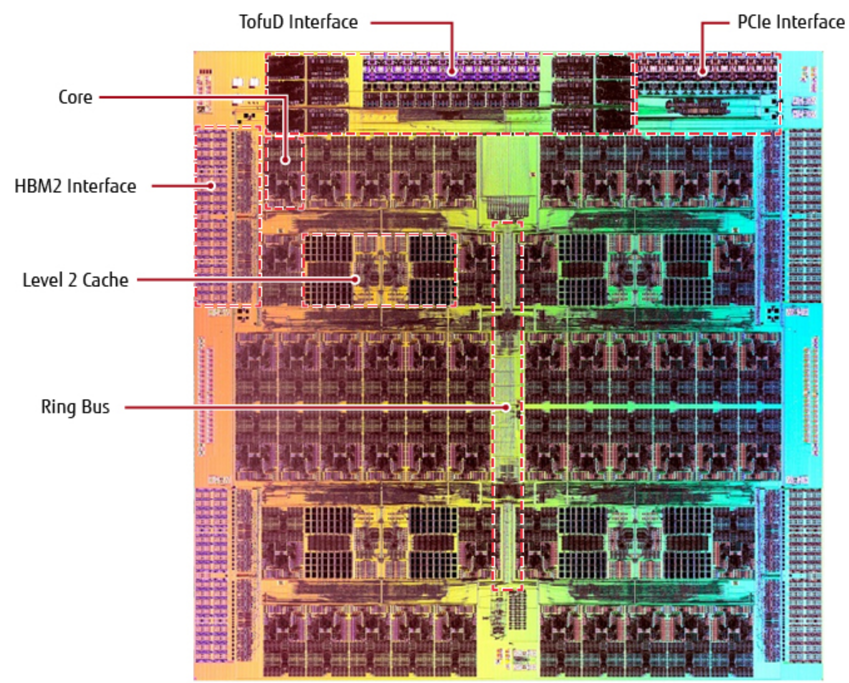
- Power Efficiency (Throughput/Power) -> FLOPS/s / W
- Area Efficiency (Throughput/Area) -> FLOPS/s / mm^2

Recap

- **Performance Metrics**
  - CPU Time
  - Throughput (Inst/Cycles)
  - CPI / IPC
- **Comparative Metrics**
- Speedup
- Amdahl's Law
- **Multi-core Evolution**



https://www.top500.org



Fujitsu A64FX

Evaluation (it is your moment)

- Go to

  https://menti.com

- Insert the Code

  4820 7008

Mentimeter

https://www.menti.com/alzx4j6q7b8u