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| --- | --- |
| **Computer Architectures 02GOLOV** | Delivery date:  **October, 9th 2024** |
| **Laboratory**  **1** | Expected delivery of lab\_01.zip including:   * lab\_01.pdf (fill and export this file to pdf) |

This first lab is very introductory. Through it, you are expected to learn how to use WinMIPS and do the assigned task.

1. The first thing to do is open the winmipstut.docx file and follow the WinMIPS documentation. Through it, you are expected to learn the basics of using WinMIPS so that you are ready to take on the next assignment.
2. Consider a MIPS architecture with the following characteristics:

* Integer ALU: 1 clock cycle
* Data memory: 1 clock cycle
* FP arithmetic unit: pipelined, 2 clock cycles
* FP multiplier unit: pipelined, 8 clock cycles
* FP divider unit: not pipelined, 10 clock cycles

Given the following piece of code, run it on WinMIPS and see what it does. For each instruction, add a comment to describe what the instruction does using the same style of commenting as the example. Next, write down the number of clock cycles required to execute the first iteration of the following code. Since this is a pipelined processor, the number of clock cycles must be calculated as the number of clock cycles required in addition to the previous instruction.

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* MIPS64 \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

|  |  |  |
| --- | --- | --- |
| .data | comments | Clock cycles |
| v1: .byte 1, 2, 3, 4, 5 |  |  |
| v2: .byte 1, 2, 3, 4, 5 |  |  |
| v3: .space 5  v4: .space 5 |  |  |
|  |  |
| .text |  |  |
| daddui r5,r0,0 | r5 ← pointer (i) | 5 |
| daddui r6,r0,5 | r6 ← 5 | 1 |
| cycle: lb r1,v1(r5) | r1 ← v1[i] | 1 |
| lb r2,v2(r5) | r2 <- v2[i] | 1 |
| daddu r3,r1,r2 | r3 <- r1 + r2 | 2 |
| dsub r4,r1,r2 | r4 <- r1 – r2 | 1 |
| sb r3,v3(r5) | v3[i] <- r3 | 1 |
| sb r4,v4(r5) | v4[i] <- r4 | 1 |
| daddui r5,r5,1 | r5 <- r5 + 1 | 1 |
| daddi r6,r6,-1 | R6 <- r6 - 1 | 1 |
| bnez r6,cycle | if r6 != 0 goto cycle | 2 |
| halt | halt | 1 |
| Total: |  | **18** |

Now, translate the above code in your preferred high-level language (i.e. C, Java, Python, C++, Javascript).

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* Used language \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

int main() {

int v1[] = {1,2,3,4,5};

int v2[] = {5,4,3,2,1};

int v3[5] = {0};

int v4[5] = {0};

int r1, r2, r3, r4, i, r6;

r1 = r2 = r3 = r4 = i = r6 = 0;

r6 = 0 + 5;

do {

r1 = v1[i];

r2 = v2[i];

r3 = r1 + r2;

r4 = r1 - r2;

v3[i] = r3;

v4[i] = r4;

i += 1;

r6 -= 1;

} while (r6 != 0);

return 0;

}

1. Now, repeat the same operation done previously with this piece of code:

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* MIPS64 \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

|  |  |  |
| --- | --- | --- |
| .data | comments | Clock cycles |
| v1: .double 1, 2, 3, 4, 5 |  |  |
| v2: .double 5, 4, 3, 2, 1 |  |  |
| v3: .double 6, 7, 8, 9, 10  v4: .double 10, 9, 8, 7, 6  v5: .space 40  v6: .space 40 |  |  |
|  |  |
|  |  |
|  |  |
|  |  |  |
| .text |  |  |
| daddui r1,r0,0 | R1 ← 0 | 5 |
| daddui r2,r0,5 | R2 ← 5 | 1 |
| cycle: l.d f1, v1(r1) | F1 ← v1[r1] | 1 |
| l.d f2, v2(r1) | F2 ← v2[r1] | 1 |
| l.d f3, v3(r1) | F3 ← v3[r1] | 1 |
| l.d f4, v4(r1) | F4 ← v4[r1] | 1 |
| mul.d f5, f1, f2 | F5 ← f1 \* f2 | 8 |
| mul.d f6, f3, f4 | F6 ← f3 \* f4 | 1 |
| s.d f5, v5(r1) | v5[r1] ← f5 | 1 |
| s.d f6, v6(r1) | v6[r1] ← f6 | 1 |
| daddui r1,r1,8 | R1 ← r1 + 8 | 1 |
| daddi r2,r2,-1 | R2 ← r2 - 1 | 1 |
| bnez r2,cycle | If (r2 != 0) goto cycle | 2 |
| halt | halt | 1 |
| Total: |  | **26** |

Now, translate the above code in your preferred high-level language (i.e. C, Java, Python, C++, Javascript).

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* Used language \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

int main() {

int v1[] = {1,2,3,4,5};

int v2[] = {5,4,3,2,1};

int v3[] = {6,7,8,9,10};

int v4[] = {10,9,8,7,6};

int v5[40] = {0};

int v6[40] = {0};

int r1, r2;

r1 = r2 = 0;

double f1, f2, f3, f4;

f1 = f2 = f3 = f4 = 0;

r2 = 0 + 5;

do {

f1 = v1[r1];

f2 = v2[r1];

f3 = v3[r1];

f4 = v4[r1];

f5 = f1 \* f2;

f6 = f3 \* f4;

v5[r1] = f5;

v6[r1] = f6;

r1 += 8;

r2 -= 1;

} while (r2 != 0);

return 0;

}

Relative to the above code, how much would the performance of the software increase if you could improve the functional unit related to the floating point multiplication of 4 clock cycles?

Using Amhdal’s law

We know the whole program takes 106 cycles.

Multiplications take (8+1)\*5=45 cycles. That’s because the loop runs 5 times.

Speedup = 1/((1-p) + p/s) = 1.23253903

where

p = 45/106 = 0.4245

s = 45/(4+1)\*5 = 45/25 = 1.8

**Appendix: *winMIPS64 Instruction Set***

***WinMIPS64***

The following assembler directives are supported

.data - start of data segment

.text - start of code segment

.code - start of code segment (same as .text)

.org <n> - start address

.space <n> - leave n empty bytes

.asciiz <s> - enters zero terminated ascii string

.ascii <s> - enter ascii string

.align <n> - align to n-byte boundary

.word <n1>,<n2>.. - enters word(s) of data (64-bits)

.byte <n1>,<n2>.. - enter bytes

.word32 <n1>,<n2>.. - enters 32 bit number(s)

.word16 <n1>,<n2>.. - enters 16 bit number(s)

.double <n1>,<n2>.. - enters floating-point number(s)

where <n> denotes a number like 24, <s> denotes a string like "fred", and

<n1>,<n2>.. denotes numbers seperated by commas.

The following instructions are supported

lb - load byte

lbu - load byte unsigned

sb - store byte

lh - load 16-bit half-word

lhu - load 16-bit half word unsigned

sh - store 16-bit half-word

lw - load 32-bit word

lwu - load 32-bit word unsigned

sw - store 32-bit word

ld - load 64-bit double-word

sd - store 64-bit double-word

l.d - load 64-bit floating-point

s.d - store 64-bit floating-point

halt - stops the program

daddi - add immediate

daddui - add immediate unsigned

andi - logical and immediate

ori - logical or immediate

xori - exclusive or immediate

lui - load upper half of register immediate

slti - set if less than or equal immediate

sltiu - set if less than or equal immediate unsigned

beq - branch if pair of registers are equal

bne - branch if pair of registers are not equal

beqz - branch if register is equal to zero

bnez - branch if register is not equal to zero

j - jump to address

jr - jump to address in register

jal - jump and link to address (call subroutine)

jalr - jump and link to address in register (call subroutine)

dsll - shift left logical

dsrl - shift right logical

dsra - shift right arithmetic

dsllv - shift left logical by variable amount

dsrlv - shift right logical by variable amount

dsrav - shift right arithmetic by variable amount

movz - move if register equals zero

movn - move if register not equal to zero

nop - no operation

and - logical and

or - logical or

xor - logical xor

slt - set if less than

sltu - set if less than unsigned

dadd - add integers

daddu - add integers unsigned

dsub - subtract integers

dsubu - subtract integers unsigned

add.d - add floating-point

sub.d - subtract floating-point

mul.d - multiply floating-point

div.d - divide floating-point

mov.d - move floating-point

cvt.d.l - convert 64-bit integer to a double FP format

cvt.l.d - convert double FP to a 64-bit integer format

c.lt.d - set FP flag if less than

c.le.d - set FP flag if less than or equal to

c.eq.d - set FP flag if equal to

bc1f - branch to address if FP flag is FALSE

bc1t - branch to address if FP flag is TRUE

mtc1 - move data from integer register to FP register

mfc1 - move data from FP register to integer register