ECE385

Fall 2020

Experiment 1

Introductory Experiment

Name: Zhang Yichi
Lab Section: LA3
TA's Name: Yu Yuqi

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1 Introduction

1.1 Purpose of Circuit

The purpose of this lab is to build a two to one multiplexer (mux) which allows us to select the signals we want. A two to one mux uses an one digital signal to select one of the two input signals to be the output signal. Using the same principle, much more complicated muxes could be built. With n signals, we can select one output signal from 2^n input signals. This can be used later in the memory to select the correct unit corresponding to the desired address.

Another prupose of this lab is to show the static hazard. In ECE120, we choose to ignore certain aspects of circuit design to emphasize a strong theoretical base for further study [1], e.g. the static hazard. However, in this lab, it will be no longer ignored. We will observe the static hazard, analyze the reason why it happens and try to eliminate it.

2 Documentation

2.1 Written Description of Circuit

There are three input signals A, B and C in our circuit. A and C are the potential output signals. B is the signal to select which one is the output. All of them form a two to one mux. Use Z to denote the output, then $Z = AB + B'C$ in part A. However, in this way, the inverter will create a delay and cause static hazard. To eliminate it, we add a new combination term of input, AC, in part B which makes the output $Z = AB + B'C + AC$. In this case, with $AC = 1$, whenever B switches from 0 to 1 or 1 to 0, the AC term will continuously give the output an 1 to make it stable at 1. Detailed illustration will be presented as timing diagram in the Documentation part.

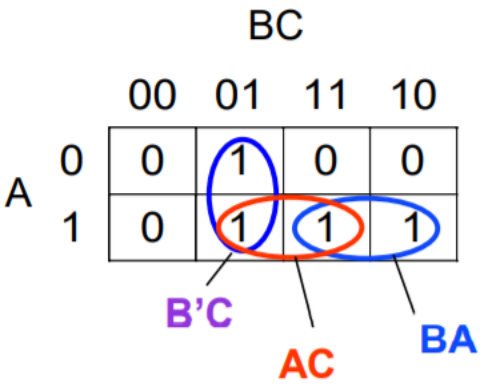

Figure 1: K-map for the theoretical principle. The blue circle is for part A and the red circle is for the added term AC in part B [2].

2.2 Logic Diagrams

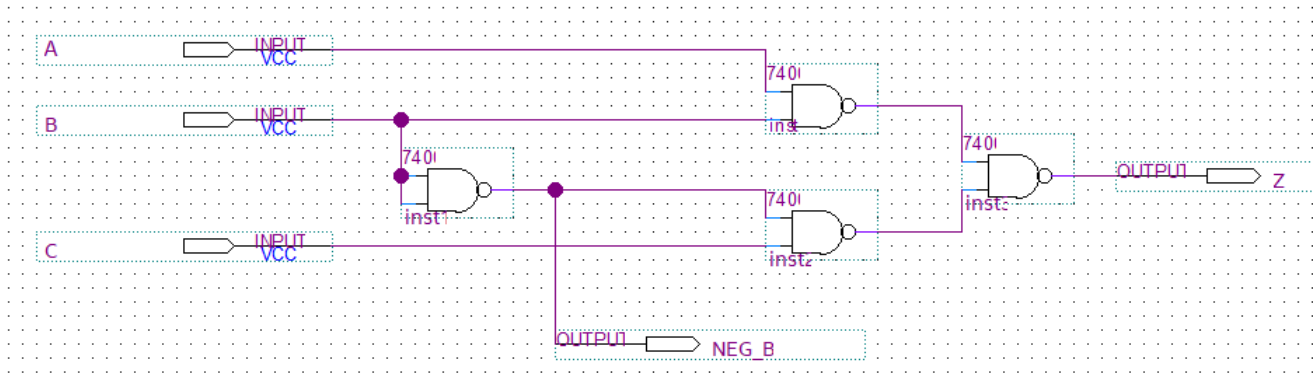

Figure 2: Circuit of part A without DELAY module

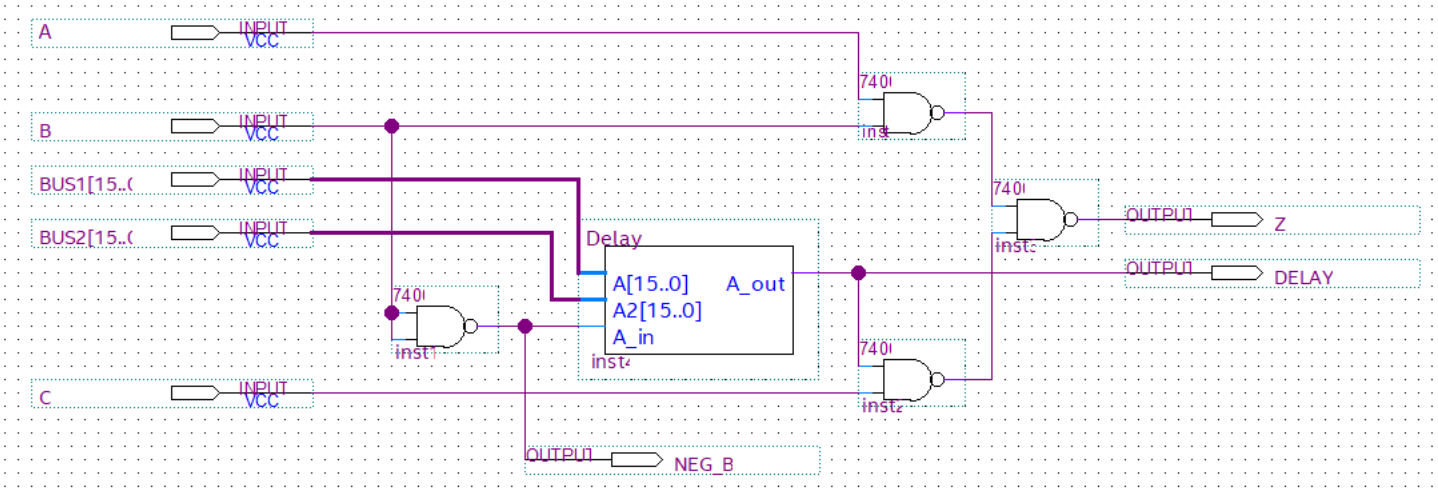

Figure 3: Circuit of part A with DELAY module

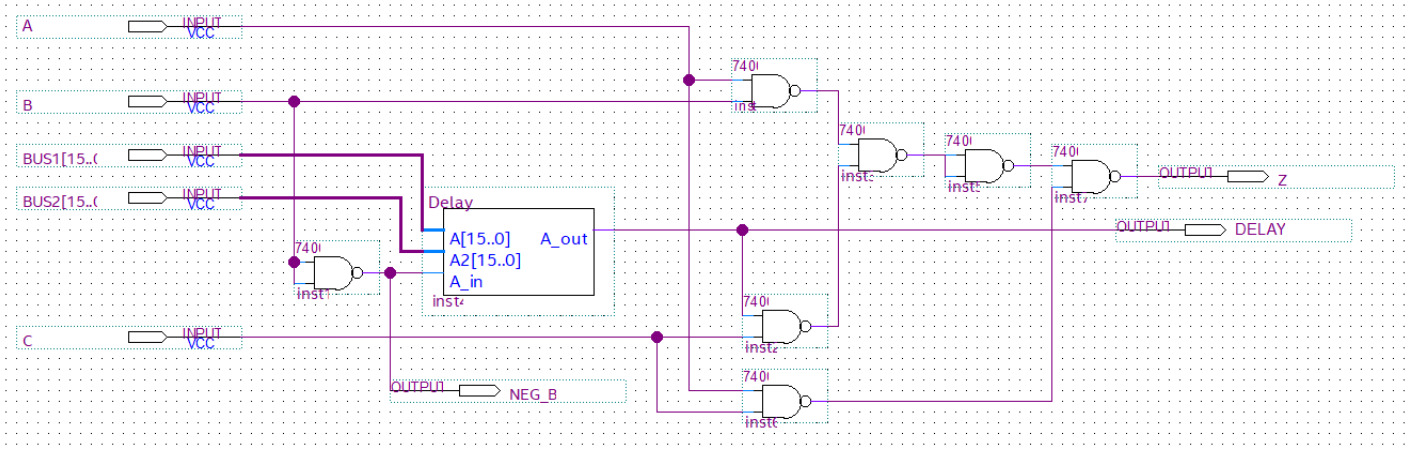

Figure 4: Circuit of part B

2.3 Annotated Simulation Waveform

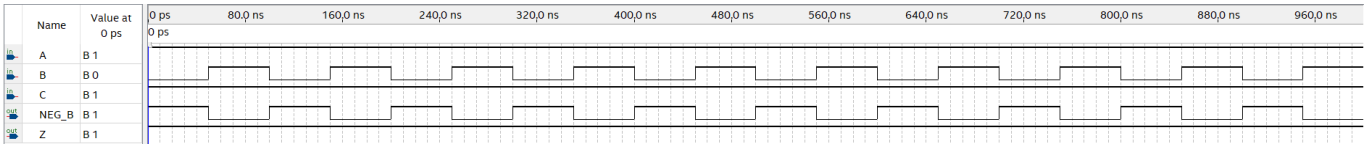

Figure 5: Waveform of part A by functional simulation. No delay considered.

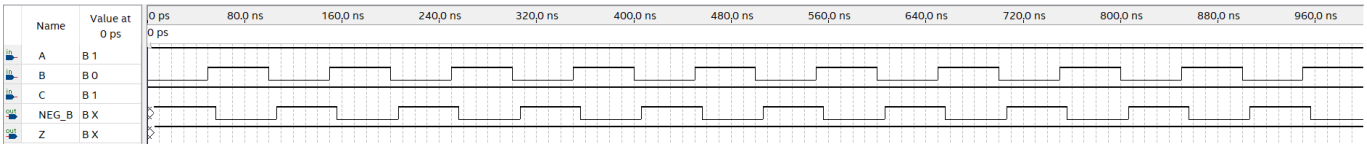

Figure 6: Waveform of part A without DELAY module. Inverter create a small delay at the beginning but too small to cause obvious glitch in Z to show the static hazard.

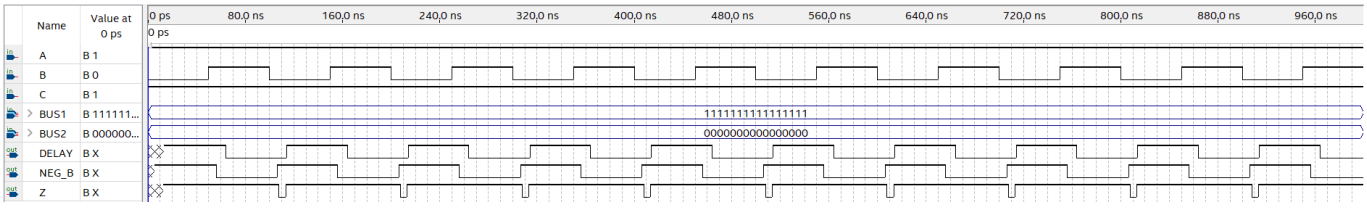

Figure 7: Waveform of part A with DELAY module. DELAY module highly increases the delay after the inverter which makes it now long enough to cause obvious glitch in Z to show the static hazard.

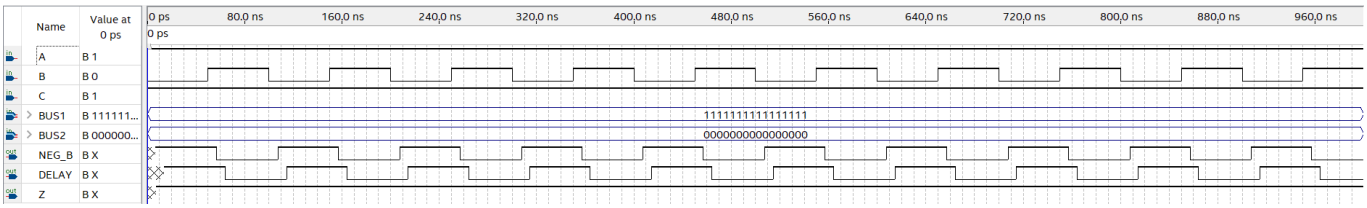

Figure 8: Waveform of part B. Adding the AC term to the circuit, the long delay still exists as the DELAY output shows, but the glitch in Z disappears which means the static hazard is successfully eliminated.

2.4 Truth Table

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 9: Truth table for both part A ($Z = AB + B'C$) and part B ($Z = AB + B'C + AC$).

3 Answers

3.1 Answers to Pre-Lab Questions

Question: No groups may observe static hazards. Why? If you do not observe a static hazard, chain an odd number of inverters together in place of the single inverter from Figure 16. But no static hazard is find, why? Wait for class and I will tell you.

Answer: Functional simulation is an ideal simulation. It calculates the final output directly from the input without considering any delay. Time simulation considers the delay but we still cannot see the static hazard because the delay of an inverter is too small to cause obvious glitch to show the static hazard. Chaining an odd number of inverters to increase the delay also failed

because the Quartus automatically optimize the circuit to make it counts only one inverter's delay.

3.2 Answers to Lab Questions

Question: Test the circuit of part A of the pre-lab by using waveform editor, simulate with Functional simulation. Complete a truth table of the output as a function of the three inputs.

Answer: Function simulation, see Fig. 4 in Documentation 2.3. Truth table, see Fig. 8 in Documentation 2.4.

Question: Test the circuit in part B of the pre-lab, including Delay module as well. Complete a truth table of the output. Does it respond like the circuit of part A? Describe and save the output and explain any differences between it and the results obtained in part 2. Consider the following question and explain: for the circuit of part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output?

Answer: Truth table, see Fig. 8 in Documentation 2.4. Yes, the static hazard is eliminated. At the **falling** edge (1 to 0), it is more likely for us to observe a glitch because when B turns from 1 to 0, the $B'C$ term will not be 1 immediately since there is a delay for the inverter which means there will be 2 gates delay. However, when B turns from 0 to 1, the AB term can turn to 1 after only 1 gate delay.

3.3 Answers to Post-Lab Questions

Question: How long does it take the output Z to stabilize on the falling edge of B (in ns)? How long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.

Answer: It takes 60 ns for the output Z to stabilize on the falling edge and the same on the rising edge. The potential glitches will happen during the two 60 ns. When B changes from 0 to 1 or 1 to 0, there will be two unstable time zones and static hazards might happen at these time.

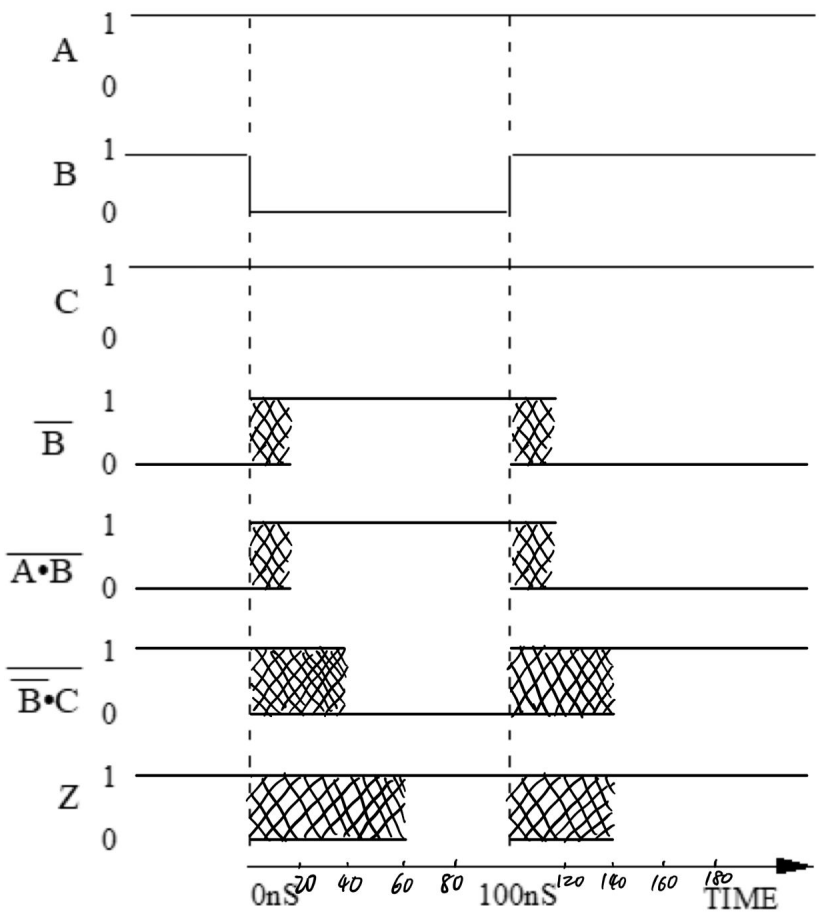

Figure 10: Timing diagram

3.4 Answers to questions from the General Guide

GG.6: What is the advantage of a larger noise immunity? Why is the last inverter observed rather than simply the first? Given a graph of output voltage (VOUT) vs. input voltage (VIN) for an inverter, how would you calculate the noise immunity for the inverter?

Answer: Larger noise immunity means higher stability. If the input is noisy, the chip can still work. Only one inverter is not able to show the stability, so we use a series of inverters to amplify the noise (instability) to give us a reliable nominal range. To calculate the noise immunity of Y, we subtract the lowest input voltage that would result in low level output from the high level output voltage. To calculate the noise immunity of X, we subtract the low level output voltage from the highest input voltage that would result in high level output. Then to get the overall noise immunity, we take the smaller one from the noise immunity of X and Y.

GG.29: If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors?
Answer: Different LEDs have different forwarding bias even with same kinds (colors) of LEDs.

Thus, sharing a resistor will make some of the LEDs brighter and some dimmer. Sometimes it can be dangerous or even blow up if one LED is too bright (getting too much current going through).

4 Conclusion

This is an introductory experiment. We build a mux and learn to eliminate static hazards which were ignored before in ECE120 but really worth paying attention to. Also, this is the first time we do simulation on the software, Quartus. We are free to debug and find out which element is broken but now trapped in solving why the compiling failed and why the simulation failed. In all, it is a good transition from ECE120 to ECE385.

References

[1] J. Patel, R. Kumar, D. Chen, and Z. Cheng, "ECE 385 DIGITAL SYSTEMS LABORATORY LABORATORY MANUAL Version 20.0," 2020. GG.22.

[2] C. Li, "ECE 385 – Digital Systems Laboratory Slides," 2020.