ECE385

Fall 2020

Experiment 3

A Logic Processor

Name: Zhou Qinren
Zhang Yichi
Lab Section: LA3
TA's Name: Yu Yuqi

Month Day Year

1 Introduction

1.1 functions and operations

1.2 prelab questions

2 Operation of the Logic Processor

2.1 load data

2.2 initiate a computation and routing operation

3 Written Description, Block Diagram and State Machine Diagram of Logic Processor

3.1 written description

3.2 high-level block diagram

3.3 state machine diagram

4 Design Steps Taken and Detailed Circuit Schematic Diagram

4.1 written procedure of the design steps taken

4.2 detailed Circuit Schematic

5 Description of All Bugs Encountered, and Corrective Measures Taken

6 Conclusion

6.1 summarization

6.2 post-lab questions

7 Waveform Generated by the Standard Testing Input