

Development Process of Athena, a Microcontroller based on RISC-V FE310 G002 Processor

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Abstract—This report outlines the work of the Athena project team in the current semester. The Athena project aims to design a Microcontroller based on Sifive’s RISC-V FE310 processor, with reference to the chip’s datasheet and official design from the Sifive website. The designed Microcontroller will be used in the undergraduate course ELEC220 offered by Rice University as a replacement for the original development board based on the TI MSP430 chip. Additionally, we plan to design some companion click boards for testing purposes. The Athena team has completed the schematic design and PCB layout of the Microcontroller and ordered relevant components. Currently, our project progress is that we can debug FE310 G002 through JTAG using Freedom Studio by modifying the firmware. Additionally, we have achieved the functions of external battery power supply and external battery charging. Our next task is to make modifications to address the issues encountered during testing and design more click boards to provide additional support for our Athena design.

Index Terms—RISC-V, Sifive, EF310

I. INTRODUCTION

RISC-V is an open-source instruction set architecture (ISA) that is gaining popularity in the semiconductor industry due to its flexibility and customization capabilities. RISC-V is expected to have a significant impact on the industry by reducing design costs and improving performance. The development of RISC-V-based products is expected to accelerate in the coming years, with SiFive being one of the key players in this space. SiFive is a leading provider of RISC-V-based microcontrollers, system-on-chips, and development boards. Their products have gained significant popularity in the maker community and are used in a wide range of applications, including IoT, automotive, and data center applications. SiFive’s offerings, such as the FE310 microcontroller, demonstrate the potential of RISC-V and its flexibility for a wide range of applications. As RISC-V adoption continues to grow, the ecosystem is expected to

expand, leading to further innovation and advancements in the field.

II. METHODS

A. Software Deployment

Freedom Studio is the fastest way to get started with software development on SiFive RISC-V processors. It is optimized for productivity and usability; your pre/post-silicon and software development teams will have all the tools necessary to write and optimize the best software, identify tough to find hot-spots, and eliminate the toughest bugs with ease. Built on the popular Eclipse IDE, Freedom Studio is packaged with the latest plugins, tools, and viewers, providing software developers crucial insight to the heart of your SoC - the Processor. Get the most performance out of your software running on Simulation Models, FPGA, an Instruction Set Simulator or HiFive Development Boards. SiFive Freedom Studio is free for everyone and can be downloaded. The download link is (<https://www.sifive.com/software>) All the files required for the project have been uploaded to Github, so you need to install the Git software. This is the reference link for Git installation configuration.(<https://git-scm.com/book/en/v2/Getting-Started-Installing-Git>). Through this link, you can find instructions on how to configure Git. Clone the repository from Github Open the Git bash and run following script shown in the Fig. 1.

```
git clone https://github.com/Rice-MECE-Capstone-Projects/Athena.git
```

Fig. 1. Git bash script

B. Hardware Deployment (schematic design)

Our project used the HiFive1 Rev B as the reference design [1] and the link to the Sifive board is (<https://www.sifive.com/boards>) Based on our usage requirements for Athena, we have made the following improvements.

- Athena board incorporates a battery management feature that enables it to be powered by either a 4.2V lithium battery or USB-C.
- The Athena board uses the FT2232 with OpenOCD instead of Segger JLINK to download and debug programs at a cheaper cost.
- Athena uses the same FE310-G002 chip as the Hifive1 Rev B, not the FE310-G000 chip of the Hifive1. The two differ mainly in frequency, boot configuration, and AON module voltage. **Therefore the FE310-G000 is not compatible with this design.**
- The Athena board replaces the Micro USB interface with USB-C, an interface that supports both charging, power supply, USB to serial, and JTAG functions.

1. Overall Framework

Which can be shown in the Fig. 2.

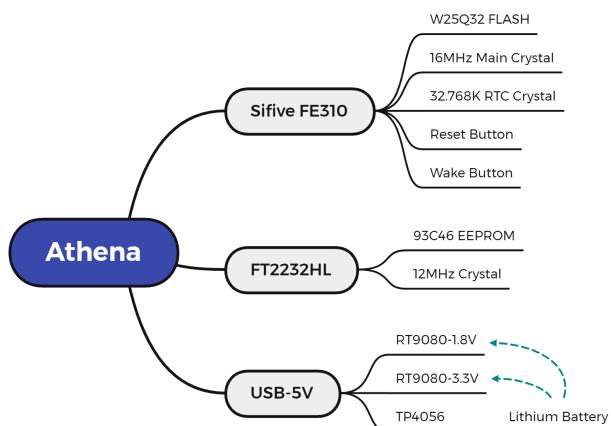


Fig. 2. Overall Framework

2. Power Supply

The Sifive FE310-G002 requires two power supply sizes, 3.3V and 1.8V, for powering peripherals and cores respectively. The power supply topology is shown in the Fig. 3

The above diagram describe the power supply topology. The following circuit shown in Fig. 4 is used to switch between USB and power supply.

Our Lithium battery management is shown in the Fig. 5.

We use the TP4056 chip for battery management. The

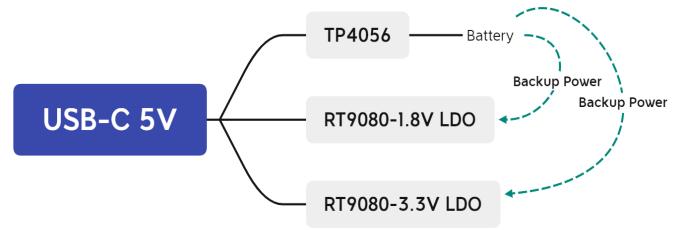


Fig. 3. Power supply topology

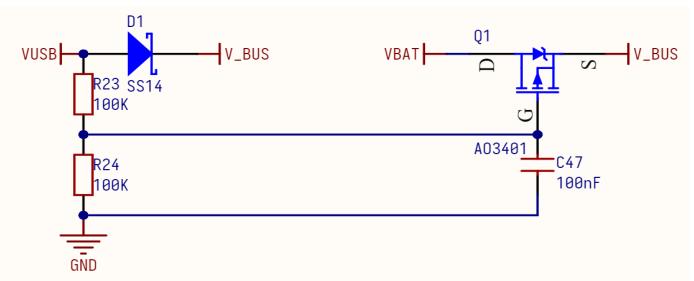


Fig. 4. Power supply switching circuit

TP4056 is a lithium-ion battery charging IC that utilizes a constant-current/constant-voltage (CC/CV) charging mechanism.

When a battery is connected to the TP4056, the IC begins the charging process by supplying a constant current to the battery. The charging current is set by the value of the external resistor connected to the IC, which is R21 in the schematic above.

Once the battery voltage reaches a certain threshold (typically 4.2V), the TP4056 switches to a constant-voltage charging mode. In this mode, the charging current gradually decreases as the battery approaches full charge, while the voltage

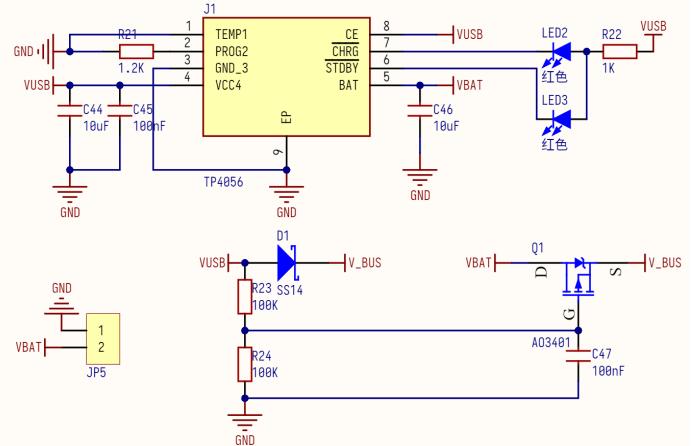


Fig. 5. Lithium Battery Management

remains constant. When the charging current drops to a certain level (typically 1/10 of the set charging current), the TP4056 terminates the charging process and goes into a low-power standby mode.

The LED2 and LED3 is to show the status of the battery charging.

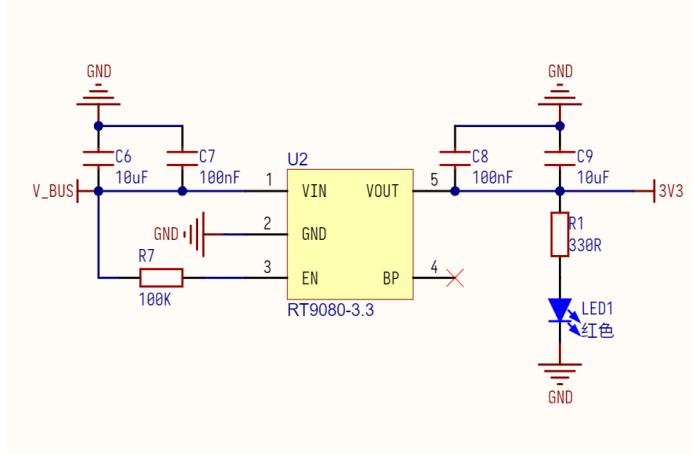


Fig. 6. 3.3V Power Supply

The diagram is shown in the Fig. 6 convert 5V to 3.3V. We use the RT9080-3.3 LDO to convert the 5V from the USB-C input to 3.3V. RT9080 is a low-dropout linear regulator IC that provides a fixed output voltage with a maximum load current of 1.5A. It has a wide input voltage range of 2.5V to 5.5V and a low dropout voltage of 300mV at 1.5A, which helps to reduce power dissipation and increase efficiency. It also includes built-in protection features and is available in a small SOT-223 package.

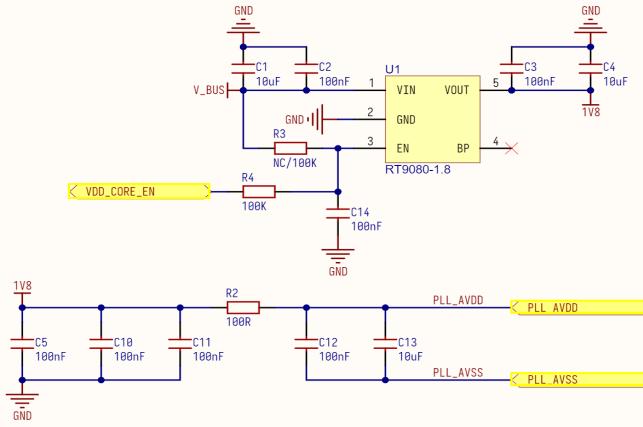


Fig. 7. 1.8V Power Supply

The diagram above shows in the Fig. 7 to convert 5V to 1.8V. We also use the RT9080-1.8 LDO to convert 5V to 1.8V. Since the PLL part is an analog circuit, which requires higher voltage stability, a (Pi)RC filter circuit is used to isolate the

PLL supply from the digital part.

3. FE310 G002

Athena's main control chip is Sifive FE310-G002, which is mainly composed of RISC V core, peripherals, Always-on, JTAG and other modules. The block diagram is shown in Fig. 8. Which is from the SiFive datasheet [2].

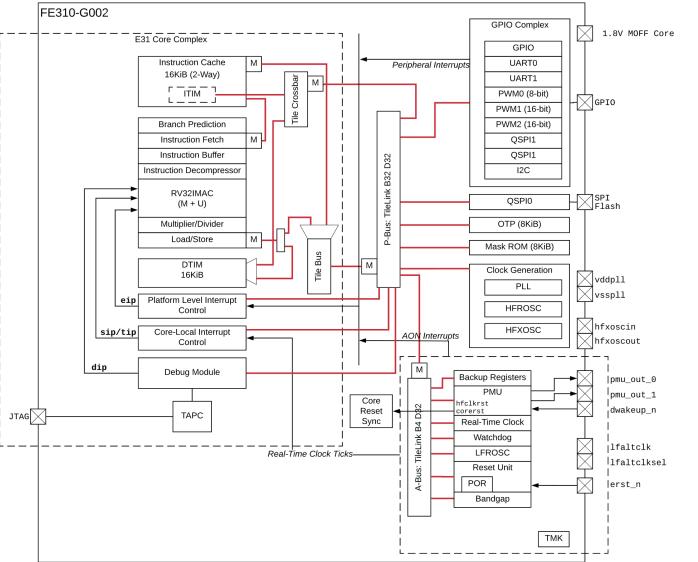


Fig. 8. FE310 G002 block diagram

FE310-G002 is a newer version of the FE310 microcontroller and has several improvements over the FE310-G000. Some of the key differences between FE310-G002 and FE310-G000 are:

- Clock speed: FE310-G002 has a higher maximum clock speed of 320 MHz compared to 150 MHz in FE310-G000.
- Memory: FE310-G002 has more internal RAM and Flash memory than FE310-G000, allowing for more complex applications.
- Power management: FE310-G002 features improved power management capabilities for better power efficiency and longer battery life compared to FE310-G000.
- Peripherals: FE310-G002 includes new peripherals, such as an I2S interface and a hardware divider, that were not available in FE310-G000.
- Security: FE310-G002 includes enhanced security features, such as a physical unclonable function (PUF) for secure key generation and storage, and a secure boot mechanism, which are not present in FE310-G000.

4. FT2232HL

FT2232 is a USB to dual-serial UART (Universal Asynchronous Receiver-Transmitter) converter chip developed by FTDI (Future Technology Devices International) for interfacing USB to various standard serial interfaces.

The FT2232 chip includes two independent UART channels,

each with its own set of TX and RX pins. It also supports several other communication interfaces, including I2C, SPI, and JTAG.

FT2232 is commonly used in a variety of applications, including programming and debugging of microcontrollers, FPGA configuration, and general-purpose USB to serial communication.

It should be noted that FT2232D and FT2232HL are two versions of the FT2232 USB to dual-serial UART converter chip developed by FTDI. While they share many similarities, there are a few key differences between them.

The main difference between FT2232D and FT2232HL is their maximum operating frequency. FT2232D has a maximum operating frequency of 6 MHz, while FT2232HL can operate up to 30 MHz. This means that FT2232HL can support faster data transfer rates compared to FT2232D.

We use the FT2232HL version in our projects. For faster download rates and debugging, use the version with the HL suffix.

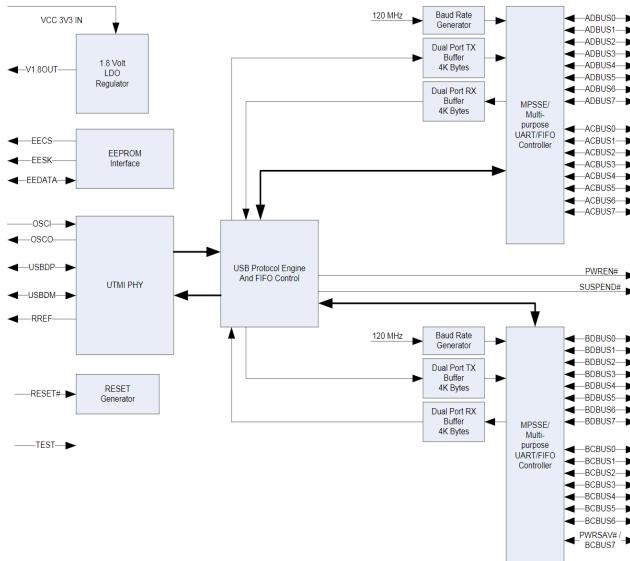


Fig. 9. Schematic block diagram of FT2232HL

The Fig. 9 is FT2232HL schematic block diagram from FT2232HL datasheet [3].

C. Hardware Deployment (PCB design)

The overall design of the PCB is shown in the Fig. 10 but there are some things to pay attention to during the design process.

1. Rules of layout

PCB layout rules are a set of design guidelines that ensure the successful operation of a printed circuit board.

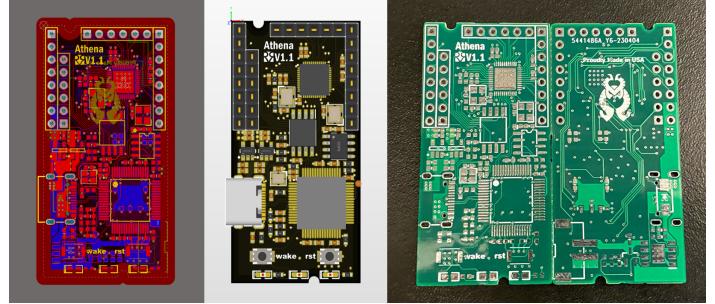


Fig. 10. Final work of our PCB

They specify the minimum clearances, trace widths, and other parameters required to meet the electrical, mechanical, and thermal requirements of the circuit design. Adhering to these rules is essential to avoid issues such as signal interference, electrical shorts, thermal problems, and mechanical failures. Non-compliance can result in increased manufacturing costs and delays. By following the PCB layout rules, designers can ensure that their boards meet the required specifications, operate correctly, and can be manufactured efficiently and cost-effectively, ultimately leading to a better end product.

Athena boards are prototyped at JLCPCB and therefore the design rules need to meet the process requirements of the JLCPCB factory.

The Athena boards use 4-layer boards and are prototyped at JLCPCB, so the design rules need to meet the process requirements for 4-layer boards at the JLCPCB factory.

The JLCPCB factory process rules are as follows. If using other manufacturers for proofing, be sure to check that the design meets their rules. You can use this link to check if your design meets the requirements or not. (<https://jlcpcb.com/capabilities/pcb-capabilities>)

- Clearance

The significance of the Clearance rule is to avoid unnecessary electrical interaction between components or between components and traces, thereby maintaining the signal integrity of the circuit board. This can significantly reduce the possibility of noise and other signal problems, ensure the normal operation of the circuit board, and improve the stability and reliability of the circuit board. The example of the clearance is shown in the Fig. 11

- Width

The significance of the Width rule is to ensure that the correct amount of current can flow through the trace without causing any damage to the board or components. Inadequate trace widths can lead to overheating, voltage drops, and even electrical shorts, which can cause the board to fail or malfunction. Following the Width rule can also help to optimize the performance of the circuit board, by minimizing signal degradation and interference. The example of the width is shown in Fig. 12

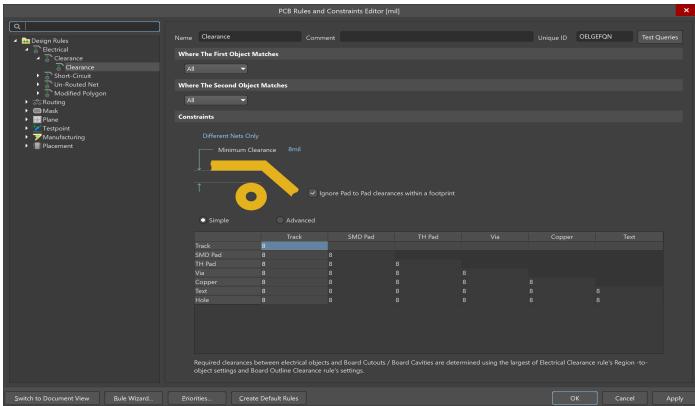


Fig. 11. Example of the clearance

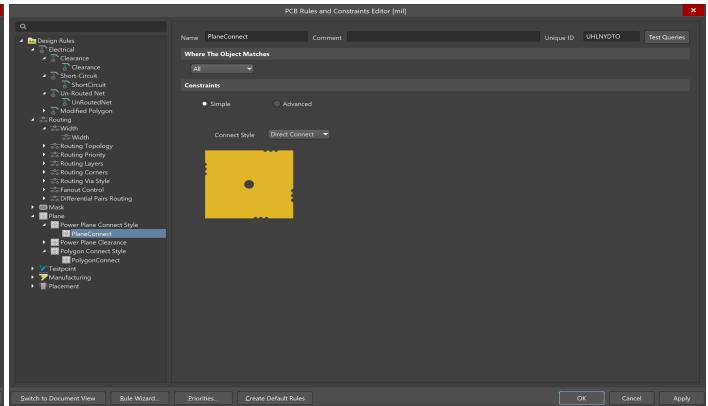


Fig. 13. Example of the Plane Connect

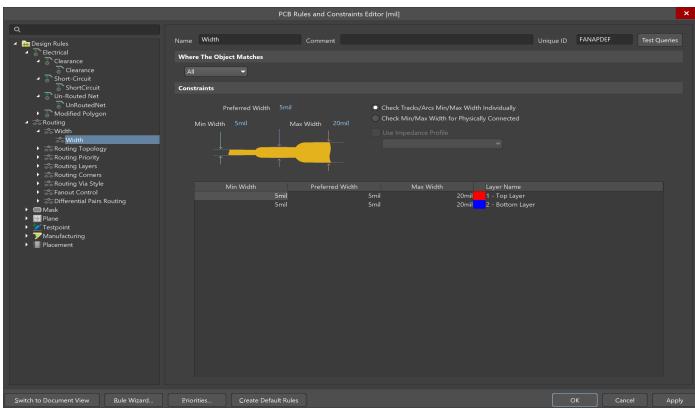


Fig. 12. Example of the width

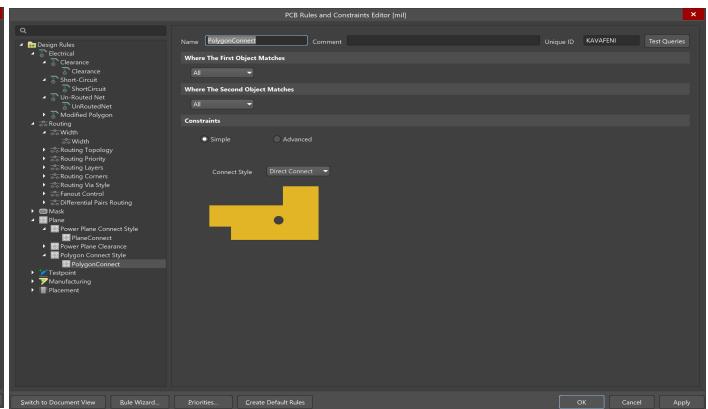


Fig. 14. Example of the Polygon connect

PlaneConnect is a feature in PCB design software that allows designers to connect different areas of copper planes on a printed circuit board. There are several ways to connect these areas, each with its own advantages and disadvantages. The most common of these are direct connection and thermal relief connection.

1. Thermal Relief Connection: This method involves using a small trace or pad to connect the plane to a component lead. The advantage of this method is that it provides a thermal break between the plane and the component, which can help prevent soldering problems. However, it can also create a weak connection and increase the resistance in the plane.

2. Direct Connection: This method involves connecting the plane directly to a pad or via on the board. The advantage of this method is that it provides a strong connection and reduces the resistance in the plane. However, it can also create a thermal problem if the plane is connected directly to a high-power component.

The example of Plane connect is shown in Fig. 13 and the example of Polygon connect is shown in the Fig. 14

2. Placement and Wiring Notes

- Crystals

In PCB design, there are several points to consider when laying out and routing passive crystal oscillators:

Placement: The crystal oscillator should be placed as close to the chip as possible, with short connection lines to minimize signal attenuation and noise interference. Additionally, the oscillator should be located away from other high-frequency interference sources such as power and clock signals.

Grounding: A solid and adequate ground connection for the oscillator is essential to ensure signal stability and reliability. The grounding area should be as large as possible, and the distance between the oscillator and the ground should be minimized. The oscillator grounding should be separated from other signal grounds to reduce interference.

Routing: The oscillator routing should be as short as possible, and impedance matching should be used to avoid signal reflection and interference. Additionally, the oscillator routing should avoid being near high-frequency interference sources such as power lines and clock signals.

In our Athena board, we put the crystal oscillator in

the center of the board and as close to the chip as possible, and there is no trace under the crystal oscillator. This improves the stability of the board.

III. RESULT

In our project, we have completed the schematic design and four-layer PCB layout for Athena. The PCBs were fabricated by JLCPCB and we have received the samples. We have ordered the required components from LCSC and Digi-Key and plan to assemble the PCBs ourselves to avoid assembly costs. We improved our design by using the FT2232HL debugger to avoid licensing fees for the commercial JLINK from Segger. We also changed the Micro-USB to USB Type-C for teaching convenience and added a power management module to switch between external power and USB power for expanded use of the Athena board.

The final work of the Athena microcontroller is shown in the Fig. 15

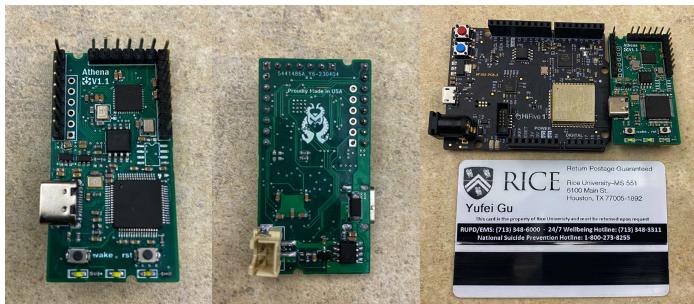


Fig. 15. Picture of our final work Rev1.1

After assembling the PCB and testing it, we were able to successfully program the FE310 G002 using the FT2232HL Debugger through JTAG by modifying the firmware in Freedom Studio. We also tested the external battery power and charging functions and confirmed that everything was working properly. The design we developed for the FE310 G002 chip met the requirements for this semester's goal (the FE310 G002 chip is from SiFive's development board), as demonstrated by the results obtained from the COM output and the COM result is shown in the Fig. 16.

We have also achieved the function of blinking the light through GPIO by using our own Demo which means we can call the IO of the Athena development board for output and the result is shown in the Fig. 17.

Testing result of external battery power supply and charging functionality is shown in the Fig. 18.

Our tests met our design expectations.

IV DISCUSSION

The discussion section of our paper presents the advantages of our design over the previous iteration. Our design stands

Fig. 16. The test result from the COM

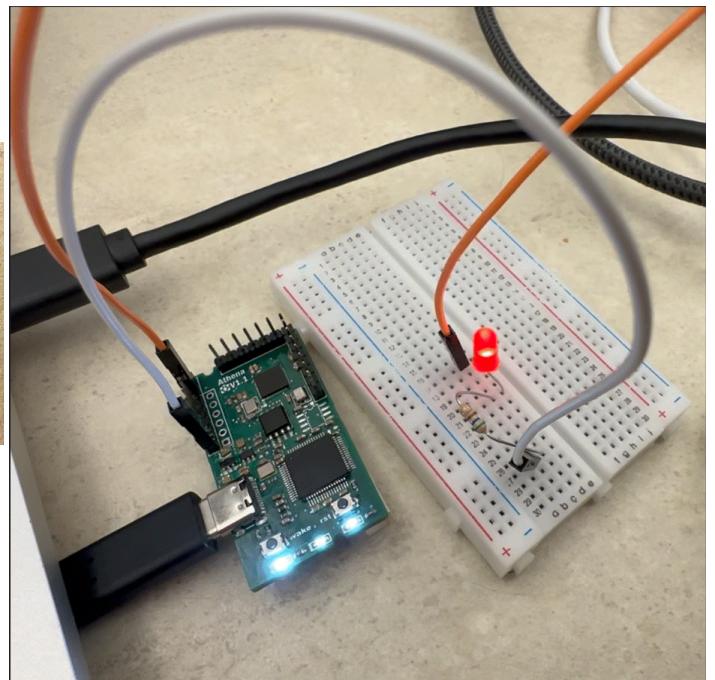


Fig. 17. The test result of blinking the LED



Fig. 18. The test result of External battery power and charging

out in terms of engineering cost control, as we managed to save on the commercial license fee for Segger's JLINK. Additionally, we assembled the PCB ourselves and used JLCPCB from China to print the board, which greatly reduced development costs compared to local PCB suppliers. The total material cost of our research and development, excluding the tools required to assemble the PCB, was 524.57 dollars (excluding shipping). The price of JLCPCB was 14 dollars, LCSC was 224.64 dollars, and DigiKey was 285.93 dollars. These parts can be used to assemble five Athena microcontrollers along with the corresponding click board for testing purposes.

Furthermore, our design is highly compatible due to its external power supply support. It can be used in a wide range of embedded development scenarios. It has UART, I2C, and SPI interface protocols. Theoretically, it supports Arduino peripheral expansion, making it a suitable tool for teaching beginners.

Lastly, we designed a click board for testing purposes, which uses the ESP32-PICO chip. With this click board, we hope to enable WIFI support for the Athena board, making it suitable for the development of IoT devices.

The click board of ESP32 is shown in the Fig. 19.

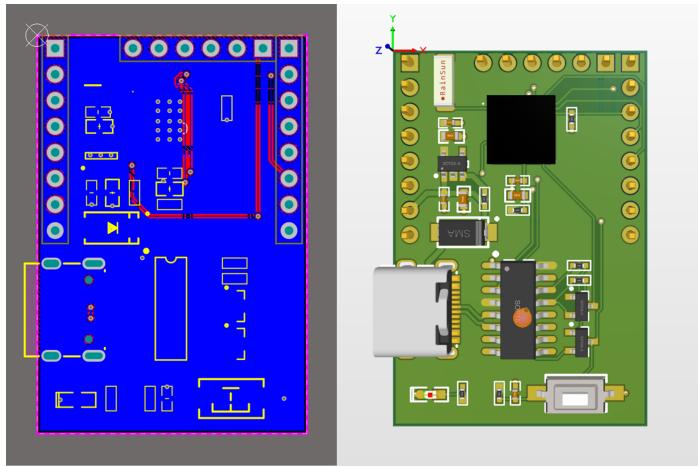


Fig. 19. Our PCB design of ESP32 click board

At the same time, many STM32 development boards have analog output function. We also want our Athena board to achieve the same function. For this purpose, we have designed the DAC click board, as shown in the Fig. 20.

RISC-V is an open-source architecture, and we believe that there will be more and more RISC-V-based ASICs in the future to meet various specialized needs. Although our Athena board is compatible with Arduino peripherals, designing more click boards for Athena will expand its usefulness.

V. ACKNOWLEDGEMENTS

We would like to express our sincere gratitude to Prof. Young for his invaluable help in purchasing components for

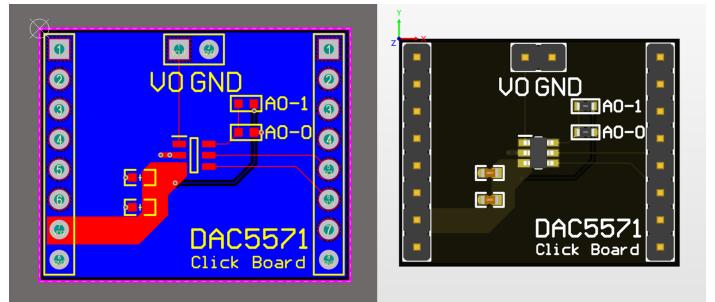


Fig. 20. Our PCB design of DAC click board

our project. Cost control was a crucial design requirement for us, and to meet this requirement, we sought suppliers from China. However, this ran into some difficulties with school procurement. Prof. Young's assistance in coordinating with suppliers and resolving procurement issues was essential in ensuring the smooth progress of our project.

We would also like to thank the Rice RVR project group for their financial support, which was instrumental in enabling us to complete our research.

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