FPGA-Based PDM-to-PCM Conversion for MEMS Microphones: A Low-Latency Approach with Custom IP Integration

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***Abstract*—This work proposes a low-cost FPGA-based solution for converting Pulse Density Modulation (PDM) signals from MEMS microphones to Pulse Code Modulation (PCM) using the Xilinx ARTY-S7-50 FPGA. The system employs a cascaded integrator-comb (CIC) compiler for decimation and noise reduction, custom IP blocks for 2.4 MHz clock generation and 1-to-2-bit stream conversion, and UART-based PCM output. Key advantages include a 40% cost reduction compared to high-end FPGAs, low power consumption < 0.1 W, and open-source toolchain compatibility (Vivado/Vitis). Partial results validate signal conversion at frequencies up to 150 Hz. Future work focuses on integrating DDR memory for data buffering, optimizing FIR compensation filters, and resolving FreeRTOS compatibility. This approach balances affordability and performance, making it suitable for scalable MEMS audio systems.**

I. Introduction

PDM is widely adopted in MEMS microphones for its simplicity, but PCM remains the standard for digital audio processing. Existing PDM-to-PCM converters often rely on proprietary, high-cost hardware, limiting flexibility. This work addresses these limitations using the Xilinx ARTY-S7-50 FPGA, which offers 52K logic cells, 180 DSP slices, and plug-and-play I/O ports for multi-microphone setups. By leveraging open-source tools and custom IP blocks, the design achieves a modular, resource-efficient conversion pipeline. Key innovations include a 1-to-2-bit converter for CIC compatibility and a low-latency CIC-FIR chain. This approach targets embedded systems requiring real-time audio processing with minimal latency and power consumption.

II. Methods

A. PDM Input

The MP54DT05-A microphone requires 1.2-3.25 MHz clock input (Table I).

Parameter	Description	Min.	Max.	Unit
f_{CLK}	Clock frequency for normal mode	1.2	3.25	MHz
f_{PD}	Clock frequency for power-down mode		0.23	MHz
T_{CLK}	Clock period for normal mode	308	1000	ns
T_{dv}	Time delay to valid data (CLOAD = 100 pF)	-	105	ns
T_{en}	Time delay to driven data	18	-	ns
T_{dis}	Time delay to High-Z	2	10	ns

TABLE I
Timing Characteristics of MP54DT05-A Microphone.

A custom clock source IP block (Fig.1) must be created in Vivado to generate a 2.4 MHz frequency for driving the PDM microphone.

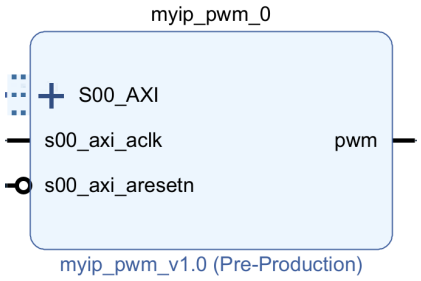

Fig. 1. Block diagram of the custom clock source IP block.

The 2.4 MHz output was successfully generated and observed using an oscilloscope (Fig.2), confirming that the desired frequency was accurately produced.

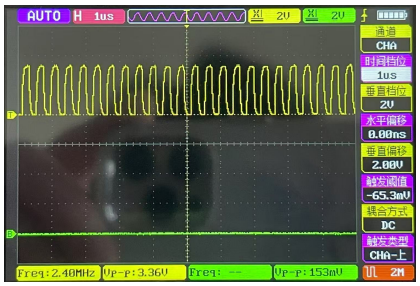

Fig. 2. Oscilloscope capturing the output results of the user-defined IP block.

When the PDM microphone is successfully driven, it generates a 1-bit bitstream. Since the CIC Compiler is designed to process bitstreams of 2 bits or higher, a bit converter is required to convert the 1-bit bitstream from the PDM microphone into a 2-bit bitstream. The IP blocks provided by Vivado do not include a bit conversion function; therefore, users must design a custom bit converter IP block (Fig.3) to meet this requirement.

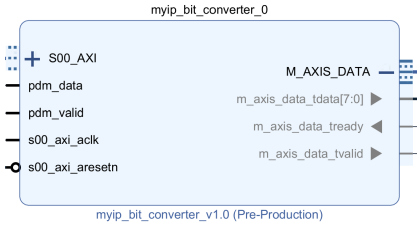

Fig. 3. Custom bit converter IP Block.

B. CIC Decimation Filter

In this application, we process the signal output from the Pulse Density Modulation (PDM) microphone using the Cascaded Integrator Comb (CIC) Compiler. The CIC Compiler performs integration and decimation on the signal, which has a sampling frequency of 2.4 MHz. The integration operation helps reduce high-frequency noise, while decimation reduces the sample rate, improving the signal-to-noise ratio and making the signal more suitable for further processing.

The CIC Compiler is fully integrated within the Vivado environment (Fig.4), allowing for direct use without the need for additional configuration. This integration significantly enhances development efficiency, reduces complexity, and simplifies the design process, enabling developers to focus on higher-level functionality rather than manual configurations.

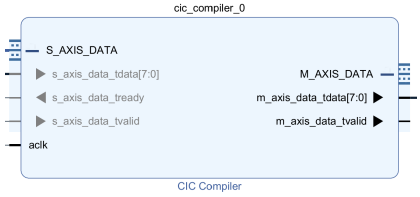

Fig. 4. CIC Compiler IP Block in Vivado.

C. PDM Output

Finally, the processed signal must be output for further use. To achieve this, a custom IP block is designed (Fig.5), incorporating a read function that stores the processed data in dedicated registers. This data can subsequently be accessed by Vitis programming, which facilitates reading from the registers. The retrieved data is then transmitted through a UART interface, enabling it to be displayed on a PC interface. This approach ensures seamless data communication and provides an efficient mechanism for outputting the processed signal, allowing for real-time monitoring and analysis on the host system.

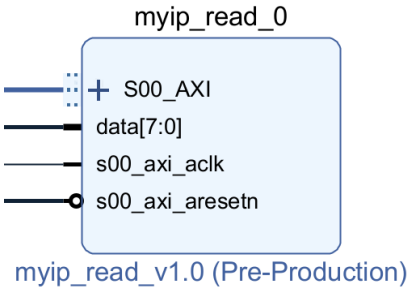

Fig. 5. Output IP Block in Vivado.

III. Results (Partial)

Functional validation was performed to ensure the accuracy and reliability of the system. The UART output was verified by testing with sinusoidal signals in the frequency range of 20–150 Hz. As shown in Fig. 8, the system successfully transmitted the processed signals, confirming the correct functionality of the output interface. This validation process ensures that the system meets the required specifications for signal transmission, demonstrating its capability for real-time data communication and output for a range of signal frequencies.

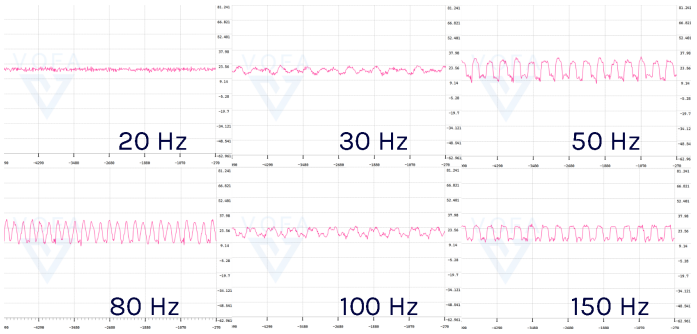

Fig. 6. UART output data to the PC port.

IV. Discussion

The current design effectively demonstrates a cost-efficient PDM-to-PCM conversion; however, it lacks full end-to-end integration. The absence of FIR filtering constrains signal fidelity, and the UART interface introduces a bottleneck, limiting real-time throughput. While this FPGA-based approach provides enhanced customization compared to commercial ICs, such as the AD1938, it necessitates further optimization, particularly for power-sensitive applications. Future enhancements, including the integration of DDR memory and the implementation of FreeRTOS, are expected to significantly improve scalability and real-time performance, addressing the limitations identified in the current design.

Acknowledgements

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