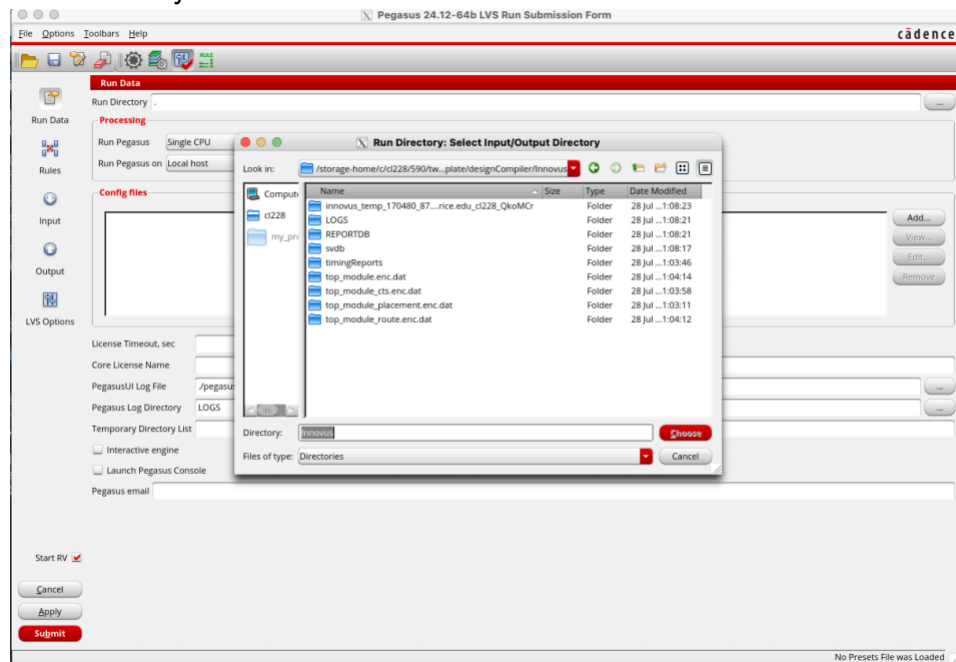
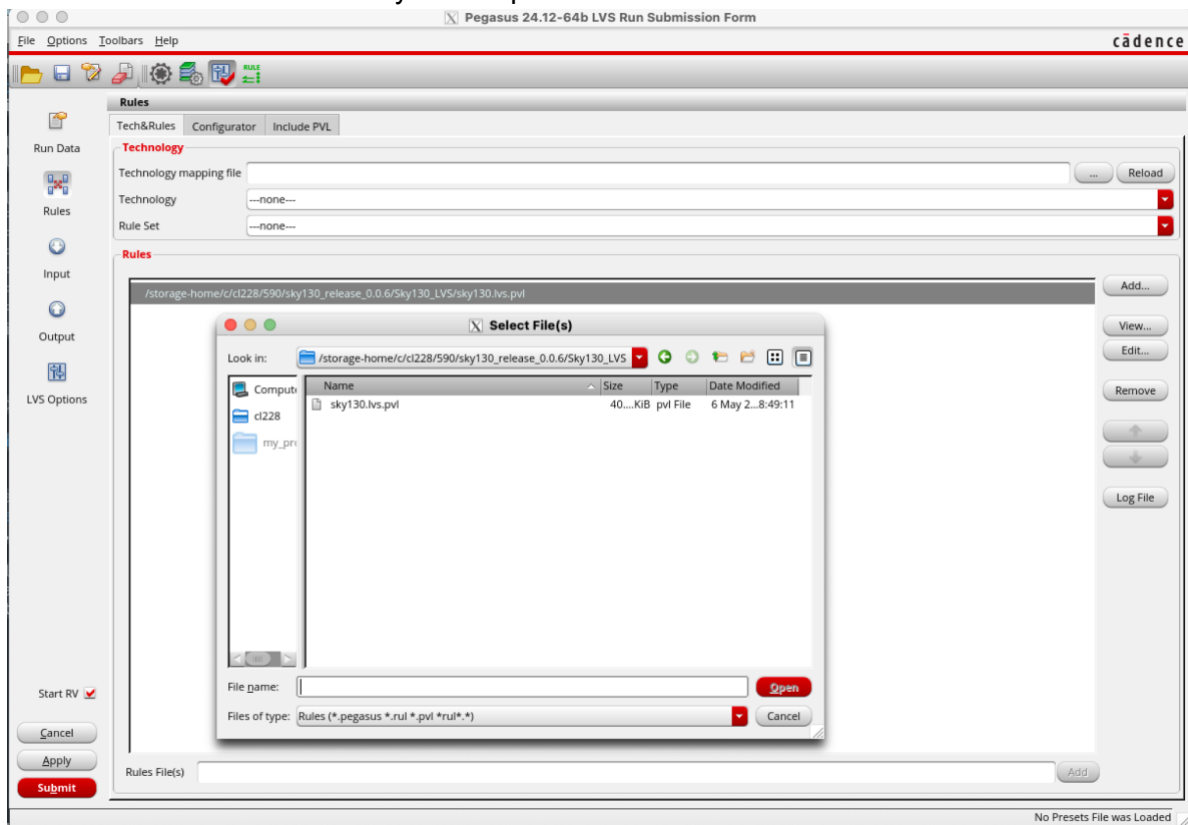


1. Set Run Directory



2. Choose "Rules"

Click "Add..." and add sky130.lvs.pvl file



3. Choose Input

Add gds file from PDK

Then set Mapfile. It should be in the same directory with gds file

Make sure it creates SPICE file

Input

Layout

Top Cell Name: top_module

Create GDSII: ☒ /top_module.gds.gz

/storage-home/c/d228/590/sky130_scl_9T_0.0.6/sky130_scl_9T/gds/sky130_scl_9T.gds

Merge File(s):

Layout Options

Map File: /storage-home/c/d228/590/sky130_scl_9T_0.0.6/sky130_scl_9T/gds/sky130_stream.mapFile

☒ Uniquify Cell Names ☐ With Prefix

DBU/UU: 1000

Additional setStreamOutMode Parameters:

Additional streamOut Parameters:

Create SPICE: ☒ /top_module.spi

☒ Abort on Layout Error

☐ Exclude Comparison Step

4. Scroll down to schematic

Add cdl file

Input

Schematic

Top Cell Name: top_module

Create Verilog: ☒ /top_module.v

/storage-home/c/d228/590/sky130_scl_9T_0.0.6/sky130_scl_9T/cdl/sky130_scl_9T.cdl

Netlist File(s): Type: Auto

CPF File:

Schematic Options

☒ Include Physical Cell Instances

☒ Exclude Leaf Cells

☒ Include Power and Ground

Additional saveNetlist Parameters:

Start RV: ☒

Cancel Apply Submit

No Presets File was Loaded

5. Choose Output

Check “Automatch” in H-Cell Settings

Check “Create Quantus Input Data” in Additional Output if need to run Quantus later

Pegasus 24.12-64b LVS Run Submission Form

File Options Toolbars Help

cadence

Output

H-Cell Settings

☒ Automatch

☐ HCell

☐ GenHierCells

☒ Run ERC Checks

ERC Report

Name: top_module.sum

Limit: 1000

☒ Replace File ☐ Append To File ☐ Statistics by Cell ☐ Caption

Output Format: ASCII /top_module.erc_errors.ascii

Output Errors Hierarchically: Rules Definition ☐ Output Complete Pathchk Results ☐ Flatten Output

☐ Use Waivers for ERC Checks

LVS Report

Name: top_module.rep

Options: -none

Limit: 50 Mismatched Nets Limit: 100

Additional Output

☐ Create Quantus Input Data

Data Dir: sydb

Keep Layers: None

☒ Output All in one Rule (-o1) lvs.o1.pvl

Start RV ☒

Cancel Apply Submit

No Presets File was Loaded

6. LVS options->Extract Options

Define Power and Ground. (I'm not sure what this step does, but the tutorial I read does it this way.)

FileOptionsToolbarsHelp

cadence

Run Data

Rules

Input

Output

LVS Options

LVS Options

ERC Rules and GroupsExtract OptionsComparison OptionsText and Connect

LVS Abort

☐ On softchk

☐ On supply error

Net Names

PowerVDD vdd☒ Globals or ports

GroundVSS vss☒ Globals or ports

Interposer

Cell namelayout&schematic

☐ LVS find shorts

☐ Flat extraction run

☐ Sconnect select by upper shape count

Start RV☒

Cancel

Apply

Submit

No Presets File was Loaded