Notes

- Use Redhat v.8
- Synthesis (Genus) → Place and Route (Innovus) →LVS & DRC (Innovus)→
- For Place and Route, if GUI does not show up, do;
    - i. innovus-2025
    - ii. 1
    - iii. source new_innovus.tcl
  - b. To load file without rerunning, type: restoreDesign top_module.enc.dat

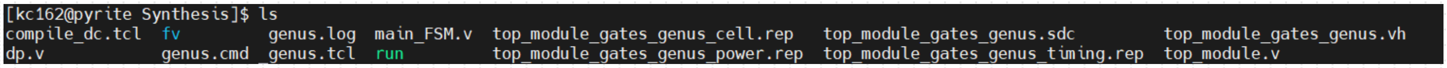
Synthesis

1. Begin by copying folder
    - i. cp -r /clear/courses/elec422/2025_spring/twoP_FSM_DP_template
2. Begin with Genus
    - a. Create genus.tcl
        - i. nano genus.tcl
    - b. Paste the following into genus.tcl:

```
set_db common_ui false


set skywater "/clear/apps/cadence-2025/rhel8/sky130-data/sky130_scl_9T"



set_attr init_hdl_search_path {./}

set_attr init_lib_search_path "$skywater/sky130_scl_9T/lib"


set_attribute library {sky130_tt_1.8_25_nldm.lib}


set_attribute information_level 6


set rtlFiles [list top_module.v dp.v main_FSM.v]

set basename top_module      ;# name of top level module

set runname gates_genus      ;# name appended to output files(every file will have the same name for runname appended)


set frequency    25.0          ;# Clock frequency in MHz
set clk1_port_name  "in_clka"  ;# Physical port name for clk1 in Verilog
set clk1_logic_name "clka"     ;# Logical name for clk1 in constraints
set clk2_port_name  "in_clkb"  ;# Physical port name for clk2 in Verilog
set clk2_logic_name "clkb"     ;# Logical name for clk2 in constraints
set input_setup  1             ;# delay from clock to inputs valid
set output_delay 1             ;# delay from clock to output valid
set clock_period [expr 1000000.0 / $frequency]   ;# Clock period in ps (picosecond)
set half_period [expr ${clock_period} / 2.0]

read_hdl -sv ${rtlFiles}
elaborate ${basename}

#sizing of the transistors part of research, try changing these values randomly
set_drive     2.0 [all_inputs]
set_load      4.0 [all_outputs]
set_max_fanout 5   [all_inputs]

# Step 1: Create the first phase clock (phi1), high for the first half of the period.

set clock [define_clock -period ${clock_period} -name ${clk1_logic_name} \
    -waveformr 0 -waveformf ${half_period} [get_ports ${clk1_port_name}]]

# Step 2: Create the second phase clock (phi2), high for the second half of the period.
set clock [define_clock -period ${clock_period} -name ${clk2_logic_name} \
    -waveformr ${half_period} -waveformf ${clock_period} [get_ports ${clk2_port_name}]]

# Step 4: Set I/O Delays, making sure to exclude clock ports
set data_inputs [remove_from_collection [all_inputs] [get_ports "${clk1_port_name} ${clk2_port_name}"]]
set data_outputs [all_outputs]

set_input_delay $input_setup -clock ${clk1_logic_name} $data_inputs
set_output_delay $output_delay -clock ${clk2_logic_name} $data_outputs
```

```
# Step 5: Check design and timing constraints
check_design -unresolved
report timing -lint

#-------------------------------------------------------------------------
# --- Synthesis ---
#-------------------------------------------------------------------------
# Synthesize the design to the target library
# synthesize -effort medium -to_mapped
set_attribute syn_generic_effort medium
set_attribute syn_map_effort medium
set_attribute syn_opt_effort medium
syn_generic
syn_map
syn_opt

#-------------------------------------------------------------------------
# --- Reporting and Output ---
#-------------------------------------------------------------------------
# Write out the reports
report timing > ${basename}_${runname}_timing.rep
report gates  > ${basename}_${runname}_cell.rep
report power  > ${basename}_${runname}_power.rep

# Write out the structural Verilog and sdc files
write_hdl -mapped >  ${basename}_${runname}.vh
write_sdc >  ${basename}_${runname}.sdc

# show result
gui_show
```

3. To run: genus -f genus.tcl
    a. You should see something like this afterwards:

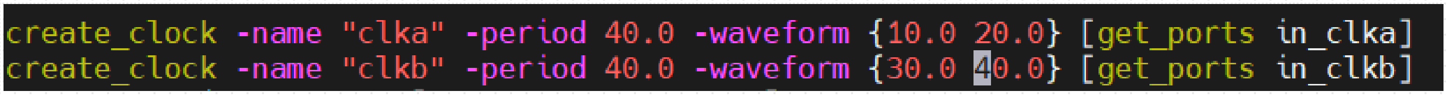


```
[kc162@pyrite Synthesis]$ ls
compile_dc.tcl  fv         genus.log  main_FSM.v  top_module_gates_genus_cell.rep   top_module_gates_genus.sdc         top_module_gates_genus.vh
dp.v            genus.cmd  genus.tcl  run         top_module_gates_genus_power.rep  top_module_gates_genus_timing.rep  top_module.v
```

4. Copy two files over to Innovus for place and route:
    i. cp top_module_gates_genus.vh ../Innovus/
    ii. cp top_module_gates_genus.sdc ../Innovus/

Place and Route

1. Find the sdc file you just copied to Innovus. (top_module_gates_genus.sdc)
    i. vim top_module_gates_genus.sdc
    b. Press “i” on your keyboard to edit the file
    c. Then, find this part and change the numbers to 30 and 40 as shown in the image:



```
create_clock -name "clka" -period 40.0 -waveform {10.0 20.0} [get_ports in_clka]
create_clock -name "clkb" -period 40.0 -waveform {30.0 40.0} [get_ports in_clkb]
```

    d. Afterwards, press “esc” on your keyboard, and type “:wq” to exit.

2. Create top_module.view in same place as when you run Innovus
    i. nano top_module.view
    b. Paste the following into top_module.view:

# Create RC corner

create_rc_corner -name RC_TYP -qx_tech_file /clear/apps/cadence-2025/rhel8/sky130-data/sky130_release/quantus/extraction/typical/qrcTechFile -pre_route_res 1.0 -pre_route_cap 1.0

create_rc_corner -name RC_SLOW -qx_tech_file /clear/apps/cadence-2025/rhel8/sky130-data/sky130_release/quantus/extraction/typical/qrcTechFile -pre_route_res 1.2 -pre_route_cap 1.2

# Create library set

create_library_set -name lib_tt -timing [list /clear/apps/cadence-2025/rhel8/sky130-data/sky130_scl_9T/sky130_scl_9T/lib/sky130_tt_1.8_25_nldm.lib]

create_library_set -name lib_ss -timing [list /clear/apps/cadence-2025/rhel8/sky130-data/sky130_scl_9T_0.0.6/sky130_scl_9T/lib/sky130_ss_1.62_125_nldm.lib]

# Define constraints

```
create_constraint_mode -name func_mode -sdc ../genus/top_module_gates_genus.sdc



# Define timing corners
create_delay_corner -name tc_tt -library_set lib_tt -rc_corner RC_TYP

create_delay_corner -name tc_ss -library_set lib_ss -rc_corner RC_SLOW

# Define analysis views
create_analysis_view -name func_tt -constraint_mode func_mode -delay_corner tc_tt

create_analysis_view -name func_ss -constraint_mode func_mode -delay_corner tc_ss

# Set default views
set_analysis_view -setup [list func_tt] -hold [list func_ss]
```

3. Create a new Innovus TCL file in same place as when you run Innovus
   i. nano new_innovus.tcl
   b. Paste the following into new_innovus.tcl:

```
######################################################################
#
#  Innovus Command File - updated Feb. 22, 2018 for ELEC 422/527
#  Run the design through Innovus 22.14
#  Minor text typo update Feb. 12, 2019
#  Minor update for Innovus Apr. 06, 2024
#
######################################################################

#######################################################################
#######################################################################
# IMPORTANT - IMPORTANT
# Change only these three lines each time to your top level cell names
```

```
#Set top module
set init_top_cell "top_module"
#Load netlist
set init_verilog "top_module.vh"
#Set mmmc file
set init_mmmc_file "top_module.view"

########################################################################
########################################################################
#
# No need to change anything below - standard design flow steps
# IMPORTANT - See note below about floorPlan if density error occurs
#
########################################################################
########################################################################
#

set skywater "/clear/apps/cadence-2025/rhel8/sky130-data/sky130_scl_9T"

# Set the Library Exchange Format cell library file wrt. the OSU root
set init_lef_file [list \
            "$skywater/sky130_scl_9T_tech/lef/sky130_scl_9T.tlef" \
            "$skywater/sky130_scl_9T/lef/sky130_scl_9T.lef" \
            "$skywater/sky130_scl_9T_tech/lef/sky130_scl_9T_phyCells.lef" \
]

set init_gnd_net VSS
set init_design_settop 0
set init_pwr_net VDD

init_design
```

```
getIoFlowFlag
setIoFlowFlag 0

floorPlan -r 1.0 0.6 21 21 21 21

globalNetConnect VDD -type pgpin -pin VDD -inst *
globalNetConnect VSS -type pgpin -pin VSS -inst *

set sprCreateIeRingNets {}
set sprCreateIeRingLayers {}
set sprCreateIeRingWidth 1.2
set sprCreateIeRingSpacing 1.2
set sprCreateIeRingOffset 1.2
set sprCreateIeRingThreshold 1.2
set sprCreateIeRingJogDistance 1.2

setPlaceMode -placeIoPins true

setAddRingMode -stacked_via_top_layer met5
setAddRingMode -stacked_via_bottom_layer met1

# Add Power and Ground rings around core
addRing -skip_via_on_wire_shape Noshape -skip_via_on_pin Standardcell -center 1 \
-type core_rings -jog_distance 1.8 -threshold 1.8 -nets {VDD VSS} -follow core \
-layer {bottom met1 top met1 right met2 left met2} -width 4.0 -spacing 1.8 -offset 1.8

addStripe -nets {VDD VSS} -layer met4 -direction vertical -width 1 -spacing 1 -set_to_set_distance 20
addStripe -nets {VDD VSS} -layer met3 -direction horizontal -width 1 -spacing 1 -set_to_set_distance 20

verifyConnectivity -type special -noAntenna -noWeakConnect -noUnroutedNet -error 1000 -warning 50 -net VDD
verifyConnectivity -type special -noAntenna -noWeakConnect -noUnroutedNet -error 1000 -warning 50 -net VSS

verify_drc



set_interactive_constraint_modes [all_constraint_modes -active]


set inputs [get_object_name [get_ports {in_clka in_clkb in_restart in_load in_d1_in[*] in_d2_in[*]}]]

set all_output_ports [get_object_name [all_outputs]]


editPin -spreadDirection counterclockwise -spacing 0.001 -layer 5 -pin $all_output_ports

editPin -spreadDirection clockwise -spacing 0.002 -layer 5 -pin $inputs


# Set data transition & clock transition

set_max_transition 0.3 [current_design]

set_max_transition 0.12 -clock [all_clocks]

# Set maximum fanout

set_max_fanout 24 [current_design]

# Set OCV

setAnalysisMode -analysisType onChipVariation -cppr both

# Crosstalk

setDelayCalMode -engine default -siAware true


#Placement setting

setPlaceMode -reset

setPlaceMode -congEffort auto -timingDriven 1 -modulePlan 1 -clkGateAware 1 -powerDriven 0 -ignoreScan 1 -reorderScan 0 -ignoreSpare 1 -placeIOPins 0 -moduleAwareSpare 0 -preserveRouting 0 -rmAffectedRouting 0 -checkRoute 0 -swapEEQ 0


setPlaceMode -place_detail_legalization_inst_gap 2

#setPlaceMode -fp false

#setOptMode -allEndPoints true
```

```
#setPlaceMode -place_global_uniform_density true
#setPlaceMode -place_opt_effort high
#setOptMode -leakagePowerOptimization true
#setOptMode -powerEffort low

setRouteMode -earlyGlobalEffortLevel standard

checkPlace

place_opt_design
saveDesign ${init_top_cell}_placement.enc

sroute -nets {VDD VSS}

# Clock Tree Synthesis
# set_ccopt_property use_inverters true

# Set clock tree constrains
 set_ccopt_property target_max_trans 0.4
 set_ccopt_property target_skew 0.06
 set_ccopt_property max_fanout 24


set clock_buffers "CLKBUFX2 CLKBUFX4 CLKBUFX8"
set clock_inverters "CLKINVX1 CLKINVX2 CLKINVX4 CLKINVX8"

set_ccopt_property use_inverters true
set_ccopt_property inverter_cells $clock_inverters

#ccopt_design -cts
clock_opt_design
```

```
report_ccopt_skew_groups -summary
saveDesign ${init_top_cell}_cts.enc

setNanoRouteMode -route_extra_via_enclosure 1

routeDesign -globalDetail

setNanoRouteMode -route_detail_post_route_wire_widen 3

saveDesign ${init_top_cell}_route.enc

# Add Filler cells at edges of cell rows
#addFiller -cell FILL -prefix FILLER -markFixed

addFiller -cell FILL1 \
          FILL2  \
          FILL4  \
          FILL8  \
          FILL16 \
          FILL32 \
          FILL64 \
       -prefix FILL

#ecoRoute

# Run DRC and Connection checks
verifyGeometry
verifyConnectivity -type all -noAntenna

# Output GDSII and include layout of subcells to later view in magic
setStreamOutMode -snapToMGrid true -supportPathType4 false
```

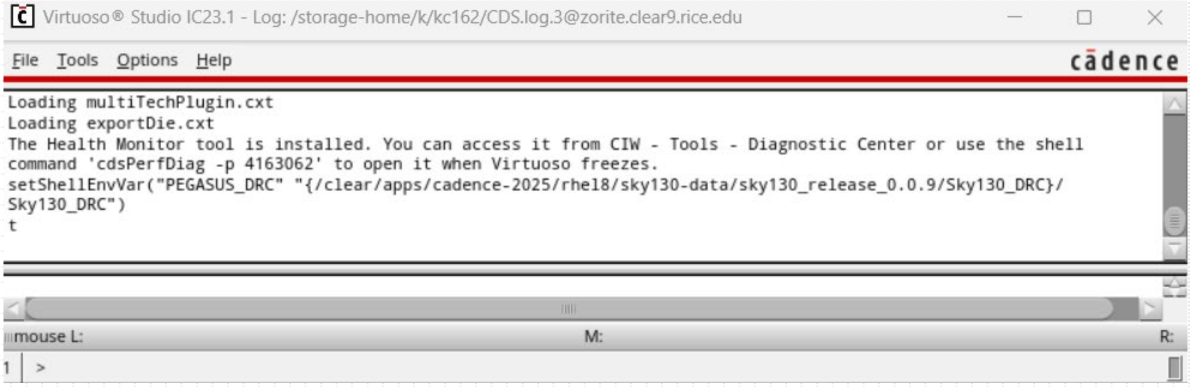
```
streamOut final.gds -mapFile $skywater/sky130_scl_9T/gds/sky130_stream.mapFile -libName DesignLib -units 1000 -merge $skywater/sky130_scl_9T/gds/sky130_scl_9T.gds -mode ALL


# Output a final Verilog file and design database with connectivity modeled

saveNetlist final.v

saveDesign $init_top_cell.enc


#/clear/apps/cadence-2025/rhel8/sky130-data
```

4. Run your file: innovus-2025 -files new_innovus.tcl
5. When it asks “Select your PDK (enter a number)”, press “1”.
6. Don’t close GUI yet. (Needed in LVS and DRC in Innovus) Or, you can open it again later.
    a. You can see what it looks

Virtuoso Setup

- Also reference documents **SKY130 DRC User Guide, rev 0.0_2.8.pdf** and **READ.ME** for the sections *“Virtuoso Setup”* and *“LVS and DRC in Innovus”*

1. Create Virtuoso directory in twoP_FSM_DP_template:
        i. mkdir Virtuoso
    b. Go to directory and run:
        i. /clear/apps/elec8/bin/virtuoso-2025
2. Then, in Virtuoso, type:
        i. setShellEnvVar("PEGASUS_DRC" "{path}/Sky130_DRC_rev_0.0_2.8")


Virtuoso® Studio IC23.1 - Log: /storage-home/k/kc162/CDS.log.3@zorite.clear9.rice.edu

```
Loading multiTechPlugin.cxt
Loading exportDie.cxt
The Health Monitor tool is installed. You can access it from CIW - Tools - Diagnostic Center or use the shell
command 'cdsPerfDiag -p 4163062' to open it when Virtuoso freezes.
setShellEnvVar("PEGASUS_DRC" "{/clear/apps/cadence-2025/rhel8/sky130-data/sky130_release_0.0.9/Sky130_DRC}/
Sky130_DRC")
t
```

- *Alternatively*, create a setup.bash in the folder where your final.v file is:
        i. nano setup.bash
    b. Paste the following into setup.bash (with your own path, name, etc.):

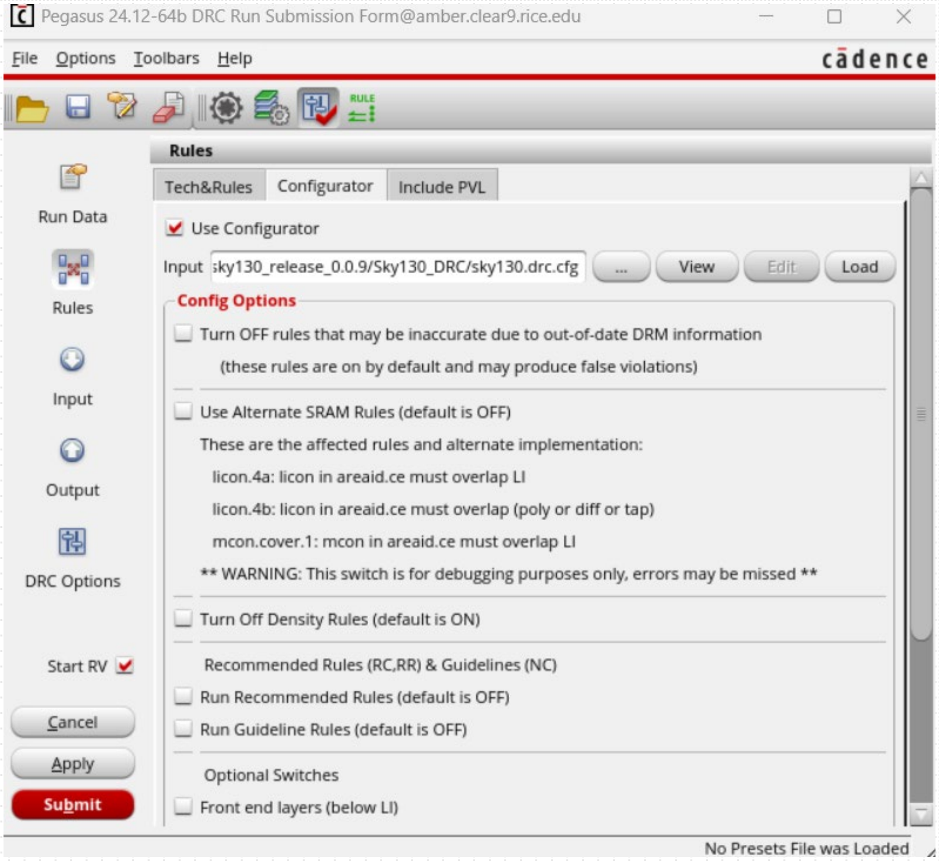
```
# ===== Kelly's Cadence + Sky130 Environment Setup =====
# (1) Source the main Cadence Sky130 environment first
source /clear/apps/cadence-2025/rhel8/sky130-data/setup.bash

# (2) Then define your own variables to make sure everything's consistent
export CDSHOME=/clear/apps/cadence-2025/rhel8
export PDK_DIR=$CDSHOME/sky130-data/sky130_release_0.0.9
export SCL_DIR=$CDSHOME/sky130-data
export PEGASUS_DRC=$PDK_DIR/Sky130_DRC

# (3) Add Cadence tools to PATH (if not already there)
export PATH=$CDSHOME/bin:$PATH

echo "Kelly's Cadence + Sky130 environment loaded successfully!"
```

Every time you run Virtuoso, you must run “source setup.bash” beforehand. (For alternative, see README)

LVS and DRC in Innovus

DRC Setup:

1. To set up environment variable in tcsh:
    a. *If using bash, follow README for step 1.*
        i. `export PEGASUS_DRC=/clear/apps/cadence-2025/rhel8/sky130-data/Sky130_DRC_rev_0.0_2.8`
    b. To check that it is correct:
        i. `echo $PEGASUS_DRC`
2. Follow README for step 2.
    a. /clear/apps/cadence-2025/rhel8/sky130-data/sky130_release_0.0.9/Sky130_DRC/sky130_rev_0.0_2.8.drc.pvl



Pegasus 24.12-64b DRC Run Submission Form@amber.clear9.rice.edu

Rules

☑ Use Configurator

Input sky130_release_0.0.9/Sky130_DRC/sky130.drc.cfg

Config Options

□ Turn OFF rules that may be inaccurate due to out-of-date DRM information
(these rules are on by default and may produce false violations)

□ Use Alternate SRAM Rules (default is OFF)
These are the affected rules and alternate implementation:
licon.4a: licon in areaid.ce must overlap LI
licon.4b: licon in areaid.ce must overlap (poly or diff or tap)
mcon.cover.1: mcon in areaid.ce must overlap LI
** WARNING: This switch is for debugging purposes only, errors may be missed **

□ Turn Off Density Rules (default is ON)

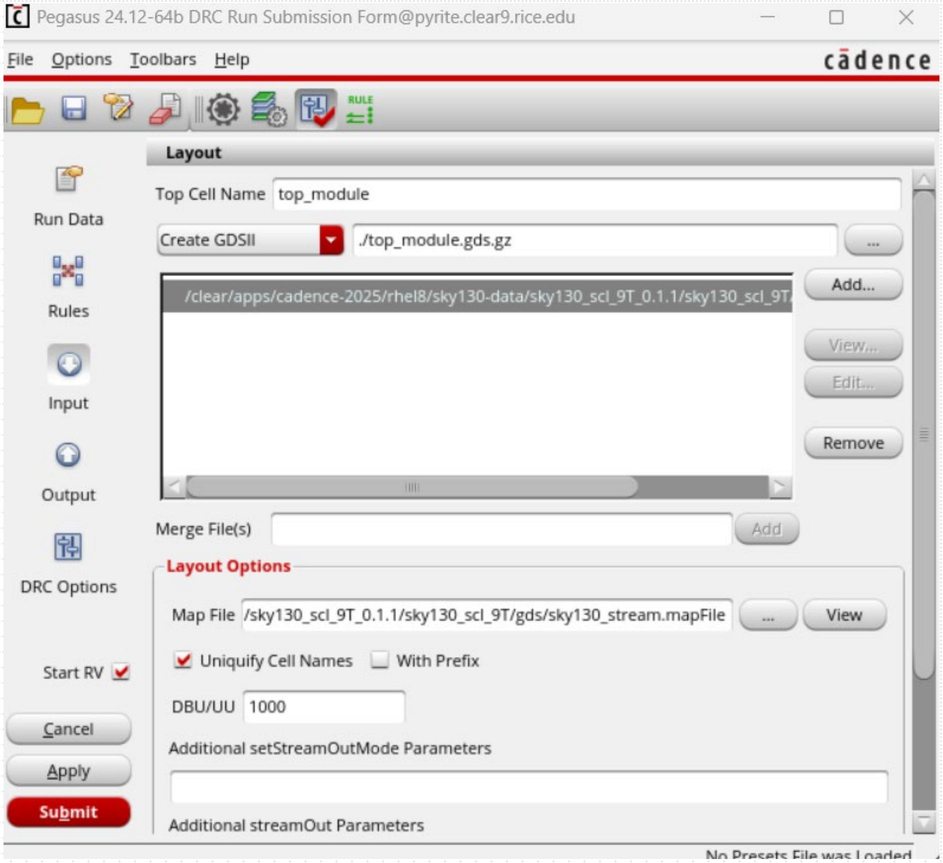
Recommended Rules (RC,RR) & Guidelines (NC)
□ Run Recommended Rules (default is OFF)
□ Run Guideline Rules (default is OFF)

Optional Switches
□ Front end layers (below LI)

Start RV ☑

No Presets File was Loaded

3. For step 3, see below picture while following README:
4. Include this for DRC:



Pegasus 24.12-64b DRC Run Submission Form@pyrite.clear9.rice.edu

Layout

Top Cell Name top_module

Create GDSII ./top_module.gds.gz

/clear/apps/cadence-2025/rhel8/sky130-data/sky130_scl_9T_0.1.1/sky130_scl_9T

Merge File(s)

Layout Options

Map File /sky130_scl_9T_0.1.1/sky130_scl_9T/gds/sky130_stream.mapFile

☑ Uniquify Cell Names □ With Prefix

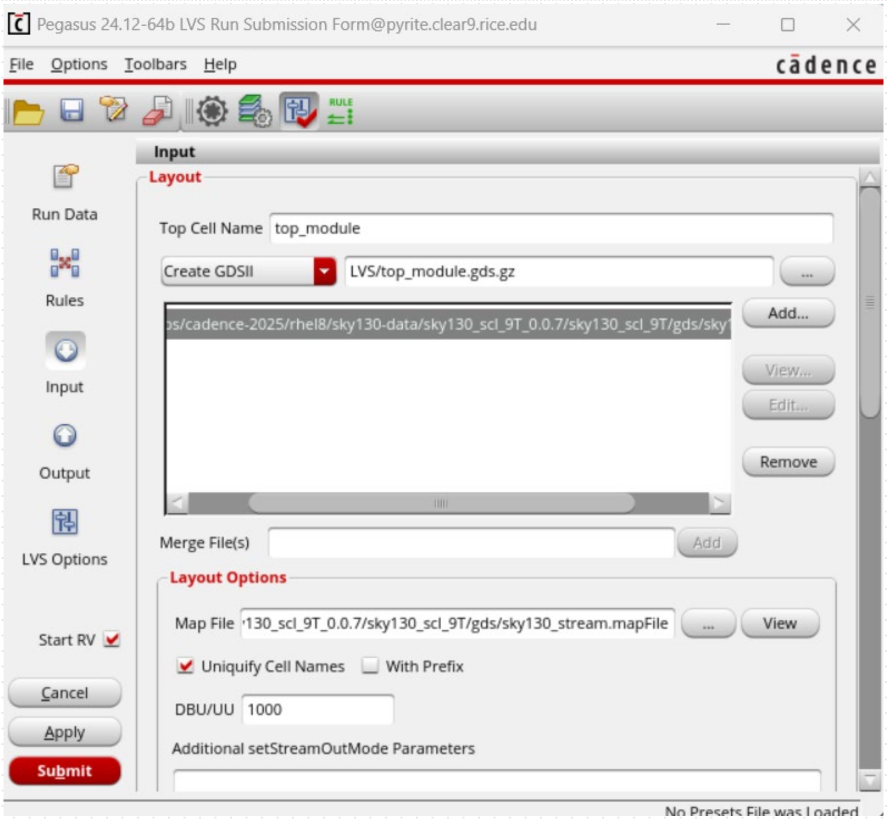
DBU/UU 1000

Additional setStreamOutMode Parameters

Additional streamOut Parameters

Start RV ☑

No Presets File was Loaded



Pegasus 24.12-64b LVS Run Submission Form@pyrite.clear9.rice.edu

Input

Layout

Top Cell Name: top_module

Create GDSII: LVS/top_module.gds.gz

ps/cadence-2025/rhel8/sky130-data/sky130_scl_9T_0.0.7/sky130_scl_9T/gds/sky

Merge File(s):

Layout Options

Map File: '130_scl_9T_0.0.7/sky130_scl_9T/gds/sky130_stream.mapFile

☑ Uniquify Cell Names ☐ With Prefix

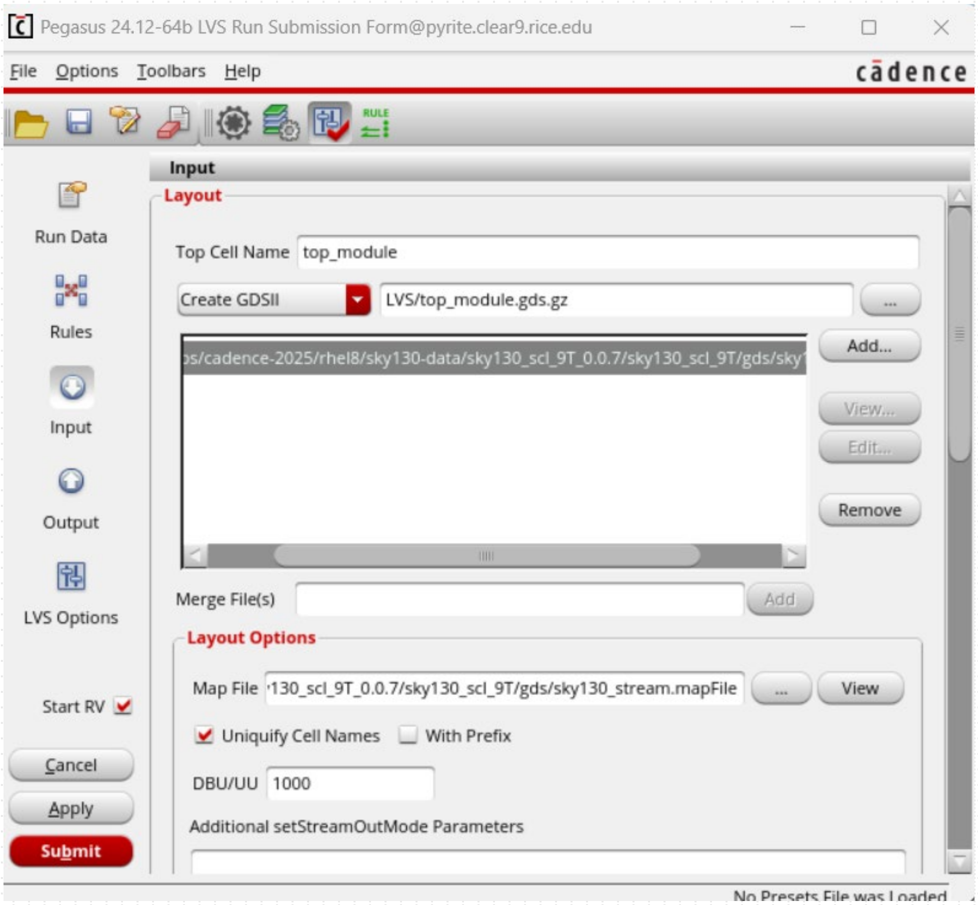
DBU/UU: 1000

Additional setStreamOutMode Parameters

Start RV ☑

No Presets File was Loaded

5. Include this for LVS:



Pegasus 24.12-64b LVS Run Submission Form@pyrite.clear9.rice.edu

Input

Layout

Top Cell Name: top_module

Create GDSII: LVS/top_module.gds.gz

ps/cadence-2025/rhel8/sky130-data/sky130_scl_9T_0.0.7/sky130_scl_9T/gds/sky

Merge File(s):

Layout Options

Map File: '130_scl_9T_0.0.7/sky130_scl_9T/gds/sky130_stream.mapFile

☑ Uniquify Cell Names ☐ With Prefix

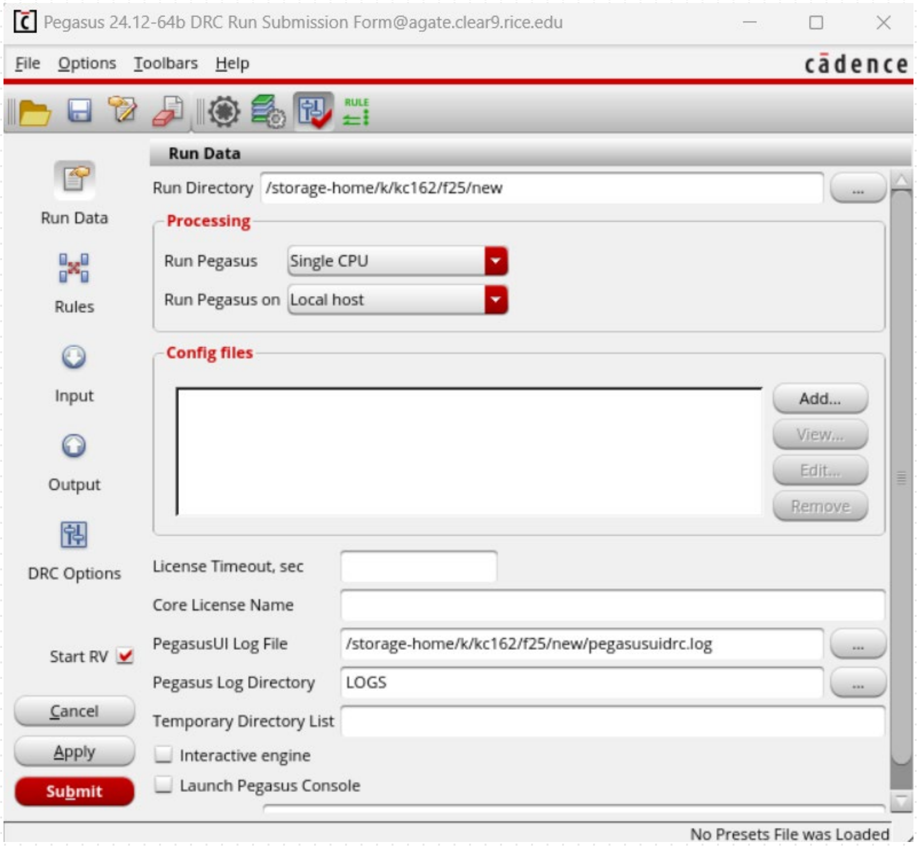
DBU/UU: 1000

Additional setStreamOutMode Parameters

Start RV ☑

No Presets File was Loaded

6. Next, set a new directory for the logs:



Pegasus 24.12-64b DRC Run Submission Form@agate.clear9.rice.edu

Run Data

Run Directory /storage-home/k/kc162/f25/new

Processing

Run Pegasus Single CPU

Run Pegasus on Local host

Config files

License Timeout, sec

Core License Name

PegasusUI Log File /storage-home/k/kc162/f25/new/pegasusuidrc.log

Pegasus Log Directory LOGS

Temporary Directory List

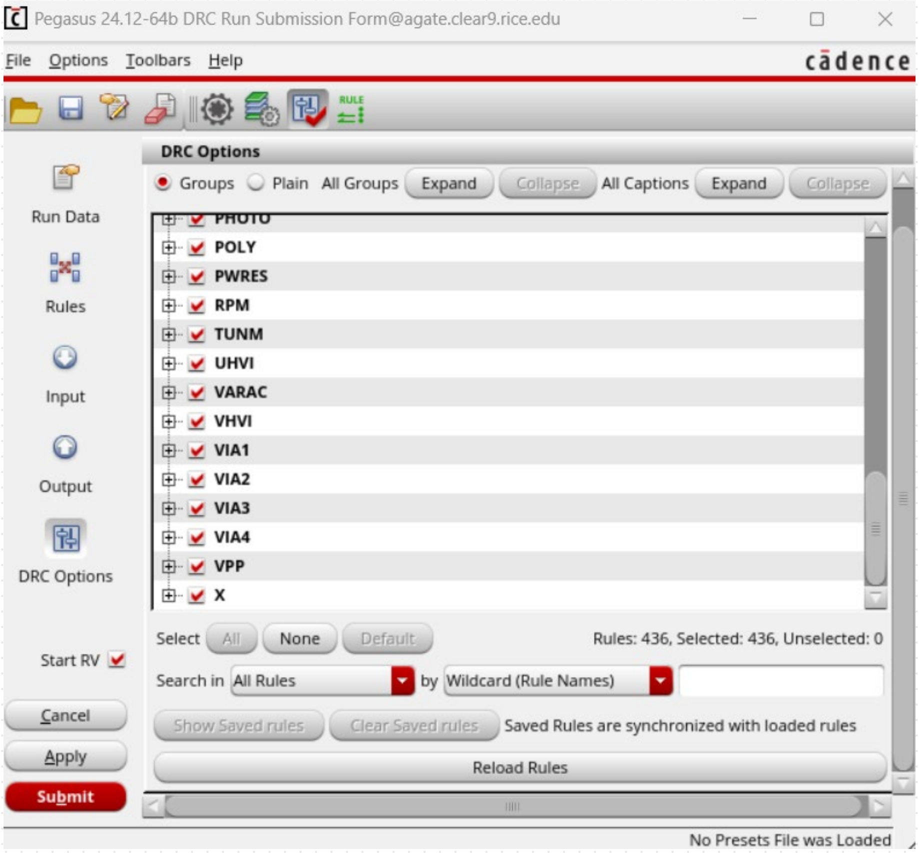
☐ Interactive engine

☐ Launch Pegasus Console

Start RV ☑

No Presets File was Loaded

7. Click “Reload Rules” at the bottom:



Pegasus 24.12-64b DRC Run Submission Form@agate.clear9.rice.edu

DRC Options

● Groups ○ Plain All Groups Expand Collapse All Captions Expand Collapse

☑ PHOTO
☑ POLY
☑ PWRES
☑ RPM
☑ TUNM
☑ UHVI
☑ VARAC
☑ VHVI
☑ VIA1
☑ VIA2
☑ VIA3
☑ VIA4
☑ VPP
☑ X

Select All None Default Rules: 436, Selected: 436, Unselected: 0

Search in All Rules by Wildcard (Rule Names)

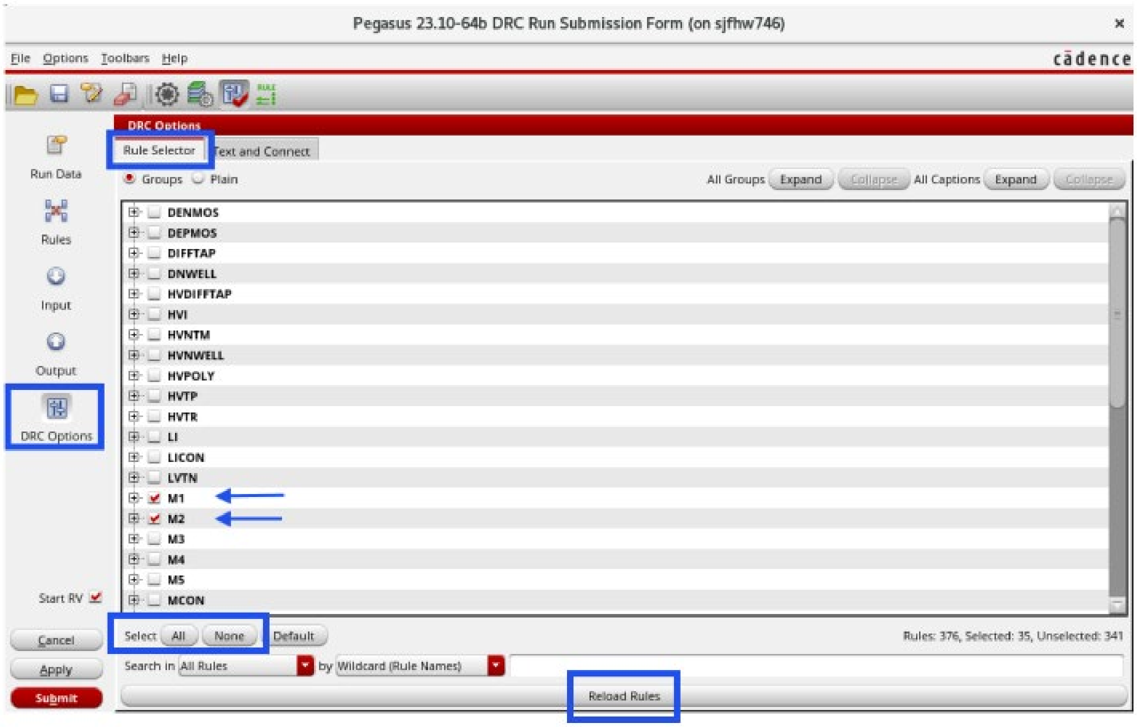
Show Saved rules Clear Saved rules Saved Rules are synchronized with loaded rules

Reload Rules

Start RV ☑

No Presets File was Loaded

8. Then, uncheck these boxes:


Pegasus 23.10-64b DRC Run Submission Form (on sjfhw746)
File Options Toolbars Help
cādence
DRC Options
Rule Selector
Text and Connect
● Groups ○ Plain
All Groups Expand Collapse All Captions Expand Collapse
Run Data
Rules
Input
Output
DRC Options
Start RV ☑
Cancel
Apply
Submit
Select All None Default
Search in All Rules by Wildcard (Rule Names)
Reload Rules

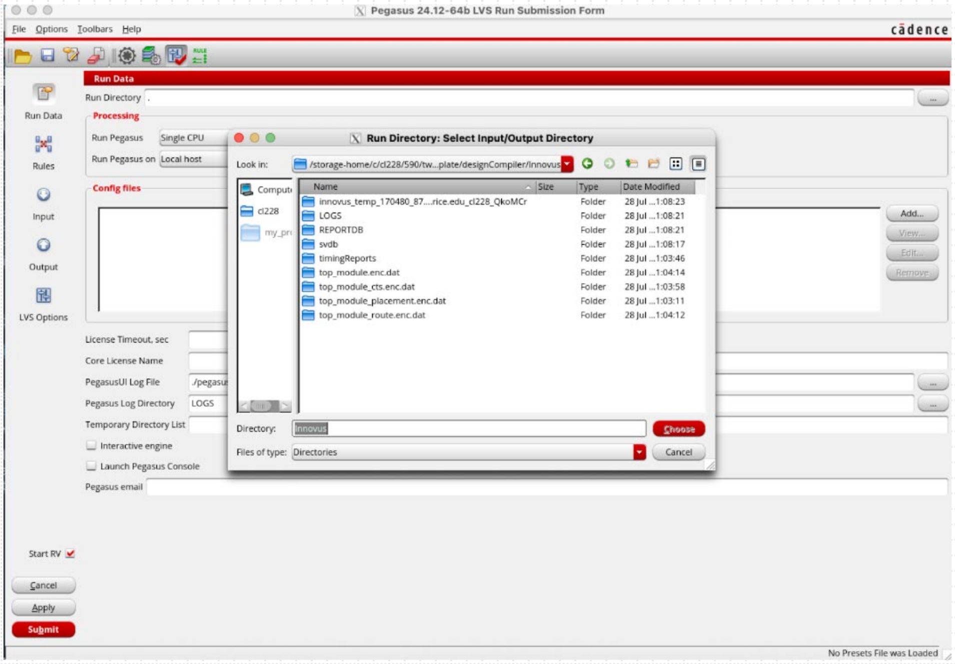
- □ DENMOS
- □ DEPMOS
- □ DIFFTAP
- □ DNWELL
- □ HVDIFFTAP
- □ HVI
- □ HVNTM
- □ HVNWELL
- □ HVPOLY
- □ HVTP
- □ HVTR
- □ LI
- □ LICON
- □ LVTN
- ☑ M1
- ☑ M2
- □ M3
- □ M4
- □ M5
- □ MCON

Rules: 376, Selected: 35, Unselected: 341

LVS Setup:

1. In Innovus GUI, go to "Pegasus" on the top, and then in the dropdown select "Run LVS".

2. Select the "Run Directory":



Run Directory .

Run Pegasus Single CPU

Run Pegasus on Local host

License Timeout, sec

Core License Name

PegasusUI Log File ./pegasu

Pegasus Log Directory LOGS

Temporary Directory List

□ Interactive engine

□ Launch Pegasus Console

Pegasus email

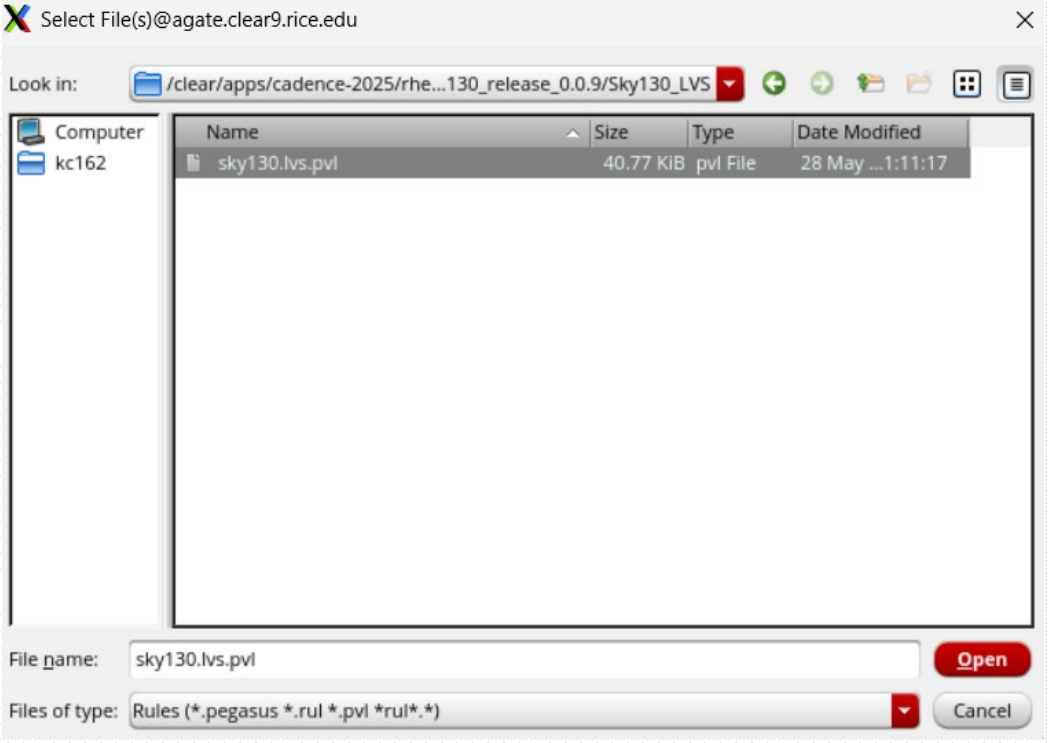
Look in: /storage-home/c/cl228/590/tw...plate/designCompiler/Innovus

Name	Size	Type	Date Modified
innovus_temp_170480_87....rice.edu_cl228_QkoMCr		Folder	28 Jul ...1:08:23
LOGS		Folder	28 Jul ...1:08:21
REPORTDB		Folder	28 Jul ...1:08:21
svdb		Folder	28 Jul ...1:08:17
timingReports		Folder	28 Jul ...1:03:46
top_module.enc.dat		Folder	28 Jul ...1:04:14
top_module_cts.enc.dat		Folder	28 Jul ...1:03:58
top_module_placement.enc.dat		Folder	28 Jul ...1:03:11
top_module_route.enc.dat		Folder	28 Jul ...1:04:12

Directory: Innovus

Files of type: Directories

3. Then, select the pvl file:



Select File(s)@agate.clear9.rice.edu

Look in: /clear/apps/cadence-2025/rhe...130_release_0.0.9/Sky130_LVS

Name	Size	Type	Date Modified
sky130.lvs.pvl	40.77 KiB	pvl File	28 May ...1:11:17

File name: sky130.lvs.pvl

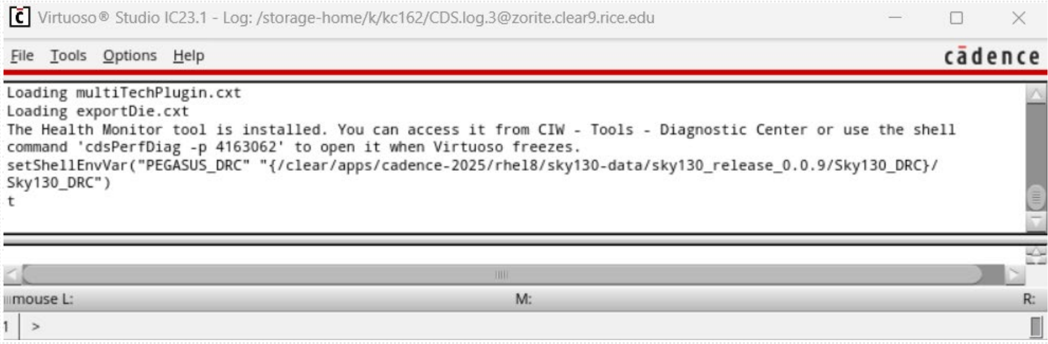
Files of type: Rules (*.pegasus *.rul *.pvl *rul*.*)

Running Virtuoso

Make sure that you pasted your path into Virtuoso (open with virtuoso-2025) first. (Instructions from section titled “Virtuoso Setup”.

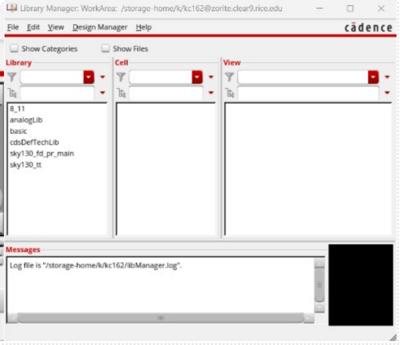
[Can also reference ELEC_590_Summary]

You will see these two windows after opening:



Virtuoso® Studio IC23.1 - Log: /storage-home/k/kc162/CDS.log.3@zorite.clear9.rice.edu

```
Loading multiTechPlugin.cxt
Loading exportDie.cxt
The Health Monitor tool is installed. You can access it from CIW - Tools - Diagnostic Center or use the shell
command 'cdsPerfDiag -p 4163062' to open it when Virtuoso freezes.
setShellEnvVar("PEGASUS_DRC" "{/clear/apps/cadence-2025/rhel8/sky130-data/sky130_release_0.0.9/Sky130_DRC}/
Sky130_DRC")
t
```



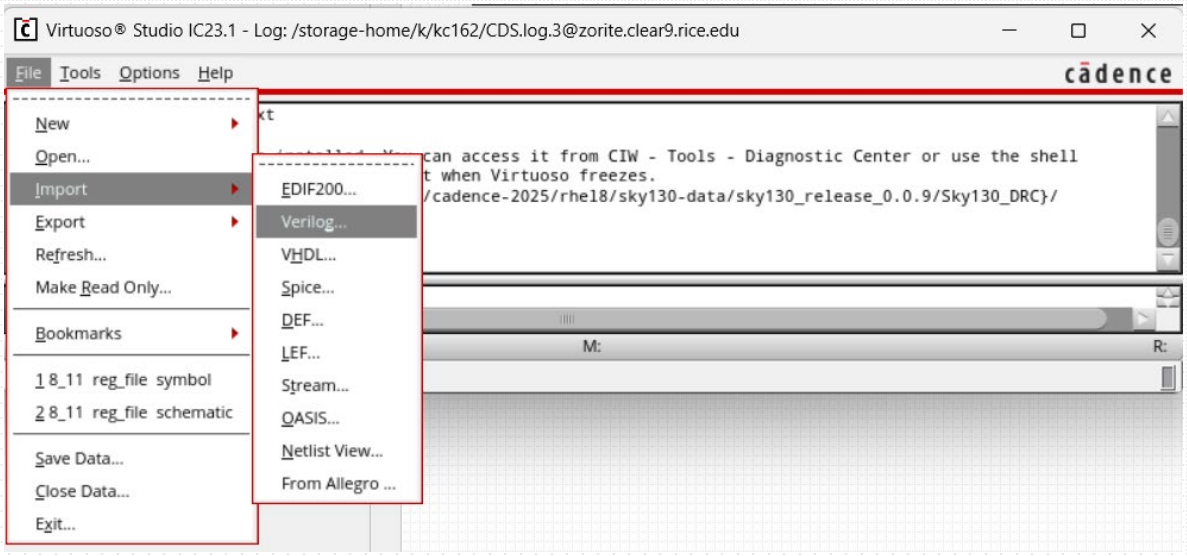
Library Manager: WorkArea: /storage-home/k/kc162@zorite.clear9.rice.edu

□ Show Categories □ Show Files

Library: 8_11, analogLib, basic, cdsDefTechLib, sky130_fd_pr_main, sky130_tt

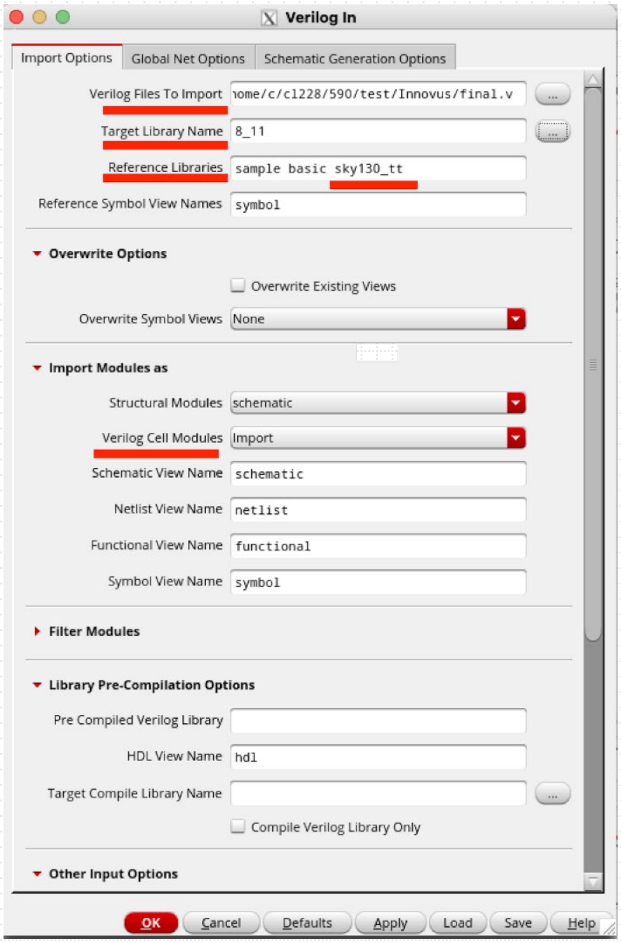
Messages: Log file is "/storage-home/k/kc162/libManager.log".

1. Import your Verilog file



```
xt

can access it from CIW - Tools - Diagnostic Center or use the shell
t when Virtuoso freezes.
/cadence-2025/rhel8/sky130-data/sky130_release_0.0.9/Sky130_DRC}/
```

2. Choose Import Options:



Verilog Files To Import: ıome/c/cl228/590/test/Innovus/final.v

Target Library Name: 8_11

Reference Libraries: sample basic sky130_tt

Reference Symbol View Names: symbol

Overwrite Options

□ Overwrite Existing Views

Overwrite Symbol Views: None

Import Modules as

Structural Modules: schematic

Verilog Cell Modules: Import

Schematic View Name: schematic

Netlist View Name: netlist

Functional View Name: functional

Symbol View Name: symbol

Filter Modules

Library Pre-Compilation Options

Pre Compiled Verilog Library:

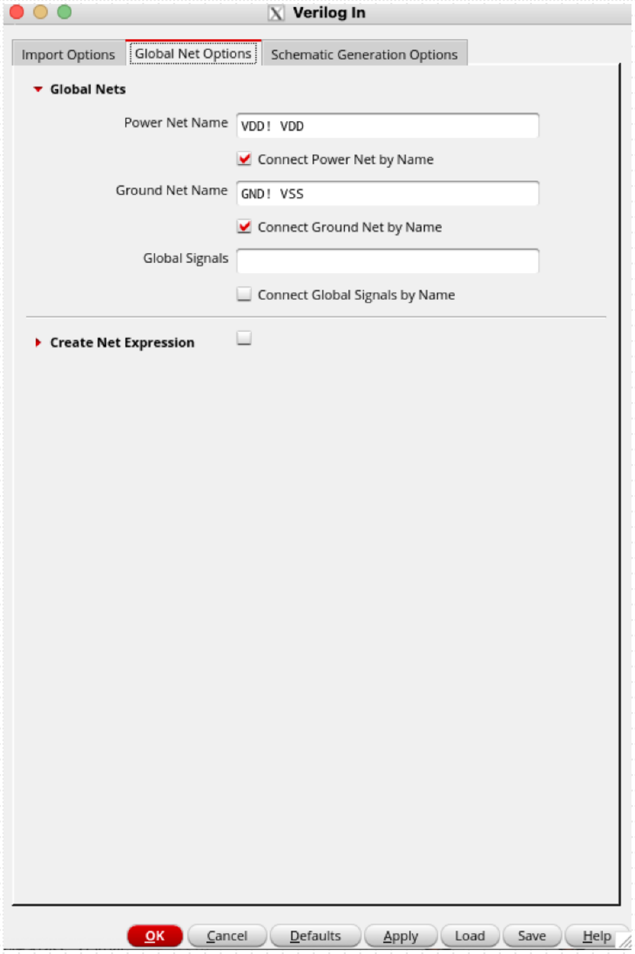
HDL View Name: hdl

Target Compile Library Name:

□ Compile Verilog Library Only

Other Input Options

3. Choose Global Net Options:



Global Nets

Power Net Name: VDD! VDD

☑ Connect Power Net by Name

Ground Net Name: GND! VSS

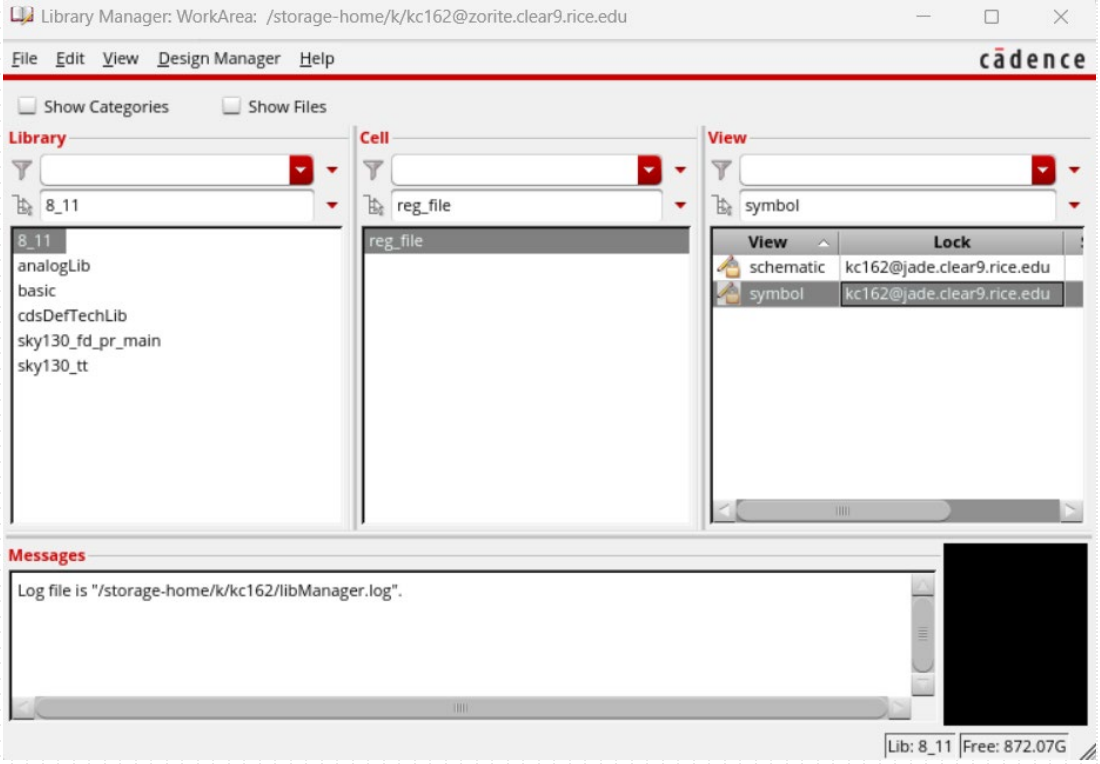
☑ Connect Ground Net by Name

Global Signals:

□ Connect Global Signals by Name

Create Net Expression □

4. To see schematics or symbol, click here:



Library Manager: WorkArea: /storage-home/k/kc162@zorite.clear9.rice.edu

□ Show Categories □ Show Files

Library: 8_11 — 8_11, analogLib, basic, cdsDefTechLib, sky130_fd_pr_main, sky130_tt

Cell: reg_file — reg_file

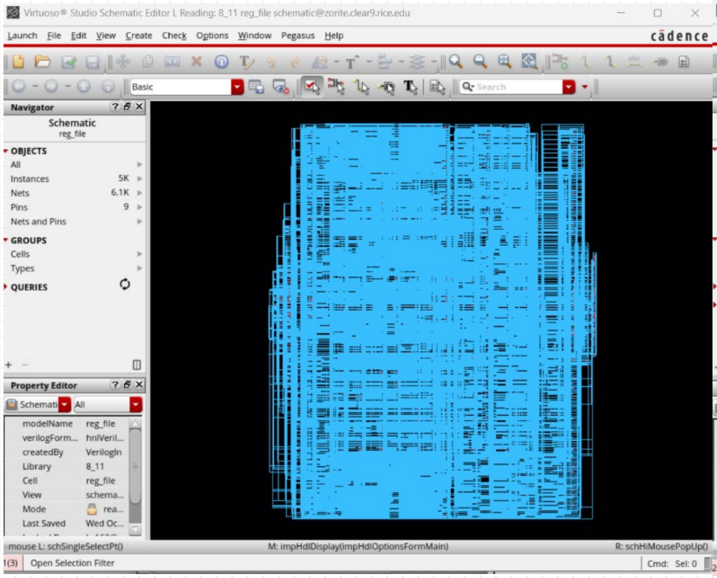
View: symbol

View	Lock
schematic	kc162@jade.clear9.rice.edu
symbol	kc162@jade.clear9.rice.edu

Log file is "/storage-home/k/kc162/libManager.log".

Lib: 8_11 Free: 872.07G

These should pop up (left-schematic, right-symbol):



Virtuoso® Studio Schematic Editor L Reading: 8_11 reg_file schematic@zorite.clear9.rice.edu

OBJECTS	
All	
Instances	5K
Nets	6.1K
Pins	9
Nets and Pins	

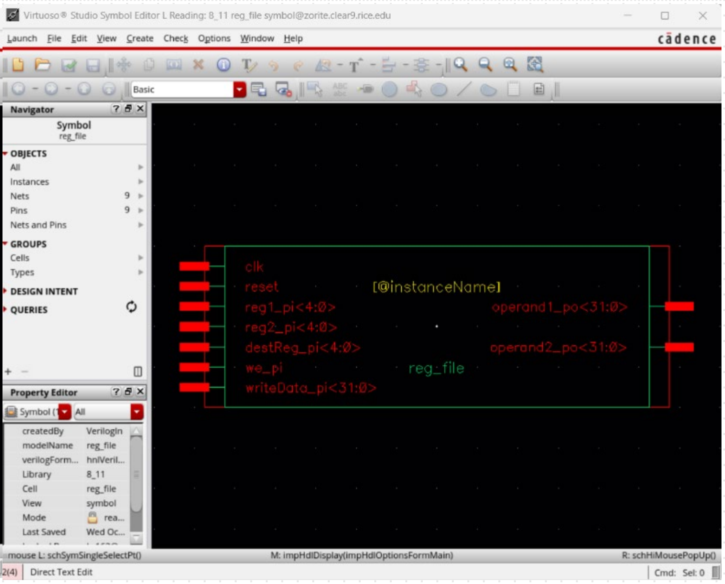
GROUPS
Cells
Types

Schemati All

modelName	reg_file
verilogForm...	hnlVeril...
createdBy	VerilogIn
Library	8_11
Cell	reg_file
View	schema...
Mode	rea...
Last Saved	Wed Oc...

mouse L: schSingleSelectPt() M: impHdlDisplay(impHdlOptionsFormMain) R: schHiMousePopUp()

1(3) Open Selection Filter Cmd: Sel: 0



Virtuoso® Studio Symbol Editor L Reading: 8_11 reg_file symbol@zorite.clear9.rice.edu

OBJECTS	
All	
Instances	
Nets	9
Pins	9
Nets and Pins	

GROUPS
Cells
Types

Symbol (1 All

createdBy	VerilogIn
modelName	reg_file
verilogForm...	hnlVeril...
Library	8_11
Cell	reg_file
View	symbol
Mode	rea...
Last Saved	Wed Oc...

mouse L: schSymSingleSelectPt() M: impHdlDisplay(impHdlOptionsFormMain) R: schHiMousePopUp()

2(4) Direct Text Edit Cmd: Sel: 0