Project file:glib.cpm SYSTEM: <SYSTEM>

EDA-02180-V2-0

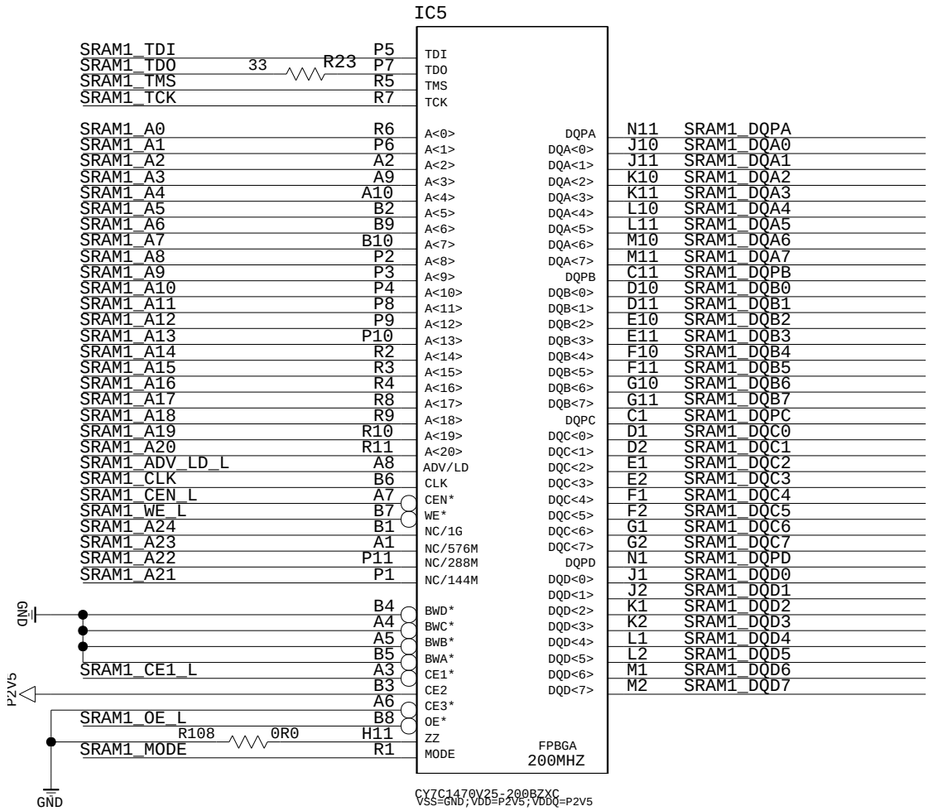
EN/ICE
CERN
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

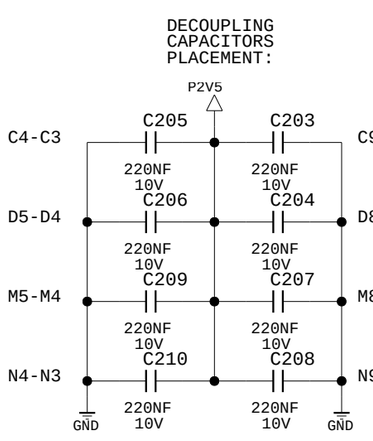
PROJECT:GLIB

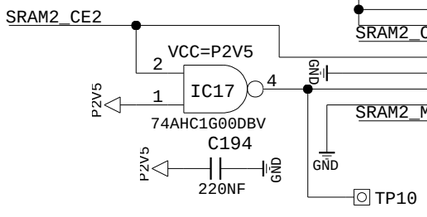
MODULE:glib Sheet: 1/15 Module: / Project: 1/15

LAST_MODIFIED=Tue Apr 26 17:33:29 2011

Design by: P.VICHOUDIS | PCB by: PV | DATE: <DATE>



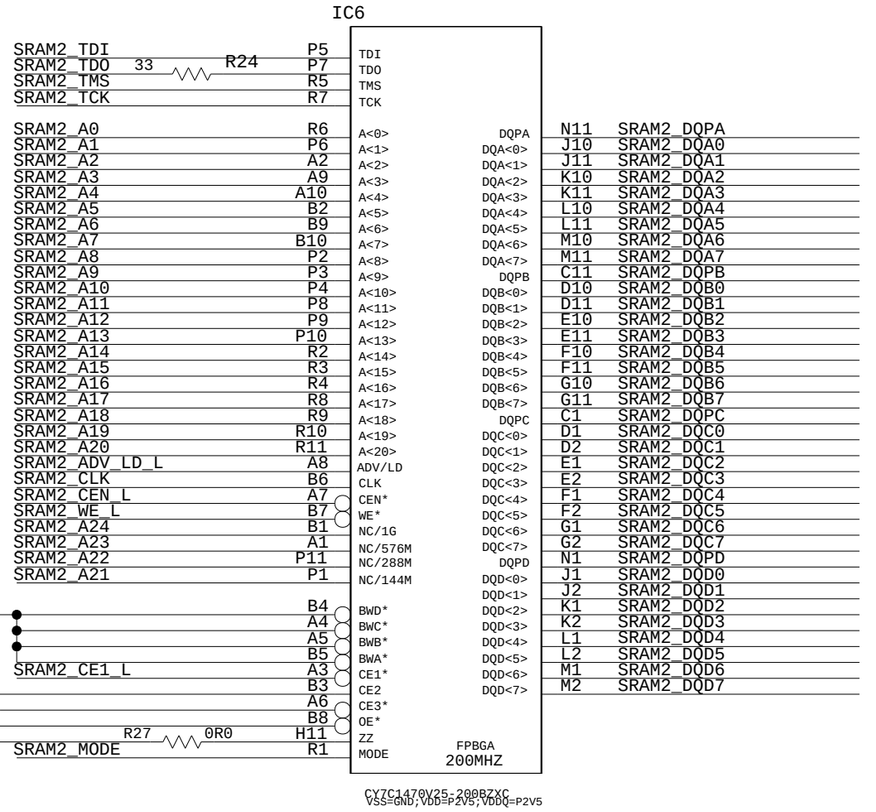


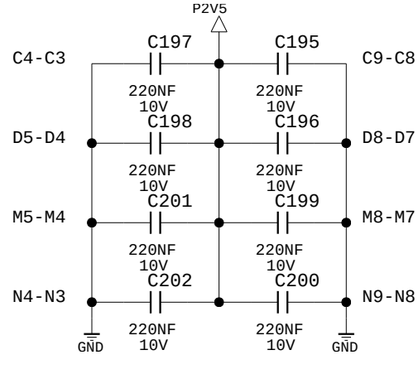


WHEN THE PLATFORM FLASH IS USED
THE CE2 GOES LOW, DISABLING THE SRAM2

ACT\SIG:	FCS_B	FWE_B	FOE_B	CE1_B	CE2	WE_B	OE_B
FLASH WR	0	0	1	X	0	X	1
FLASH RD	0	1	0	X	0	X	1
SRAM2 WR	1	X	1	0	1	0	X
SRAM2 RD	1	X	1	0	1	1	0

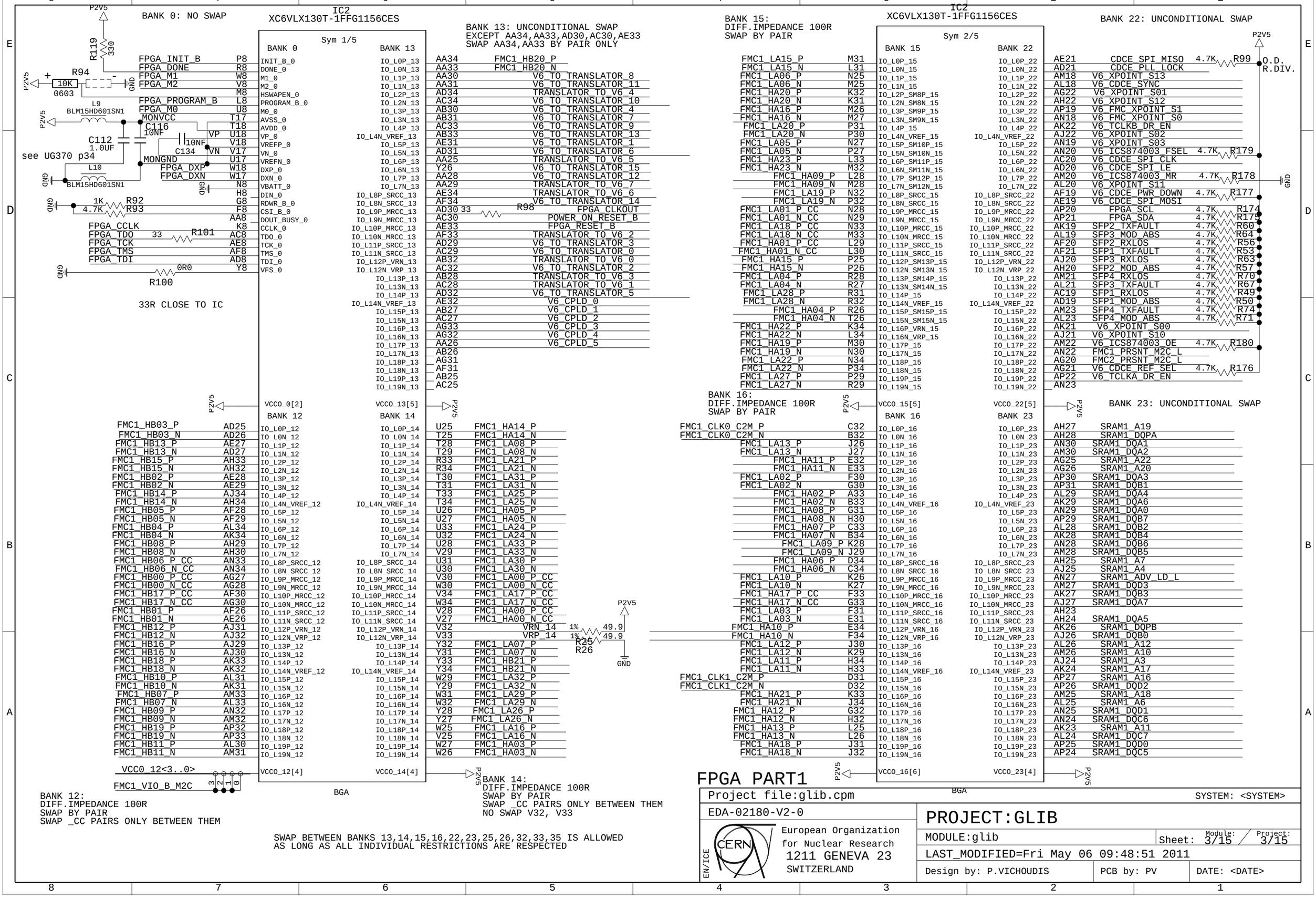
1. FCS_B -> CE2
2. FWE_B -> WE_B
3. FPGA IO -> CE1_B
4. OE_B -> NOT CE2





SRAMS

Project file:glib.cpm	SYSTEM: <SYSTEM>
EDA-02180-V2-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:glib — Sheet: 2/15 (Module: 2/15, Project: 2/15)
EN/ICE	LAST_MODIFIED=Fri May 06 09:48:51 2011
	Design by: P.VICHOUDIS — PCB by: PV — DATE: <DATE>


IC2
XC6VLX130T-1FFG1156CES
Sym 1/5
BANK 0
BANK 13
BANK 12
BANK 14
BANK 0: NO SWAP
BANK 13: UNCONDITIONAL SWAP
EXCEPT AA34,AA33,AD30,AC30,AE33
SWAP AA34,AA33 BY PAIR ONLY
BANK 15:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
BANK 16:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
IC2
XC6VLX130T-1FFG1156CES
Sym 2/5
BANK 15
BANK 22
BANK 16
BANK 23
BANK 22: UNCONDITIONAL SWAP
BANK 23: UNCONDITIONAL SWAP
P2V5
GND
R119 330
R94 10K 0603
L9 BLM15HD601SN1
L10 BLM15HD601SN1
see UG370 p34
C112 1.0UF
C116 10NF
C134 10NF
MONVCC
MONGND
VP
VN
R92 1K
R93 4.7K
R101 33
R100 0R0
33R CLOSE TO IC
R98 33
R25 49.9
R26 49.9
1%
FPGA_INIT_B P8
FPGA_DONE R8
FPGA_M1 W8
FPGA_M2 V8
M8
FPGA_PROGRAM_B L8
FPGA_M0 U8
T17
T18
U18
V18
V17
U17
FPGA_DXP W18
FPGA_DXN W17
N8
H8
G8
F8
AA8
FPGA_CCLK K8
FPGA_TDO AC8
FPGA_TCK AE8
FPGA_TMS AF8
FPGA_TDI AD8
Y8
FMC1_HB03_P AD25
FMC1_HB03_N AD26
FMC1_HB13_P AE27
FMC1_HB13_N AD27
FMC1_HB15_P AH33
FMC1_HB15_N AH32
FMC1_HB02_P AE28
FMC1_HB02_N AE29
FMC1_HB14_P AJ34
FMC1_HB14_N AH34
FMC1_HB05_P AF28
FMC1_HB05_N AF29
FMC1_HB04_P AL34
FMC1_HB04_N AK34
FMC1_HB08_P AH29
FMC1_HB08_N AH30
FMC1_HB06_P_CC AN33
FMC1_HB06_N_CC AN34
FMC1_HB00_P_CC AG27
FMC1_HB00_N_CC AG28
FMC1_HB17_P_CC AF30
FMC1_HB17_N_CC AG30
FMC1_HB01_P AF26
FMC1_HB01_N AE26
FMC1_HB12_P AJ31
FMC1_HB12_N AJ32
FMC1_HB16_P AJ29
FMC1_HB16_N AJ30
FMC1_HB18_P AK33
FMC1_HB18_N AK32
FMC1_HB10_P AL31
FMC1_HB10_N AK31
FMC1_HB07_P AM33
FMC1_HB07_N AL33
FMC1_HB09_P AN32
FMC1_HB09_N AM32
FMC1_HB19_P AP32
FMC1_HB19_N AP33
FMC1_HB11_P AL30
FMC1_HB11_N AM31
VCC0_12<3..0>
FMC1_VIO_B_M2C
AA34 FMC1_HB20_P
AA33 FMC1_HB20_N
AA30 V6_TO_TRANSLATOR_8
AA31 V6_TO_TRANSLATOR_11
AD34 TRANSLATOR_TO_V6_4
AC34 V6_TO_TRANSLATOR_10
AB30 V6_TO_TRANSLATOR_4
AB31 V6_TO_TRANSLATOR_7
AC33 V6_TO_TRANSLATOR_9
AB33 V6_TO_TRANSLATOR_13
AE31 V6_TO_TRANSLATOR_1
AD31 V6_TO_TRANSLATOR_6
AA25 TRANSLATOR_TO_V6_5
Y26 V6_TO_TRANSLATOR_15
AA28 V6_TO_TRANSLATOR_12
AA29 TRANSLATOR_TO_V6_7
AE34 TRANSLATOR_TO_V6_6
AF34 V6_TO_TRANSLATOR_14
AD30 33 FPGA_CLKOUT
AC30 POWER_ON_RESET_B
AE33 FPGA_RESET_B
AF33 TRANSLATOR_TO_V6_2
AD29 V6_TO_TRANSLATOR_3
AC29 V6_TO_TRANSLATOR_0
AB32 TRANSLATOR_TO_V6_0
AC32 V6_TO_TRANSLATOR_2
AB28 TRANSLATOR_TO_V6_3
AC28 TRANSLATOR_TO_V6_1
AD32 V6_TO_TRANSLATOR_5
AE32 V6_CPLD_0
AB27 V6_CPLD_1
AC27 V6_CPLD_2
AG33 V6_CPLD_3
AG32 V6_CPLD_4
AA26 V6_CPLD_5
AB26
AG31
AF31
AB25
AC25
U25 FMC1_HA14_P
T25 FMC1_HA14_N
T28 FMC1_LA08_P
T29 FMC1_LA08_N
R33 FMC1_LA21_P
R34 FMC1_LA21_N
T30 FMC1_LA31_P
T31 FMC1_LA31_N
T33 FMC1_LA25_P
T34 FMC1_LA25_N
U26 FMC1_HA05_P
U27 FMC1_HA05_N
U33 FMC1_LA24_P
U32 FMC1_LA24_N
U28 FMC1_LA33_P
V29 FMC1_LA33_N
U31 FMC1_LA30_P
U30 FMC1_LA30_N
V30 FMC1_LA00_P_CC
W30 FMC1_LA00_N_CC
V34 FMC1_LA17_P_CC
W34 FMC1_LA17_N_CC
V28 FMC1_HA00_P_CC
V27 FMC1_HA00_N_CC
V32 VRN_14
V33 VRP_14
Y32 FMC1_LA07_P
Y31 FMC1_LA07_N
Y33 FMC1_HB21_P
Y34 FMC1_HB21_N
W29 FMC1_LA32_P
Y29 FMC1_LA32_N
W31 FMC1_LA29_P
W32 FMC1_LA29_N
Y28 FMC1_LA26_P
Y27 FMC1_LA26_N
W25 FMC1_LA16_P
V25 FMC1_LA16_N
W27 FMC1_HA03_P
W26 FMC1_HA03_N
FMC1_LA15_P M31
FMC1_LA15_N L31
FMC1_LA06_P N25
FMC1_LA06_N M25
FMC1_HA20_P K32
FMC1_HA20_N K31
FMC1_HA16_P M26
FMC1_HA16_N M27
FMC1_LA20_P P31
FMC1_LA20_N P30
FMC1_LA05_P N27
FMC1_LA05_N P27
FMC1_HA23_P L33
FMC1_HA23_N M32
FMC1_HA09_P L28
FMC1_HA09_N M28
FMC1_LA19_P N32
FMC1_LA19_N P32
FMC1_LA01_P_CC N28
FMC1_LA01_N_CC N29
FMC1_LA18_P_CC N33
FMC1_LA18_N_CC M33
FMC1_HA01_P_CC L29
FMC1_HA01_N_CC L30
FMC1_HA15_P P25
FMC1_HA15_N P26
FMC1_LA04_P R28
FMC1_LA04_N R27
FMC1_LA28_P R31
FMC1_LA28_N R32
FMC1_HA04_P R26
FMC1_HA04_N T26
FMC1_HA22_P K34
FMC1_HA22_N L34
FMC1_HA19_P M30
FMC1_HA19_N N30
FMC1_LA22_P N34
FMC1_LA22_N P34
FMC1_LA27_P P29
FMC1_LA27_N R29
FMC1_CLK0_C2M_P C32
FMC1_CLK0_C2M_N B32
FMC1_LA13_P J26
FMC1_LA13_N J27
FMC1_HA11_P E32
FMC1_HA11_N E33
FMC1_LA02_P F30
FMC1_LA02_N G30
FMC1_HA02_P A33
FMC1_HA02_N B33
FMC1_HA08_P G31
FMC1_HA08_N H30
FMC1_HA07_P C33
FMC1_HA07_N B34
FMC1_LA09_P K28
FMC1_LA09_N J29
FMC1_HA06_P D34
FMC1_HA06_N C34
FMC1_LA10_P K26
FMC1_LA10_N K27
FMC1_HA17_P_CC F33
FMC1_HA17_N_CC G33
FMC1_LA03_P F31
FMC1_LA03_N E31
FMC1_HA10_P E34
FMC1_HA10_N F34
FMC1_LA12_P J30
FMC1_LA12_N K29
FMC1_LA11_P H34
FMC1_LA11_N H33
FMC1_CLK1_C2M_P D31
FMC1_CLK1_C2M_N D32
FMC1_HA21_P K33
FMC1_HA21_N J34
FMC1_HA12_P G32
FMC1_HA12_N H32
FMC1_HA13_P L25
FMC1_HA13_N L26
FMC1_HA18_P J31
FMC1_HA18_N J32
AE21 CDCE_SPI_MISO
AD21 CDCE_PLL_LOCK
AM18 V6_XPOINT_S13
AL18 V6_CDCE_SYNC
AG22 V6_XPOINT_S01
AH22 V6_XPOINT_S12
AP19 V6_FMC_XPOINT_S1
AN18 V6_FMC_XPOINT_S0
AK22 V6_TCLKB_DR_EN
AJ22 V6_XPOINT_S02
AN19 V6_XPOINT_S03
AN20 V6_ICS874003_FSEL
AC20 V6_CDCE_SPI_CLK
AD20 V6_CDCE_SPI_LE
AM20 V6_ICS874003_MR
AL20 V6_XPOINT_S11
AF19 V6_CDCE_PWR_DOWN
AE19 V6_CDCE_SPI_MOSI
AP20 FPGA_SCL
AP21 FPGA_SDA
AK19 SFP2_TXFAULT
AL19 SFP3_MOD_ABS
AF20 SFP2_RXLOS
AF21 SFP1_TXFAULT
AJ20 SFP3_RXLOS
AH20 SFP2_MOD_ABS
AM21 SFP4_RXLOS
AL21 SFP3_TXFAULT
AC19 SFP1_RXLOS
AD19 SFP1_MOD_ABS
AM23 SFP4_TXFAULT
AL23 SFP4_MOD_ABS
AK21 V6_XPOINT_S00
AJ21 V6_XPOINT_S10
AM22 V6_ICS874003_OE
AN22 FMC1_PRSNT_M2C_L
AG20 FMC2_PRSNT_M2C_L
AG21 V6_CDCE_REF_SEL
AP22 V6_TCLKA_DR_EN
AN23
AH27 SRAM1_A19
AH28 SRAM1_DQPA
AN30 SRAM1_DQA1
AM30 SRAM1_DQA2
AG25 SRAM1_A22
AG26 SRAM1_A20
AP30 SRAM1_DQA3
AP31 SRAM1_DQB1
AL29 SRAM1_DQA4
AK29 SRAM1_DQA6
AN29 SRAM1_DQA0
AP29 SRAM1_DQB7
AL28 SRAM1_DQB2
AK28 SRAM1_DQB4
AN28 SRAM1_DQB6
AM28 SRAM1_DQB5
AH25 SRAM1_A7
AJ25 SRAM1_A4
AN27 SRAM1_ADV_LD_L
AM27 SRAM1_DQD3
AK27 SRAM1_DQB3
AJ27 SRAM1_DQA7
AH23
AH24 SRAM1_DQA5
AK26 SRAM1_DQPB
AJ26 SRAM1_DQB0
AL26 SRAM1_A12
AM26 SRAM1_A10
AJ24 SRAM1_A3
AK24 SRAM1_A17
AP27 SRAM1_A16
AP26 SRAM1_DQD2
AM25 SRAM1_A18
AL25 SRAM1_A6
AN25 SRAM1_DQD1
AN24 SRAM1_DQC6
AK23 SRAM1_A11
AL24 SRAM1_DQC7
AP25 SRAM1_DQD0
AP24 SRAM1_DQC5
R99 0.D. R.DIV.
R179
R178
R177
R174
R175
R60
R64
R56
R53
R63
R57
R70
R67
R49
R50
R74
R71
R180
R176
R172
R173
R61
R65
R55
R54
R62
R58
R69
R66
R48
R51
R73
R72
R181
R177
R171
R170
R59
R68
R52
R54
R62
R58
R69
R66
R48
R51
R73
R72
BANK 12:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM
BANK 14:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM
NO SWAP V32, V33
SWAP BETWEEN BANKS 13,14,15,16,22,23,25,26,32,33,35 IS ALLOWED
AS LONG AS ALL INDIVIDUAL RESTRICTIONS ARE RESPECTED
BGA
FPGA PART1
Project file:glib.cpm
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SWITZERLAND
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LAST_MODIFIED=Fri May 06 09:48:51 2011
Design by: P.VICHOUDIS
PCB by: PV
DATE: <DATE>

IC2 XC6VLX130T-1FFG1156CES

BANK 33:
DIFF.IMPEDANCE 100R
SWAP BY PAIR

	FMC2_HA14_P	AE13
	FMC2_HA14_N	AE12
	FMC2_LA16_P	AJ11
	FMC2_LA16_N	AK11
	FMC2_LA19_P	AD14
	FMC2_LA19_N	AC14
	FMC2_HA20_P	AK12
	FMC2_HA20_N	AJ12
	FMC2_HA10_P	AF11
	FMC2_HA10_N	AE11
	FMC2_HA06_P	AM10
	FMC2_HA06_N	AL10
	FMC2_HA11_P	AG11
	FMC2_HA11_N	AG10
	FMC2_LA21_P	AL11
	FMC2_LA21_N	AM11
AMC_P2_TX_P		AJ10
AMC_P2_TX_N		AH10
AMC_P2_RX_P		AC13
AMC_P2_RX_N		AC12
AMC_P3_TX_P		AD12
AMC_P3_TX_N		AD11
AMC_P3_RX_P		AP11
AMC_P3_RX_N		AP12
AMC_P12_TX_P		AF13
AMC_P12_TX_N		AG13
AMC_P12_RX_P		AM12
AMC_P12_RX_N		AN12
AMC_P13_TX_P		AE14
AMC_P13_TX_N		AF14
AMC_P13_RX_P		AN13
AMC_P13_RX_N		AM13
AMC_P14_TX_P		AG12
AMC_P14_TX_N		AH12
AMC_P14_RX_P		AK13
AMC_P14_RX_N		AL13
AMC_P15_TX_P		AH13
AMC_P15_TX_N		AH14
AMC_P15_RX_P		AP14
AMC_P15_RX_N		AN14

P2V5

BANK 34: NO SWAP

XPOINT_CLK3_P		J9
XPOINT_CLK3_N		H9
MCLK_0_P		A10
MCLK_0_N		B10
FA15	SRAM2_A15	F9
FA14	SRAM2_A14	F10
FA13	SRAM2_A13	C10
FA12	SRAM2_A12	D10
FA11	SRAM2_A11	C9
FA10	SRAM2_A10	D9
FA9	SRAM2_A9	A9
FA8	SRAM2_A8	A8
FA7	SRAM2_A7	E8
FA6	SRAM2_A6	E9
FA5	SRAM2_A5	B8
FA4	SRAM2_A4	C8
	SRAM2_DQPA	L9
	SRAM2_DQPB	K9
SRAM2_CLK	33 R84	L10
		M10
	SRAM2_CEN_L	AC10
	SRAM2_MODE	AB10
	SRAM2_ADV_LD_L	AH9
SRAM2_DQD7		AJ9
FA3	SRAM2_A3	AD10
FA2	SRAM2_A2	AC9
FA1	SRAM2_A1	AK8
FA0	SRAM2_A0	AL8
SRAM2_DQD6		AD9
	SRAM2_A24	AE9
	SRAM2_A23	AK9
FA22	SRAM2_A22	AL9
FA21	SRAM2_A21	AF9
FA20	SRAM2_A20	AF10
FA19	SRAM2_A19	AN9
FA18	SRAM2_A18	AP9
FA17	SRAM2_A17	AG8
FA16	SRAM2_A16	AH8
R107	49.9 VRN_34	AN10
R105	49.9 VRP_34	AP10

GND

33R CLOSE TO IC

P2V5

Sym 4/5

BANK 33	BANK 35
IO_L0P_33	IO_L0P_35
IO_L0N_33	IO_L0N_35
IO_L1P_33	IO_L1P_35
IO_L1N_33	IO_L1N_35
IO_L2P_33	IO_L2P_SM0P_35
IO_L2N_33	IO_L2N_SM0N_35
IO_L3P_33	IO_L3P_SM1P_35
IO_L3N_33	IO_L3N_SM1N_35
IO_L4P_33	IO_L4P_35
IO_L4N_VREF_33	IO_L4N_VREF_35
IO_L5P_33	IO_L5P_SM2P_35
IO_L5N_33	IO_L5N_SM2N_35
IO_L6P_33	IO_L6P_SM3P_35
IO_L6N_33	IO_L6N_SM3N_35
IO_L7P_33	IO_L7P_SM4P_35
IO_L7N_33	IO_L7N_SM4N_35
IO_L8P_SRCC_33	IO_L8P_SRCC_35
IO_L8N_SRCC_33	IO_L8N_SRCC_35
IO_L9P_MRCC_33	IO_L9P_MRCC_35
IO_L9N_MRCC_33	IO_L9N_MRCC_35
IO_L10P_MRCC_33	IO_L10P_MRCC_35
IO_L10N_MRCC_33	IO_L10N_MRCC_35
IO_L11P_SRCC_33	IO_L11P_SRCC_35
IO_L11N_SRCC_33	IO_L11N_SRCC_35
IO_L12P_VRN_33	IO_L12P_SM5P_35
IO_L12N_VRP_33	IO_L12N_SM5N_35
IO_L13P_33	IO_L13P_SM6P_35
IO_L13N_33	IO_L13N_SM6N_35
IO_L14P_33	IO_L14P_35
IO_L14N_VREF_33	IO_L14N_VREF_35
IO_L15P_33	IO_L15P_SM7P_35
IO_L15N_33	IO_L15N_SM7N_35
IO_L16P_33	IO_L16P_VRN_35
IO_L16N_33	IO_L16N_VRP_35
IO_L17P_33	IO_L17P_35
IO_L17N_33	IO_L17N_35
IO_L18P_33	IO_L18P_GC_35
IO_L18N_33	IO_L18N_GC_35
IO_L19P_33	IO_L19P_GC_35
IO_L19N_33	IO_L19N_GC_35
VCCO_33[5]	VCCO_35[5\]
BANK 34	BANK 36
IO_L0P_GC_34	IO_L0P_36
IO_L0N_GC_34	IO_L0N_36
IO_L1P_GC_34	IO_L1P_36
IO_L1N_GC_34	IO_L1N_36
IO_L2P_A15_D31_34	IO_L2P_36
IO_L2N_A14_D30_34	IO_L2N_36
IO_L3P_A13_D29_34	IO_L3P_36
IO_L3N_A12_D28_34	IO_L3N_36
IO_L4P_A11_D27_34	IO_L4P_36
IO_L4N_VREF_A10_D26_34	IO_L4N_VREF_36
IO_L5P_A09_D25_34	IO_L5P_36
IO_L5N_A08_D24_34	IO_L5N_36
IO_L6P_A07_D23_34	IO_L6P_36
IO_L6N_A06_D22_34	IO_L6N_36
IO_L7P_A05_D21_34	IO_L7P_36
IO_L7N_A04_D20_34	IO_L7N_36
IO_L8P_SRCC_34	IO_L8P_SRCC_36
IO_L8N_SRCC_34	IO_L8N_SRCC_36
IO_L9P_MRCC_34	IO_L9P_MRCC_36
IO_L9N_MRCC_34	IO_L9N_MRCC_36
IO_L10P_MRCC_34	IO_L10P_MRCC_36
IO_L10N_MRCC_34	IO_L10N_MRCC_36
IO_L11P_SRCC_34	IO_L11P_SRCC_36
IO_L11N_SRCC_34	IO_L11N_SRCC_36
IO_L12P_A03_D19_34	IO_L12P_VRN_36
IO_L12N_A02_D18_34	IO_L12N_VRP_36
IO_L13P_A01_D17_34	IO_L13P_36
IO_L13N_A00_D16_34	IO_L13N_36
IO_L14P_A25_34	IO_L14P_36
IO_L14N_VREF_A24_34	IO_L14N_VREF_36
IO_L15P_A23_34	IO_L15P_36
IO_L15N_A22_34	IO_L15N_36
IO_L16P_A21_34	IO_L16P_36
IO_L16N_A20_34	IO_L16N_36
IO_L17P_A19_34	IO_L17P_36
IO_L17N_A18_34	IO_L17N_36
IO_L18P_A17_34	IO_L18P_36
IO_L18N_A16_34	IO_L18N_36
IO_L19P_VRN_34	IO_L19P_36
IO_L19N_VRP_34	IO_L19N_36
VCCO_34[6]	VCCO_36[4]

BGA

P2V5

BANK 35:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM

G13	FMC2_LA24_P	
H14	FMC2_LA24_N	
D14	FMC2_HA23_P	
C14	FMC2_HA23_N	
G11	FMC2_LA08_P	
F11	FMC2_LA08_N	
A13	FMC2_HA22_P	
A14	FMC2_HA22_N	
G12	FMC2_LA31_P	
H13	FMC2_LA31_N	
F14	FMC2_HA21_P	
E14	FMC2_HA21_N	
H10	FMC2_LA28_P	
G10	FMC2_LA28_N	
B12	FMC2_LA15_P	
B13	FMC2_LA15_N	
K14	FMC2_LA29_P	
J14	FMC2_LA29_N	
L13	FMC2_LA17_P_CC	
M13	FMC2_LA17_N_CC	
M12	FMC2_HA17_P_CC	
M11	FMC2_HA17_N_CC	
C13	FMC2_LA12_P	
C12	FMC2_LA12_N	
H12	FMC2_LA33_P	
J12	FMC2_LA33_N	
A11	FMC2_HA18_P	
B11	FMC2_HA18_N	
J11	FMC2_LA30_P	
J10	FMC2_LA30_N	
E13	FMC2_HB21_P	
F13	FMC2_HB21_N	
K11	FMC2_LA32_P	
L11	FMC2_LA32_N	
D12	FMC2_HA12_P	
E12	FMC2_HA12_N	
K13	FMCX_CLK0_M2C_COPY2_P	
K12	FMCX_CLK0_M2C_COPY2_N	
D11	FMC1_CLK1_M2C_P	
E11	FMC1_CLK1_M2C_N	
F18	FMC2_HB08_P	
E17	FMC2_HB08_N	
E18	FMC2_HB15_P	
D17	FMC2_HB15_N	
K18	FMC2_HB09_P	
K17	FMC2_HB09_N	
H17	FMC2_HB07_P	
G17	FMC2_HB07_N	
L19	FMC2_HB10_P	
L18	FMC2_HB10_N	
C17	FMC2_HB16_P	
B17	FMC2_HB16_N	
K19	FMC2_HB05_P	
J19	FMC2_HB05_N	
M18	FMC2_HB03_P	
M17	FMC2_HB03_N	
G18	FMC2_HB04_P	
H18	FMC2_HB04_N	
K16	FMC2_HB00_P_CC	
L16	FMC2_HB00_N_CC	
L15	FMC2_HB06_P_CC	
L14	FMC2_HB06_N_CC	
A16	FMC2_HB17_P_CC	
B16	FMC2_HB17_N_CC	
F16	FMC2_HB02_P	
G16	FMC2_HB02_N	
E16	FMC2_HB14_P	
D16	FMC2_HB14_N	
J17	FMC2_HB13_P	
J16	FMC2_HB13_N	
A15	FMC2_HB18_P	
B15	FMC2_HB18_N	
G15	FMC2_HB12_P	
F15	FMC2_HB12_N	
M16	FMC2_HB19_P	
M15	FMC2_HB19_N	
H15	FMC2_HB11_P	
J15	FMC2_HB11_N	
D15	FMC2_HB01_P	
C15	FMC2_HB01_N	

VCC0_36<3..0>

3 2 1 0

FMC2_VIO_B_M2C

BANK 36:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM

SWAP BETWEEN BANKS 13,14,15,16,22,23,25,26,32,33,35 IS ALLOWED
AS LONG AS ALL INDIVIDUAL RESTRICTIONS ARE RESPECTED

IC2 XC6VLX130T-1FFG1156CES

BANK 24:
NO SWAP

MGT_REFCLK_COPY_0_P		L23
MGT_REFCLK_COPY_0_N		M22
MGT_REFCLK_COPY_1_P		K24
MGT_REFCLK_COPY_1_N		K23
FD15	SRAM2_DQB7	M23
FD14	SRAM2_DQB6	L24
FD13	SRAM2_DQB5	F24
FD12	SRAM2_DQB4	F23
FD11	SRAM2_DQB3	N23
FD10	SRAM2_DQB2	N24
FD9	SRAM2_DQB1	H23
FD8	SRAM2_DQB0	G23
FD7	SRAM2_DQA7	R24
FD6	SRAM2_DQA6	P24
FD5	SRAM2_DQA5	H25
FD4	SRAM2_DQA4	H24
	SRAM2_DQC7	T24
	SRAM2_DQC6	T23
	SRAM2_DQC5	J25
	SRAM2_DQC4	J24
	SRAM2_DQC3	U23
	SRAM2_DQC2	V23
	SRAM2_DQC1	AD24
	SRAM2_DQC0	AE24
FD3	SRAM2_DQA3	V24
FD2	SRAM2_DQA2	W24
FD1	SRAM2_DQA1	AF25
FD0	SRAM2_DQA0	AF24
FCS_B	SRAM2_CE2	Y24
FOE_B	SRAM2_OE_L	AA24
FWE_B	SRAM2_WE_L	AF23
FPGA_RS1		AG23
FPGA_RS0		AA23
	SRAM2_DQD5	AB23
R103	49.9 VRN_24	AE23
R104	49.9 VRP_24	AE22
L18P_24	SRAM2_CE1_L	AC23
	SRAM2_DQD2	AC24
	SRAM2_DQD1	AC22
	SRAM2_DQD0	AD22

P2V5 GND

BANK 25:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
EXCEPT H28,H29,B31,A31

	FMC2_HA16_P	D25
	FMC2_HA16_N	D26
	FMC2_LA05_P	C24
	FMC2_LA05_N	C25
	FMC2_LA09_P	E26
	FMC2_LA09_N	F26
	FMC2_LA06_P	B25
	FMC2_LA06_N	A25
	FMC2_HA13_P	D27
	FMC2_HA13_N	E27
	FMC2_HA09_P	B26
	FMC2_HA09_N	A26
	FMC2_LA07_P	G26
	FMC2_LA07_N	G27
	FMC2_HA05_P	B27
	FMC2_HA05_N	C27
	FMC1_LA23_P	D24
	FMC1_LA23_N	E24
	FMC2_HA00_P_CC	C28
	FMC2_HA00_N_CC	B28
	FMC2_HA01_P_CC	C29
	FMC2_HA01_N_CC	D29
	FMC1_LA14_P	F25
	FMC1_LA14_N	G25
	FMC2_LA11_P	H27
	FMC2_LA11_N	G28
FMC2_CLK0_C2M_P		A28
FMC2_CLK0_C2M_N		A29
	FMC2_LA03_P	F28
	FMC2_LA03_N	E28
	FMC2_HA03_P	A30
	FMC2_HA03_N	B30
	FMC2_HA04_P	E29
	FMC2_HA04_N	F29
	FMC2_CLK1_C2M_P	C30
	FMC2_CLK1_C2M_N	D30
CLK125_0_P		H28
CLK125_0_N		H29
FMC2_CLK1_M2C_P		B31
FMC2_CLK1_M2C_N		A31

P2V5

Sym 3/5

BANK 24	BANK 26
IO_L0P_GC_24	IO_L0P_26
IO_L0N_GC_24	IO_L0N_26
IO_L1P_GC_24	IO_L1P_26
IO_L1N_GC_24	IO_L1N_26
IO_L2P_D15_24	IO_L2P_26
IO_L2N_D14_24	IO_L2N_26
IO_L3P_D13_24	IO_L3P_26
IO_L3N_D12_24	IO_L3N_26
IO_L4P_D11_24	IO_L4P_26
IO_L4N_VREF_D10_24	IO_L4N_VREF_26
IO_L5P_D9_24	IO_L5P_26
IO_L5N_D8_24	IO_L5N_26
IO_L6P_D7_24	IO_L6P_26
IO_L6N_D6_24	IO_L6N_26
IO_L7P_D5_24	IO_L7P_26
IO_L7N_D4_24	IO_L7N_26
IO_L8P_SRCC_24	IO_L8P_SRCC_26
IO_L8N_SRCC_24	IO_L8N_SRCC_26
IO_L9P_MRCC_24	IO_L9P_MRCC_26
IO_L9N_MRCC_24	IO_L9N_MRCC_26
IO_L10P_MRCC_24	IO_L10P_MRCC_26
IO_L10N_MRCC_24	IO_L10N_MRCC_26
IO_L11P_SRCC_24	IO_L11P_SRCC_26
IO_L11N_SRCC_24	IO_L11N_SRCC_26
IO_L12P_D3_24	IO_L12P_VRN_26
IO_L12N_D2_FS2_24	IO_L12N_VRP_26
IO_L13P_D1_FS1_24	IO_L13P_26
IO_L13N_D0_FS0_24	IO_L13N_26
IO_L14P_FCS_B_24	IO_L14P_26
IO_L14N_VREF_24	IO_L14N_VREF_26
IO_L15P_FWE_B_24	IO_L15P_26
IO_L15N_RS1_24	IO_L15N_26
IO_L16P_RS0_24	IO_L16P_26
IO_L16N_CSO_B_24	IO_L16N_26
IO_L17P_VRN_24	IO_L17P_26
IO_L17N_VRP_24	IO_L17N_26
IO_L18P_24	IO_L18P_26
IO_L18N_24	IO_L18N_26
IO_L19P_24	IO_L19P_26
IO_L19N_24	IO_L19N_26
VCCO_24[6]	VCCO_26[5]
BANK 25	BANK 32
IO_L0P_25	IO_L0P_32
IO_L0N_25	IO_L0N_32
IO_L1P_25	IO_L1P_32
IO_L1N_25	IO_L1N_32
IO_L2P_25	IO_L2P_32
IO_L2N_25	IO_L2N_32
IO_L3P_25	IO_L3P_32
IO_L3N_25	IO_L3N_32
IO_L4P_25	IO_L4P_32
IO_L4N_VREF_25	IO_L4N_VREF_32
IO_L5P_25	IO_L5P_32
IO_L5N_25	IO_L5N_32
IO_L6P_25	IO_L6P_32
IO_L6N_25	IO_L6N_32
IO_L7P_25	IO_L7P_32
IO_L7N_25	IO_L7N_32
IO_L8P_SRCC_25	IO_L8P_SRCC_32
IO_L8N_SRCC_25	IO_L8N_SRCC_32
IO_L9P_MRCC_25	IO_L9P_MRCC_32
IO_L9N_MRCC_25	IO_L9N_MRCC_32
IO_L10P_MRCC_25	IO_L10P_MRCC_32
IO_L10N_MRCC_25	IO_L10N_MRCC_32
IO_L11P_SRCC_25	IO_L11P_SRCC_32
IO_L11N_SRCC_25	IO_L11N_SRCC_32
IO_L12P_25	IO_L12P_VRN_32
IO_L12N_25	IO_L12N_VRP_32
IO_L13P_25	IO_L13P_32
IO_L13N_25	IO_L13N_32
IO_L14P_25	IO_L14P_32
IO_L14N_VREF_25	IO_L14N_VREF_32
IO_L15P_25	IO_L15P_32
IO_L15N_25	IO_L15N_32
IO_L16P_VRN_25	IO_L16P_32
IO_L16N_VRP_25	IO_L16N_32
IO_L17P_25	IO_L17P_32
IO_L17N_25	IO_L17N_32
IO_L18P_GC_25	IO_L18P_32
IO_L18N_GC_25	IO_L18N_32
IO_L19P_GC_25	IO_L19P_32
IO_L19N_GC_25	IO_L19N_32
VCCO_25[4]	VCCO_32[5]

BGA

P2V5

BANK 26:
DIFF.IMPEDANCE 100R
SWAP BY PAIR
SWAP _CC PAIRS ONLY BETWEEN THEM

C20	FMC2_LA26_P	
D20	FMC2_LA26_N	
A23	FMC2_LA10_P	
A24	FMC2_LA10_N	
G21	FMC2_LA02_P	
G22	FMC2_LA02_N	
B23	FMC2_HA15_P	
C23	FMC2_HA15_N	
J20	FMC2_HA02_P	
J21	FMC2_HA02_N	
B21	FMC2_LA14_P	
B22	FMC2_LA14_N	
E22	FMC2_LA13_P	
E23	FMC2_LA13_N	
A20	FMC2_HA19_P	
A21	FMC2_HA19_N	
F19	FMC2_LA22_P	
F20	FMC2_LA22_N	
B20	FMC2_LA18_P_CC	
C19	FMC2_LA18_N_CC	
F21	FMC2_LA00_P_CC	
G20	FMC2_LA00_N_CC	
H19	FMC2_LA01_P_CC	
H20	FMC2_LA01_N_CC	
D21	FMC2_LA23_P	
E21	FMC2_LA23_N	
E19	FMC2_LA25_P	
D19	FMC2_LA25_N	
H22	FMC2_HA07_P	
J22	FMC2_HA07_N	
A18	FMC2_LA27_P	
A19	FMC2_LA27_N	
K21	FMC2_HA08_P	
K22	FMC2_HA08_N	
B18	FMC2_HB20_P	
C18	FMC2_HB20_N	
L20	FMC2_LA04_P	
L21	FMC2_LA04_N	
C22	FMC2_LA20_P	
D22	FMC2_LA20_N	

P2V5

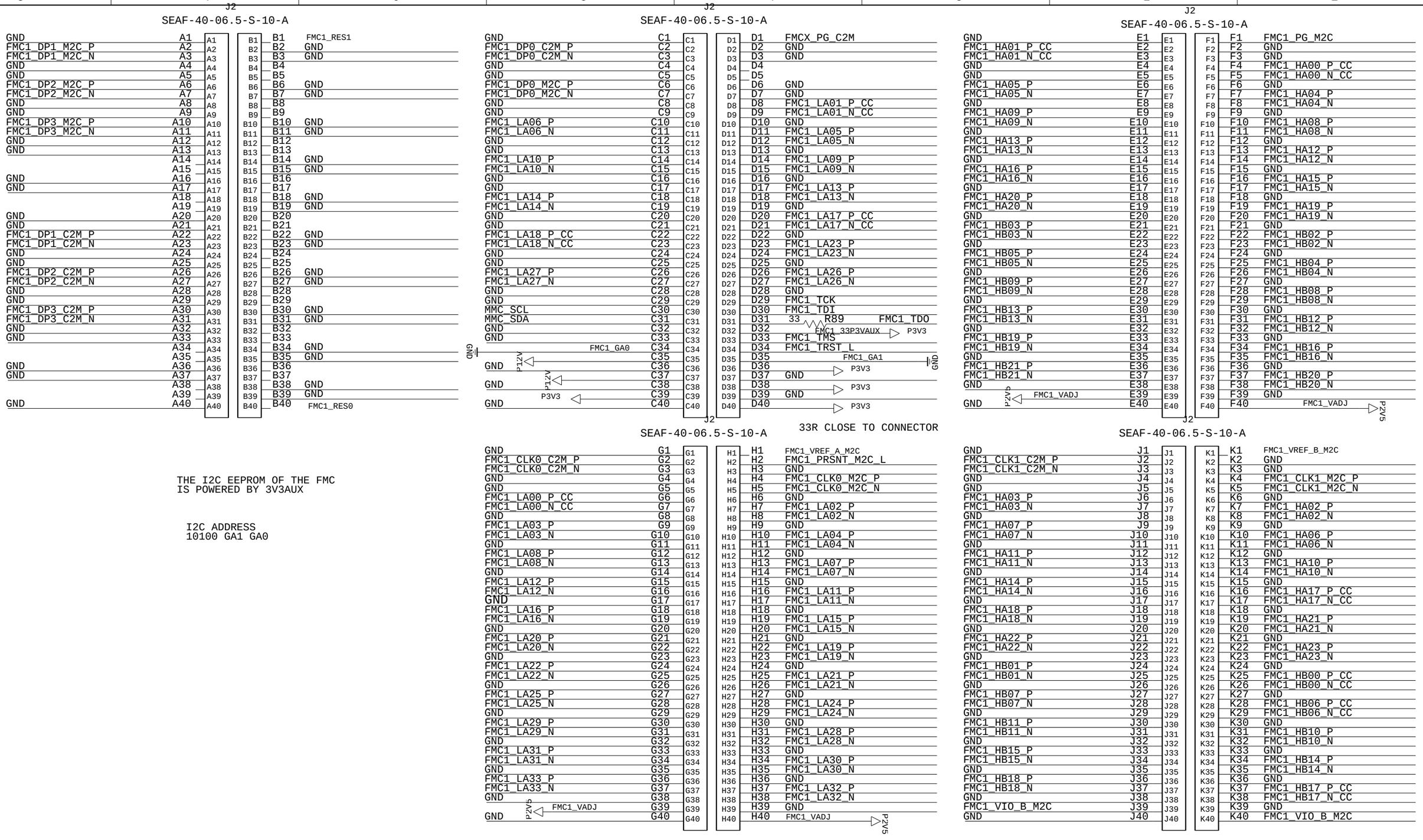
BANK 26:
UNCONDITIONAL SWAP
EXCEPT AC15

AG15	SRAM2_DQPC	
AF15	SRAM2_DQPD	
AK14	SRAM2_DQD4	
AJ14	SRAM2_DQD3	
AJ15	SRAM1_DQD4	
AH15	SRAM1_DQPD	
AL15	GBE_INT_N	
AL14	GBE_SDA 4.7K R212	P2V5
AG16	SRAM1_DQC0	
AF16	SRAM1_DQC4	
AN15	SRAM1_A14	
AM15	SRAM1_MODE	
AJ17	SRAM1_A2	
AJ16	SRAM1_A24	
AP16	SRAM1_A21	
AP15	SRAM1_A15	
AH17	SRAM1_A5	
AG17	SRAM1_CE1_L	
AC15	33 R102 SRAM1_CLK	
AD15		
AE16	SRAM1_DQD5	
AD16	SRAM1_DQC1	
AC18	SRAM1_OE_L	
AC17	SRAM1_A13	
AH18	SRAM1_DQC2	
AG18	SRAM1_DQC3	
AN17	SRAM1_A9	
AP17	SRAM1_DQD6	
AJ19		
AH19		
AM17	SRAM1_A8	
AM16	SRAM1_DQD7	
AD17	SRAM1_WE_L	
AE17	SRAM1_CEN_L	
AK18	SRAM1_DQPC	
AK17	SRAM1_A23	
AE18	SRAM1_A0	
AF18	SRAM1_A1	
AL16	GBE_SCL 4.7K R211	P2V5
AK16	GBE_RESET_N	

33R CLOSE TO IC

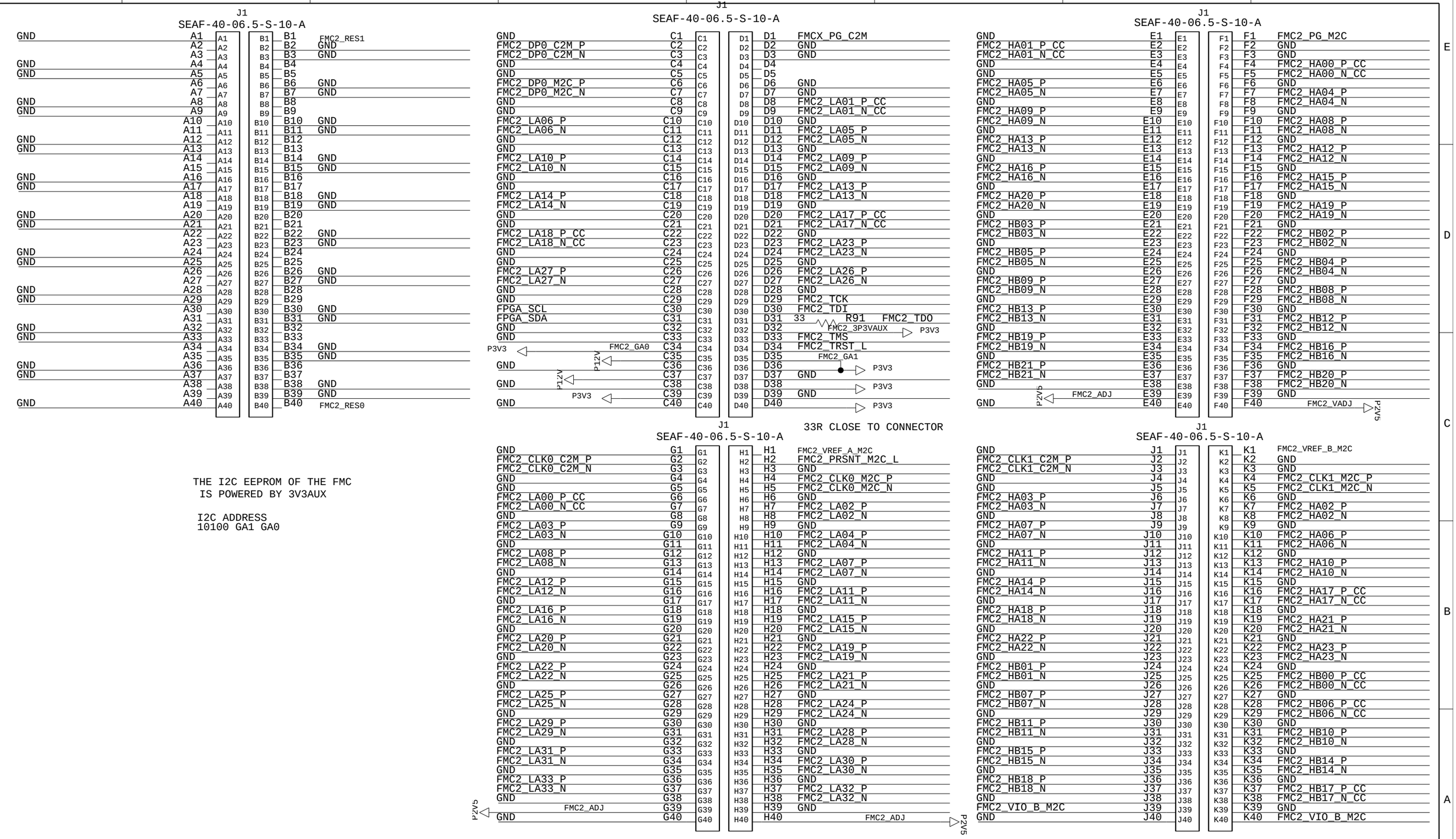
FPGA PART2

Project file:glib.cpm	SYSTEM: <SYSTEM>
EDA-02180-V2-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (EN/ICE)	MODULE:glib — Sheet: Module: 4/15 / Project: 4/15
	LAST_MODIFIED=Fri May 06 09:48:51 2011
	Design by: P.VICHOUDIS — PCB by: PV — DATE: <DATE>



FMC#1

Project file:glib.cpm	SYSTEM: <SYSTEM>
EDA-02180-V2-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:glib — Sheet: Module: 5/15 / Project: 5/15
EN/ICE	LAST_MODIFIED=Fri May 06 09:48:52 2011
	Design by: P.VICHOUDIS — PCB by: PV — DATE: <DATE>



FMC#2

Project file:glib.cpm — SYSTEM: <SYSTEM>

EDA-02180-V2-0

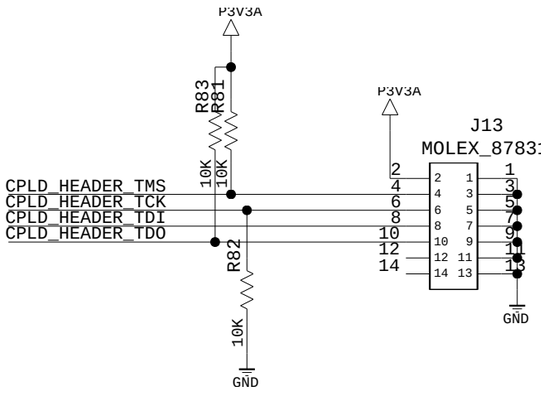
EN/ICE
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

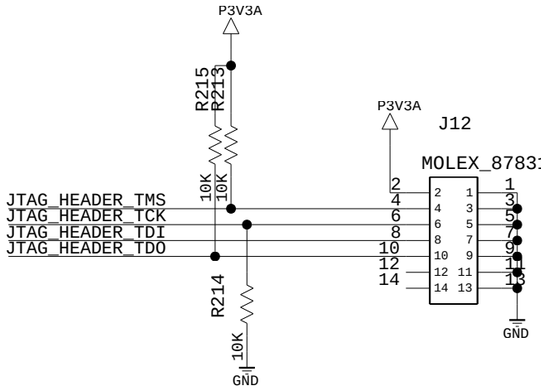
PROJECT:GLIB

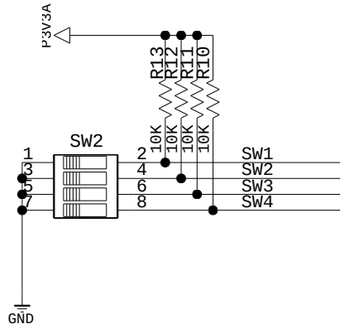
MODULE:glib — Sheet: 6/15 (Module: 6/15 / Project: 6/15)

LAST_MODIFIED=Fri May 06 15:03:06 2011

Design by: P.VICHOUDIS | PCB by: PV | DATE: <DATE>







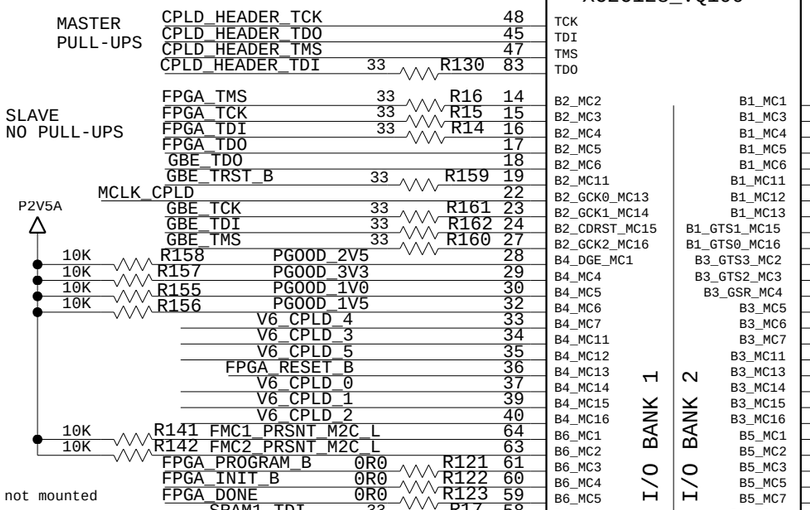
WHEN FMC PRESENT, PRSNT_M2C -> LOW

PGOOD ARE OPEN DRAIN

MMC RELOAD FPGAS IS OPEN DRAIN

LEDS EG L29K G2J1

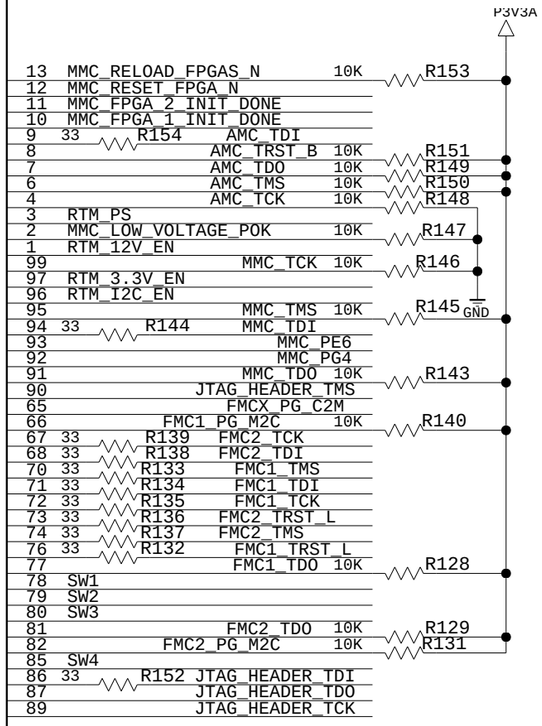
R121 R122 R123 are not mounted



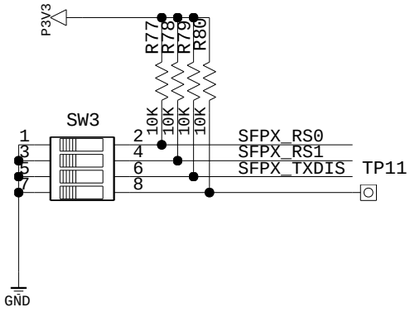
IC3

XC2C128_VQ100

I/O BANK1: ALL SWAPPABLE EXCEPT PIN22
I/O BANK2: ALL SWAPPABLE



33R CLOSE TO IC



JTAG SCHEME

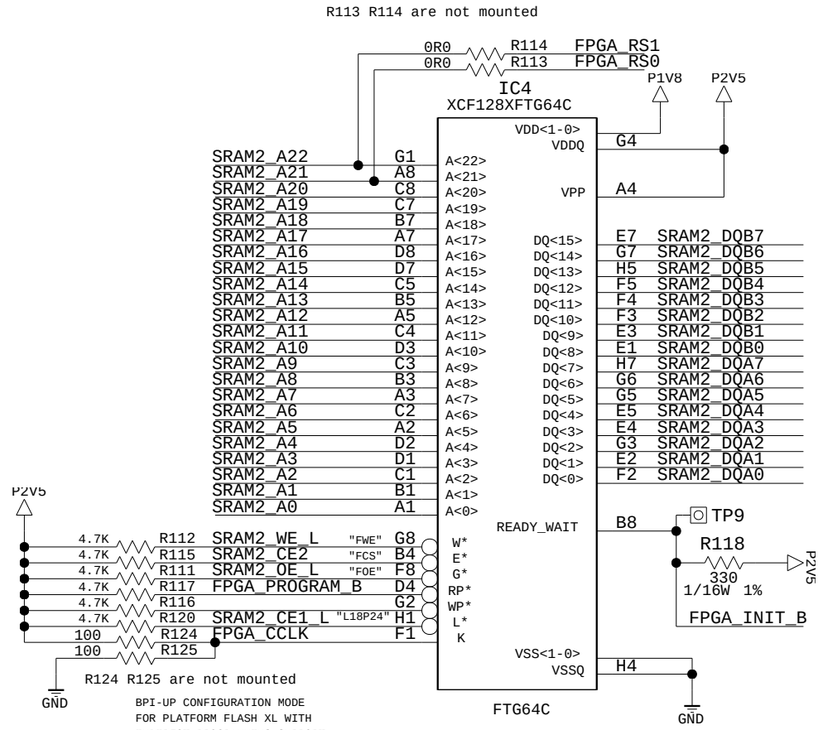
CLPD AS "SLAVE" : DRIVES "MASTER"DEVICE'S TDI

JTAG "MASTERS" ARE:
- CPLD JTAG HEADER
- JTAG HEADER FOR V6 & MMC
- JTAG FSM DRIVEN BY V6
- AMC JTAG
- MMC JTAG

JTAG "SLAVES" ARE:
- V6, FMCS, SRAMS, GBE

JTAG DRIVER PINS HAVE 33R IN SERIES
PULL-UP/DOWN RESISTORS ARE USED LINES DRIVEN
BY PLUGGABLE JTAG DEVICES

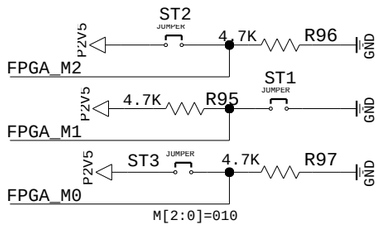
R113 R114 are not mounted

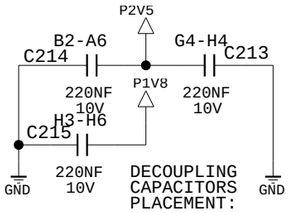


R124 R125 are not mounted

BPI-UP CONFIGURATION MODE
FOR PLATFORM FLASH XL WITH
INDIRECT PROGRAMMINS SUPPORT

UG438, PAGE34, FIGURE 3-2



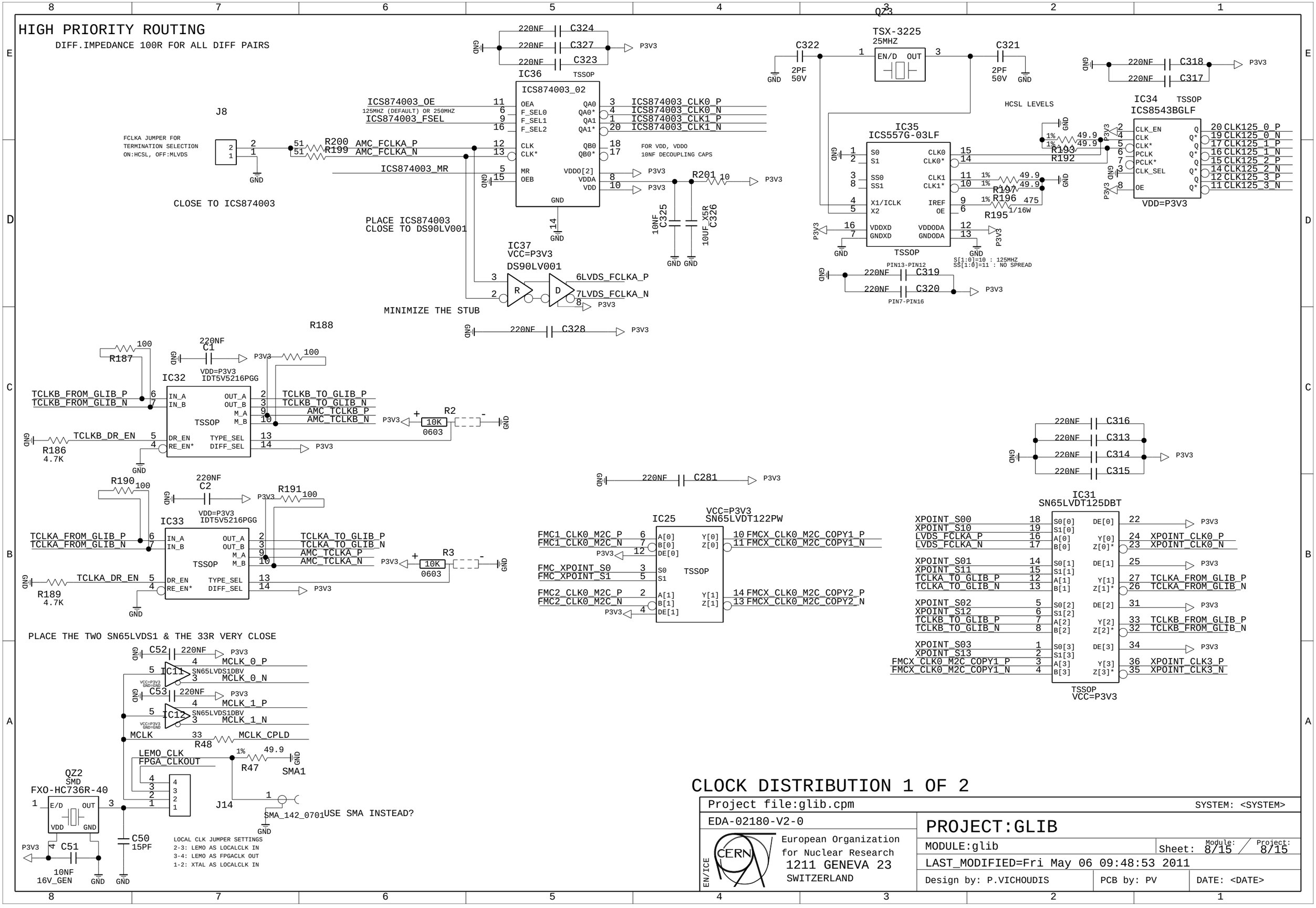


CONFIGURATION

Project file:glib.cpm	SYSTEM: <SYSTEM>
EDA-02180-V2-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (EN/ICE)	MODULE:glib — Sheet: Module: 7/15 / Project: 7/15
	LAST_MODIFIED=Fri May 06 09:48:52 2011
	Design by: P.VICHOUDIS — PCB by: PV — DATE: <DATE>

HIGH PRIORITY ROUTING

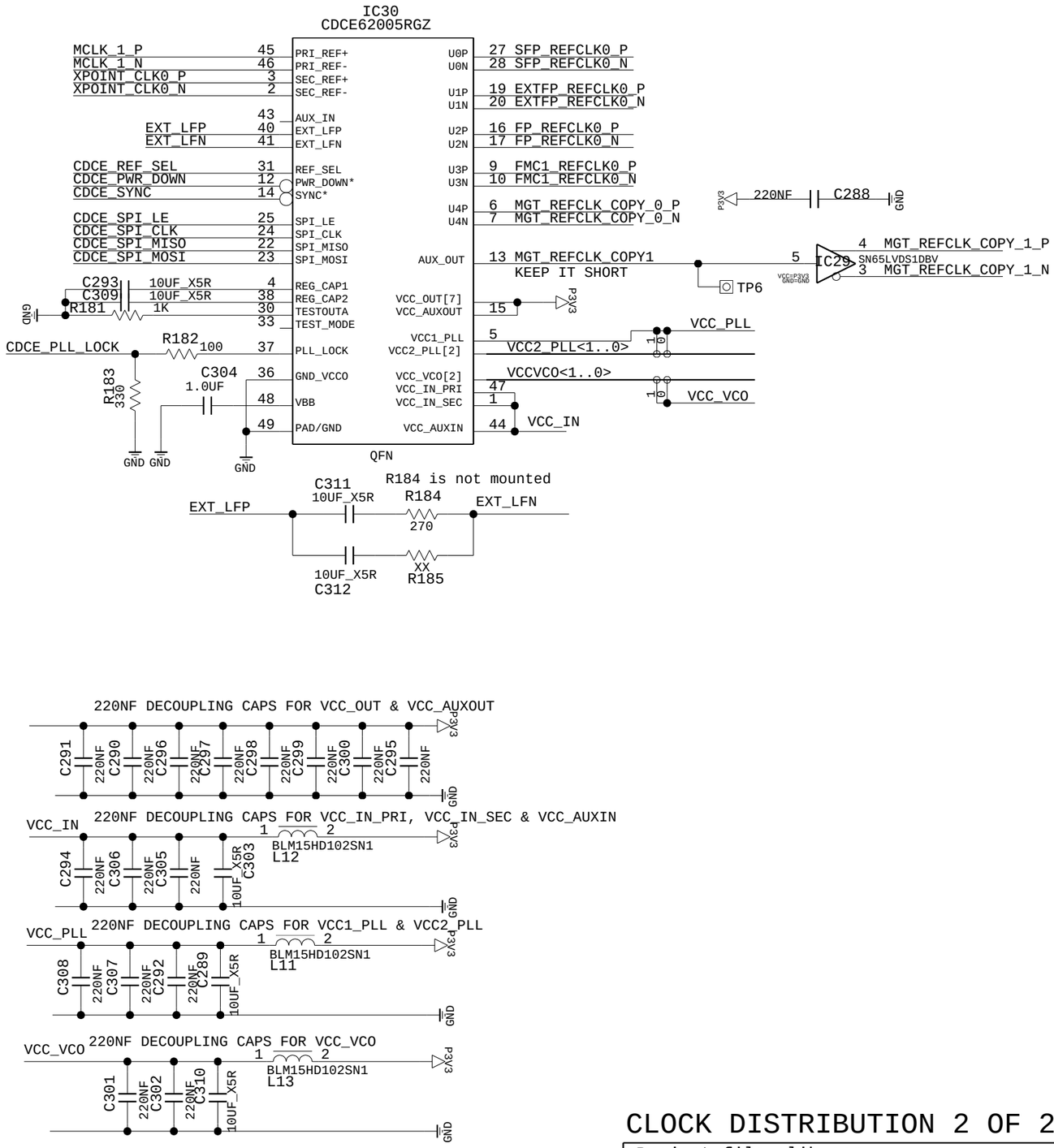
DIFF.IMPEDANCE 100R FOR ALL DIFF PAIRS



CLOCK DISTRIBUTION 1 OF 2

Project file:glib.cpm	SYSTEM: <SYSTEM>
EDA-02180-V2-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:glib — Sheet: Module: 8/15 / Project: 8/15
	LAST_MODIFIED=Fri May 06 09:48:53 2011
	Design by: P.VICHOUDIS — PCB by: PV — DATE: <DATE>

HIGH PRIORITY ROUTING



CLOCK DISTRIBUTION 2 OF 2

Project file:glib.cpm	SYSTEM: <SYSTEM>
EDA-02180-V2-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (EN/ICE)	MODULE:glib — Sheet: Module: 9/15 / Project: 9/15
	LAST_MODIFIED=Fri May 06 09:48:53 2011
	Design by: P.VICHOUDIS — PCB by: PV — DATE: <DATE>

HIGH PRIORITY ROUTING

SFP1 — J15 1888247-1

SFP1_TXP 18 TD+ RD+ 13 SFP1_RXP
SFP1_TXN 19 TD- RD- 12 SFP1_RXN
SFPX_TXDIS 3 TX_DIS SCA 5 4.7K R51 P3V3
SFP1_TXFAULT 2 TX_FAULT SDA 4 4.7K R52 P3V3
SFP1_RXLOS 8 LOS MOD_ABS 6 SFP1_MOD_ABS
SFPX_RS1 9 RS1 RS0 7 SFPX_RS0
SFP1_VCCT 16 VCCT VCCR 15 SFP1_VCCR L1 4.7UH P3V3
1 VEET VEER 10 C55 100NF C56 100NF 22UF 6.3V C59 100NF
17 VEET VEER 11
20 VEET VEER 14
GND GND GND

SFP2 — J16 1888247-1

SFP2_TXP 18 TD+ RD+ 13 SFP2_RXP
SFP2_TXN 19 TD- RD- 12 SFP2_RXN
SFPX_TXDIS 3 TX_DIS SCA 5 4.7K R58 P3V3
SFP2_TXFAULT 2 TX_FAULT SDA 4 4.7K R59 P3V3
SFP2_RXLOS 8 LOS MOD_ABS 6 SFP2_MOD_ABS
SFPX_RS1 9 RS1 RS0 7 SFPX_RS0
SFP2_VCCT 16 VCCT VCCR 15 SFP2_VCCR L3 4.7UH P3V3
1 VEET VEER 10 C61 100NF C62 100NF 22UF 6.3V C65 100NF
17 VEET VEER 11
20 VEET VEER 14
GND GND GND

SFP3 — J17 1888247-1

SFP3_TXP 18 TD+ RD+ 13 SFP3_RXP
SFP3_TXN 19 TD- RD- 12 SFP3_RXN
SFPX_TXDIS 3 TX_DIS SCA 5 4.7K R65 P3V3
SFP3_TXFAULT 2 TX_FAULT SDA 4 4.7K R66 P3V3
SFP3_RXLOS 8 LOS MOD_ABS 6 SFP3_MOD_ABS
SFPX_RS1 9 RS1 RS0 7 SFPX_RS0
SFP3_VCCT 16 VCCT VCCR 15 SFP3_VCCR L5 4.7UH P3V3
1 VEET VEER 10 C67 100NF C68 100NF 22UF 6.3V C71 100NF
17 VEET VEER 11
20 VEET VEER 14
GND GND GND

SFP4 — J18 1888247-1

SFP4_TXP 18 TD+ RD+ 13 SFP4_RXP
SFP4_TXN 19 TD- RD- 12 SFP4_RXN
SFPX_TXDIS 3 TX_DIS SCA 5 4.7K R72 P3V3
SFP4_TXFAULT 2 TX_FAULT SDA 4 4.7K R73 P3V3
SFP4_RXLOS 8 LOS MOD_ABS 6 SFP4_MOD_ABS
SFPX_RS1 9 RS1 RS0 7 SFPX_RS0
SFP4_VCCT 16 VCCT VCCR 15 SFP4_VCCR L7 4.7UH P3V3
1 VEET VEER 10 C73 100NF C74 100NF 22UF 6.3V C77 100NF
17 VEET VEER 11
20 VEET VEER 14
GND GND GND

SFP CAGE

100NF CLOSE TO FPGA

SFP4_TXN			AK2	MGTTXN3_112
SFP4_RXN			AJ4	MGTRXN3_112
SFP4_TXP			AK1	MGTTXP3_112
SFP4_RXP			AJ3	MGTRXP3_112
SFP3_TXN			AM2	MGTTXN2_112
SFP3_RXN			AL4	MGTRXN2_112
SFP3_TXP			AM1	MGTTXP2_112
CLK125_1_P	100NF	C255	AH6	MGTREFCLK1P_112
CLK125_1_N	100NF	C254	AH5	MGTREFCLK1N_112
SFP3_RXP			AL3	MGTRXP2_112
SFP_REFCLK0_P	100NF	C264	AK6	MGTREFCLK0P_112
SFP_REFCLK0_N	100NF	C265	AK5	MGTREFCLK0N_112
SFP2_TXN			AN4	MGTTXN1_112
SFP2_RXN			AM6	MGTRXN1_112
SFP2_TXP			AN3	MGTTXP1_112
SFP2_RXP			AM5	MGTRXP1_112
SFP1_TXN			AP2	MGTTXN0_112
SFP1_RXN			AP6	MGTRXN0_112
SFP1_TXP			AP1	MGTTXP0_112
SFP1_RXP			AP5	MGTRXP0_112
AMC_P11_TX_N			AB2	MGTTXN3_113
AMC_P11_RX_N	100NF	C262	AC4	MGTRXN3_113
AMC_P11_TX_P			AB1	MGTTXP3_113
AMC_P11_RX_P	100NF	C263	AC3	MGTRXP3_113
AMC_P10_TX_N			AD2	MGTTXN2_113
AMC_P10_RX_N	100NF	C260	AE4	MGTRXN2_113
AMC_P10_TX_P			AD1	MGTTXP2_113
ICS874003_CLK1_P	100NF	C251	AB6	MGTREFCLK1P_113
ICS874003_CLK1_N	100NF	C250	AB5	MGTREFCLK1N_113
AMC_P10_RX_P	100NF	C261	AE3	MGTRXP2_113
EXTFP_REFCLK0_P	100NF	C252	AD6	MGTREFCLK0P_113
EXTFP_REFCLK0_N	100NF	C253	AD5	MGTREFCLK0N_113
AMC_P9_TX_N			AF2	MGTTXN1_113
AMC_P9_RX_N	100NF	C258	AF6	MGTRXN1_113
AMC_P9_TX_P			AF1	MGTTXP1_113
AMC_P9_RX_P	100NF	C259	AF5	MGTRXP1_113
AMC_P8_TX_N			AH2	MGTTXN0_113
AMC_P8_RX_N	100NF	C256	AG4	MGTRXN0_113
AMC_P8_TX_P			AH1	MGTTXP0_113
AMC_P8_RX_P	100NF	C257	AG3	MGTRXP0_113
FMC2_DP0_C2M_N			P2	MGTTXN3_114
FMC2_DP0_M2C_N			R4	MGTRXN3_114
FMC2_DP0_C2M_P			P1	MGTTXP3_114
FMC2_DP0_M2C_P			R3	MGTRXP3_114
GBE_SIN_N	100NF	C6	GBETX_N T2	MGTTXN2_114
GBE_SOUT_N	100NF	C242	U4	MGTRXN2_114
GBE_SIN_P	100NF	C5	GBETX_P T1	MGTTXP2_114
			T6	MGTREFCLK1P_114
			T5	MGTREFCLK1N_114
GBE_SOUT_P	100NF	C243	U3	MGTRXP2_114
CLK125_2_P	100NF	C245	V6	MGTREFCLK0P_114
CLK125_2_N	100NF	C244	V5	MGTREFCLK0N_114
AMC_P0_TX_N			V2	MGTTXN1_114
AMC_P0_RX_N	100NF	C247	W4	MGTRXN1_114
AMC_P0_TX_P			V1	MGTTXP1_114
AMC_P0_RX_P	100NF	C246	W3	MGTRXP1_114
AMC_P1_TX_N			Y2	MGTTXN0_114
AMC_P1_RX_N	100NF	C248	AA4	MGTRXN0_114
AMC_P1_TX_P			Y1	MGTTXP0_114
AMC_P1_RX_P	100NF	C249	AA3	MGTRXP0_114

IC2
XC6VLX130T-1FFG1156CES
Sym 5/5
BGA

BANK 112	BANK 115	BANK 116	BANK 113	BANK 114
MGTTXN3_112	MGTTXN3_115	MGTTXN3_116	MGTTXN3_113	MGTTXN3_114
MGTRXN3_112	MGTRXN3_115	MGTRXN3_116	MGTRXN3_113	MGTRXN3_114
MGTTXP3_112	MGTTXP3_115	MGTTXP3_116	MGTTXP3_113	MGTTXP3_114
MGTRXP3_112	MGTRXP3_115	MGTRXP3_116	MGTRXP3_113	MGTRXP3_114
MGTTXN2_112	MGTTXN2_115	MGTTXN2_116	MGTTXN2_113	MGTTXN2_114
MGTRXN2_112	MGTRXN2_115	MGTRXN2_116	MGTRXN2_113	MGTRXN2_114
MGTTXP2_112	MGTTXP2_115	MGTTXP2_116	MGTTXP2_113	MGTTXP2_114
MGTREFCLK1P_112	MGTREFCLK1P_115	MGTREFCLK1P_116	MGTREFCLK1P_113	MGTREFCLK1P_114
MGTREFCLK1N_112	MGTREFCLK1N_115	MGTREFCLK1N_116	MGTREFCLK1N_113	MGTREFCLK1N_114
MGTRXP2_112	MGTRXP2_115	MGTRXP2_116	MGTRXP2_113	MGTRXP2_114
MGTREFCLK0P_112	MGTAVTTRCAL_115	MGTREFCLK0P_116	MGTREFCLK0P_113	MGTREFCLK0P_114
MGTREFCLK0N_112	MGTRREF_115	MGTREFCLK0N_116	MGTREFCLK0N_113	MGTREFCLK0N_114
MGTTXN1_112	MGTREFCLK0P_115	MGTTXN1_116	MGTTXN1_113	MGTTXN1_114
MGTRXN1_112	MGTREFCLK0N_115	MGTRXN1_116	MGTRXN1_113	MGTRXN1_114
MGTTXP1_112	MGTTXN1_115	MGTTXP1_116	MGTTXP1_113	MGTTXP1_114
MGTRXP1_112	MGTRXN1_115	MGTRXP1_116	MGTRXP1_113	MGTRXP1_114
MGTTXN0_112	MGTTXP1_115	MGTTXN0_116	MGTTXN0_113	MGTTXN0_114
MGTRXN0_112	MGTRXP1_115	MGTRXN0_116	MGTRXN0_113	MGTRXN0_114
MGTTXP0_112	MGTTXN0_115	MGTTXP0_116	MGTTXP0_113	MGTTXP0_114
MGTRXP0_112	MGTRXN0_115	MGTRXP0_116	MGTRXP0_113	MGTRXP0_114
	MGTTXP0_115			
	MGTRXP0_115			

NA
MGTAVTT_N[5..0] → VTT
MGTAVCC_N[5..0] → VCCA
MGTAVTT_S[9..0] → VTT
MGTAVCC_S[9..0] → VCCA
VCCAUX[12..0] → P2V5
VCCINT[54..0] → P1V0
GND[252..0] → GND

BANK[112..116]: DIFF.IMPEDANCE 100R
HIGH SPEED: ALL AMC_*, FMC*, SFP*, GBE*

NO SWAP

F2			AMC_P7_TX_N
J4	100NF	C230	AMC_P7_RX_N
F1			AMC_P7_TX_P
J3	100NF	C231	AMC_P7_RX_P
H2			AMC_P6_TX_N
K6	100NF	C232	AMC_P6_RX_N
H1			AMC_P6_TX_P
M6	100NF	C239	ICS874003_CLK0_P
M5	100NF	C238	ICS874003_CLK0_N
K5	100NF	C233	AMC_P6_RX_P
AP7	0.1%_GEN		
AN7	100	R106	SEE NOTE1 BELOW → VTT
P6	100NF	C240	FP_REFCLK0_P
P5	100NF	C241	FP_REFCLK0_N
K2			AMC_P5_TX_N
L4	100NF	C235	AMC_P5_RX_N
K1			AMC_P5_TX_P
L3	100NF	C234	AMC_P5_RX_P
M2			AMC_P4_TX_N
N4	100NF	C236	AMC_P4_RX_N
M1			AMC_P4_TX_P
N3	100NF	C237	AMC_P4_RX_P
A4			FMC1_DP3_C2M_P
B6			FMC1_DP3_M2C_P
A3			FMC1_DP3_C2M_N
B5			FMC1_DP3_M2C_N
B2			FMC1_DP2_C2M_P
D6			FMC1_DP2_M2C_N
B1			FMC1_DP2_C2M_N
F6	100NF	C226	CLK125_3_P
F5	100NF	C227	CLK125_3_N
D5			FMC1_DP2_M2C_P
H6	100NF	C228	FMC1_REFCLK0_P
H5	100NF	C229	FMC1_REFCLK0_N
C4			FMC1_DP1_C2M_P
E4			FMC1_DP1_M2C_N
C3			FMC1_DP1_C2M_N
E3			FMC1_DP1_M2C_P
D2			FMC1_DP0_C2M_N
G4			FMC1_DP0_M2C_N
D1			FMC1_DP0_C2M_P
G3			FMC1_DP0_M2C_P

J3
AMC.0_R2.0
EDGE

AMC_P20_RX_P	160	RX20+	TX20+	163 AMC_P20_TX_P
AMC_P20_RX_N	159	RX20-	TX20-	162 AMC_P20_TX_N
AMC_P19_RX_P	154	RX19+	TX19+	157 AMC_P19_TX_P
AMC_P19_RX_N	153	RX19-	TX19-	156 AMC_P19_TX_N
AMC_P18_RX_P	148	RX18+	TX18+	151 AMC_P18_TX_P
AMC_P18_RX_N	147	RX18-	TX18-	150 AMC_P18_TX_N
AMC_P17_RX_P	142	RX17+	TX17+	145 AMC_P17_TX_P
AMC_P17_RX_N	141	RX17-	TX17-	144 AMC_P17_TX_N
AMC_P15_RX_P	130	RX15+	TX15+	133 AMC_P15_TX_P
AMC_P15_RX_N	129	RX15-	TX15-	132 AMC_P15_TX_N
AMC_P14_RX_P	124	RX14+	TX14+	127 AMC_P14_TX_P
AMC_P14_RX_N	123	RX14-	TX14-	126 AMC_P14_TX_N
AMC_P13_RX_P	118	RX13+	TX13+	121 AMC_P13_TX_P
AMC_P13_RX_N	117	RX13-	TX13-	120 AMC_P13_TX_N
AMC_P12_RX_P	112	RX12+	TX12+	115 AMC_P12_TX_P
AMC_P12_RX_N	111	RX12-	TX12-	114 AMC_P12_TX_N
AMC_P11_RX_P	106	RX11+	TX11+	109 AMC_P11_TX_P
AMC_P11_RX_N	105	RX11-	TX11-	108 AMC_P11_TX_N
AMC_P10_RX_P	100	RX10+	TX10+	103 AMC_P10_TX_P
AMC_P10_RX_N	99	RX10-	TX10-	102 AMC_P10_TX_N
AMC_P9_RX_P	94	RX9+	TX9+	97 AMC_P9_TX_P
AMC_P9_RX_N	93	RX9-	TX9-	96 AMC_P9_TX_N
AMC_P8_RX_P	88	RX8+	TX8+	91 AMC_P8_TX_P
AMC_P8_RX_N	87	RX8-	TX8-	90 AMC_P8_TX_N
AMC_P7_RX_P	68	RX7+	TX7+	65 AMC_P7_TX_P
AMC_P7_RX_N	69	RX7-	TX7-	66 AMC_P7_TX_N
AMC_P6_RX_P	62	RX6+	TX6+	59 AMC_P6_TX_P
AMC_P6_RX_N	63	RX6-	TX6-	60 AMC_P6_TX_N
AMC_P5_RX_P	53	RX5+	TX5+	50 AMC_P5_TX_P
AMC_P5_RX_N	54	RX5-	TX5-	51 AMC_P5_TX_N
AMC_P4_RX_P	47	RX4+	TX4+	44 AMC_P4_TX_P
AMC_P4_RX_N	48	RX4-	TX4-	45 AMC_P4_TX_N
AMC_P3_RX_P	38	RX3+	TX3+	35 AMC_P3_TX_P
AMC_P3_RX_N	39	RX3-	TX3-	36 AMC_P3_TX_N
AMC_P2_RX_P	32	RX2+	TX2+	29 AMC_P2_TX_P
AMC_P2_RX_N	33	RX2-	TX2-	30 AMC_P2_TX_N
AMC_P1_RX_P	23	RX1+	TX1+	20 AMC_P1_TX_P
AMC_P1_RX_N	24	RX1-	TX1-	21 AMC_P1_TX_N
AMC_P0_RX_P	14	RX0+	TX0+	11 AMC_P0_TX_P
AMC_P0_RX_N	15	RX0-	TX0-	12 AMC_P0_TX_N
AMC_FCLKA_P	80	FCLKA+		
AMC_FCLKA_N	81	FCLKA-		
AMC_GA2	26	GA2		
AMC_GA1	17	GA1		
AMC_GA0	5	GA0		
AMC_MP	4	MP		
AMC_PS1_N	3	PS1*		
AMC_PS0_N	83	PS0*		
AMC_ENABLE_N	41	ENABLE*		
	8	RSRVD8		
	6	RSRVD6		
AMC_SCL	56	SCL_L		
AMC_SDA	71	SDA_L		
AMC_TCLKA_P	74	TCLKA+		
AMC_TCLKA_N	75	TCLKA-		
AMC_TCLKB_P	77	TCLKB+		
AMC_TCLKB_N	78	TCLKB-		
	136	TCLKC+		
	135	TCLKC-		
	139	TCLKD+		
	138	TCLKD-		

JTAG

AMC_TCK	33	R221	165 TCK	TDO 168 33 R222 AMC_TDO
AMC_TDI			169 TDI	
AMC_TMS	33	R223	166 TMS	
AMC_TRST_B	33	R224	167 TRST*	

POWER
P12V → PWR[8] GND[54] → GND

NOTE1
TRACE LENGTH FROM THE FPGA PINS MGTRREF AND MGTVTTRCAL
TO THE THE RESISTOR PINS MUST BE EQUAL IN LENGTH & GEOMETRY
NOTE2
ALL DIFF. PAIRS OF BANKS 112,113,114,115,116
MUST HAVE DIFF. IMPEDANCE 100 OHM.
NO SWAPPING POSSIBLE
HIGHEST PRIORITY ROOTING - HIGH SPEED LINES ~5GBPS

SFP1_VCCT L2 4.7UH P3V3 — C58 100NF, C57 22UF 6.3V, C60 100NF — GND
SFP2_VCCT L4 4.7UH P3V3 — C64 100NF, C63 22UF 6.3V, C66 100NF — GND
SFP3_VCCT L6 4.7UH P3V3 — C70 100NF, C69 22UF 6.3V, C72 100NF — GND
SFP4_VCCT L8 4.7UH P3V3 — C76 100NF, C75 22UF 6.3V, C78 100NF — GND

IC13 TSSOP — VCC=P3V3 — P3V3

SFP1_RXLOS	1	2	R54 330	LD2 SML-311UT
SFP1_TXFAULT	3	4	R55 330	LD3 SML-311UT
SFP2_RXLOS	9	8	R61 330	LD4 SML-311UT
SFP2_TXFAULT	11	10	R62 330	LD5 SML-311UT

IC14 TSSOP — VCC=P3V3 — P3V3

SFP3_RXLOS	1	2	R68 330	LD6 SML-311UT
SFP3_TXFAULT	3	4	R69 330	LD7 SML-311UT
SFP4_RXLOS	9	8	R75 330	LD8 SML-311UT
SFP4_TXFAULT	11	10	R76 330	LD9 SML-311UT

SERIAL INTERFACES

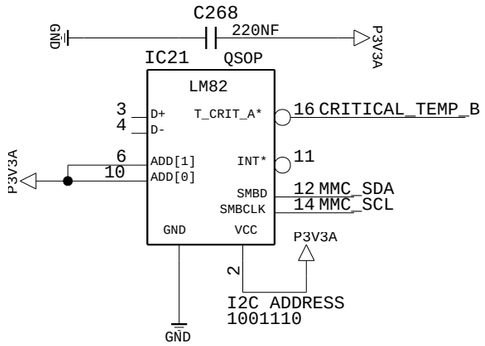
Project file:glib.cpm — SYSTEM: <SYSTEM>
EDA-02180-V2-0

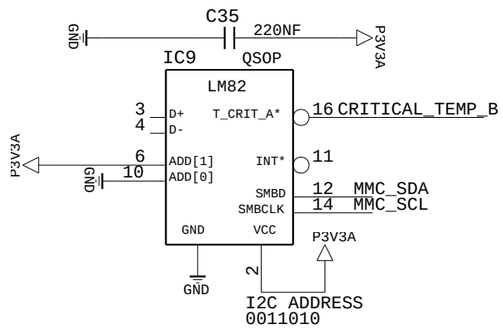
EN/ICE
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

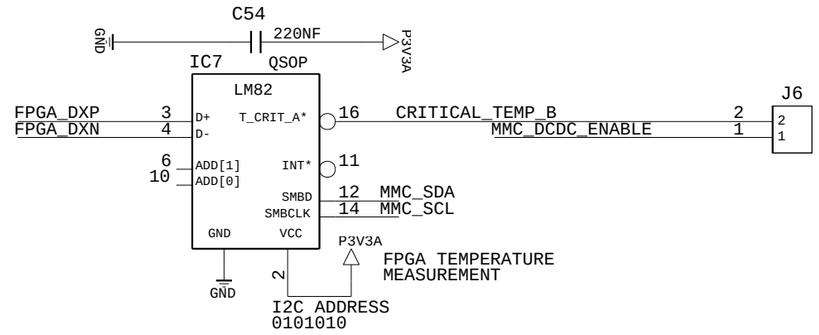
PROJECT:GLIB
MODULE:glib — Sheet: Module: 10/15 / Project: 10/15
LAST_MODIFIED=Fri May 06 09:48:49 2011
Design by: P.VICHOUDIS — PCB by: PV — DATE: <DATE>

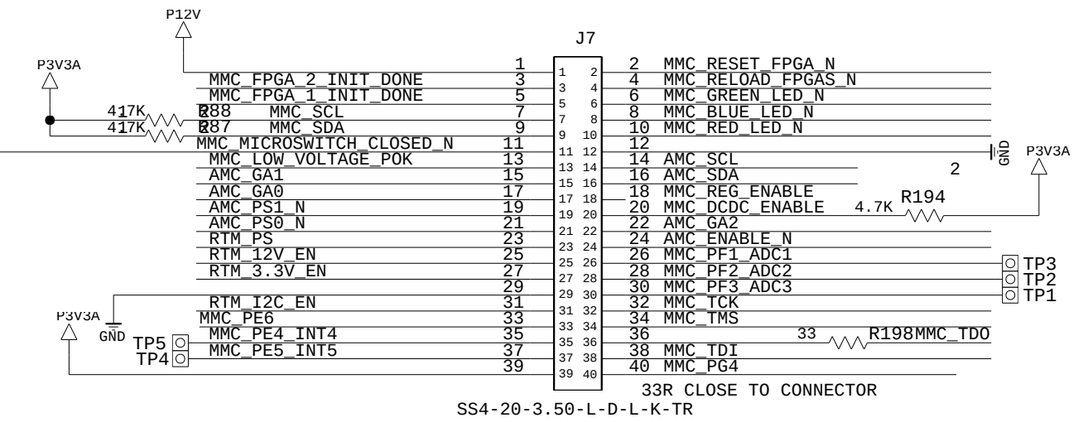
2007178

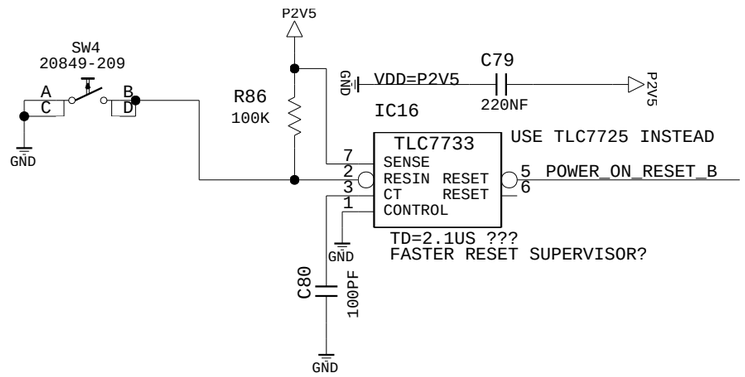
TRI-LEVEL I2C ADDRESSING

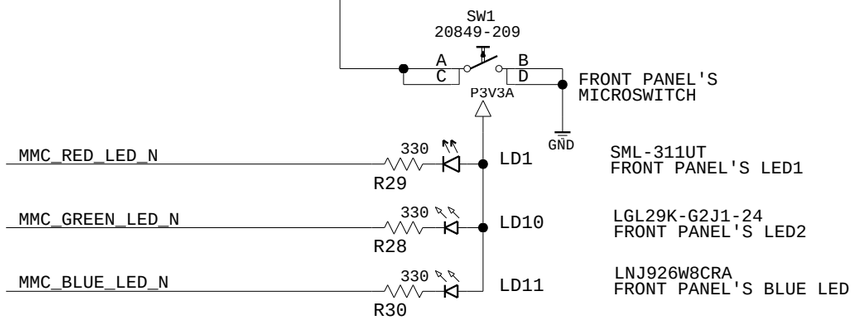


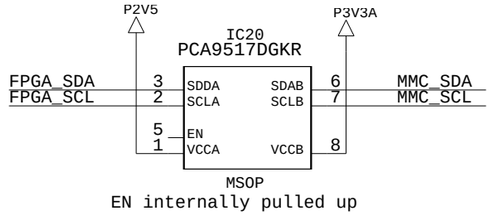


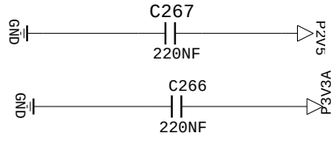


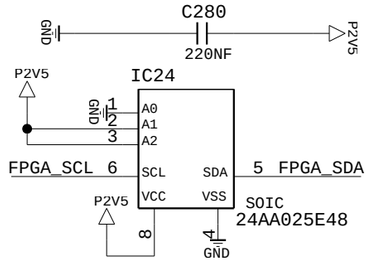












I2C ADDRESSING

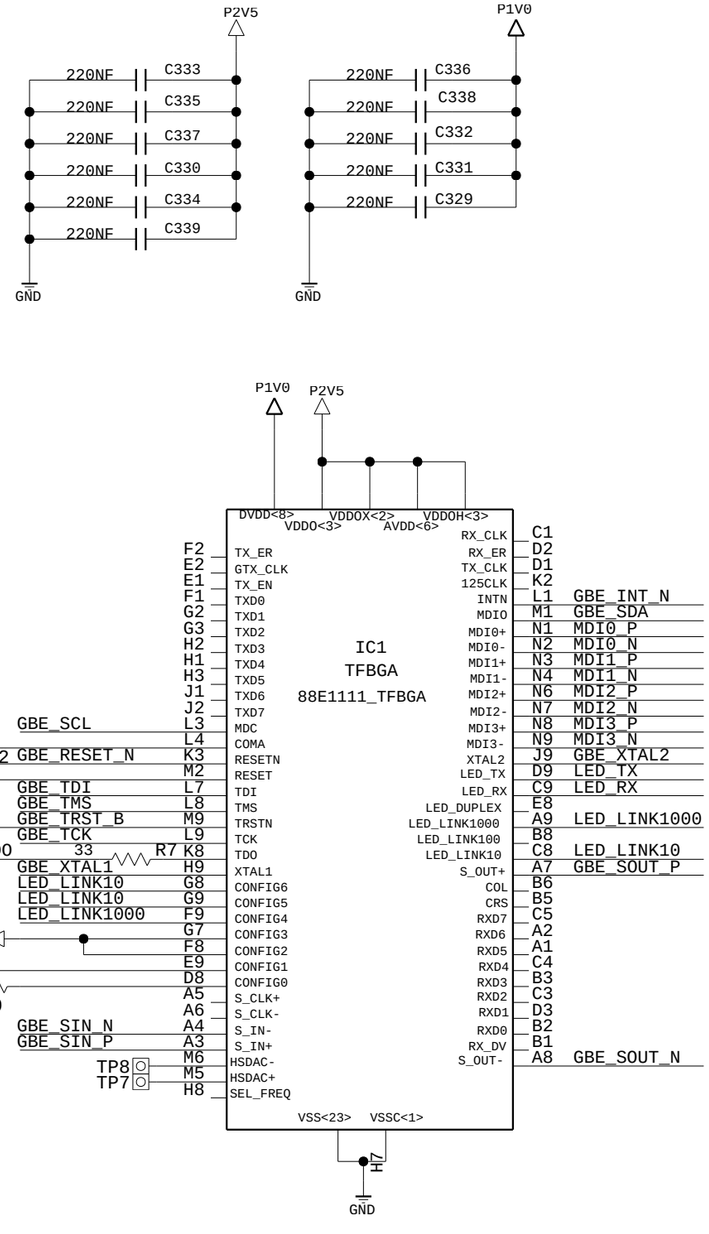
I2CBUS1: I2C MASTER: MMC

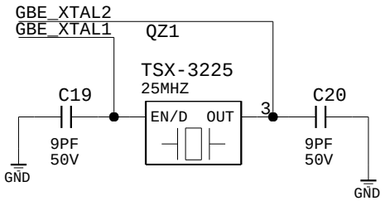
0101010: GLIB FPGA TEMPERATURE
0011010: GLIB BOARD TEMPERATURE #1
1001110: GLIB BOARD TEMPERATURE #2
XXXXX00: FMC#1
XXXXX11: FMC#2

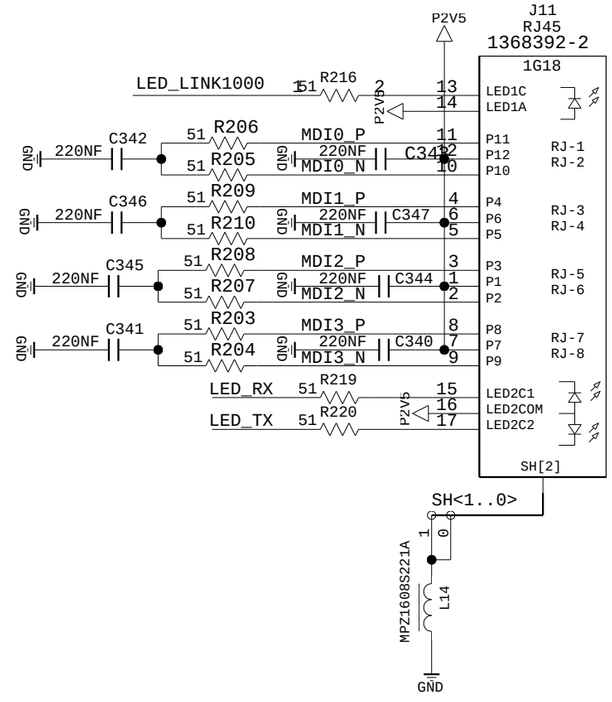
I2CBUS2: I2C MASTER: FPGA
1010110: GLIB EEPROM

MODULE MANAGEMENT

Project file:glib.cpm	SYSTEM: <SYSTEM>
EDA-02180-V2-0	PROJECT:GLIB
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE:glib — Sheet: Module: 11/15 / Project: 11/15
EN/ICE	LAST_MODIFIED=Fri May 06 15:03:42 2011
	Design by: P.VICHOUDIS — PCB by: PV — DATE: <DATE>







111: VCC2V5
110: LED_LINK10
101: LED_LINK100
100: LED_LINK1000
011: LED_DUPLEX
010: LED_RX
001: LED_TX
000: GND

CFG0:	PHYADR[2]	PHYADR[1]	PHYADR[0] :111
CGF1:	ENA PAUSE	PHYADR[4]	PHYADR[3] :000
CFG2:	AUTONEG[3]	AUTONEG[2]	AUTONEG[1] :111
CFG3:	AUTONEG[0]	ENABLE XC	DIS125MHZ :111
CFG4:	HWCFGMD[2]	HWCFGMD[1]	HWCFGMD[0] :100
CGF5:	DISABLE FC	DIS SLEEP	HWCFGMD[3] :110
CFG6:	SEL BDT	INT_POL	75/50 OHM :110

GBE PHY

Project file:glib.cpm — SYSTEM: <SYSTEM>

EDA-02180-V2-0

EN/ICE
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

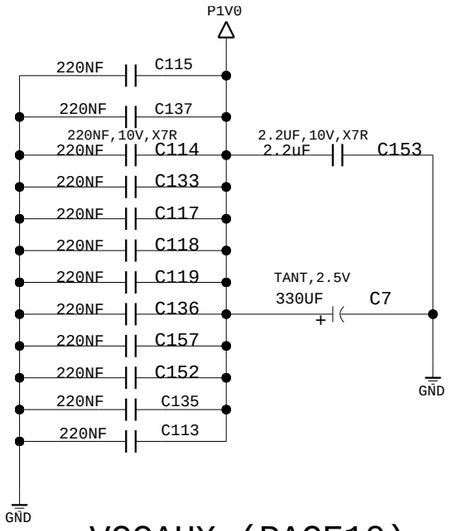
PROJECT:GLIB

MODULE:glib — Module: Sheet: 12/15 — Project: 12/15

LAST_MODIFIED=Fri May 13 10:55:16 2011

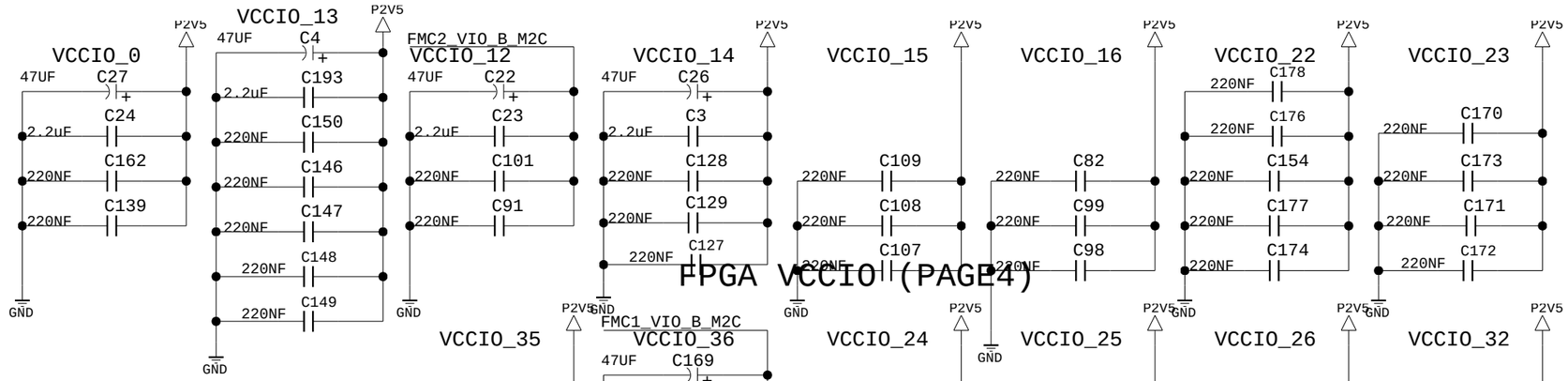
Design by: P.VICHOUDIS | PCB by: PV | DATE: <DATE>

FPGA VCCINT (PAGE10)

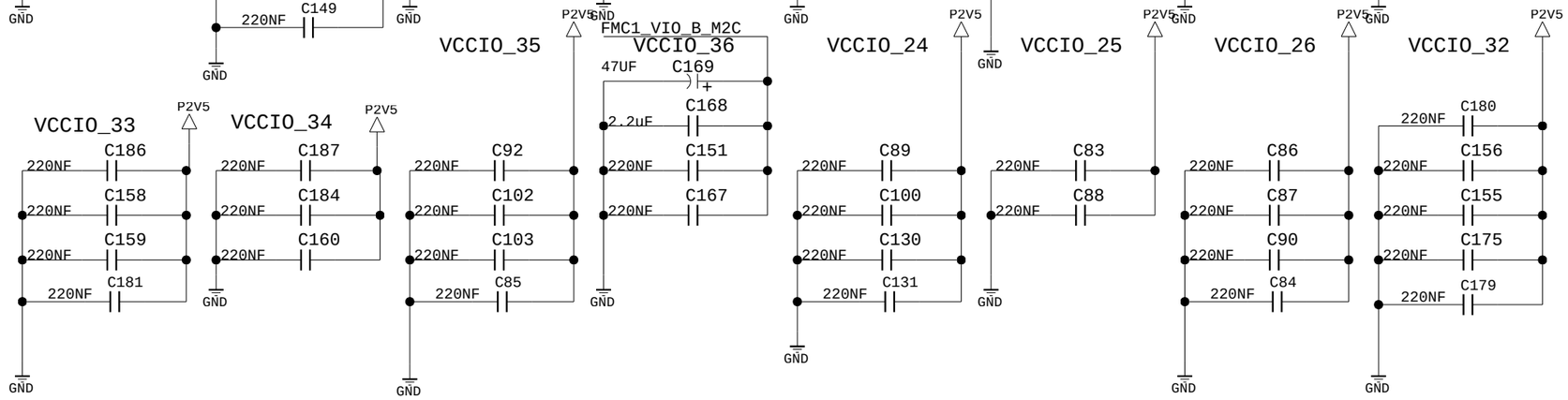


FPGA DECOUPLING CAPS PLACEMENT RULES:
330UF,47UF,33UF,22UF,10UF: ANYWHERE ON BOARD BUT AS CLOSE AS POSSIBLE TO FPGA
220NF: NO MORE THAN 1" FROM PERIPHERY OF FPGA BUT AS CLOSE AS POSSIBLE
2.2UF: NO MORE THAN 3" FROM PERIPHERY OF FPGA BUT AS CLOSE AS POSSIBLE

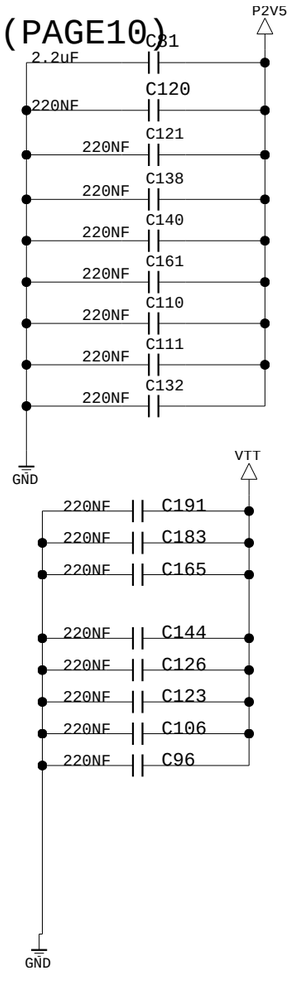
FPGA VCCIO (PAGE3)



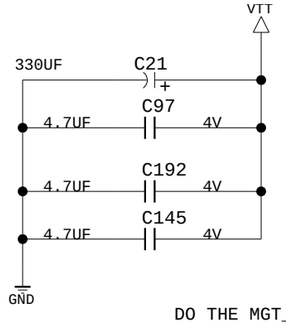
FPGA VCCIO (PAGE4)



VCCAUX (PAGE10)

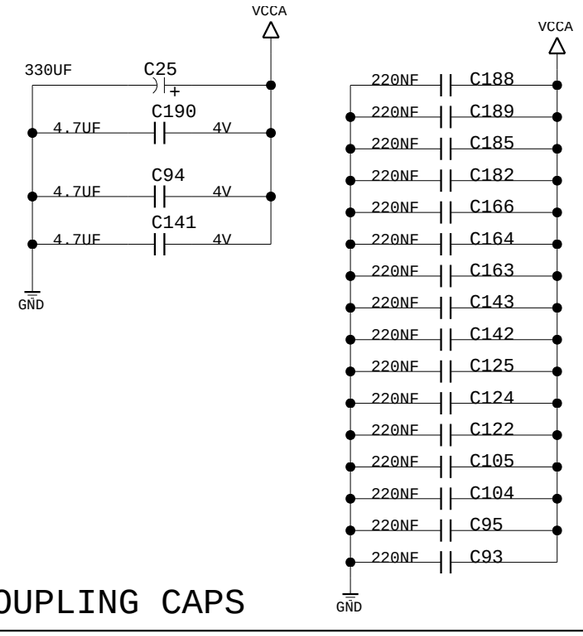


MGT_AVTT (PAGE10)



DO THE MGT_AVTT & MGT_AVCC DECOUPLING AS IN UG366 PAGE286

MGT_AVCC (PAGE10)



FPGA DECOUPLING CAPS

EDMS REF: X	VERSION: 1	PCB: X	SYSTEM: X
REF:		TITLE: GIGABIT LINK INTERFACE BOARD	
IT/CE CERN DIV. 1211 GENEVA 23 SWITZERLAND		ABBREV: GLIB	PAGE:
		DRAWING LAST_MODIFIED=Fri May 06 09:48:54 2011	
		DESSIN:	ETUDE: DATE:

SWAP BY PAIR ("NET" WITH THE CORRESPONDING "V6_NET")

IC27

220NF C285 P2V5 GND
220NF C284 P3V3 GND

74AVC8T 245

V6_XPOINT_S10	10	A7	B7	14	XPOINT_S10
V6_XPOINT_S00	9	A6	B6	15	XPOINT_S00
V6_XPOINT_S11	8	A5	B5	16	XPOINT_S11
V6_XPOINT_S01	7	A4	B4	17	XPOINT_S01
V6_XPOINT_S12	6	A3	B3	18	XPOINT_S12
V6_XPOINT_S02	5	A2	B2	19	XPOINT_S02
V6_XPOINT_S13	4	A1	B1	20	XPOINT_S13
V6_XPOINT_S03	3	A0	B0	21	XPOINT_S03

DIR OE

TSSOP
VCCA=P2V5;VCCB=P3V3
P2V5 2 22 GND

SWAP BY PAIR ("NET" WITH THE CORRESPONDING "V6_NET")

IC28

220NF C287 P2V5 GND
220NF C286 P3V3 GND

74AVC8T 245

V6_FMC_XPOINT_S0	10	A7	B7	14	FMC_XPOINT_S0
V6_FMC_XPOINT_S1	9	A6	B6	15	FMC_XPOINT_S1
V6_ICS874003_MR	8	A5	B5	16	ICS874003_MR
V6_ICS874003_FSEL	7	A4	B4	17	ICS874003_FSEL
V6_ICS874003_OE	6	A3	B3	18	ICS874003_OE
	5	A2	B2	19	
V6_TCLKB_DR_EN	4	A1	B1	20	TCLKB_DR_EN
V6_TCLKA_DR_EN	3	A0	B0	21	TCLKA_DR_EN

DIR OE

TSSOP
VCCA=P2V5;VCCB=P3V3
P2V5 2 22 GND

SWAP BY PAIR ("NET" WITH THE CORRESPONDING "V6_NET")

IC26

220NF C283 P2V5 GND
220NF C282 P3V3 GND

74AVC8T 245

	10	A7	B7	14	
	9	A6	B6	15	
V6_CDCE_REF_SEL	8	A5	B5	16	CDCE_REF_SEL
V6_CDCE_PWR_DOWN	7	A4	B4	17	CDCE_PWR_DOWN
V6_CDCE_SYNC	6	A3	B3	18	CDCE_SYNC
V6_CDCE_SPI_MOSI	5	A2	B2	19	CDCE_SPI_MOSI
V6_CDCE_SPI_LE	4	A1	B1	20	CDCE_SPI_LE
V6_CDCE_SPI_CLK	3	A0	B0	21	CDCE_SPI_CLK

DIR OE

TSSOP
VCCA=P2V5;VCCB=P3V3
P2V5 2 22 GND

UNCONDITIONAL SWAP OF BUS TRANSLATOR_TO_MLVDS
UNCONDITIONAL SWAP OF BUS MLVDS_TO_TRANSLATOR

IC39

220NF C16 P2V5 GND
220NF C13 P3V3 GND

74AVC8T 245

V6_TO_TRANSLATOR_12	10	A7	B7	14	
V6_TO_TRANSLATOR_14	9	A6	B6	15	
V6_TO_TRANSLATOR_8	8	A5	B5	16	
V6_TO_TRANSLATOR_10	7	A4	B4	17	
V6_TO_TRANSLATOR_11	6	A3	B3	18	
V6_TO_TRANSLATOR_9	5	A2	B2	19	
V6_TO_TRANSLATOR_15	4	A1	B1	20	
V6_TO_TRANSLATOR_13	3	A0	B0	21	

DIR OE

VCCA=P2V5;VCCB=P3V3
TSSOP
P2V5 2 22 GND

IC40

220NF C17 P2V5 GND
220NF C14 P3V3 GND

74AVC8T 245

TRANSLATOR_TO_V6_1	10	A7	B7	14	
TRANSLATOR_TO_V6_0	9	A6	B6	15	
TRANSLATOR_TO_V6_3	8	A5	B5	16	
TRANSLATOR_TO_V6_2	7	A4	B4	17	
TRANSLATOR_TO_V6_5	6	A3	B3	18	
TRANSLATOR_TO_V6_4	5	A2	B2	19	
TRANSLATOR_TO_V6_7	4	A1	B1	20	
TRANSLATOR_TO_V6_6	3	A0	B0	21	

DIR OE

VCCA=P2V5;VCCB=P3V3
TSSOP
2 22 GND GND

IC41

220NF C18 P2V5 GND
220NF C15 P3V3 GND

74AVC8T 245

V6_TO_TRANSLATOR_3	10	A7	B7	14	
V6_TO_TRANSLATOR_1	9	A6	B6	15	
V6_TO_TRANSLATOR_7	8	A5	B5	16	
V6_TO_TRANSLATOR_5	7	A4	B4	17	
V6_TO_TRANSLATOR_4	6	A3	B3	18	
V6_TO_TRANSLATOR_6	5	A2	B2	19	
V6_TO_TRANSLATOR_0	4	A1	B1	20	
V6_TO_TRANSLATOR_2	3	A0	B0	21	

DIR OE

VCCA=P2V5;VCCB=P3V3
TSSOP
P2V5 2 22 GND

220NF C9
220NF C8
220NF C12
220NF C10
220NF C11
GND P3V3

IC42 VCC=P3V3

SN65MLVD080

TRANSLATOR_TO_MLVDS_15	31	DE	A	24	AMC_P17_TX_P
TRANSLATOR_TO_MLVDS_14	40	D	B	25	AMC_P17_TX_N
MLVDS_TO_TRANSLATOR_7	41	R			
TRANSLATOR_TO_MLVDS_13	32	DE	A	26	AMC_P17_RX_P
TRANSLATOR_TO_MLVDS_12	39	D	B	27	AMC_P17_RX_N
MLVDS_TO_TRANSLATOR_6	38	R			
TRANSLATOR_TO_MLVDS_11	29	DE	A	18	AMC_P18_TX_P
TRANSLATOR_TO_MLVDS_10	46	D	B	19	AMC_P18_TX_N
MLVDS_TO_TRANSLATOR_5	47	R			
TRANSLATOR_TO_MLVDS_9	30	DE	A	20	AMC_P18_RX_P
TRANSLATOR_TO_MLVDS_8	45	D	B	21	AMC_P18_RX_N
MLVDS_TO_TRANSLATOR_4	44	R			
TRANSLATOR_TO_MLVDS_7	3	DE	A	12	AMC_P19_TX_P
TRANSLATOR_TO_MLVDS_6	52	D	B	13	AMC_P19_TX_N
MLVDS_TO_TRANSLATOR_3	53	R			
TRANSLATOR_TO_MLVDS_5	4	DE	A	14	AMC_P19_RX_P
TRANSLATOR_TO_MLVDS_4	51	D	B	15	AMC_P19_RX_N
MLVDS_TO_TRANSLATOR_2	50	R			
TRANSLATOR_TO_MLVDS_3	1	DE	A	6	AMC_P20_TX_P
TRANSLATOR_TO_MLVDS_2	58	D	B	7	AMC_P20_TX_N
MLVDS_TO_TRANSLATOR_1	59	R			
TRANSLATOR_TO_MLVDS_1	2	DE	A	8	AMC_P20_RX_P
TRANSLATOR_TO_MLVDS_0	57	D	B	9	AMC_P20_RX_N
MLVDS_TO_TRANSLATOR_0	56	R			
GND	33	RE*			

NOTE: PHYSICS PROFILE SUGGESTION

AMC MLVDS, LEVEL TRANSLATORS

Project file:glib.cpm — SYSTEM: <SYSTEM>

EDA-02180-V2-0

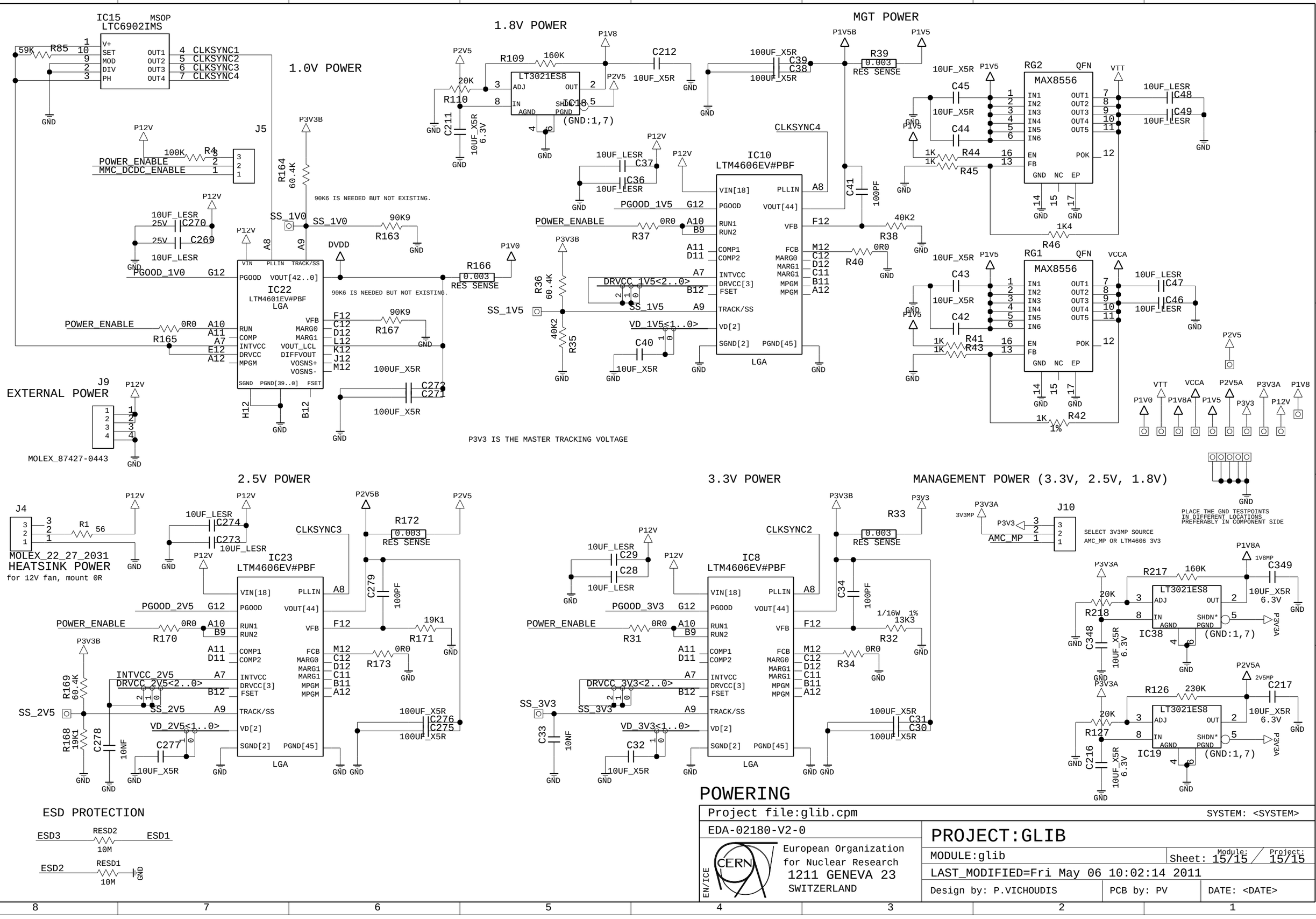
CERN EN/ICE
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

PROJECT:GLIB

MODULE:glib — Sheet: 14/15 (Module: / Project:)

LAST_MODIFIED=Fri May 06 09:48:54 2011

Design by: P.VICHOUDIS | PCB by: PV | DATE: <DATE>


1.8V POWER
MGT POWER
1.0V POWER
IC15 MSOP
LTC6902IMS
59K
R85
CLKSYNC1
CLKSYNC2
CLKSYNC3
CLKSYNC4
LT3021ES8
(GND:1,7)
R109
160K
20K
R110
C212
C211
10UF_X5R
6.3V
100UF_X5R
C39
C38
R39
0.003
RES SENSE
J5
P12V
100K
R4
POWER_ENABLE
MMC_DCDC_ENABLE
P3V3B
R164
60.4K
90K6 IS NEEDED BUT NOT EXISTING.
10UF_LESR
25V
C270
C269
SS_1V0
90K9
R163
DVDD
P1V0
R166
IC22
LTM4601EV#PBF
LGA
PGOOD_1V0
G12
POWER_ENABLE
0R0
R165
R167
100UF_X5R
C272
C271
H12
B12
J9
EXTERNAL POWER
MOLEX_87427-0443
IC10
LTM4606EV#PBF
PGOOD_1V5
POWER_ENABLE
R37
R36
DRVCC_1V5<2..0>
SS_1V5
VD_1V5<1..0>
C40
R35
40K2
C41
100PF
R38
R40
RG2
QFN
MAX8556
VTT
C45
C44
R44
R45
C48
C49
1K4
R46
RG1
VCCA
C43
C42
R41
R43
C47
C46
R42
1%
P2V5
P1V0
P1V8A
P1V5
P3V3
P3V3A
P1V8
P3V3 IS THE MASTER TRACKING VOLTAGE
2.5V POWER
3.3V POWER
MANAGEMENT POWER (3.3V, 2.5V, 1.8V)
J4
HEATSINK POWER
for 12V fan, mount 0R
R1
56
IC23
LTM4606EV#PBF
CLKSYNC3
R172
R170
R171
19K1
R169
INTVCC_2V5
DRVCC_2V5<2..0>
SS_2V5
R168
C278
10NF
C277
VD_2V5<1..0>
C279
C276
C275
ESD PROTECTION
RESD2
RESD1
10M
IC8
LTM4606EV#PBF
CLKSYNC2
R33
R31
R32
R34
PGOOD_3V3
INTVCC_3V3
DRVCC_3V3<2..0>
SS_3V3
VD_3V3<1..0>
C33
C32
C34
C31
C30
J10
SELECT 3V3MP SOURCE
AMC_MP OR LTM4606 3V3
PLACE THE GND TESTPOINTS
IN DIFFERENT LOCATIONS
PREFERABLY IN COMPONENT SIDE
IC38
IC19
R217
R218
R126
R127
C349
C348
C217
C216
POWERING
Project file:glib.cpm
SYSTEM: <SYSTEM>
EDA-02180-V2-0
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
EN/ICE
PROJECT:GLIB
MODULE:glib
Sheet: 15/15
Module: 15/15
Project:
LAST_MODIFIED=Fri May 06 10:02:14 2011
Design by: P.VICHOUDIS
PCB by: PV
DATE: <DATE>