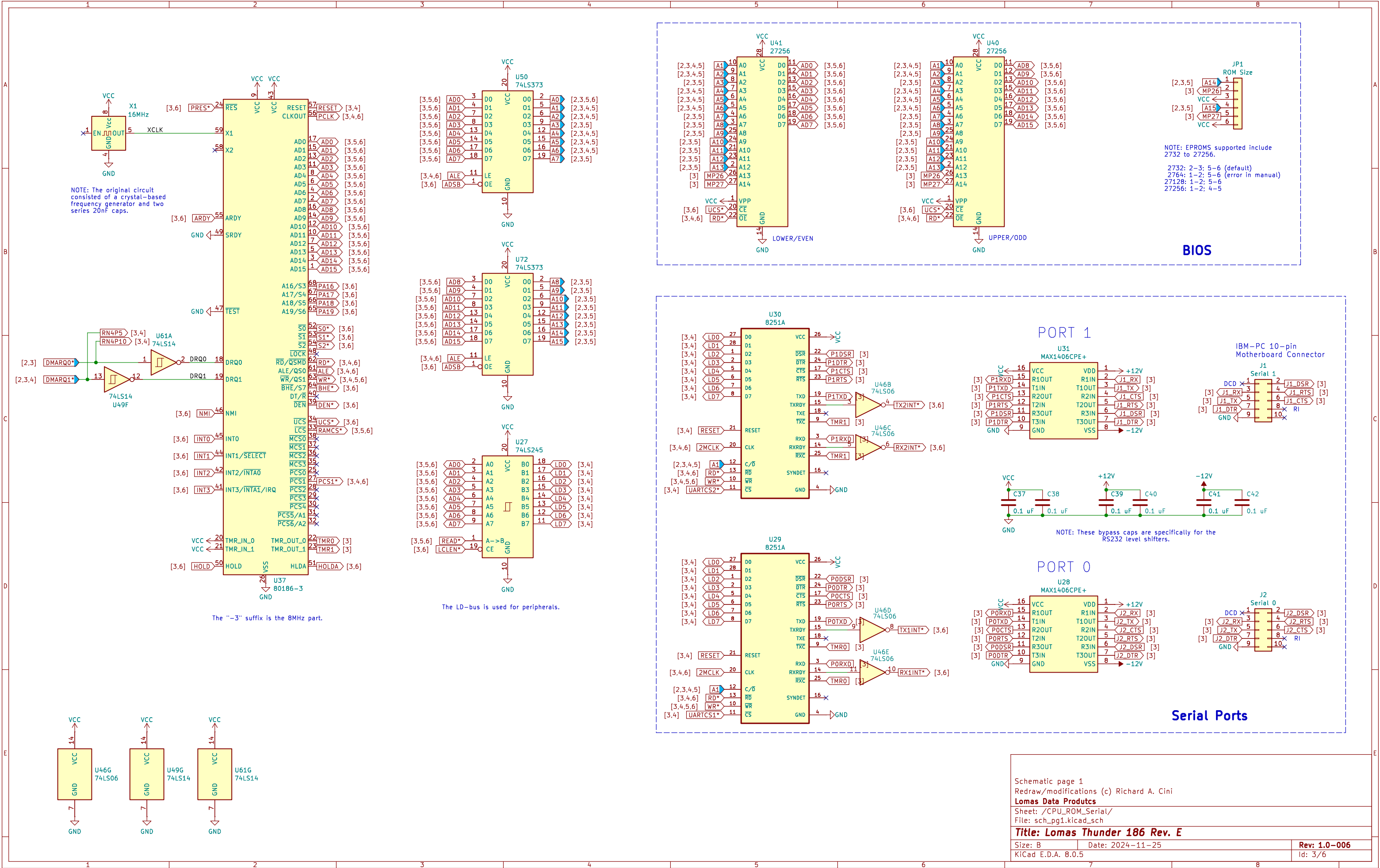
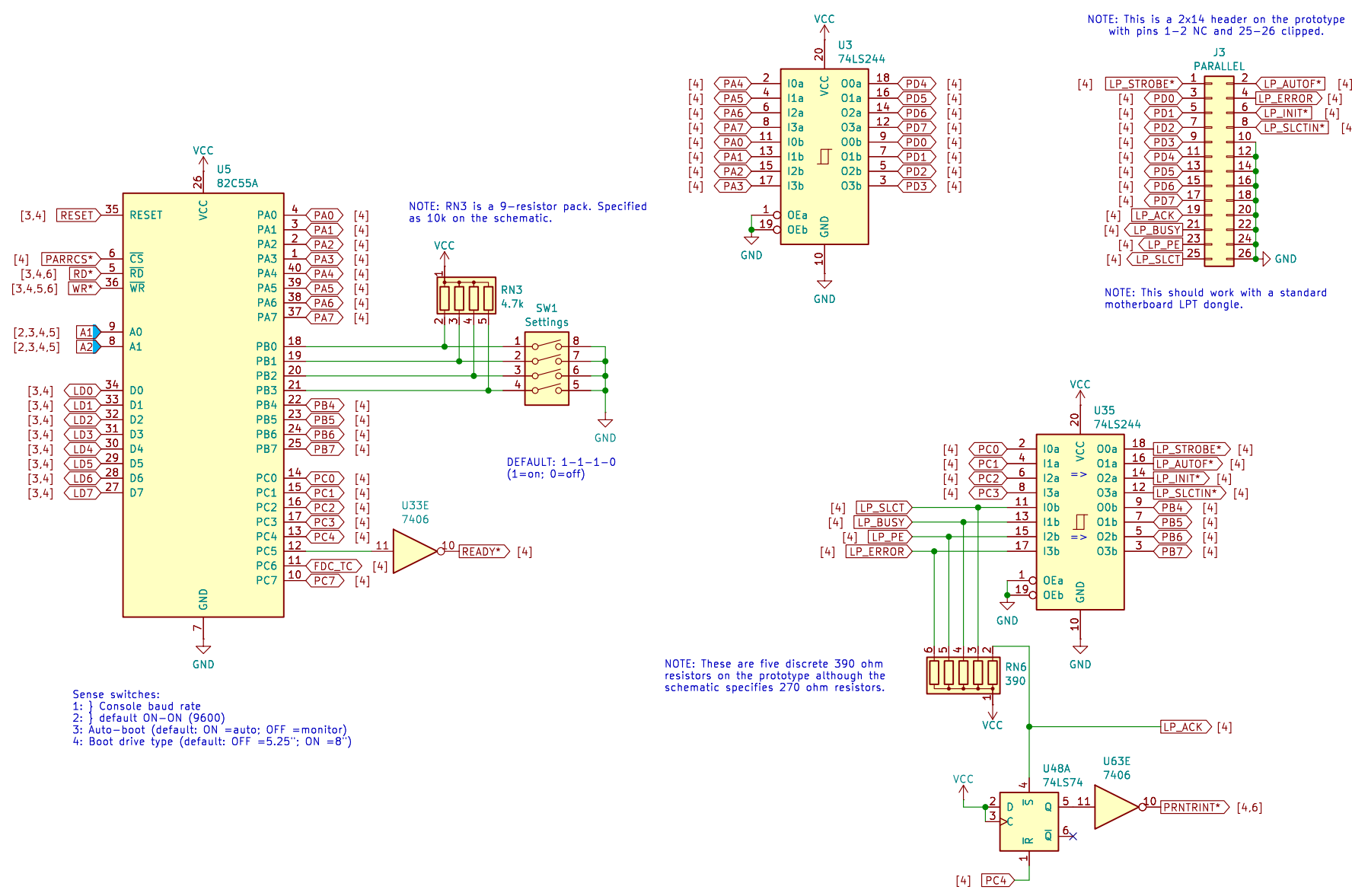


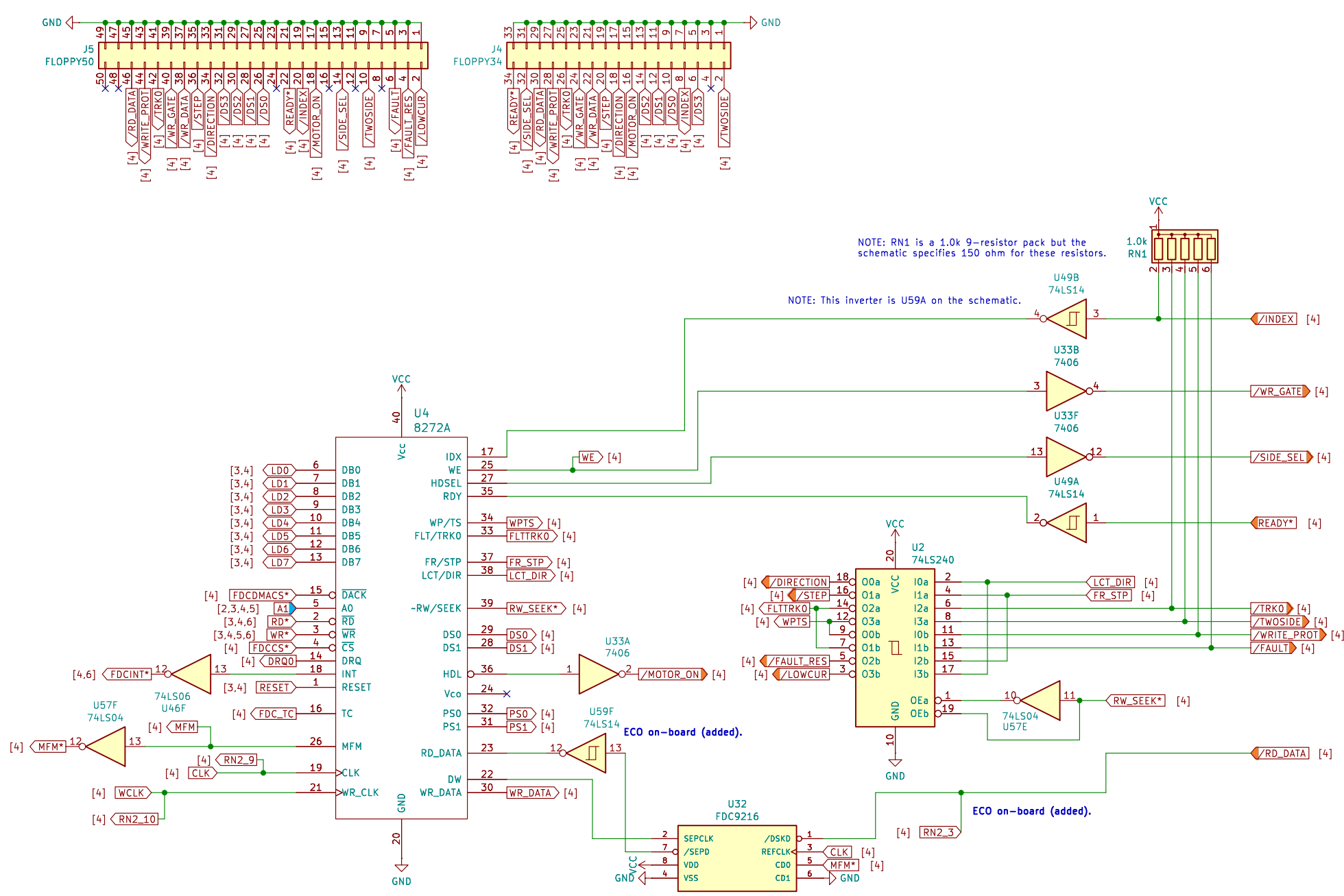
	1	2	3	4	5	
A	<div>Power_Buss_IF</div> <div></div> <div>File: pwr_S100buss.kicad_sch</div>	<div>CPU_ROM_Serial</div> <div></div> <div>File: sch_pg1.kicad_sch</div>	<div>Floppy_Parallel_IF</div> <div></div> <div>File: sch_pg2.kicad_sch</div>	<div>Memory</div> <div></div> <div>File: sch_pg3.kicad_sch</div>	<div>S100 Bus Interface</div> <div></div> <div>File: sch_pg4.kicad_sch</div>	A
B	<div>General Notes:</div> <div>01. Schematics are labeled "REV E".</div> <div>02. The CPU must be an original 80186. The "C" or "XL" suffix chips require different configuration register settings to be compatible and to have the right UCS/LCS configuration.</div> <div>03. Notwithstanding the dual footprint for the TMS4500/TMS4501, (which would accommodate higher density RAM), the board cannot use more than 256k on-board due to the LCS* chip select. There is another version of this board called the ThunderPlus which has 512k base memory, up to 1MB. Not sure how that would work given the BIOS ROM area but it would likely require a different version of the BIOS and circuit changes to use the other chip select lines from the 80186.</div>		<div>Design Changes:</div> <div>01. 16MHz crystal replaced by TTL oscillator.</div> <div>02. Adjustable voltage regulators replaced with either a switching regulator (5V) or small linear regulators (which are only used for serial level shifters).</div> <div>03. Entire DRAM section removed (saves 40 chips) in favor of high-density 55ns SRAM.</div> <div>04. MC1488/1489 level shifters replaced with higher-density MAX1406 shifters. J1/J2 changed to modern IBM-PC style motherboard headers.</div> <div>05. CPU package changed from LCC to PLCC which are easier to find.</div> <div>06. Prototype had four RPACKs (1k x2 and 4.7k x2) of which only two were partially used. Pull-up resistors were specified in other parts of the circuit but not used on the prototype.</div>		<div>ECOs on the original board:</div> <div>There are 4 changes on the back of the board:</div> <div>01. Added 1k pull-up from RN2.2 to U32.1 (pull-up on the RD_DATA* signal from the floppy).</div> <div>02. U45.2 disconnected from U45.4 and connected to U45.1 and .13 (correct on schematic).</div> <div>U45.4 and U45.10 NOT connected to VCC.</div> <div>03. U59 inverter added to U32.7 (correct on schematic).</div> <div>04. Added jumper J9 to allow connecting U44.40 and U44.41 to VCC.</div>	B
C	<div>NOTES/ERRATA from 1.0-001 to 1.0-002 (not manufactured):</div> <div>00. 10/15/24</div> <div>01. Alternative memory arrangement using high-density SRAM like the AS6C4008 512kx8-55 configured as 2x128k.</div> <div>NOTES/ERRATA from 1.0-002 to 1.0-003 (manufactured):</div> <div>00. 10/18/24</div> <div>01. Changed serial level shifters to higher-density versions; changed serial port headers to accommodate PC motherboard DE9 dongles.</div> <div>NOTES/ERRATA from 1.0-003 to 1.0-004 (not manufactured):</div> <div>00. 10/18/24. Transient version; not routed.</div> <div>01. U28.7 not connected to J2.7 (bad net name)</div> <div>02. Capacitors C3 and C8 are polarity reversed on the 79L12 regulator.</div> <div>03. Renamed address bus nets as the internal bus goes right out to the external bus.</div> <div>NOTES/ERRATA from 1.0-004 to 1.0-005:</div> <div>00. 11/14/24</div> <div>01. Discovered that the footprint for the 80186 was wrong (apparently Intel misnumbered the pins from the standard PLCC68, thus needing a custom footprint).</div> <div>NOTES/ERRATA from 1.0-005 to 1.0-006:</div> <div>00. 11/25/24</div> <div>01. Shifted the bypass caps around the CPU to increase spacing.</div> <div>02. Shifter oscillator down slightly to increase spacing.</div>					C
D	<div>Schematic page 1</div> <div>Redraw/modifications (c) Richard A. Cini</div> <div>Lomas Data Productcs</div> <div>Sheet: /</div> <div>File: s100_Thunder186-1.0-006.kicad_sch</div> <div>Title: Lomas Thunder 186 Rev. E</div> <div>Size: USLetter Date: 2024-11-25 Rev: 1.0-006</div> <div>KiCad E.D.A. 8.0.5 Id: 1/6</div>					D



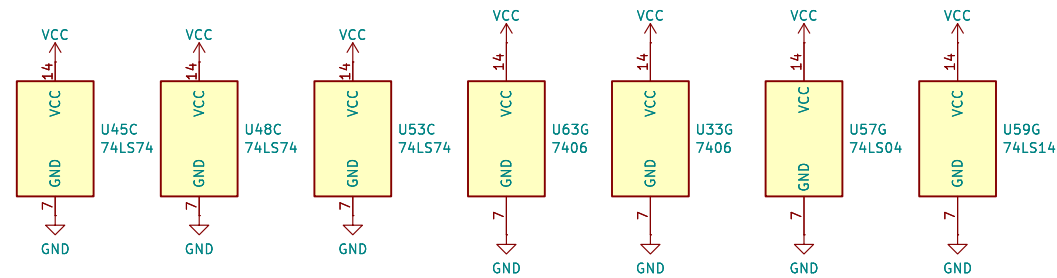
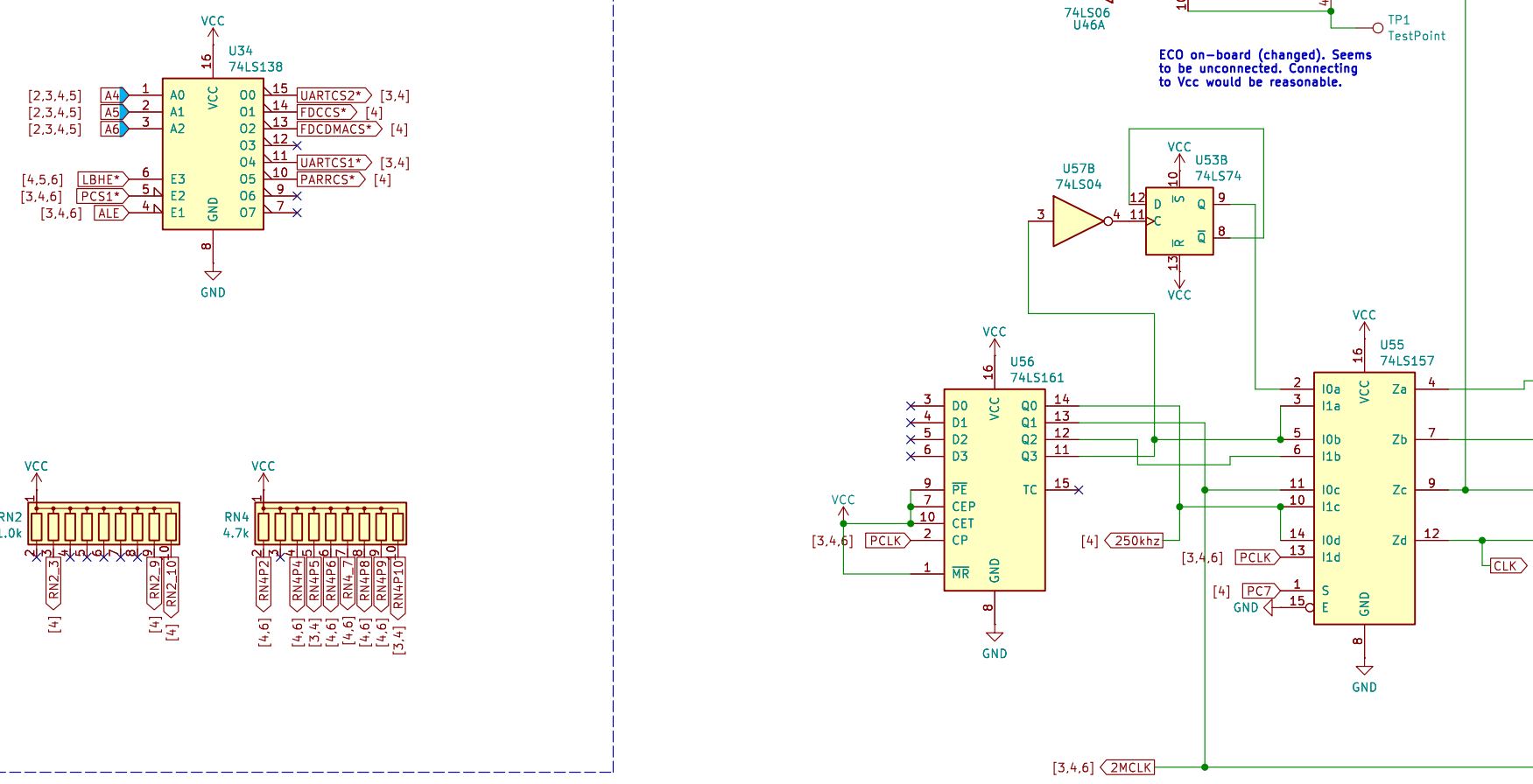
Parallel Printer Port & Sense Switches



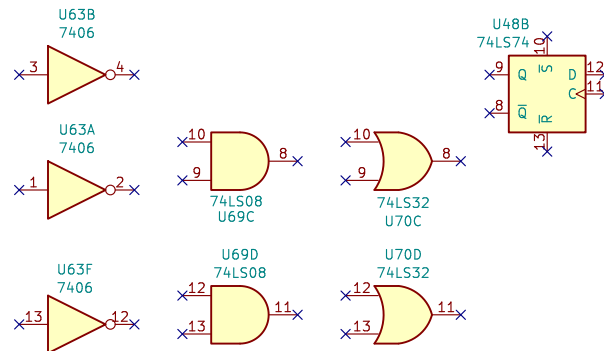
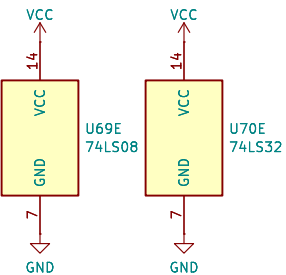
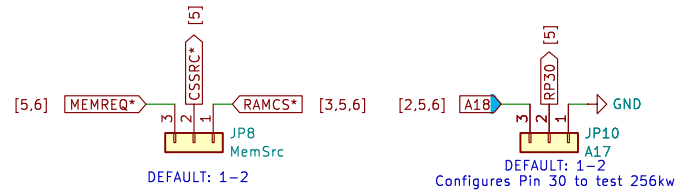
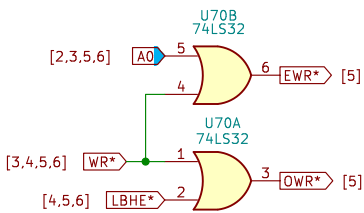
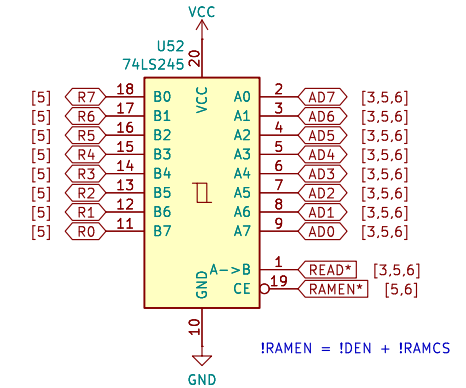
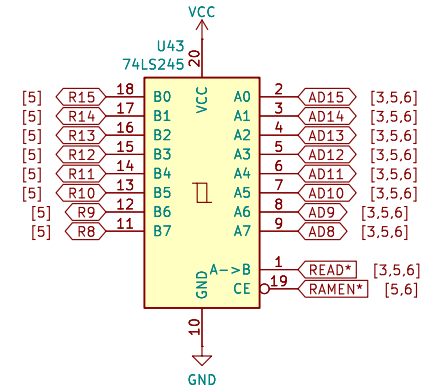
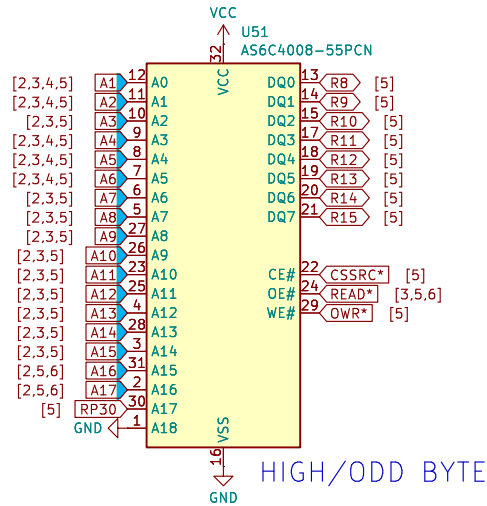
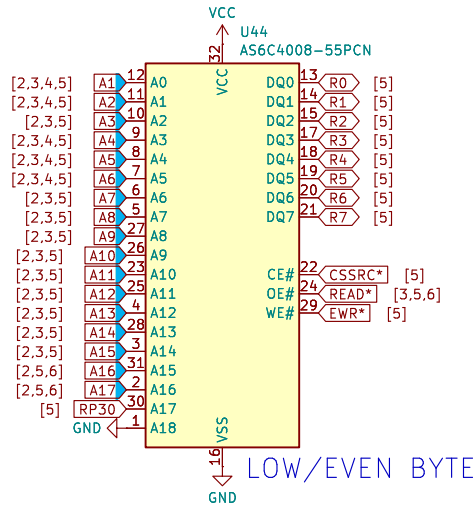
Floppy Interface



Peripheral Decode



The DRAM subsystem was replaced with high-density Alliance AS6C4008-55LP which is 512kx8 and cheap/plentiful. The maximum on-board memory is 256k due to the chip select logic. Forcing A17 and A18 to GND makes the 512k byte device a 128k byte device. Jumper provided in case it needs to be connected to A18.



Schematic page 3
Redraw/modifications (c) Richard A. Cini

Lomas Data Products

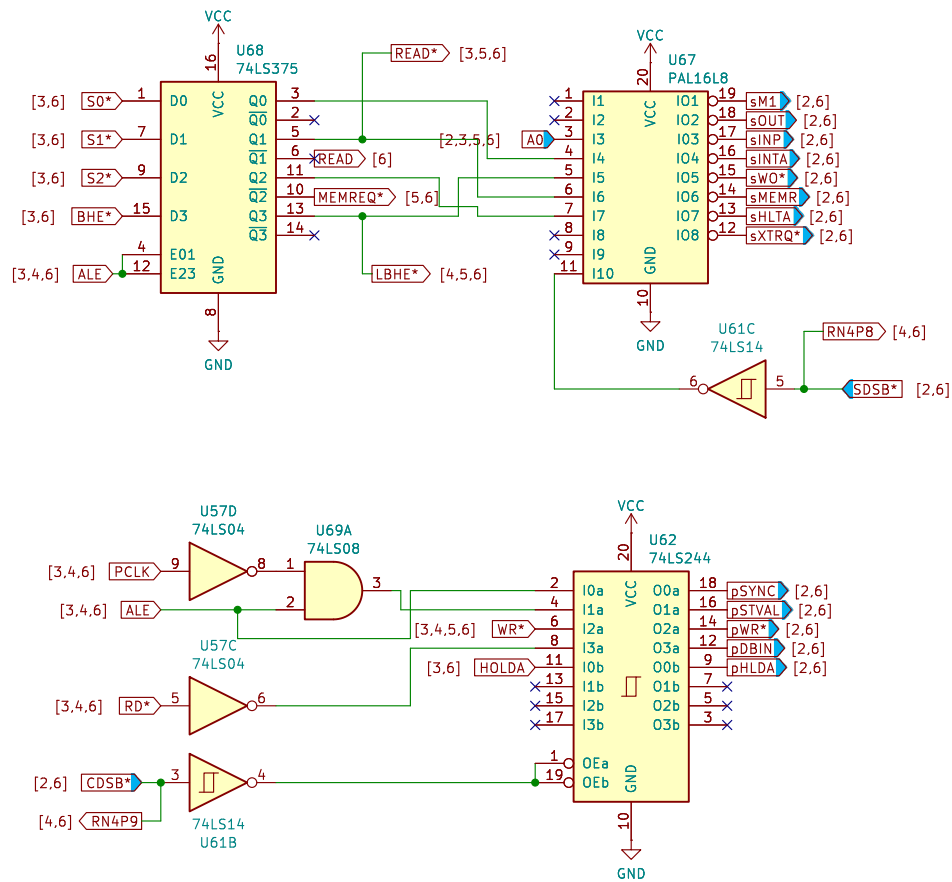
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Title: Lomas Thunder 186 Rev. E

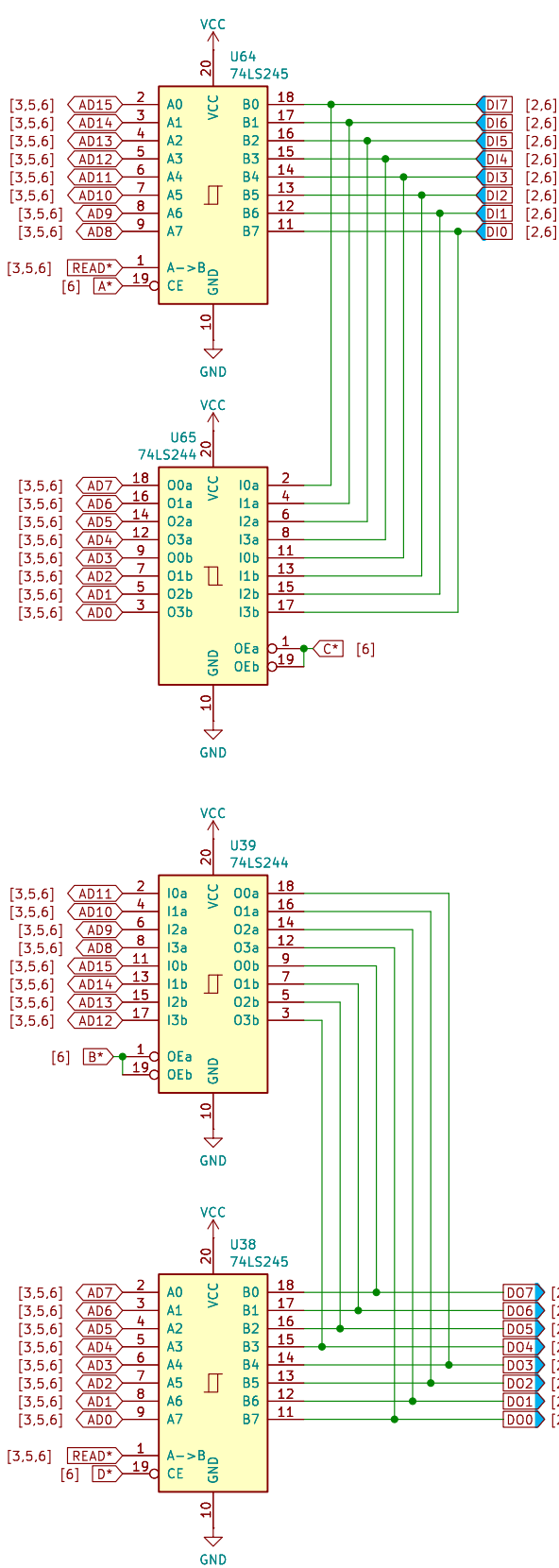
Size: A Date: 2024-11-25
KiCad E.D.A. 8.0.5

Rev: 1.0-006
Id: 5/6

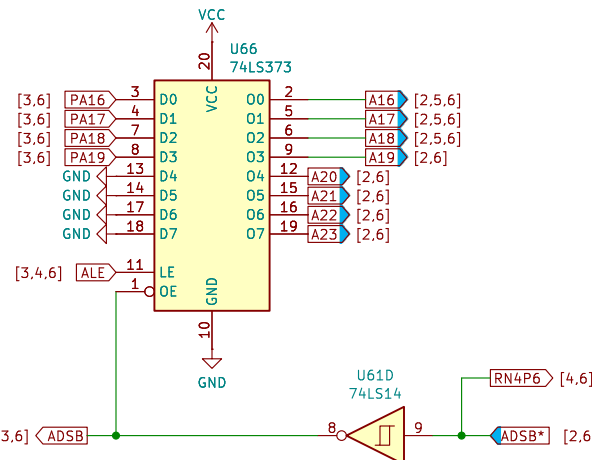
Buss Status Decode



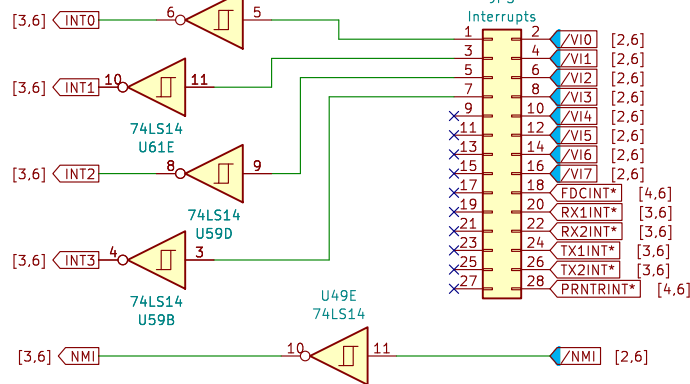
Data Buss Steering



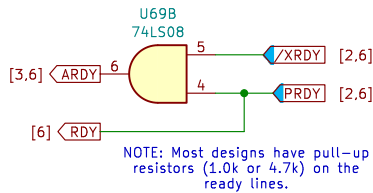
External Address Buss Interface



Interrupt Selection

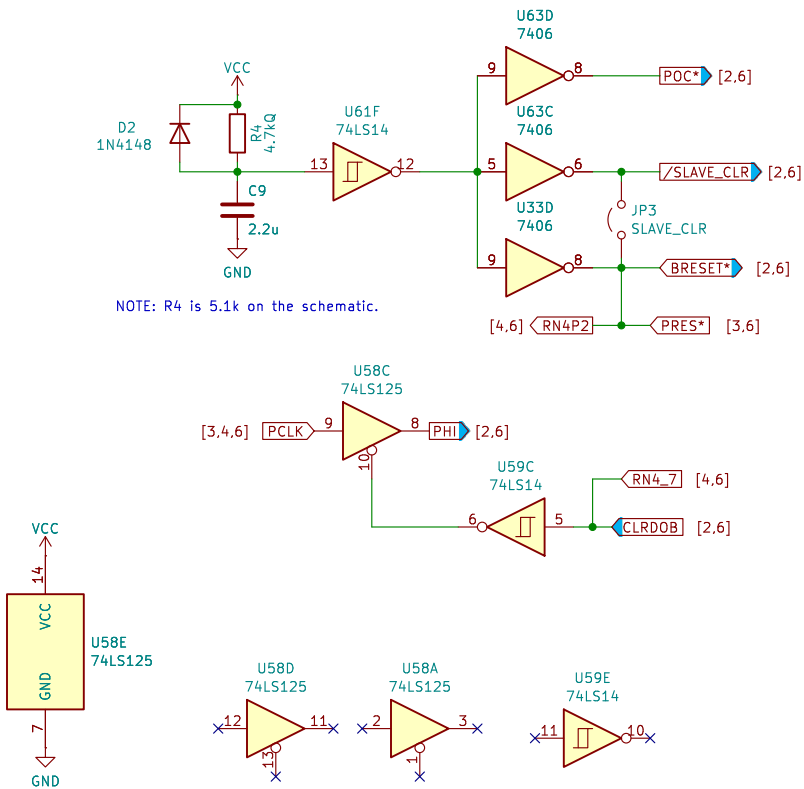


DEFAULT:
INT0 == /VIO
INT1 == /V1
INT2 == RX1INT* + RX2INT*

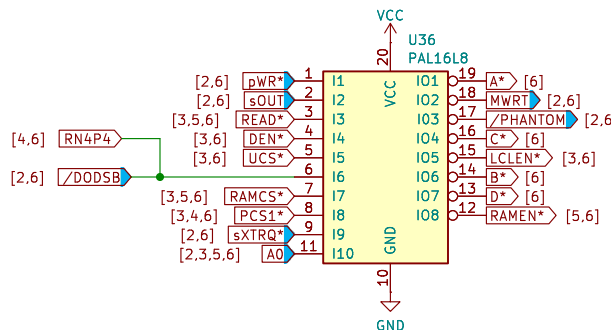


NOTE: Most designs have pull-up resistors (1.0k or 4.7k) on the ready lines.

Reset & Buss Clock



NOTE: R4 is 5.1k on the schematic.



Schematic page 4
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Lomas Data Products
Sheet: /S100 Bus Interface/
File: sch_pg4.kicad_sch

Title: Lomas Thunder 186 Rev. E

Size: B Date: 2024-11-25
KiCad E.D.A. 8.0.5

Rev: 1.0-006
Id: 6/6