Power_Buss_IF

File: pwr_S100buss.kicad_sch

Buffers_Memory

File: buffmem.kicad_sch

Video Generator

File: vidgen.kicad_sch

Clock_and_address

File: clockaddr.kicad_sch

Video Timing

File: timing.kicad_sch

IO Chips

File: inout.kicad_sch

NOTES/ERRATA from 1.0:

01. Resistor footprints are one size too small -- 1/4w uses 1/8w, etc.
02. U49/78L12 silkscreen is backwards -- mount device opposite.
03. Several chips have unconnected VCC or GND leads that might be from the use of ONE and ZERO.

Schematic page 1A
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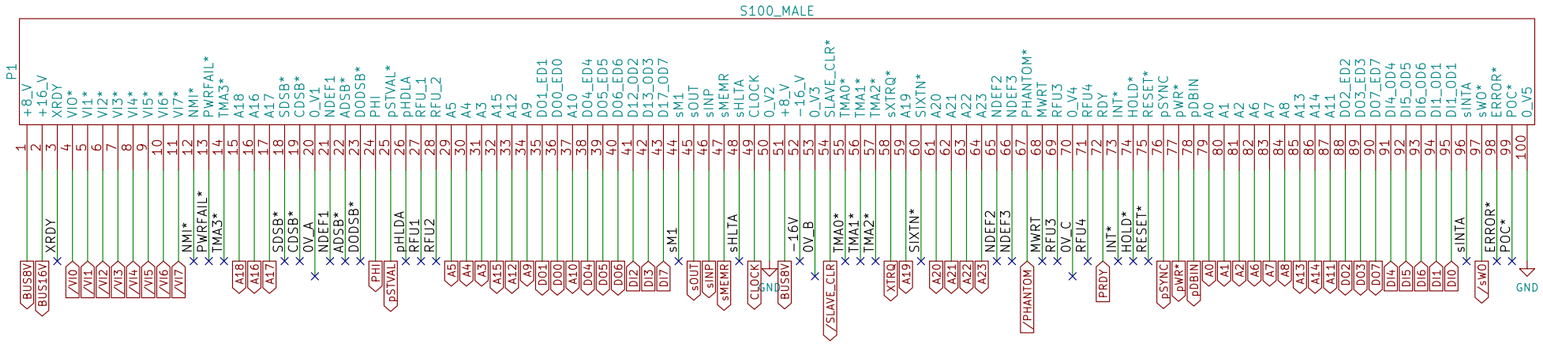
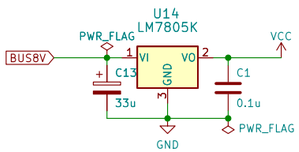
Lomas Data Produtcs

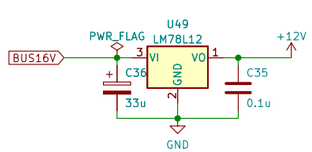
Sheet: /
File: s100_ColorMagic-1.1-001.kicad_sch

Title: Lomas Color Magic Redux

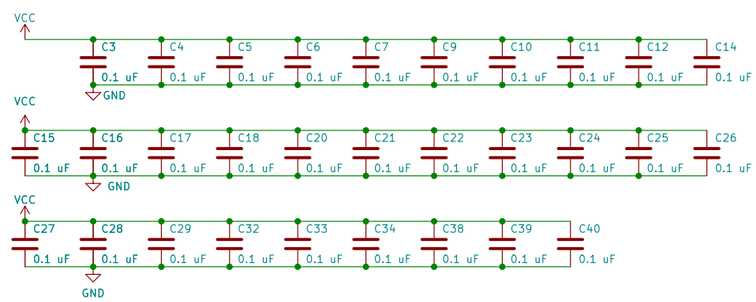
Size: USLetter	Date: 2024-02-15	**Rev: 1.1-001**
KiCad E.D.A. kicad (6.0.10-0)		Id: 1/7







NOTE: Original board used adjustible regulators rather than fixed. So R19 (1.3k) and R20 (160) on the LM317(7812) is not used and R12 (470) and R13 (150) on the LM338 (7805K) is not used.



CARD EJECTOR HOLES

H1

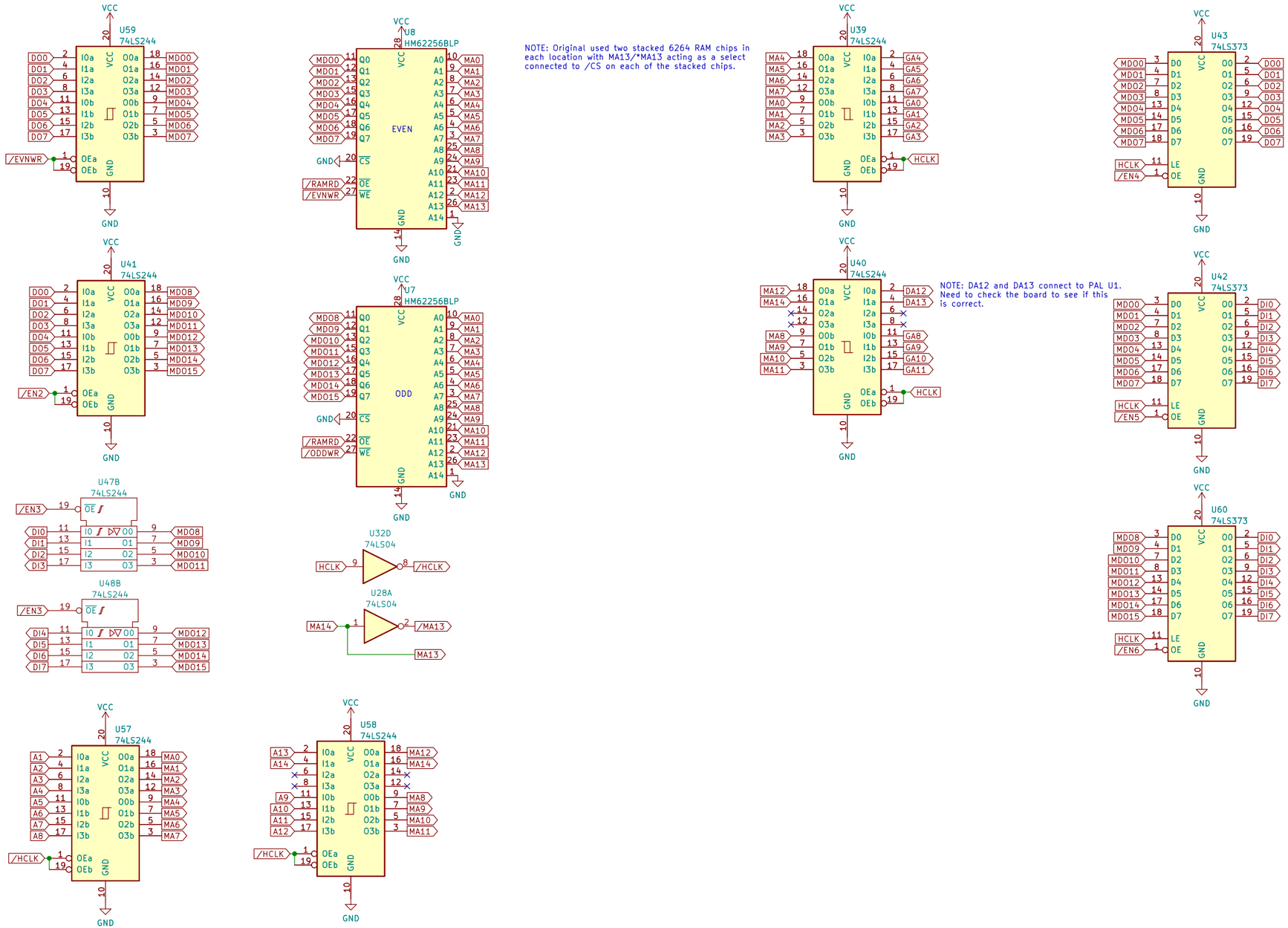
H2

Schematic page 1A
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

Sheet: /Power_Buss_IF/
File: pwr_S100buss.kicad_sch

Title: Lomas Color Magic Redux

Size: B	Date: 2024-02-15	**Rev: 1.1-001**
KiCad E.D.A. kicad (6.0.10-0)		Id: 2/7

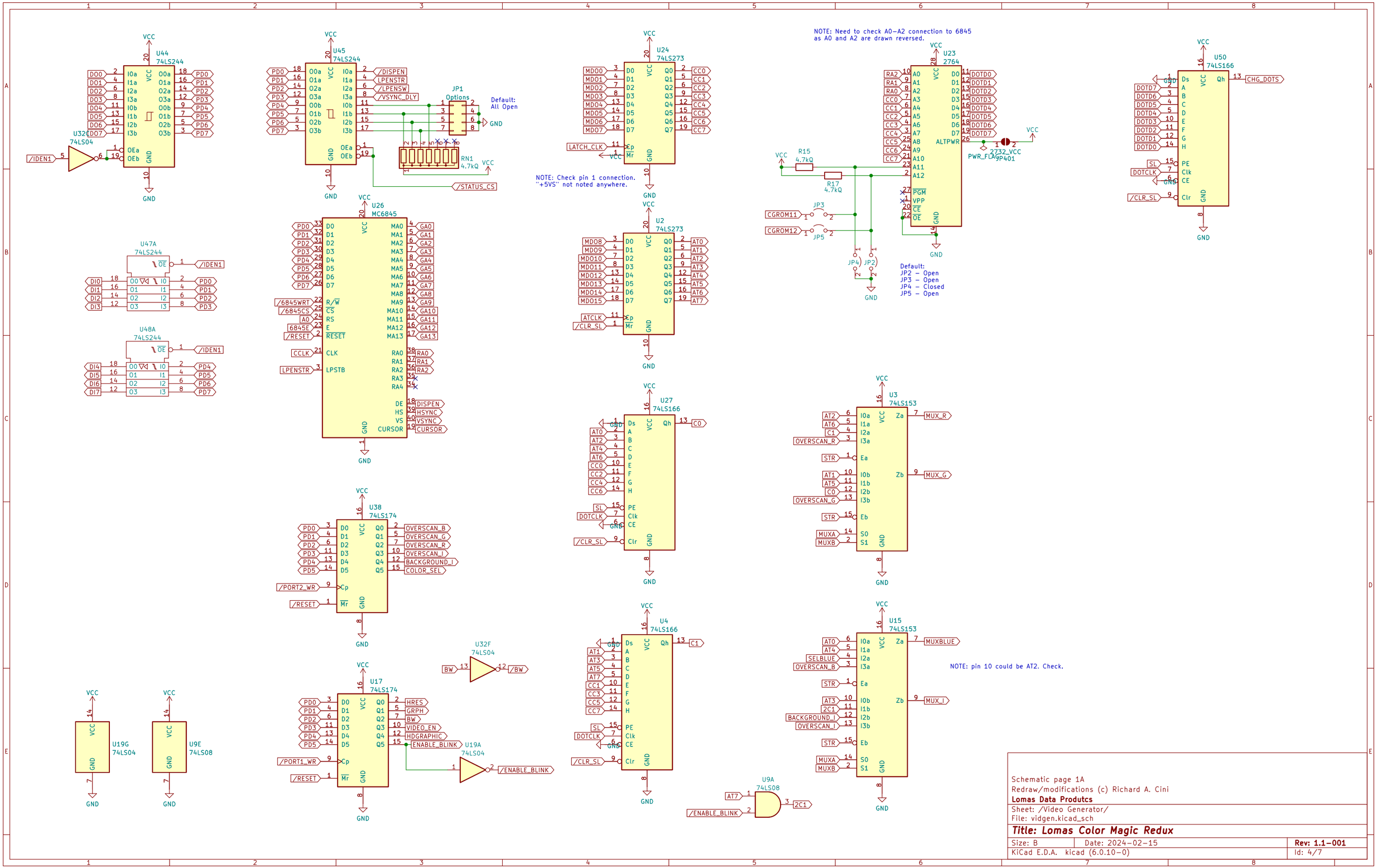


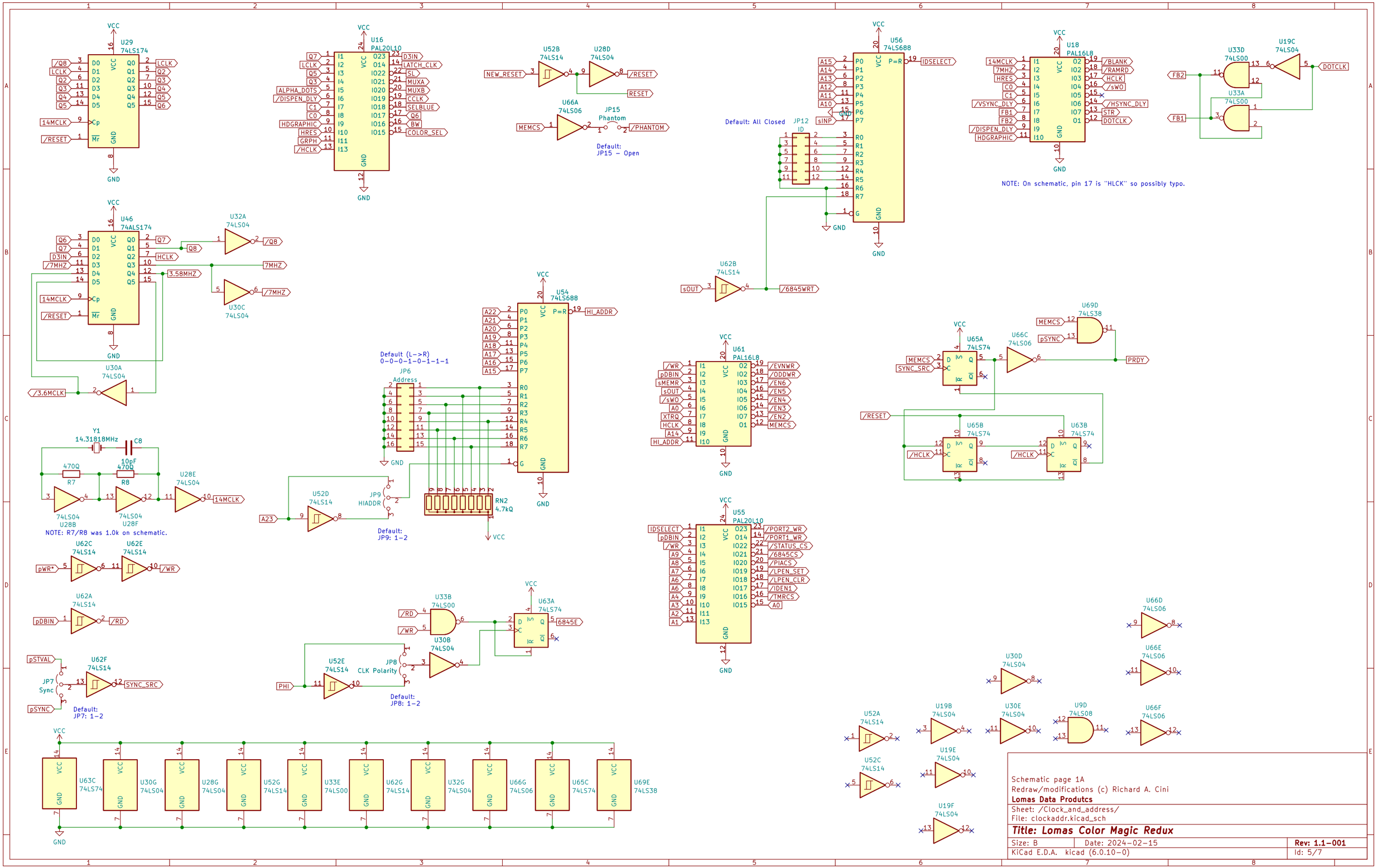
Schematic page 1A
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

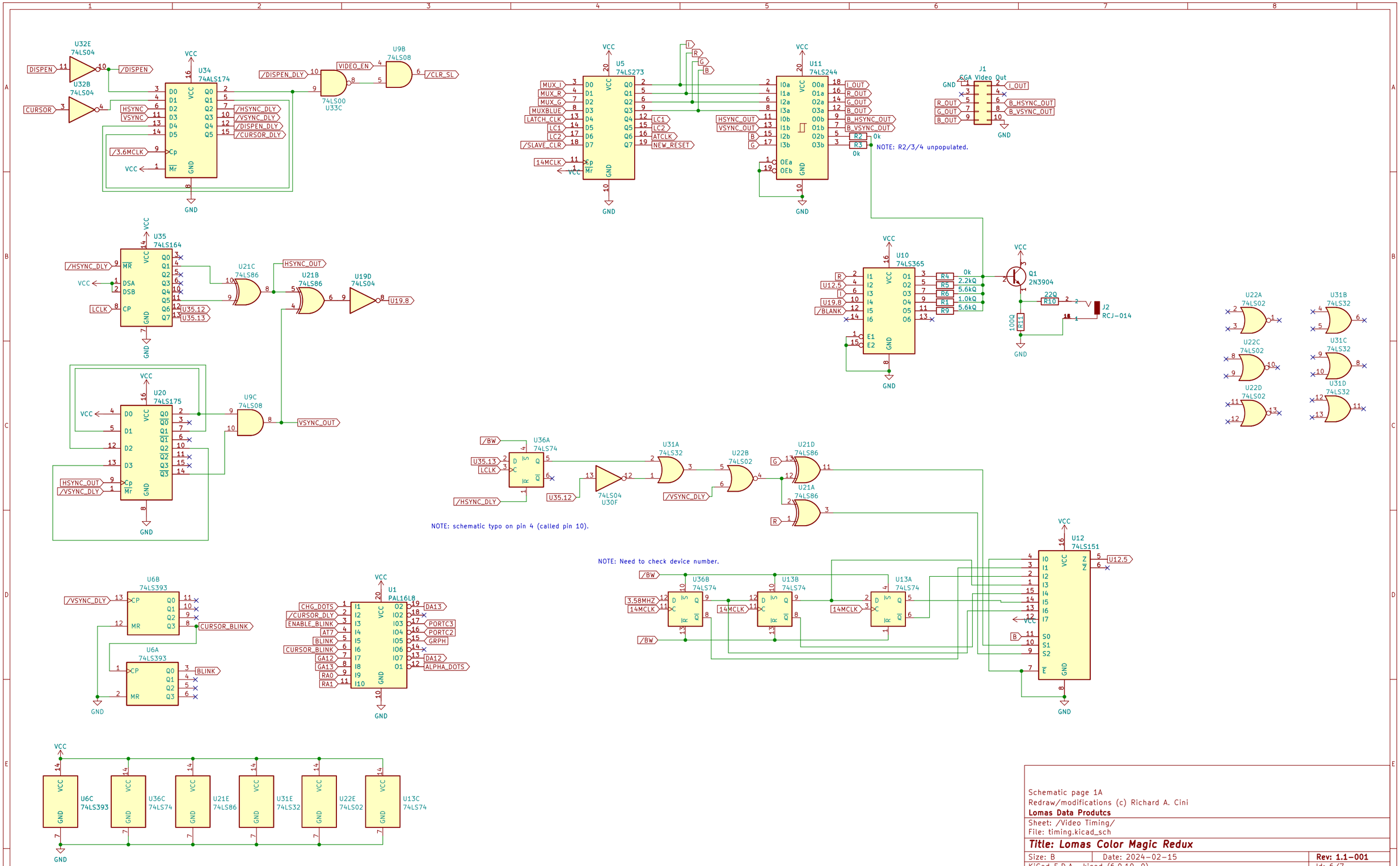
Sheet: /Buffers_Memory/
File: buffmem.kicad_sch

Title: Lomas Color Magic Redux

Size: B	Date: 2024-02-15	**Rev: 1.1-001**
KiCad E.D.A. kicad (6.0.10-0)		Id: 3/7


U44 74LS244
U32 74LS04
U45 74LS244
JP1 Options
Default: All Open
RN1 4.7kQ
U24 74LS273
NOTE: Check pin 1 connection. "+5VS" not noted anywhere.
NOTE: Need to check A0–A2 connection to 6845 as A0 and A2 are drawn reversed.
U23 2764
R15 4.7kQ
R17 4.7kQ
JP3
JP5
JP4
JP2
Default:
JP2 – Open
JP3 – Open
JP4 – Closed
JP5 – Open
PWR_FLAG
2732_VCC
U50 74LS166
U47A 74LS244
U48A 74LS244
U26 MC6845
U2 74LS273
U27 74LS166
U3 74LS153
U38 74LS174
U17 74LS174
U4 74LS166
U15 74LS153
NOTE: pin 10 could be AT2. Check.
U32F 74LS04
U19A 74LS04
U19G 74LS04
U9E 74LS08
U9A 74LS08
Schematic page 1A
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Video Generator/
File: vidgen.kicad_sch
Title: Lomas Color Magic Redux
Size: B
Date: 2024-02-15
Rev: 1.1-001
KiCad E.D.A. kicad (6.0.10-0)
Id: 4/7


U29 74LS174
U16 PAL20L10
U52B 74LS14
U28D 74LS04
U66A 74LS06
JP15 Phantom
Default: JP15 – Open
U56 74LS688
U18 PAL16L8
U33D 74LS00
U19C 74LS04
U33A 74LS00
Default: All Closed
JP12 ID
NOTE: On schematic, pin 17 is "HLCK" so possibly typo.
U46 74ALS174
U32A 74LS04
U30C 74LS04
U30A 74LS04
U62B 74LS14
U54 74LS688
Default (L->R) 0-0-0-1-0-1-1-1
JP6 Address
U61 PAL16L8
U69D 74LS38
U66C 74LS06
U65A 74LS74
U65B 74LS74
U63B 74LS74
Y1 14.31818MHz
C8 10pF
R7 470Ω
R8 470Ω
U28E 74LS04
U28B 74LS04
U28F 74LS04
NOTE: R7/R8 was 1.0k on schematic.
U52D 74LS14
JP9 HIADDR
Default: JP9: 1–2
RN2 4.7kΩ
U55 PAL20L10
U62C 74LS14
U62E 74LS14
U62A 74LS14
U33B 74LS00
U63A 74LS74
U30B 74LS04
U52E 74LS14
JP8 CLK Polarity
Default: JP8: 1–2
U62F 74LS14
JP7 Sync
Default: JP7: 1–2
U66D 74LS06
U66E 74LS06
U30D 74LS04
U52A 74LS14
U19B 74LS04
U30E 74LS04
U9D 74LS08
U66F 74LS06
U52C 74LS14
U19E 74LS04
U19F 74LS04
U63C 74LS74
U30G 74LS04
U28G 74LS04
U52G 74LS14
U33E 74LS00
U62G 74LS14
U32G 74LS04
U66G 74LS06
U65C 74LS74
U69E 74LS38
Schematic page 1A
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Clock_and_address/
File: clockaddr.kicad_sch
Title: Lomas Color Magic Redux
Size: B
Date: 2024-02-15
Rev: 1.1-001
KiCad E.D.A. kicad (6.0.10-0)
Id: 5/7

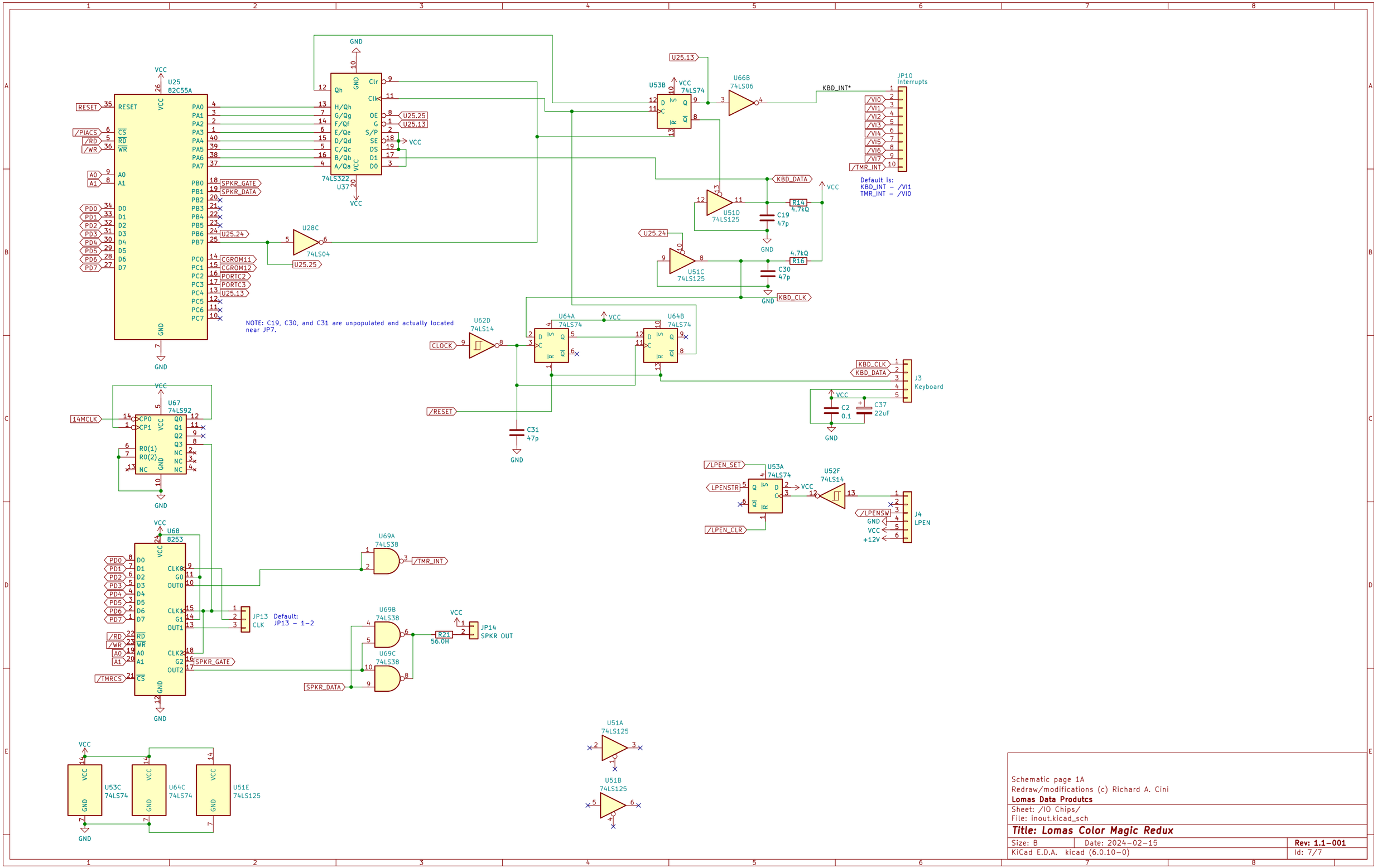


Schematic page 1A
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

Sheet: /Video Timing/
File: timing.kicad_sch

Title: Lomas Color Magic Redux

Size: B	Date: 2024-02-15	Rev: 1.1-001
KiCad E.D.A. kicad (6.0.10-0)		Id: 6/7



Schematic page 1A
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

Sheet: /IO Chips/
File: inout.kicad_sch

Title: Lomas Color Magic Redux

Size: B	Date: 2024-02-15	**Rev: 1.1-001**
KiCad E.D.A. kicad (6.0.10-0)		Id: 7/7