Power_Buss_IF

File: pwr_S100buss.kicad_sch

CPU_ROM_Serial

File: sch_pg1.kicad_sch

Floppy_Parallel_IF

File: sch_pg2.kicad_sch

Memory

File: sch_pg3.kicad_sch

S100 Bus Interface

File: sch_pg4.kicad_sch

General Notes:

01. Schematics are labeled "REV E".
02. The CPU must be an original 80186. The "C" or "XL" suffix chips require different configuration register settings to be compatible and to have the right UCS/LCS configuration.
03. Notwithstanding the dual footprint for the TMS4500/TMS4501, (which would accommodate higher density RAM), the board cannot use more than 256k on-board due to the LCS* chip select. There is another version of this board called the ThunderPlus which has 512k base memory, up to 1MB. Not sure how that would work given the BIOS ROM area but it would likely require a different version of the BIOS and circuit changes to use the other chip select lines from the 80186.
04. Note that the two serial ports are configured as NULL, but not a standard NULL pinout. RX/TX are fine, but the handshaking lines are not standard.

Design Changes:

01. 16MHz crystal replaced by TTL oscillator.
02. Adjustible voltage regulators replaced with either a switching regulator (5V) or small linear regulators (which are only used for serial level shifters).
03. Entire DRAM section removed (saves 40 chips) in favor of high-density 55ns SRAM.
04. MC1488/1489 level shifters replaced with higher-density MAX1406 shifters. J1/J2 changed to modern IBM-PC style motherboard headers.
05. CPU package changed from LCC to PLCC which are easier to find.
06. Prototype had four RPACKs (1k x2 and 4.7k x2) of which only two were partially used. Pull-up resistors were specified in other parts of the circuit but not used on the prototype.

ECOs on the original board:

There are 4 changes on the back of the board:

01. Added 1k pull-up from RN2.2 to U32.1 (pull-up on the RD_DATA* signal from the floppy).
02. U45.2 disconnected from U45.4 and connected to U45.1 and .13 (correct on schematic). U45.4 and U45.10 NOT connected to VCC.
03. U59 inverter added to U32.7 (correct on schematic).
04. Added jumper J9 to allow connecting U44.40 and U44.41 to VCC.

NOTES/ERRATA from 1.0-001 to 1.0-002 (not manufactured):
00. 10/15/24
01. Alternative memory arrangement using high-denisity SRAM like the AS6C4008 512kx8-55 configured as 2x128k.

NOTES/ERRATA from 1.0-002 to 1.0-003 (manufactured):
00. 10/18/24
01. Changed serial level shifters to higher-density versions; changed serial port headers to accommodate PC motherboard DE9 dongles.

NOTES/ERRATA from 1.0-003 to 1.0-004 (not manfactured):
00. 10/18/24. Transient version; not routed.
01. U28.7 not connected to J2.7 (bad net name)
02. Capacitors C3 and C8 are polairty reversed on the 79L12 regulator.
03. Renamed address bus nets as the internal bus goes right out to the external bus.

NOTES/ERRATA from 1.0-004 to 1.0-005:
00. 11/14/24
01. Discovered that the footprint for the 80186 was wrong (apparently Intel misnumbered the pins from the standard PLCC68, thus needing a custom footprint).

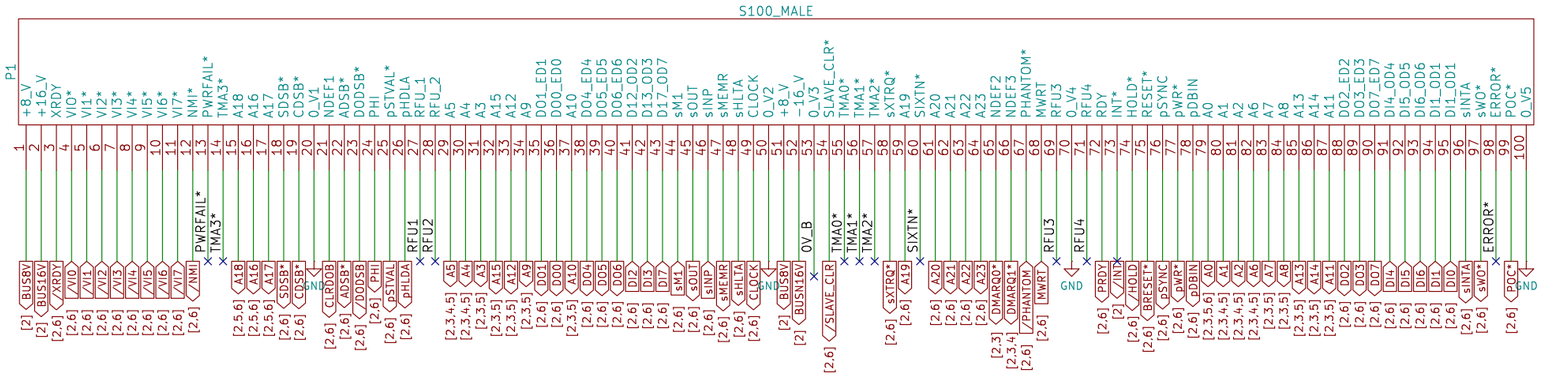
NOTES/ERRATA from 1.0-005 to 1.0-006:
00. 11/25/24
01. Shifted the bypass caps around the CPU to increase spacing.
02. Shifter oscillator down slightly to increase spacing.
03. Went back to original 2x10 header to allow for DM25F as used on the original board.
04. C9 in the POC circuit should be 22uf polarized. It's mis-drawn on the original schematic. Due to spacing, original footprint is used with a silkscreen polarity marking.

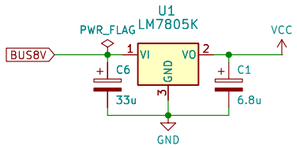
Schematic page 1
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

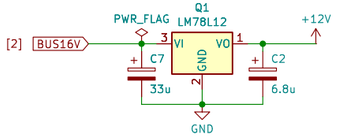
Sheet: /
File: s100_Thunder186-1.0-006.kicad_sch

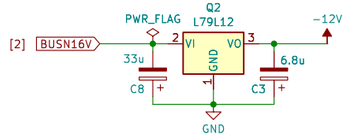
Title: Lomas Thunder 186 Rev. E

Size: USLetter	Date: 2024-11-28	**Rev: 1.0-006**
KiCad E.D.A. 8.0.5		Id: 1/6



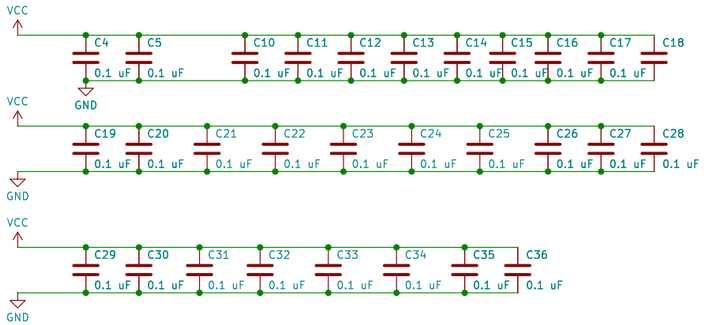






NOTE: Original board used adjustible regulators rather than fixed.

CARD EJECTOR HOLES



Schematic page 2
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Power_Buss_IF/
File: pwr_S100buss.kicad_sch

Title: Lomas Thunder 186 Rev. E

Size: B	Date: 2024-11-28	**Rev: 1.0-006**
KiCad E.D.A. 8.0.5		Id: 2/6

NOTE: The original circuit consisted of a crystal-based frequency generator and two series 20nF caps.

The "-3" suffix is the 8MHz part.

The LD-bus is used for peripherals.

BIOS

NOTE: EPROMS supported include 2732 to 27256.

2732: 2-3; 5-6 (default)
2764: 1-2; 5-6 (error in manual)
27128: 1-2; 5-6
27256: 1-2; 4-5

Serial Ports

PORT 1

PORT 0

NOTE: These bypass caps are specifically for the RS232 level shifters.

NOTE: J1/J2 connect by a 20-conductor ribbon cable to an IDC DB25F, pin 1 justified.

Schematic page 1
Redraw/modifications (c) Richard A. Cini
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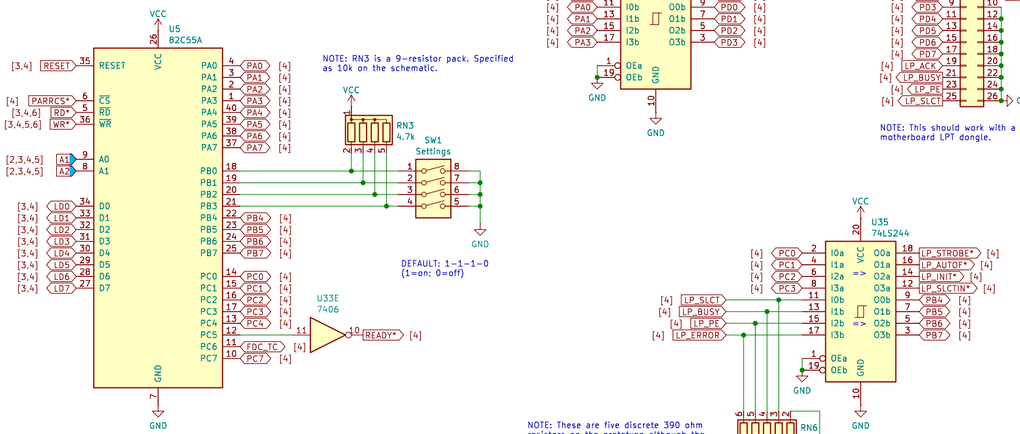
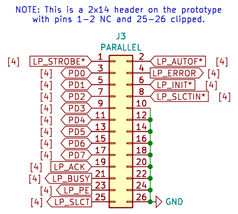
Sheet: /CPU_ROM_Serial/
File: sch_pg1.kicad_sch

Title: Lomas Thunder 186 Rev. E

Size: B	Date: 2024-11-28	**Rev: 1.0-006**
KiCad E.D.A. 8.0.5		Id: 3/6

Parallel Printer Port & Sense Switches



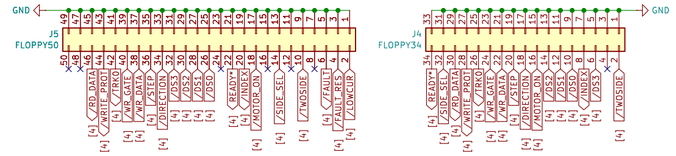


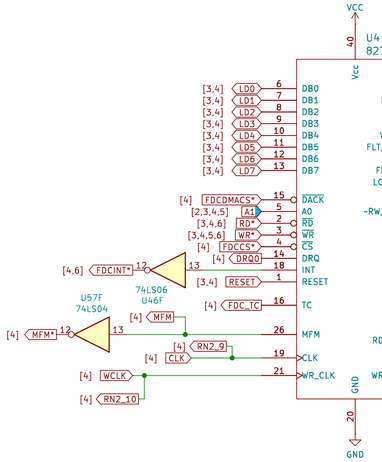
NOTE: This is a 2x14 header on the prototype with pins 1-2 NC and 25-26 clipped.

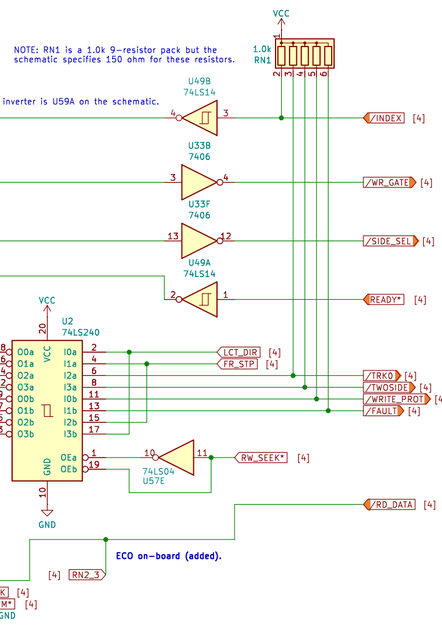
NOTE: This should work with a standard motherboard LPT dongle.

NOTE: These are five discrete 390 ohm resistors on the prototype although the schematic specifies 270 ohm resistors.

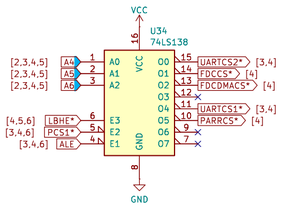
Floppy Interface

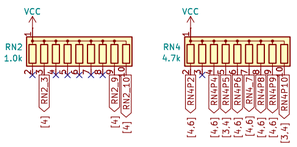


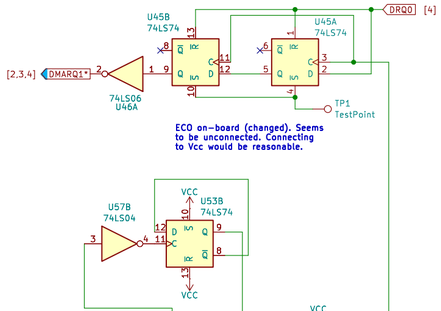


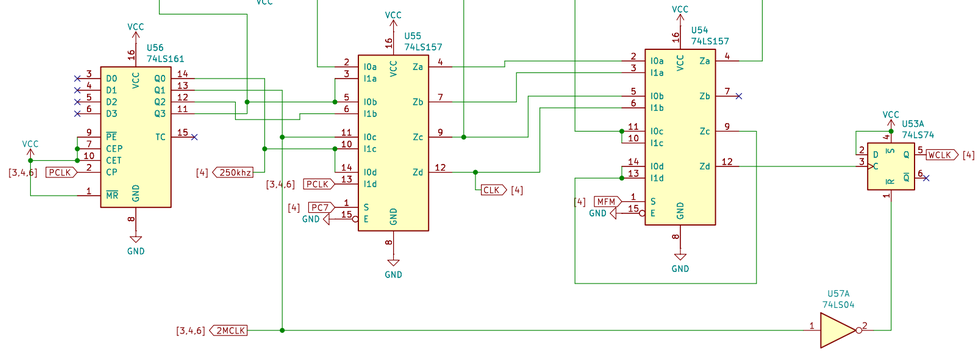


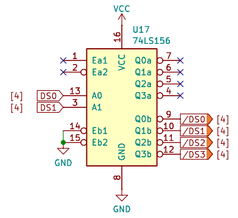
Peripheral Decode

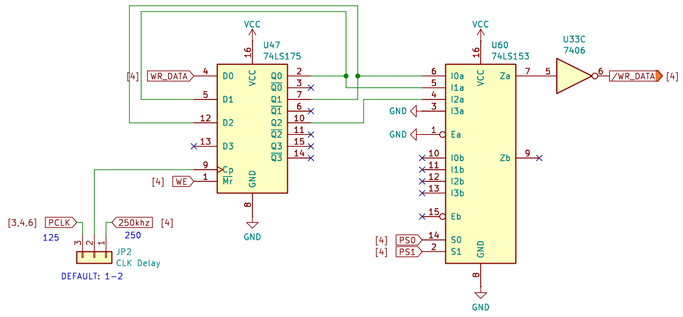


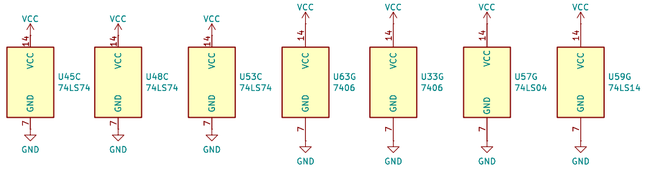












Schematic page 2
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Floppy_Parallel_IF/
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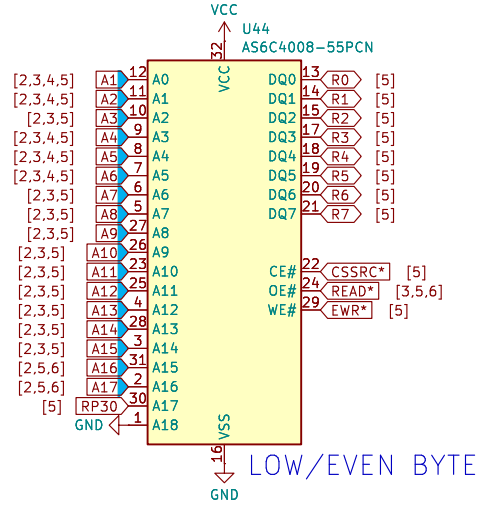
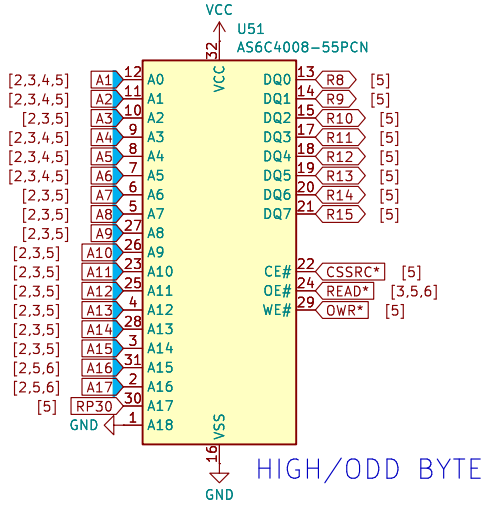
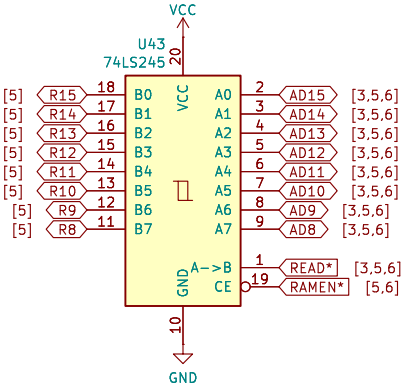
Title: Lomas Thunder 186 Rev. E

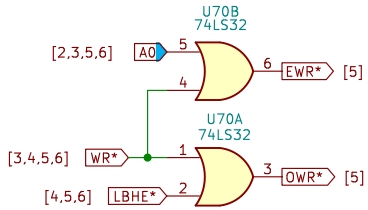
Size: C	Date: 2024-11-28	**Rev: 1.0-006**
KiCad E.D.A. 8.0.5		Id: 4/6

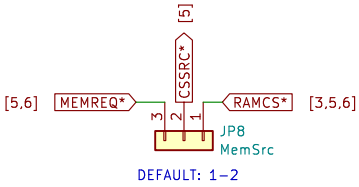
The DRAM subsystem was replaced with high-density Alliance AS6C4008-55LP which is 512kx8 and cheap/plentiful. The maximum on-board memory is 256k due to the chip select logic. Forcing A17 and A18 to GND makes the 512k byte device a 128k byte device. Jumper provided in case it needs to be connected to A18.

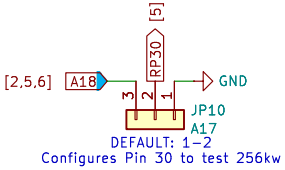


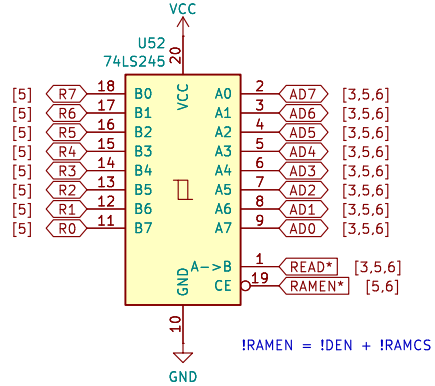


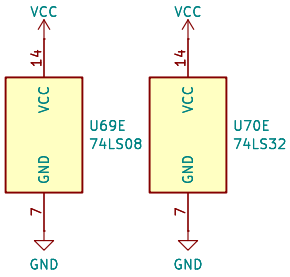


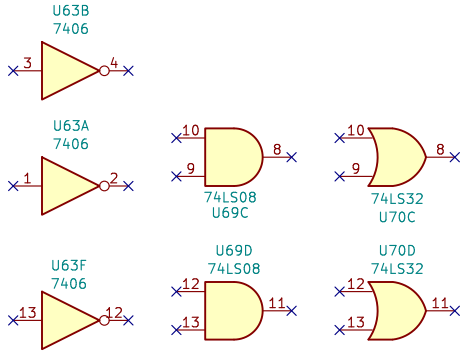


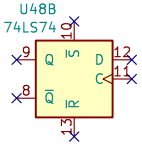










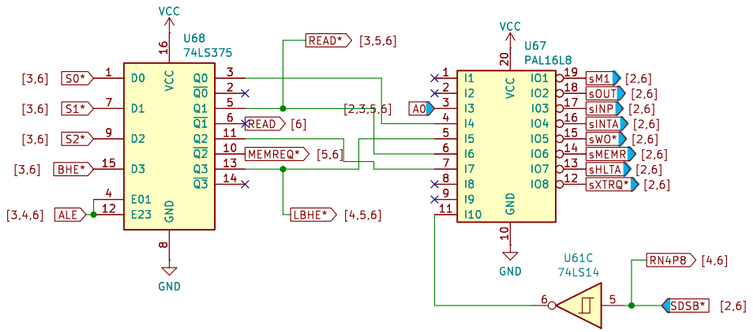


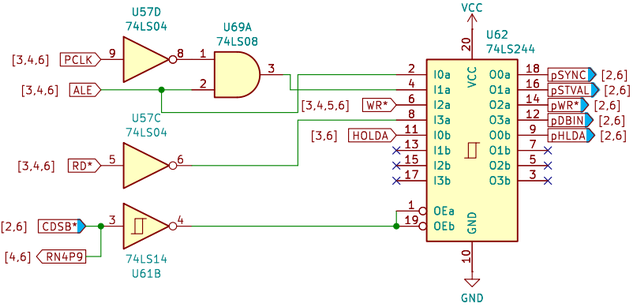
Schematic page 3
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Memory/
File: sch_pg3.kicad_sch

Title: Lomas Thunder 186 Rev. E

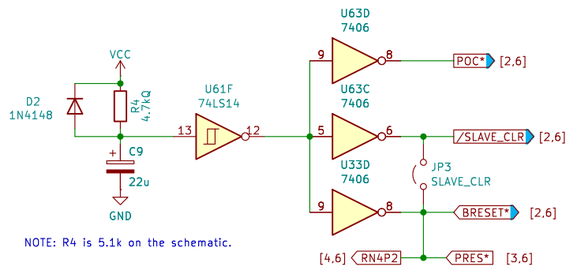
Size: A	Date: 2024-11-28	**Rev: 1.0-006**
KiCad E.D.A. 8.0.5		Id: 5/6

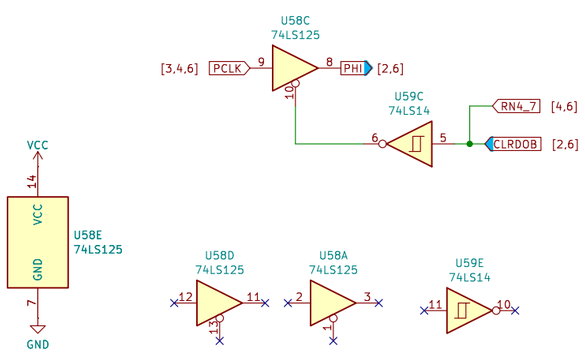
Buss Status Decode



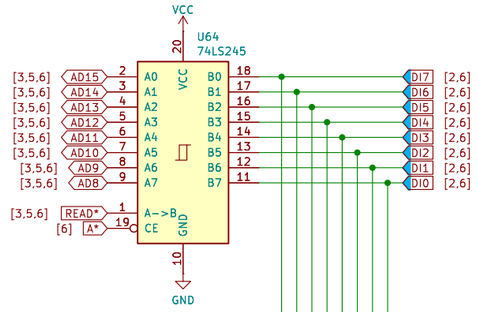


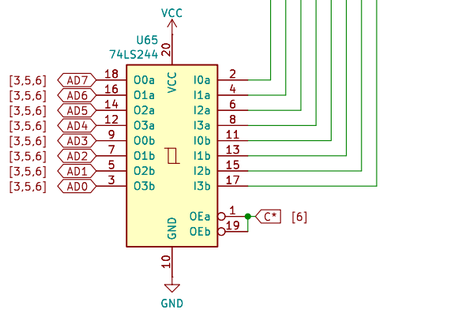
Reset & Buss Clock

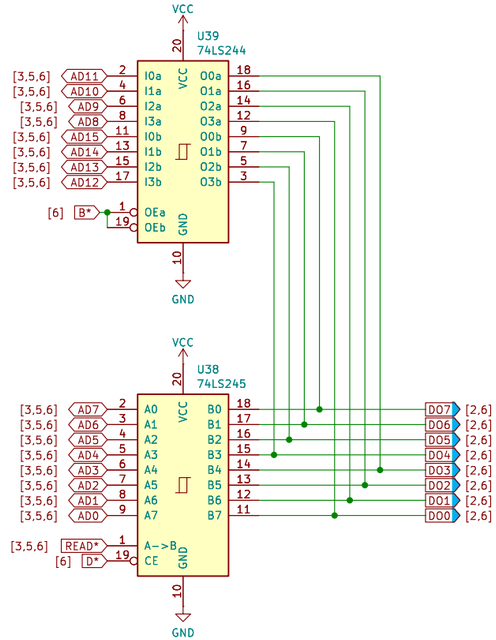




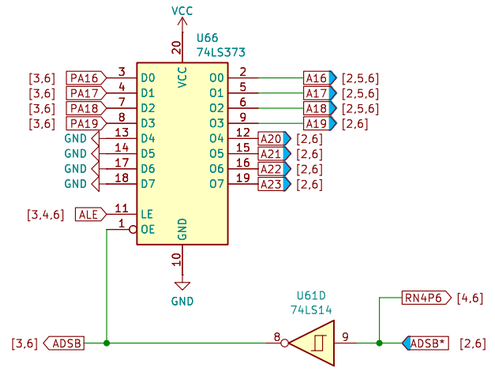
Data Buss Steering





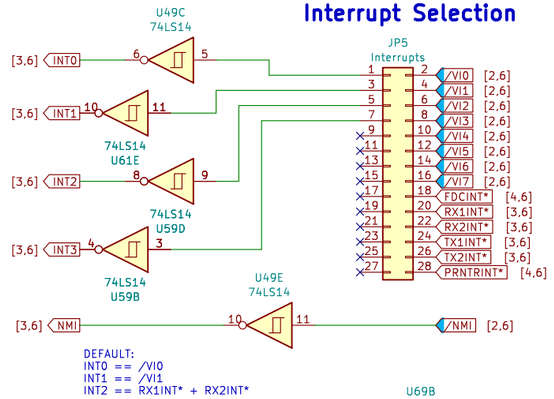


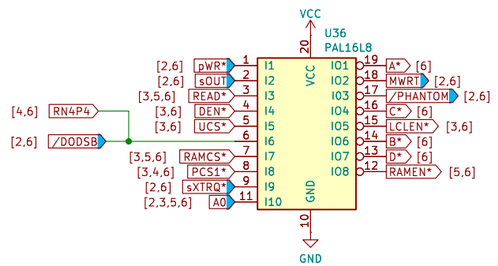
External Address Buss Interface

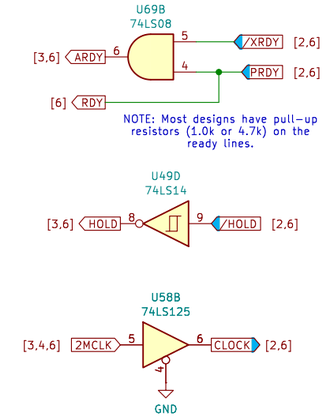


NOTE: Original J5 used two single-row headers but the spacing is off, making it hard to use standard jumpers. So, it was changed to a standard dual-row header which can be modified to fit.

Interrupt Selection







Schematic page 4
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

Sheet: /S100 Bus Interface/
File: sch_pg4.kicad_sch

Title: Lomas Thunder 186 Rev. E

Size: B	Date: 2024-11-28	**Rev: 1.0-006**
KiCad E.D.A. 8.0.5		Id: 6/6