Power_Buss_IF

File: pwr_S100buss.kicad_sch

Buffers_Memory

File: buffmem.kicad_sch

Video Generator

File: vidgen.kicad_sch

Clock_and_address

File: clockaddr.kicad_sch

Video Timing

File: timing.kicad_sch

IO Chips

File: inout.kicad_sch

ERRATA from 1.0 to 1.1-002:
00. v1.0 of board was trashed.
01. Resistor footprints are one size too small -- 1/4w uses 1/8w, etc.
    Due to space limitations, left at 1/8w.
02. U49/78L12 silkscreen is backwards. Corrected.
03. Several chips have unconnected VCC or GND leads that might be from
    the use of ONE and ZERO. Corrected.

ERRATA from 1.1-002 to 1.1-003
    v.003 was never manufactured.

ERRATA from 1.1-003 to 1.1-004
01. J6 (address select) is flipped. Rotated 180.
02. Design relies on SLAVE_CLR [54] for reset, but not all boards (like
    the SCP 200B) generate that signal. Reused spare gate of the LS125
    and added a jumper and pull-up to generate that signal driven by
    POC [99].
03. Changed memory chip wiring to be similar to the original, using
    MA13 as the CS* and grounding A13 and A14 of the 62256 (thus making
    it a 6264 albeit with only one chip select).
04. Discovered that A6 is connected twice on U55. Changed second to
    A5.

The 1.1-004 version works.

Version 1.1.005
01. Removed tie points TP2-TP5 and permanently connected the pins to
    their respective endpoints. Run of 15 "proto finish" boards was made.

ERRATA from 1.1-005 to 1.1-006
01. Edge-case memory access issue. MA13 was inadvertently connected to CS*
    of the memory chips. This was discovered trying to get Windows running
    which uses Mode 6 640x200 B&W resolution (the full 16k of memory).
    Other Mode 6 apps like Sim City also do not work. Bodge wire changes
    oddly do not improve the performance, so there is another issue maybe
    in one of the PAL equations.

NOTE:

The board has a number of drill-outs and jumpers on the back of the board but there are no known ECO documents to support this. When looking at the changes, they match the connections on the published schematic. So, I'm guessing that these were merely changes to fix defective boards from the board shop rather than true ECOs.

There are 9 jumpers and several drill-outs, with the jumpers easier to document:

Jumpers
=======
1. U23 (EPROM): ties socket pin 28 to socket pin 26, Vcc for 2764.
2. U65.13 to U66.5 } PRDY flip-flop control
3. U65.5 to U63.13 }
4. U46.2 to U16.1 (Q7) (was inverted)
5. U3.4 to U4.13 (C1) (swaps C0 and C1)
6. U3.12 to U27.13 (C0)
7. U25.13 to U53.9 (Keyboard INT out)
8. U5.19 - U52.3 } Connects SLAVE_CLR to internal RESET circuit.
9. U5.18 to bus [54] }

Drill-outs
==========
1. U64.5 x U65.4
2. U63.4 x U63.13
3. U63.13 x Vcc
4. U32.1 x from whatever U46.2 went to.
5. [54] from wherever U5.19 went to.
6. U3.4 x U3.12
7. U3.12 x U4.13 (?)

NOTE 2:

After using an automated BOM analysis and comparing to the actual board, there are four connections on three chips that do not match the schematic. All are drawn connecting to VCC yet they are open connections on the board.

U63.4
U64.4 and U64.10
U65.4

U64.10 and U65.4 are connected together.

Drafting Notes:

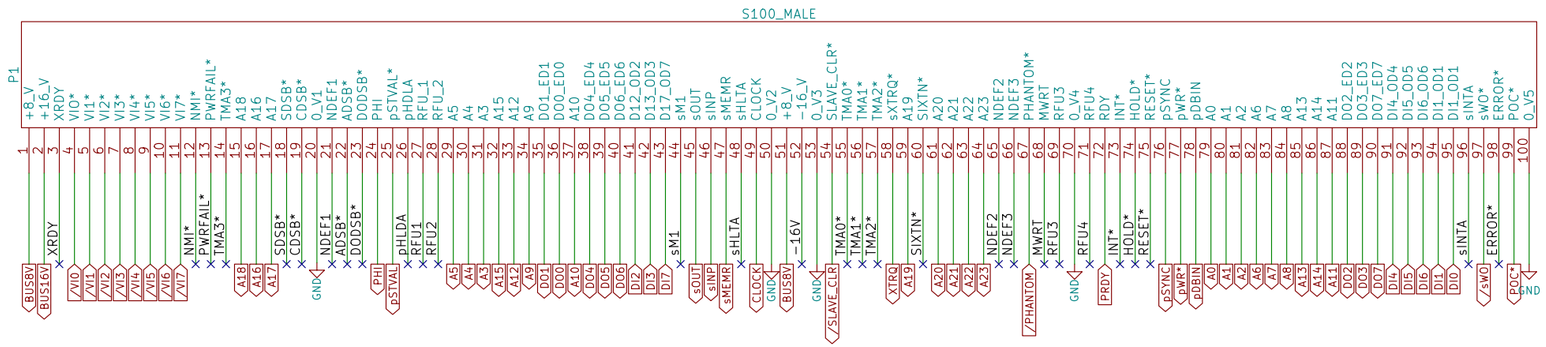
1. Green tags on signal flags denote S100 signal.

Lomas Data Produtcs

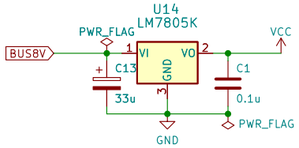
Sheet: /
File: s100_ColorMagic-1.1-006.kicad_sch

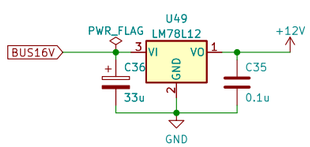
Title: Lomas Color Magic Redux

Size: USLetter	Date: 2025-02-13	**Rev: 1.1-006**
KiCad E.D.A. kicad (6.0.11-0)		Id: 1/7

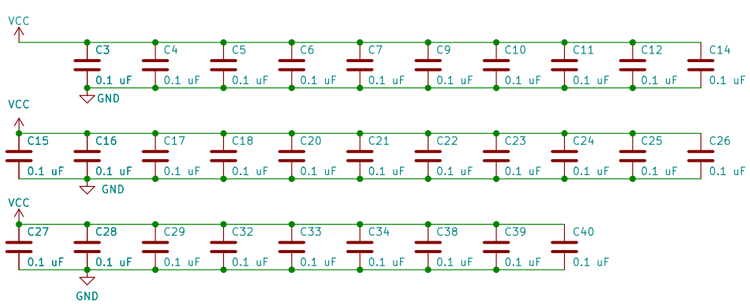


NOTE: Pins 20, 53, and 70 are grounded to be compliant with IEEE-696 (post-Altair/IMSAI or any front-panel based system).





NOTE: Original board used adjustible regulators rather than fixed. So R19 (1.3k) and R20 (160) on the LM317(7812) are not used, and R12 (470) and R13 (150) on the LM338 (7805K) are not used.



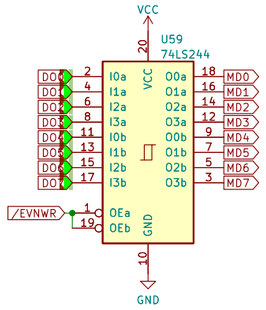
CARD EJECTOR HOLES

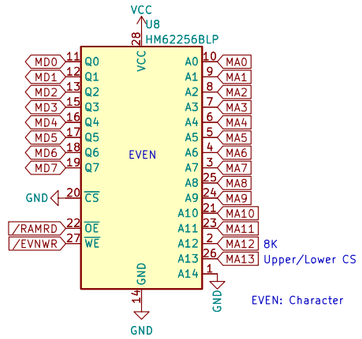
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

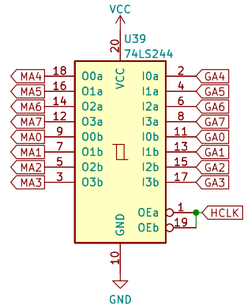
Sheet: /Power_Buss_IF/
File: pwr_S100buss.kicad_sch

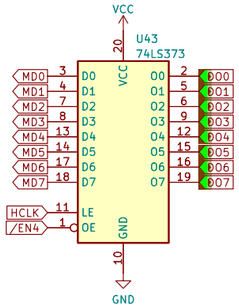
Title: Lomas Color Magic Redux

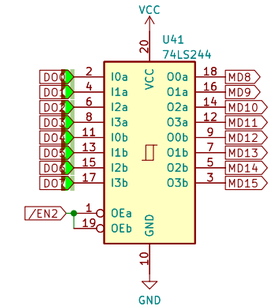
Size: B	Date: 2025-02-13	**Rev: 1.1-006**
KiCad E.D.A. kicad (6.0.11-0)		Id: 2/7

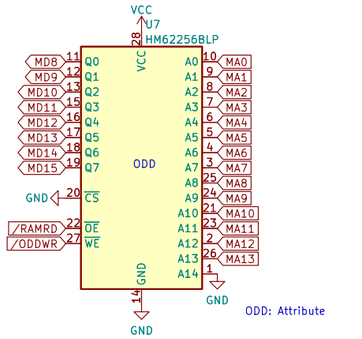


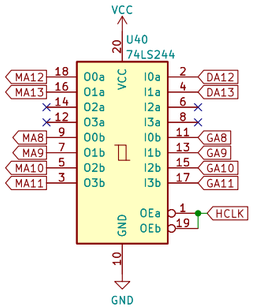


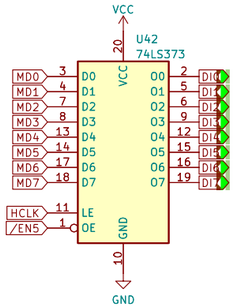


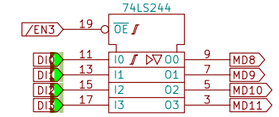


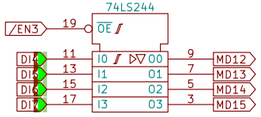




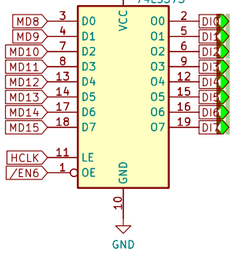


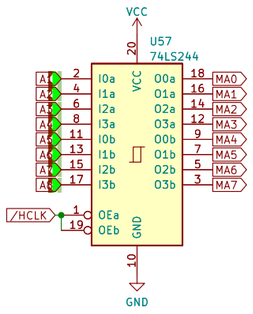


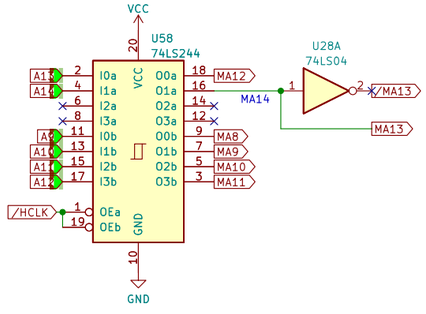




NOTE: Original used two stacked 6264 RAM chips in each location with MA13 connecting to /CS1 and /MA13 connecting to CS2. To select the chip, MA13 = L, driving /CS1 low. Gate 28A inverts MA13 to drive CS2 = H.







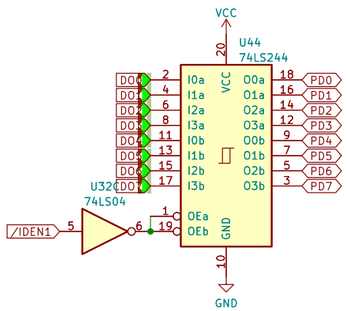
Redraw/modifications (c) Richard A. Cini

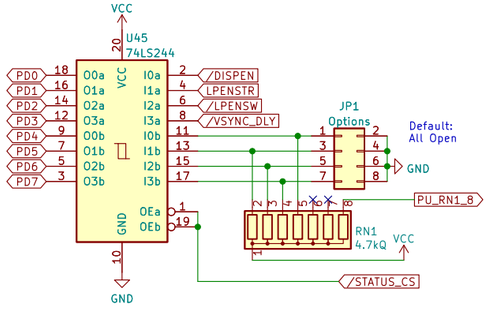
Lomas Data Produtcs

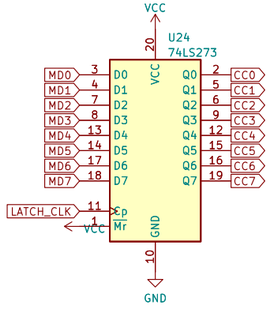
Sheet: /Buffers_Memory/
File: buffmem.kicad_sch

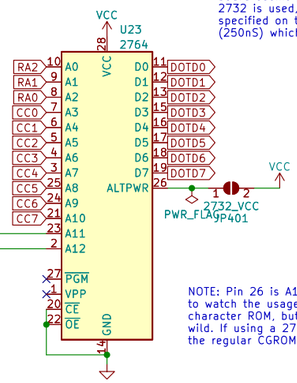
Title: Lomas Color Magic Redux

Size: B	Date: 2025-02-13	**Rev: 1.1-006**
KiCad E.D.A. kicad (6.0.11-0)		Id: 3/7

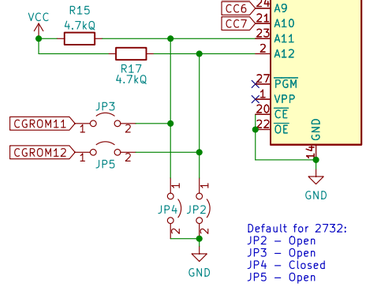






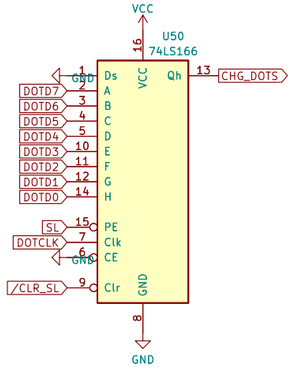


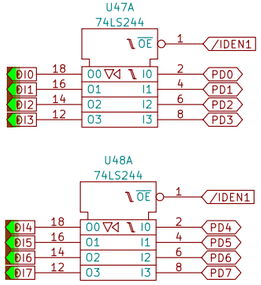
NOTE: The Color Magic uses an Intel D2732A (250nS). The board seems particularly sensitive to what brand/type of 2732 is used, likely due to the access time not being specified on the device. I used a Fujitsu MBM2732A-25 (250nS) which worked fine.

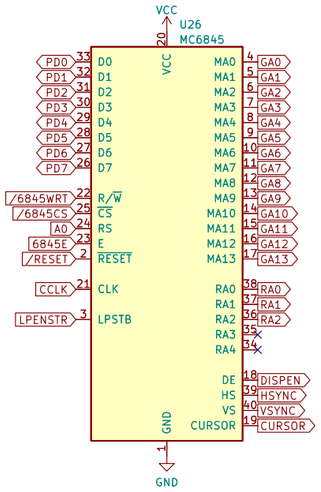


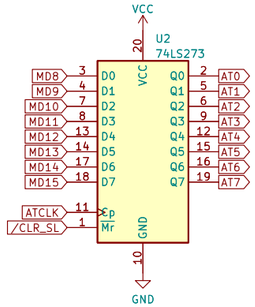
Default for 2732:
JP2 – Open
JP3 – Open
JP4 – Closed
JP5 – Open

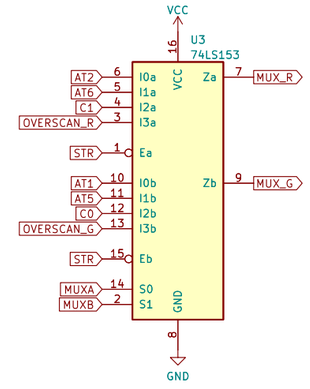
NOTE: Pin 26 is A13 on the 2764 so you neeed to watch the usage. There was a 2764-based character ROM, but I haven't seen it in the wild. If using a 2764 in place of a 2732 for the regular CGROM, special care is needed.

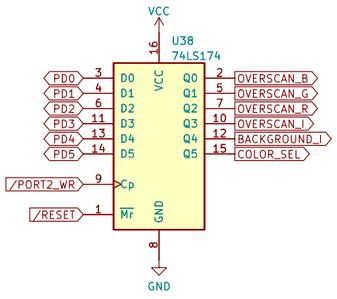


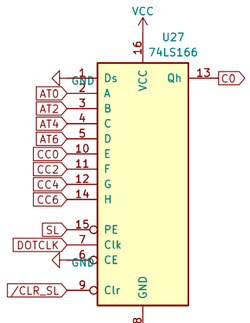


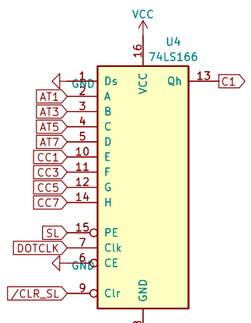


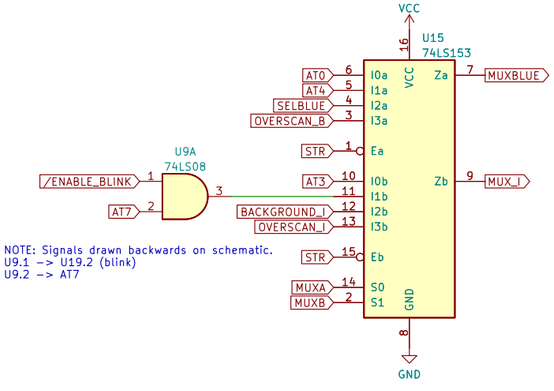




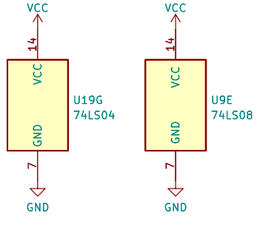


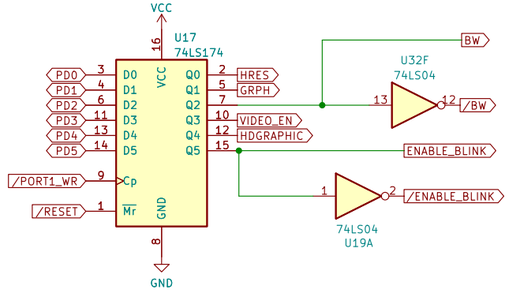






NOTE: Signals drawn backwards on schematic.
U9.1 -> U19.2 (blink)
U9.2 -> AT7





Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

Sheet: /Video Generator/		
File: vidgen.kicad_sch		
Title: Lomas Color Magic Redux		
Size: B	Date: 2025-02-13	**Rev: 1.1-006**
KiCad E.D.A. kicad (6.0.11-0)		Id: 4/7

U29
74LS174
U16
PAL20L10
U18
PAL16L8
U56
74LS688
U55
PAL20L10
U33D
74LS00
U19C
74LS04
U46
74ALS174
U32A
74LS04
U30C
74LS04
U32D
74LS04
U30A
74LS04
U54
74LS688
U61
PAL16L8
U52B
74LS14
U28D
74LS04
U66A
7406
JP15
Phantom
U62C
74LS14
U62E
74LS14
U62A
74LS14
JP6
Address
U52D
74LS14
JP9
HIADDR
RN2
4.7kQ
U62B
74LS14
JP12
ID
U33B
74LS00
U30B
74LS04
U52E
74LS14
JP8
CLK Polarity
U63A
74LS74
U62F
74LS14
JP7
Sync
U65A
74LS74
U66C
7406
U69D
74LS38
U65B
74LS74
U63B
74LS74
U30D
74LS04
U52A
74LS14
U30E
74LS04
U52C
74LS14
U9D
74LS08
U28E
74LS04
U28B
74LS04
U28F
74LS04
U66D
7406
U19B
74LS04
U66E
7406
U19E
74LS04
U66F
7406
U19F
74LS04
U63C
74LS74
U30G
74LS04
U28G
74LS04
U52G
74LS14
U33E
74LS00
U62G
74LS14
U32G
74LS04
U66G
7406
U65C
74LS74
U69E
74LS38
X1
14.31818MHz
TP1
TestPoint

Default: All Closed
0000-00xx-xxxx-xxxx
03xx

Board Select

Default (L->R)
0-0-0--1-0-1-1--1
------{-- B --}{8}
[0x0B800]

Default:
JP9: 1-2

Default:
JP8: 1-2

Default:
JP7: 2-3

Default:
JP15 - Open

TP4: On the prototype U65.4 is connected
to U64.10. TIE TO VCC.

TP3: On the prototype U63.4 is left floating.
In the IBM CGA adapter, it's tied to Vcc.

TIE TO VCC

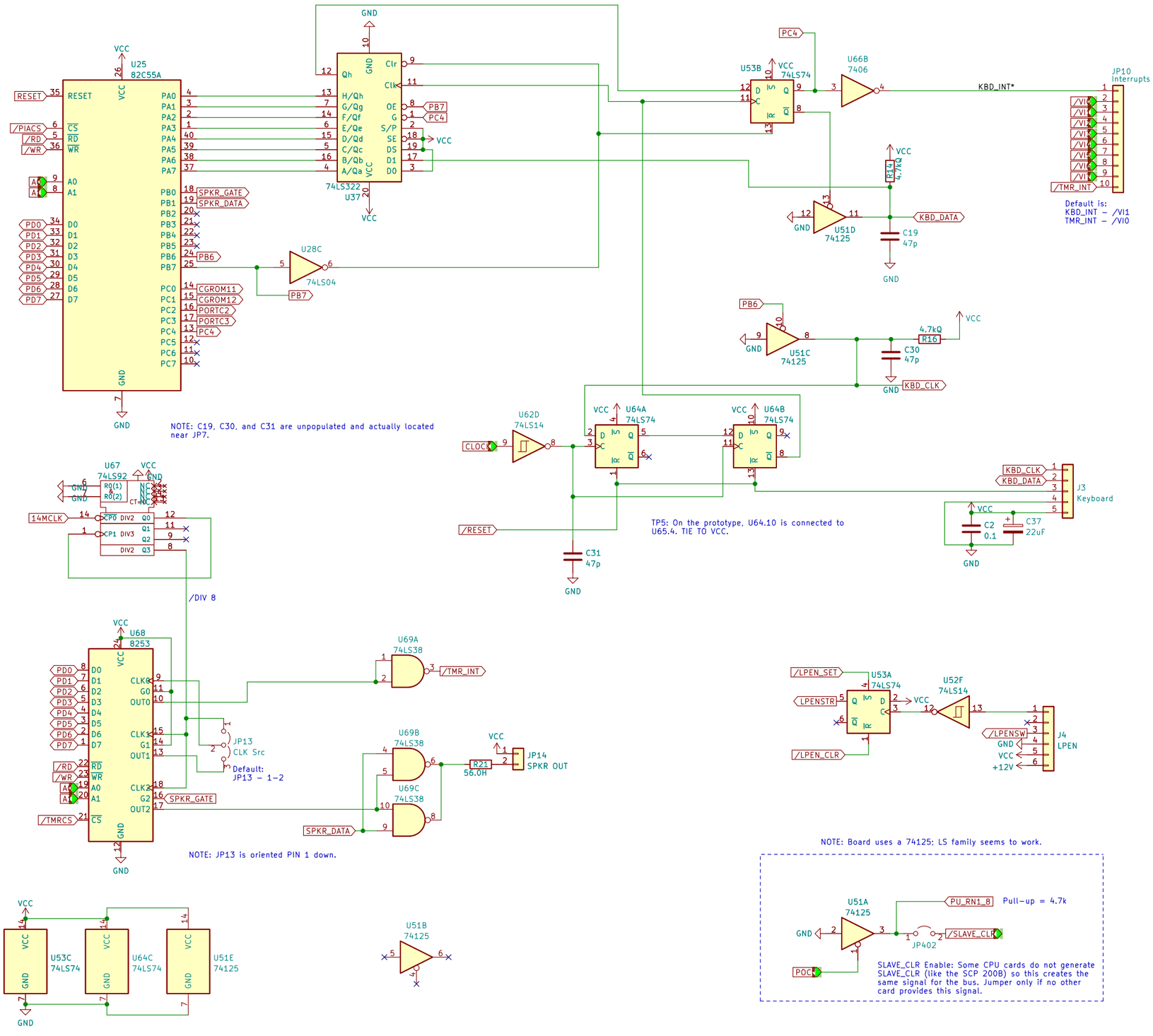
NOTE: The original circuit
consisted of a crystal-based
frequency generator using 3
gates from U28, a parallel
capacitor and two resistors.

NOTE: R7/R8 was specified as 1.0kQ on schematic but 470Q
was used in the actual manufacturing of the board. Prior
to converting to a TTL oscillator, 1.0kQ was determined to
work better. Also, install a jumper in place of C8. This
should result in a frequency of ~14.305MHz.

NOTE: Board uses 7406; LS family seems to work fine.

Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Clock_and_address/
File: clockaddr.kicad_sch
Title: Lomas Color Magic Redux
Size: B | Date: 2025-02-13 | **Rev: 1.1-006**
KiCad E.D.A. kicad (6.0.11-0) | Id: 5/7

U32E
74LS04
DISPEN
/DISPEN
U32B
74LS04
CURSOR
U34
74ALS174
HSYNC
VSYNC
/3.6MCLK
/HSYNC_DLY
/VSYNC_DLY
/DISPEN_DLY
/CURSOR_DLY
U9B
74LS08
/DISPEN_DLY
VIDEO_EN
/CLR_SL
74LS00
U33C
U1
PAL16L8
CHG_DOTS
/CURSOR_DLY
ENABLE_BLINK
AT7
BLINK
CURSOR_BLINK
GA12
GA13
RA0
RA1
DA13
PORTC3
PORTC2
GRPH
DA12
ALPHA_DOTS
U5
74LS273
MUX_I
MUX_R
MUX_G
MUXBLUE
LATCH_CLK
LC1
LC2
/SLAVE_CLR
14MCLK
ATCLK
NEW_RESET
I
R
G
B
U11
74LS244
HSYNC_OUT
VSYNC_OUT
I_OUT
R_OUT
G_OUT
B_OUT
B_HSYNC_OUT
B_VSYNC_OUT
R2
R3
0k
NOTE: R2/3/4 unpopulated.
B&W Composite
J1
CGA Out
GND
I_OUT
R_OUT
G_OUT
B_OUT
B_HSYNC_OUT
B_VSYNC_OUT
U35
74LS164
/HSYNC_DLY
MR
DSA
DSB
CP
U35.12
U35.13
U21C
74LS86
HSYNC_OUT
U21B
74LS86
U19D
74LS04
COMPOSITE_SYNC
U10
74LS367
R
COLOR_COMPOSITE
I
COMPOSITE_SYNC
/BLANK
R4
R5
R6
R1
R9
0k
2.2kΩ
5.6kΩ
1.0kΩ
5.6kΩ
Q1
2N3904
22Ω
R10
J2
RCJ-014
100Ω
R11
U20
74LS175
HSYNC_OUT
/VSYNC_DLY
U9C
74LS08
VSYNC_OUT
U6B
74LS393
/VSYNC_DLY
CURSOR_BLINK
U6A
74LS393
BLINK
TP2: Pin 4 is misdrawn on the LDP schematics –
it is shown as pin 10 and connects to /BW. The
IBM CGA card also has it connected to /BW.
TIE TO /BW.
/BW
U36A
74LS74
U35.13
LCLK
/HSYNC_DLY
U31A
74LS32
U22B
74LS02
/VSYNC_DLY
U21D
74LS86
U21A
74LS86
U30F
74LS04
U36B
74LS74
3.58MHZ
14MCLK
U13B
74LS74
U13A
74LS74
U12
74LS151
BLUE
GREEN
CYAN
RED
MAGENTA
YELLOW_BURST
S0
S1
S2
U6C
74LS393
U36C
74LS74
U21E
74LS86
U31E
74LS32
U22E
74LS02
U13C
74LS74
U22A
74LS02
U22C
74LS02
U22D
74LS02
U31B
74LS32
U31C
74LS32
U31D
74LS32
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Video Timing/
File: timing.kicad_sch
Title: Lomas Color Magic Redux
Size: B | Date: 2025-02-13 | **Rev: 1.1-006**
KiCad E.D.A. kicad (6.0.11-0) | Id: 6/7



Redraw/modifications (c) Richard A. Cini

Lomas Data Produtcs

Sheet: /IO Chips/

File: inout.kicad_sch

Title: Lomas Color Magic Redux

Size: B	Date: 2025–02–13	**Rev: 1.1–006**
KiCad E.D.A. kicad (6.0.11–0)		Id: 7/7