

	1	2	3	4	5	
A	<div>Power_Buss_IF</div> <div></div> <div>File: pwr_S100buss.kicad_sch</div>	<div>Buffers_Memory</div> <div></div> <div>File: buffmem.kicad_sch</div>	<div>Video Generator</div> <div></div> <div>File: vidgen.kicad_sch</div>	<div>Clock_and_address</div> <div></div> <div>File: clockaddr.kicad_sch</div>	<div>Video Timing</div> <div></div> <div>File: timing.kicad_sch</div>	A
B	<div>IO Chips</div> <div></div> <div>File: inout.kicad_sch</div>	<div>NOTE:</div> <div>The board has a number of drill-outs and jumpers on the back of the board but there are no known ECO documents to support this. When looking at the changes, they match the connections on the published schematic. So, I'm guessing that these were merely changes to fix defective boards from the board shop rather than true ECOs.</div> <div>There are 9 jumpers and several drill-outs, with the jumpers easier to document:</div> <div>Jumpers</div> <div>=====</div> <div>1. U23 (EPROM): ties socket pin 28 to socket pin 26, Vcc for 2764.</div> <div>2. U65.13 to U66.5 } PRDY flip-flop control</div> <div>3. U65.5 to U63.13 }</div> <div>4. U46.2 to U16.1 (C7) (was inverted)</div> <div>5. U3.4 to U4.13 (C1) (swaps C0 and C1)</div> <div>6. U3.12 to U27.13 (C0)</div> <div>7. U25.13 to U53.9 (Keyboard INT out)</div> <div>8. U5.19 - U52.3 } Connects SLAVE_CLR to internal RESET circuit.</div> <div>9. U5.18 to bus [54] }</div> <div>Drill-outs</div> <div>=====</div> <div>1. U64.5 x U65.4</div> <div>2. U63.4 x U63.13</div> <div>3. U63.13 x Vcc</div> <div>4. U32.1 x from whatever U46.2 went to.</div> <div>5. [54] from wherever U5.19 went to.</div> <div>6. U3.4 x U3.12</div> <div>7. U3.12 x U4.13 (?)</div>			<div>NOTE 2:</div> <div>After using an automated BOM analysis and comparing to the actual board, there are four connections on three chips that do not match the schematic. All are drawn connecting to VCC yet they are open connections on the board.</div> <div>U63.4</div> <div>U64.4 and U64.10</div> <div>U65.4</div> <div>U64.10 and U65.4 are connected together.</div> <div>These are drawn with tie points to help with further analysis, which shows all of them can be safely tied to Vcc.</div>	B
C	<div>ERRATA from 1.0 to 1.1-002:</div> <div>00. v1.0 of board was trashed.</div> <div>01. Resistor footprints are one size too small -- 1/4w uses 1/8w, etc. Due to space limitations, left at 1/8w.</div> <div>02. U49/78L12 silkscreen is backwards. Corrected.</div> <div>03. Several chips have unconnected VCC or GND leads that might be from the use of ONE and ZERO. Corrected.</div> <div>ERRATA from 1.1-002 to 1.1-003</div> <div>v.003 was never manufactured.</div> <div>ERRATA from 1.1-003 to 1.1-004</div> <div>01. J6 (address select) is flipped. Rotated 180.</div> <div>02. Design relies on SLAVE_CLR [54] for reset, but not all boards (like the SCP 200B) generate that signal. Reused spare gate of the LS125 and added a jumper and pull-up to generate that signal driven by POC [99].</div> <div>03. Changed memory chip wiring to be similar to the original, using MA13 as the CS* and grounding A13 and A14 of the 62256 (thus making it a 6264 albeit with only one chip select).</div> <div>04. Discovered that A6 is connected twice on U55. Changed second to A5.</div> <div>The 1.1-004 version works.</div> <div>Final Version 1.1.005</div> <div>01. Removed tie points TP2-TP5 and permanently connected the pins to their respective endpoints.</div>					C
D	<div>Drafting Notes:</div> <div>1. Green tags on signal flags denote S100 signal.</div> <div>Redraw/modifications (c) Richard A. Cini</div> <div>Lomas Data Productcs</div> <div>Sheet: /</div> <div>File: s100_ColorMagic-1.1-005.kicad_sch</div> <div>Title: Lomas Color Magic Redux</div> <div>Size: USLetter Date: 2024-09-24</div> <div>KiCad E.D.A. kicad (6.0.11-0)</div> <div>Rev: 1.1-005</div> <div>Id: 1/7</div>					D
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