

Power_Buss_IF

File: pwr_S100buss.kicad_sch

SCSI Interface

File: sch_pg1.kicad_sch

Serial Ports

File: sch_pg2.kicad_sch

IO_Timer_RTC

File: sch_pg3.kicad_sch

S100 Bus Interface

File: sch_pg4.kicad_sch

General Notes:

01.

Design Changes:

01.

ECOs on the original board:

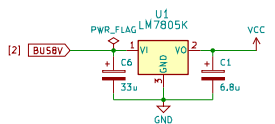
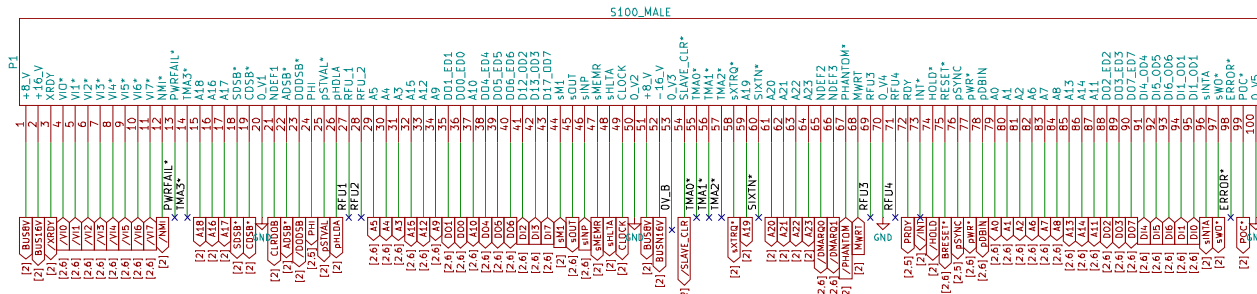
NOTES/ERRATA from 1.0-001 to 1.0-002:
01. Alternative memory arrangement using high-density
SRAM like the AS6C4008 512kx8-55 configured as
2x128k.

Schematic page 1
Redraw/modifications (c) Richard A. Cini
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Sheet: /
File: s100_LomasSCSI-1.0-001.kicad_sch

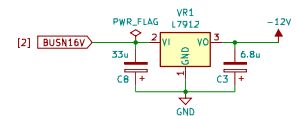
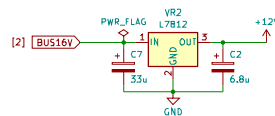
Title: Lomas SCSI

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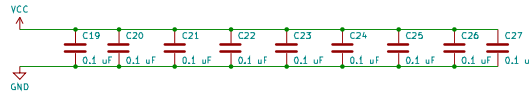
Rev: 1.0-001
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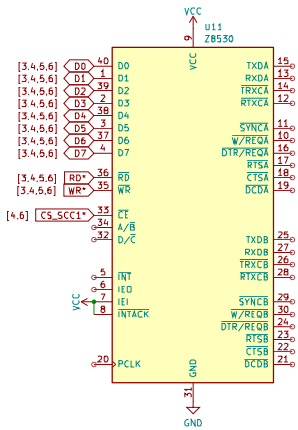


NOTE: Original board used an adjustable regulator for the 5v rather than fixed.

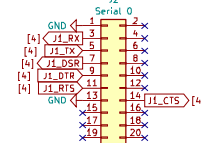
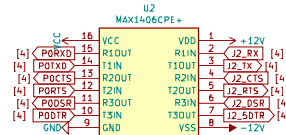


CARD EJECTOR HOLES

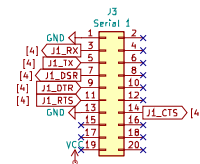
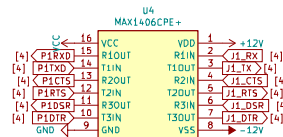




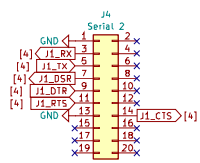
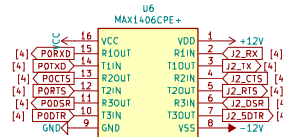
PORT 0



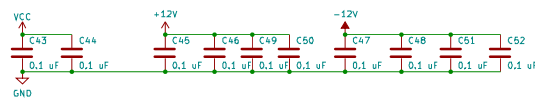
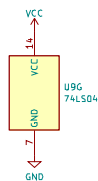
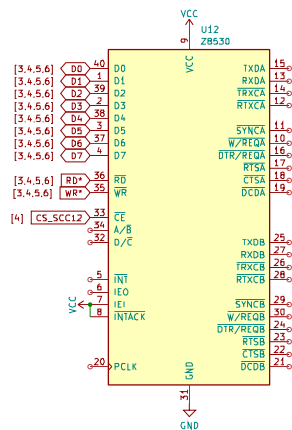
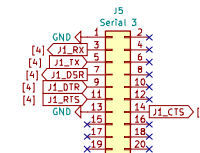
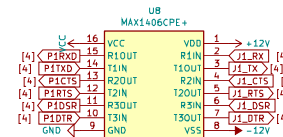
PORT 1



PORT 2



PORT 3



Schematic page 2
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Size: B Date: 2024-12-16 Rev: 1.0-001
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