Power_Buss_IF

File: pwr_S100buss.kicad_sch

CPU_ROM_Serial

File: sch_pg1.kicad_sch

Floppy_Parallel_IF

File: sch_pg2.kicad_sch

Memory

File: sch_pg3.kicad_sch

S100 Bus Interface

File: sch_pg4.kicad_sch

General Notes:

01. The CPU must be an original 80186. The "C" or "XL" suffix chips require different configuration register settings to be compatible and to have the right UCS/LCS configuration.
02. Notwithstanding the dual footprint for the TMS4500/TMS4501, (which would accommodate higher density RAM), the board cannot use more than 256k on-board due to the LCS* chip select.

NOTES/ERRATA from 1.0-001 to 1.0-002:
01. Alternative memory arrangement using high-denisity SRAM like the AS6C4008 512kx8-55 configured as 2x128k.

NOTES/ERRATA from 1.0-002 to 1.0-003:
01. Changed serial level shifters to higher-density versions; changed serial port headers to accommodate PC motherboard DE9 dongles.

Design Changes:

01. 16MHz crystal replaced by TTL oscillator.
02. Adjustible voltage regulators replaced with either a switching regulator (5V) or small linear regulators (which are only used for serial level shifters).
03. Entire DRAM section removed (saves 40 chips) in favor of high-density 55ns SRAM.
04. MC1488/1489 level shifters replaced with higher-density MAX1406 shifters. J1/J2 changed to modern IBM-PC style motherboard headers.
05. CPU package changed from LCC to PLCC which are easier to find.
06. Prototype had four RPACKs (1k x2 and 4.7k x2) of which only two were partially used. Pull-up resistors were specified in other parts of the circuit but not used on the prototype. These have been included mut may not need to be populated.

ECOs on the original board:

There are 4 changes on the back of the board:

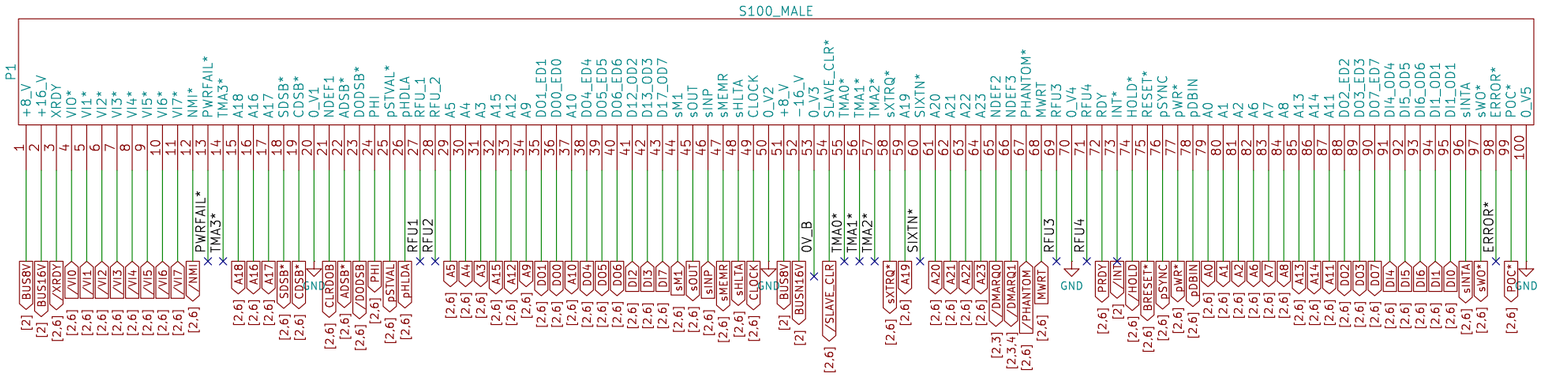
01. Added 1k pull-up from RN2.2 to U32.1 (pull-up on the RD_DATA* signal from the floppy).
02. U45.2 disconnected from U45.4 and connected to U45.1 and .13 (correct on schematic). U45.4 and U45.10 NOT connected to VCC.
03. U59 inverter added to U32.7 (correct on schematic).
04. Added jumper J9 to allow connecting U44.40 and U44.41 to VCC.

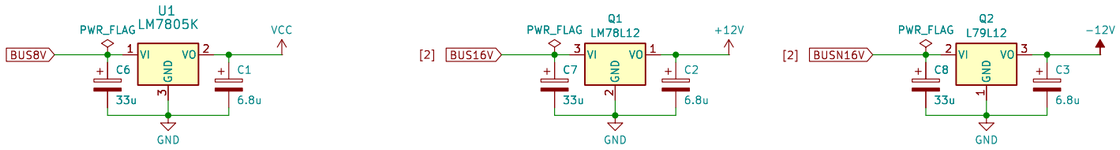
Schematic page 1
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

Sheet: /
File: s100_Thunder186-1.0-003.kicad_sch

Title: Lomas Thunder 186

Size: USLetter	Date: 2024-10-17	**Rev: 1.0-003**
KiCad E.D.A. 8.0.5		Id: 1/6



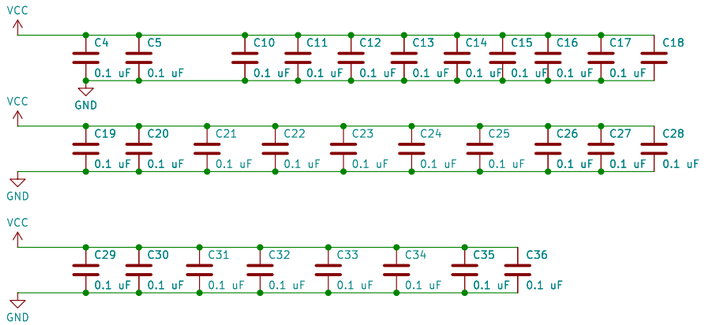


NOTE: Original board used adjustible regulators rather than fixed.

CARD EJECTOR HOLES

H1

H2

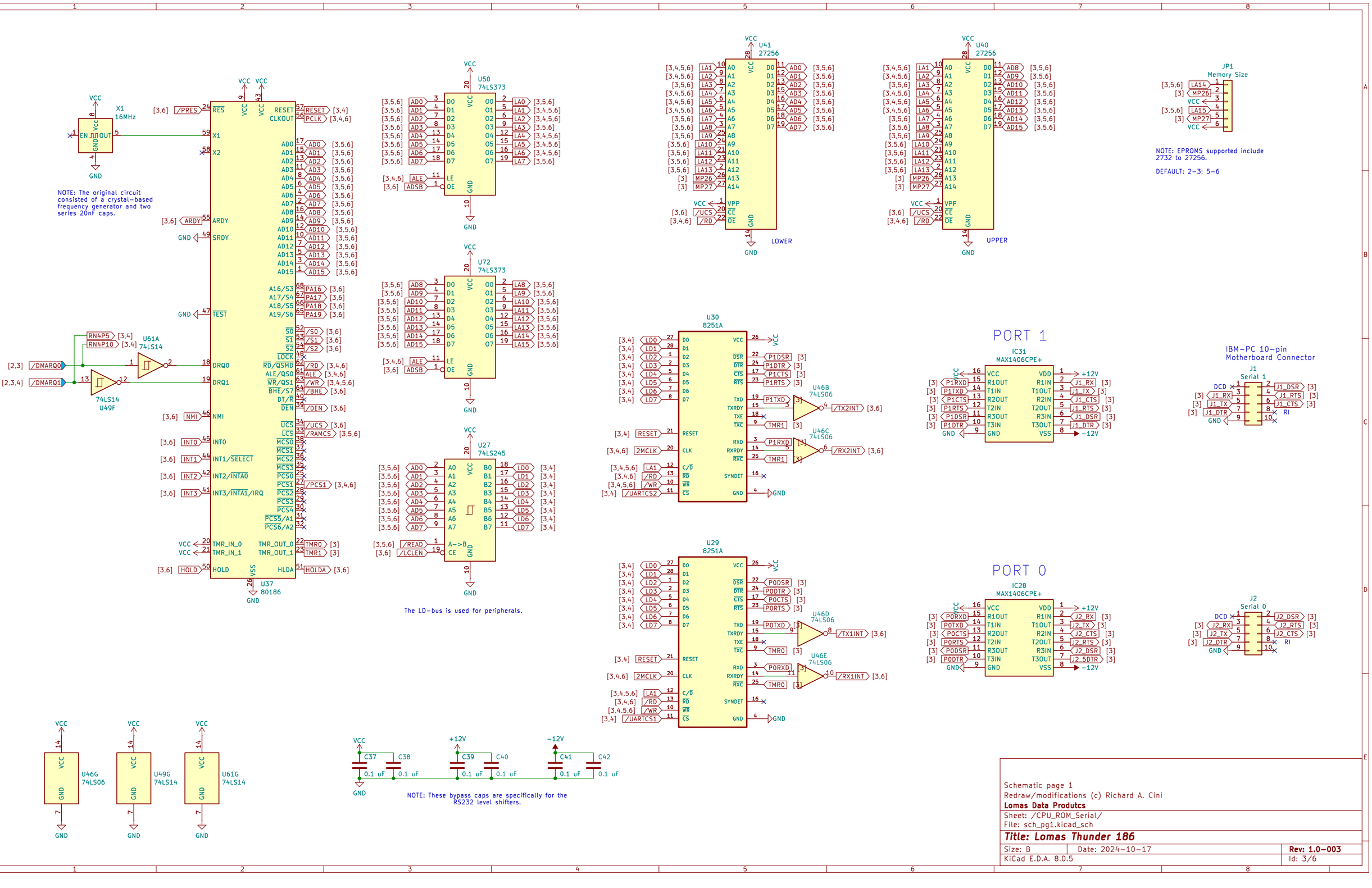


Schematic page 2
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

Sheet: /Power_Buss_IF/
File: pwr_S100buss.kicad_sch

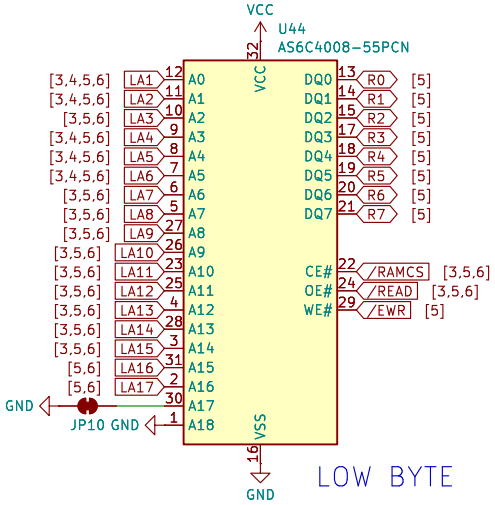
Title: Lomas Thunder 186

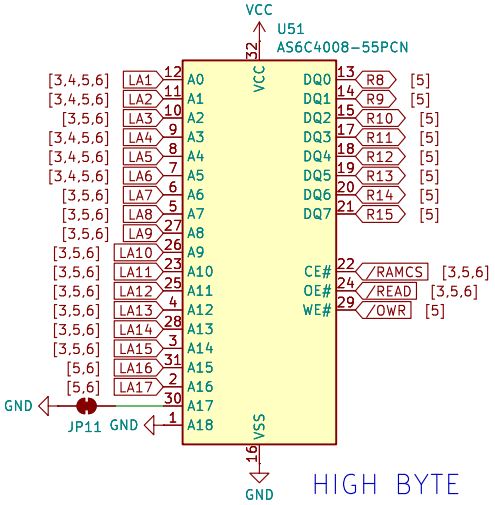
Size: B	Date: 2024-10-17	**Rev: 1.0-003**
KiCad E.D.A. 8.0.5		Id: 2/6

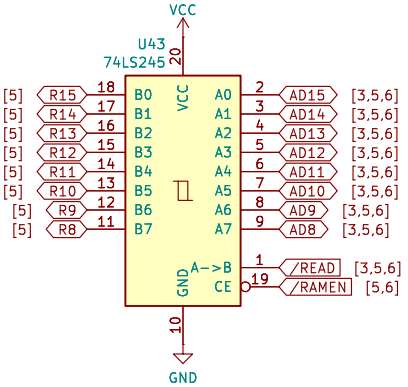

X1
16MHz
VCC
GND
NOTE: The original circuit consisted of a crystal-based frequency generator and two series 20nF caps.
U37
80186
RES
CLKOUT
X1
X2
ARDY
SRDY
TEST
NMI
INTO
INT1/SELECT
INT2/INTAO
INT3/INTA1/IRQ
TMR_IN_0
TMR_IN_1
HOLD
HLDA
TMR_OUT_0
TMR_OUT_1
VSS
AD0 [3,5,6]
AD1 [3,5,6]
AD2 [3,5,6]
AD3 [3,5,6]
AD4 [3,5,6]
AD5 [3,5,6]
AD6 [3,5,6]
AD7 [3,5,6]
AD8 [3,5,6]
AD9 [3,5,6]
AD10 [3,5,6]
AD11 [3,5,6]
AD12 [3,5,6]
AD13 [3,5,6]
AD14 [3,5,6]
AD15 [3,5,6]
/PRES [3,6]
RESET [3,4]
PCLK [3,4,6]
A16/S3 PA16 [3,6]
A17/S4 PA17 [3,6]
A18/S5 PA18 [3,6]
A19/S6 PA19 [3,6]
/S0 [3,6]
/S1 [3,6]
/S2 [3,6]
LOCK
RD/QSMD /RD [3,4,6]
ALE/QS0 ALE [3,4,6]
WR/QS1 /WR [3,4,5,6]
BHE/S7 /BHE [3,6]
DT/R
DEN /DEN [3,6]
UCS /UCS [3,6]
LCS /RAMCS [3,5,6]
MCS0
MCS1
MCS2
MCS3
PCS0
PCS1 /PCS1 [3,4,6]
PCS2
PCS3
PCS4
PCS5/A1
PCS6/A2
ARDY [3,6]
HOLD [3,6]
HLDA /HOLDA [3,6]
TMR0 [3]
TMR1 [3]
U61A
74LS14
RN4P5 [3,4]
RN4P10 [3,4]
/DMARQ0 [2,3]
/DMARQ1 [2,3,4]
DRQ0
DRQ1
74LS14
U49F
U50
74LS373
U72
74LS373
U27
74LS245
/READ
/LCLEN
A->B
The LD-bus is used for peripherals.
U41
27256
LOWER
U40
27256
UPPER
/UCS
/RD
JP1
Memory Size
NOTE: EPROMS supported include 2732 to 27256.
DEFAULT: 2-3; 5-6
U30
8251A
LD0 [3,4]
LD1 [3,4]
LD2 [3,4]
LD3 [3,4]
LD4 [3,4]
LD5 [3,4]
LD6 [3,4]
LD7 [3,4]
RESET [3,4]
2MCLK [3,4,6]
/RD [3,4,6]
/WR [3,4,5,6]
/UARTCS2 [3,4]
C/D
SYNDET
TXD
TXRDY
TXE
TXC
RXD
RXRDY
RXC
P1DSR [3]
P1DTR [3]
P1CTS [3]
P1RTS [3]
TMR1 [3]
P1RXD [3]
U46B
74LS06
/TX2INT [3,6]
/RX2INT [3,6]
U46C
74LS06
PORT 1
IC31
MAX1406CPE+
VCC
VDD +12V
R1IN J1_RX [3]
R1OUT
T1IN
T1OUT J1_TX [3]
R2OUT
R2IN J1_CTS [3]
T2IN
T2OUT J1_RTS [3]
R3OUT
R3IN J1_DSR [3]
T3IN
T3OUT J1_DTR [3]
GND
VSS -12V
P1RXD [3]
P1TXD [3]
P1CTS [3]
P1RTS [3]
P1DSR [3]
P1DTR [3]
IBM-PC 10-pin
Motherboard Connector
J1
Serial 1
DCD
RI
GND
J1_RX [3]
J1_TX [3]
J1_DTR [3]
J1_DSR [3]
J1_RTS [3]
J1_CTS [3]
U29
8251A
PODSR [3]
PODTR [3]
POCTS [3]
PORTS [3]
POTXD [3]
PORXD [3]
U46D
74LS06
U46E
74LS06
/TX1INT [3,6]
/RX1INT [3,6]
PORT 0
IC28
MAX1406CPE+
P0RXD [3]
P0TXD [3]
P0CTS [3]
PORTS [3]
P0DSR [3]
P0DTR [3]
J2_RX [3]
J2_TX [3]
J2_CTS [3]
J2_RTS [3]
J2_DSR [3]
J2_5DTR [3]
J2
Serial 0
U46G
74LS06
U49G
74LS14
U61G
74LS14
C37 0.1 uF
C38 0.1 uF
C39 0.1 uF
C40 0.1 uF
C41 0.1 uF
C42 0.1 uF
+12V
-12V
NOTE: These bypass caps are specifically for the RS232 level shifters.
Schematic page 1
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /CPU_ROM_Serial/
File: sch_pg1.kicad_sch
Title: Lomas Thunder 186
Size: B
Date: 2024-10-17
Rev: 1.0-003
KiCad E.D.A. 8.0.5
Id: 3/6

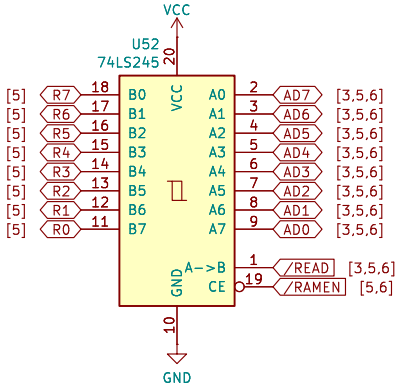
U5
82C55A
RESET
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
CS
RD
WR
A0
A1
D0
D1
D2
D3
D4
D5
D6
D7
VCC
GND
[3,4] RESET
[4] /PARRCS
[3,4,6] /RD
[3,4,5,6] /WR
[3,4,5,6] LA1
[3,4,5,6] LA2
[3,4] LD0
[3,4] LD1
[3,4] LD2
[3,4] LD3
[3,4] LD4
[3,4] LD5
[3,4] LD6
[3,4] LD7
[4] PA0
[4] PA1
[4] PA2
[4] PA3
[4] PA4
[4] PA5
[4] PA6
[4] PA7
[4] PB4
[4] PB5
[4] PB6
[4] PB7
[4] PC0
[4] PC1
[4] PC2
[4] PC3
[4] PC4
[4] FDC_TC
[4] PC7
VCC
NOTE: RN3 is a 9-resistor pack.
RN3
4.7k
SW1
Settings
GND
DEFAULT: 1-1-1-0
(1=on; 0=off)
U33E
7406
/READY [4]
U3
74LS244
I0a
I1a
I2a
I3a
I0b
I1b
I2b
I3b
O0a
O1a
O2a
O3a
O0b
O1b
O2b
O3b
OEa
OEb
VCC
GND
[4] PA4
[4] PA5
[4] PA6
[4] PA7
[4] PA0
[4] PA1
[4] PA2
[4] PA3
[4] PD4
[4] PD5
[4] PD6
[4] PD7
[4] PD0
[4] PD1
[4] PD2
[4] PD3
NOTE: This is a 2x14 header on the prototype
with pins 1-2 NC and 25-26 clipped.
J3
PARALLEL
[4] /LP_STROBE
[4] PD0
[4] PD1
[4] PD2
[4] PD3
[4] PD4
[4] PD5
[4] PD6
[4] PD7
[4] LP_ACK
[4] LP_BUSY
[4] LP_PE
[4] LP_SLCT
[4] /LP_AUTOF
[4] LP_ERROR
[4] /LP_INIT
[4] /LP_SLCTIN
NOTE: This should work with a standard
motherboard LPT dongle.
GND
J5
FLOPPY50
[4] /RD_DATA
[4] /WR_DATA
[4] /TRK0
[4] /WRGATE
[4] /WR_DATA
[4] /STEP
[4] /DIRECTION
[4] /DS3
[4] /DS2
[4] /DS1
[4] /DS0
[4] /READY
[4] /MOTOR_ON
[4] /SIDE_SEL
[4] /TWOSIDE
[4] /FAULT
[4] /FAULT_RES
[4] /LOWCUR
GND
J4
FLOPPY34
[4] /READY
[4] /SIDE_SEL
[4] /RD_DATA
[4] /WR_PROT
[4] /TRK0
[4] /WRGATE
[4] /STEP
[4] /WR_DATA
[4] /DIRECTION
[4] /DS3
[4] /DS2
[4] /DS1
[4] /DS0
[4] /INDEX
[4] /DS3
[4] /TWOSIDE
GND
NOTE: RN1 is a 9-resistor pack but the schematic
specifies 150 ohm for these resistors. Mount RPAK
to be removable.
RN1
1.0k
/INDEX [4]
/WRGATE [4]
/SIDE_SEL [4]
/READY [4]
/TRK0 [4]
/TWOSIDE [4]
/WRITE_PROT [4]
/FAULT [4]
U49B
74LS14
U33B
7406
U33F
7406
U49A
74LS14
NOTE: This inverter is U59A on the schematic.
U35
74LS244
[4] PC0
[4] PC1
[4] PC2
[4] PC3
[4] LP_SLCT
[4] LP_BUSY
[4] LP_PE
[4] LP_ERROR
[4] /LP_STROBE
[4] /LP_AUTOF
[4] /LP_INIT
[4] /LP_SLCTIN
[4] PB4
[4] PB5
[4] PB6
[4] PB7
RN6
390
NOTE: These are discrete 390 ohm resistors.
LP_ACK [4]
U4
8272A
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
IDX
WE
HDSEL
RDY
WP/TS
FLT/TRK0
FR/STP
LCT/DIR
~RW/SEEK
DS0
DS1
HDL
Vco
PS0
PS1
RD_DATA
DW
WR_DATA
DACK
A0
RD
WR
CS
DRQ
INT
RESET
TC
MFM
CLK
WR_CLK
[3,4] LD0
[3,4] LD1
[3,4] LD2
[3,4] LD3
[3,4] LD4
[3,4] LD5
[3,4] LD6
[3,4] LD7
[4] WE
[4] FR_STP
[4] LCT_DIR
[4] /RW_SEEK
[4] DS0
[4] DS1
[4] /MOTOR_ON
[4] PS0
[4] PS1
[4] /RD_DATA
[4] /WR_DATA
[4] /FDCDMACS
[3,4,5,6] LA1
[3,4,6] /RD
[3,4,5,6] /WR
[4] /FDCCS
[4] DRQ0
[4] /FDCINT
[4] RESET
[4] FDC_TC
[4] MFM
[4] RN2_9
[4] CLK
[4] WCLK
[4] RN2_10
[4] /MFM
U57F
74LS04
74LS06
U46F
7406
U33A
U59F
74LS14
ECO on-board (added).
U2
74LS240
[4] /DIRECTION
[4] /STEP
[4] /FAULT_RES
[4] /LOWCUR
LCT_DIR [4]
FR_STP [4]
/TRK0 [4]
/TWOSIDE [4]
/WRITE_PROT [4]
/FAULT [4]
74LS04
U57E
/RW_SEEK [4]
/RD_DATA [4]
U32
FDC9216
SEPCLK
/SEPD
VDD
VSS
/DSKD
REFCLK
CD0
CD1
/CLK [4]
/MFM [4]
ECO on-board (added).
[4] RN2_3
U17
74LS156
[4] DS0
[4] DS1
/DS0 [4]
/DS1 [4]
/DS2 [4]
/DS3 [4]
U34
74LS138
A0
A1
A2
E3
E2
E1
O0
O1
O2
O3
O4
O5
O6
O7
[3,4,5,6] LA4
[3,4,5,6] LA5
[3,4,5,6] LA6
[4,5,6] /LBHE
[3,4,6] /PCS1
[3,4,6] ALE
/UARTCS2 [3,4]
/FDCCS [4]
/FDCDMACS [4]
/UARTCS1 [3,4]
/PARRCS [4]
U48A
74LS74
U63E
7406
/PRNTRINT [4,6]
[4] PC4
U45A
74LS74
U46A
74LS06
DRQ0 [4]
[2,3,4] /DMARQ1
TP1
TestPoint
ECO on-board (changed). Seems
to be unconnected.
RN2
1.0k
RN4
4.7k
[4] RN2_3
[4] RN2_9
[4] RN2_10
[4] RN4P2
[4] RN4P4
[4] RN4P5
[4] RN4P6
[4] RN4P7
[4] RN4P8
[4] RN4P9
[4] RN4P10
U57B
74LS04
U53B
74LS74
U56
74LS161
U55
74LS157
U54
74LS157
U53A
74LS74
U57A
74LS04
[3,4,6] PCLK
[4] 250khz
[3,4,6] 2MCLK
[4] PC7
[4] MFM
[4] CLK
[4] WCLK
U47
74LS175
U60
74LS153
U33C
7406
[4] WR_DATA
/WR_DATA [4]
[3,4,6] PCLK
125
250khz [4]
250
JP2
CLK Delay
DEFAULT: 1-2
[4] PS0
[4] PS1
[4] WE
U45C
74LS74
U48C
74LS74
U53C
74LS74
U63G
7406
U33G
7406
U57G
74LS04
U59G
74LS14
74LS14
U59A
Schematic page 2
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Floppy_Parallel_IF/
File: sch_pg2.kicad_sch
Title: Lomas Thunder 186
Size: C
Date: 2024-10-17
Rev: 1.0-003
KiCad E.D.A. 8.0.5
Id: 4/6

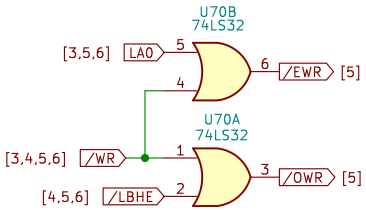
The DRAM subsystem was replaced with high-density Alliance AS6C4008-55LP which is 512kx8 and cheap/plentiful. The maximum on-board memory is 256k due to the chip select logic. Forcing A17 and A18 to GND makes the 512k byte device a 128k byte device. Bridged jumpers used in case it needs to be connected to LA18.

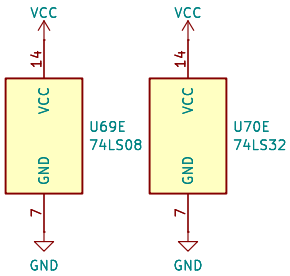


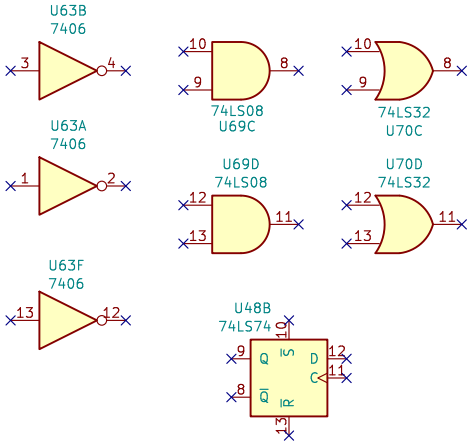










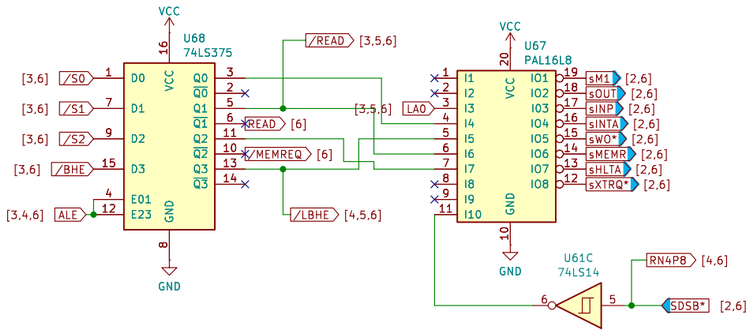


Schematic page 3
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs
Sheet: /Memory/
File: sch_pg3.kicad_sch

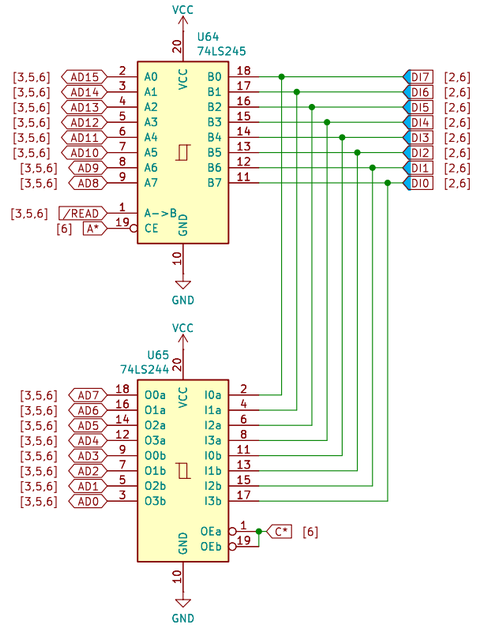
Title: Lomas Thunder 186

Size: A	Date: 2024-10-17	**Rev: 1.0-003**
KiCad E.D.A. 8.0.5		Id: 5/6

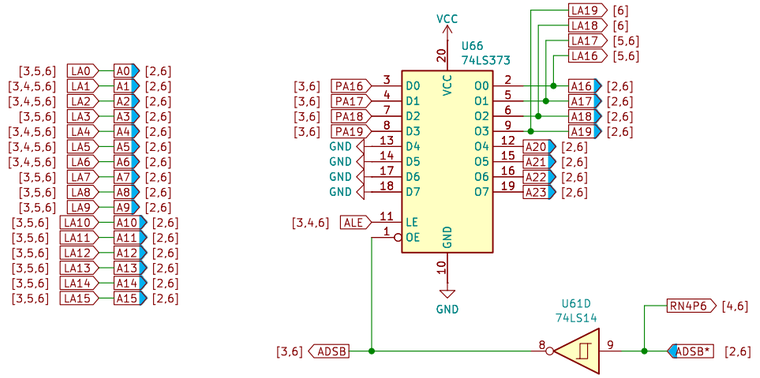
Buss Status Decode



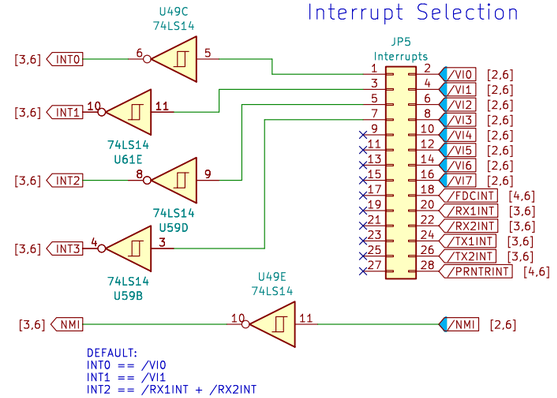
Data Buss Steering



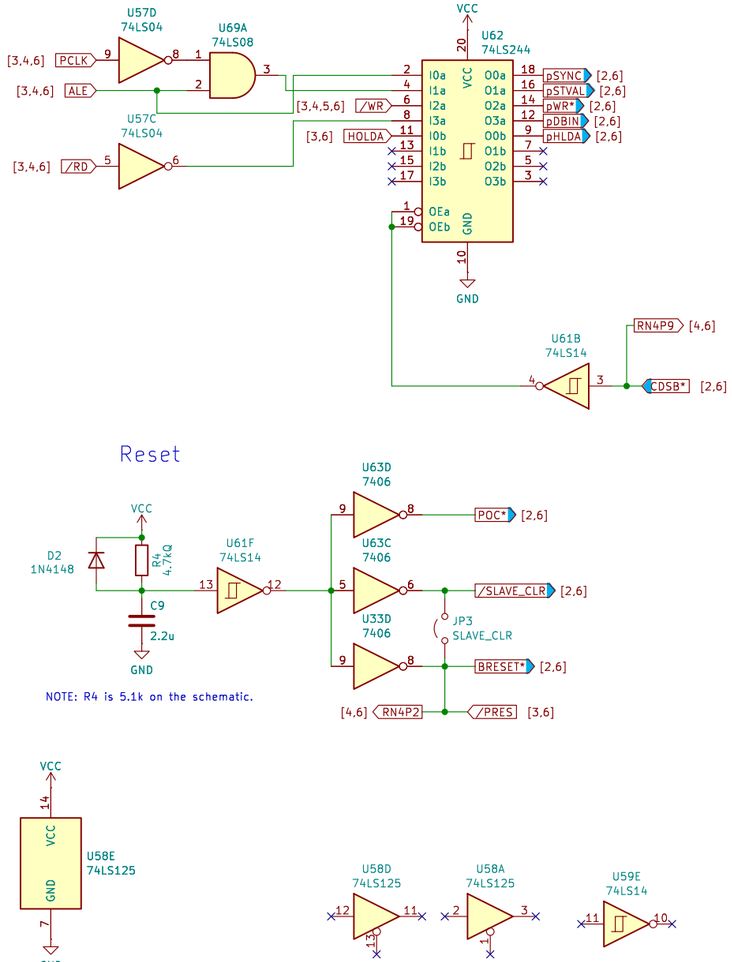
External Address Buss Interface

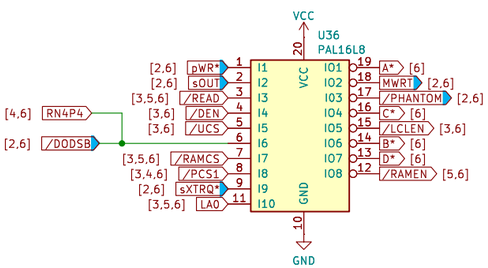


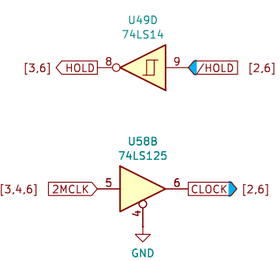
Interrupt Selection

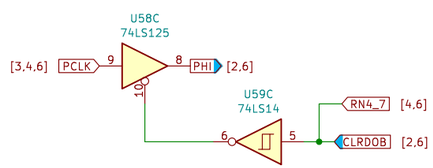


NOTE: Original J5 used two single-row headers but the spacing is off, making it hard to use standard jumpers. So, it was changed to a standard dual-row header which can be trimmed to fit.









Schematic page 4
Redraw/modifications (c) Richard A. Cini
Lomas Data Produtcs

Sheet: /S100 Bus Interface/
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Title: Lomas Thunder 186

Size: B	Date: 2024-10-17	**Rev: 1.0-003**
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