# ECE:3350 Spring 2019 -Computer Architecture and Organization Simple Instruction Set Computer (SISC) Project

#### Part 4: Due Monday, April 29, @ 8:30 am

This part of the project worth 66 points. You are to implement the LDP, LDR, STP, and STR instructions. Note that the new instructions effectively allow for auto-increment and decrement load and store instructions.

### You are given:

• Your own solution to Part 3. Again, you will not be able to succeed in Part 4 without first completing Part 3.

#### You are required to:

- Modify any of the project .v files as needed to implement the new instructions
- Write a testbench program in imem.data that tests <u>every</u> SISC-supported instruction and addressing mode (I recommend modifying the one provided with part 3). **Save this instruction memory file as all\_instr.data.** If there is an associated data memory file this program uses, save it as all\_data.data.
- Follow these guidelines while making your changes to the datapath: You may create any new control lines or modules you deem necessary.
  - O You may not remove any provided file but you may modify any file provided.
  - Your final solution must still correctly execute all of the previous instructions.
- Update the FSM state diagram and datapath diagram to reflect your modifications needed for the new instructions.
- Compress your project folder, along with the 'work' directory, the instruction memory files, the data memory files, updated state diagram, and all .v files into a .zip file named "Project p4.zip".

#### **Details/Notes:**

Like the SWAP instruction, the new LOAD instruction addressing modes will require that two values be written to the register file during instruction execution. Be careful with the timing!

# **Submission Overview:**

- Your .zip file should be named "Project\_p4.zip" and contain the following:
  - o All the .v and .data files
  - o The 'work' directory.
  - O Your updated FSM state diagram.
  - o An updated datapath diagram.

# **Rubric:**

FSM and Datapath Diagrams	10 pts
Load and Store Implementation	40 pts
Instr.data	16 pts

Total 66 pts