CSCI 113 (Intro. Computer Organization) Exam 2 Spring 2021

//submit photo files to jpark@csufresno.edu. //Write email subject as CS113-Exam2-yourName.

(40 pts.) 1. Computer arithmetic

(a) Draw a schematic diagram of 4-bit ALU for {and, or, add, sub, nor, slt, overflow_checking}.
In your diagram, please use a blank box for 1-bit ALU and show all input/output with name/value.

(b) Consider the 4-bit ALU in (a) and write control signals for ***nor*** operation and explain the reason.

(c) Draw the hardware components of Booth's multiplier with 4-bit data.

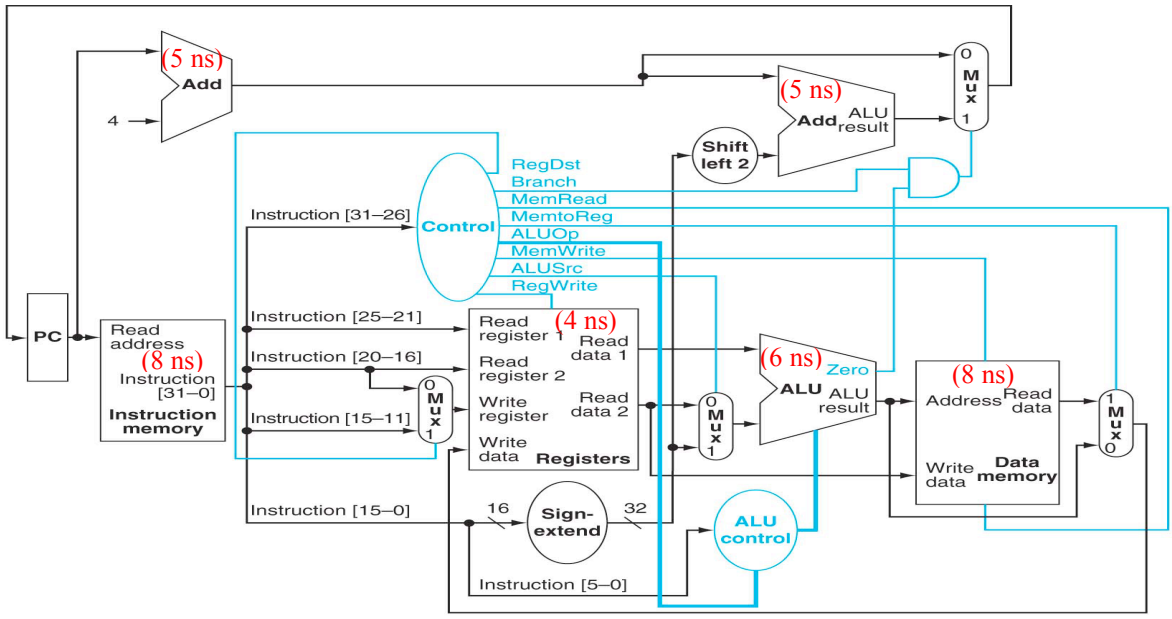
(d) Perform 4-bit Booth's multiplication for (-7*-5) and show registers' contents step by step for only the first 2 iterations.

(e) Perform 4-bit non-restoring division for (12/3) and show registers' contents step by step for only the first 2 iterations.

(25 pts.) 2. CPU – single-cycled implementation

(a) Compute the critical path time (in ns) for each of the following three instructions: ***lw***, ***sw***, ***beq***

(b) For ***lw*** instruction, show control signal values for: RegDst, ALUSrc, MemtoReg, RegWrite



(35 pts.) 3. CPU – multi-cycled implementation

(a) Consider the following instruction sequence to be executed and compute the speedup of the multi-cycled CPU (shown in the following diagram) over the single-cycled CPU (shown in the diagram in #2).
add $s5, $s2, $s4; **lw** $s2, 20($s1); **sw** $s3, 10($s1); **or** $s7, $s2, $s4; **beq** $s2, $s4, 100;

(b) Write the micro operations for the 2nd cycle of a ***beq*** instruction.

(c) Write the micro operations for the 3rd cycle of a ***lw*** instruction

(d) Show all control signal names and values used in the 5th cycle of a ***lw*** instruction execution.