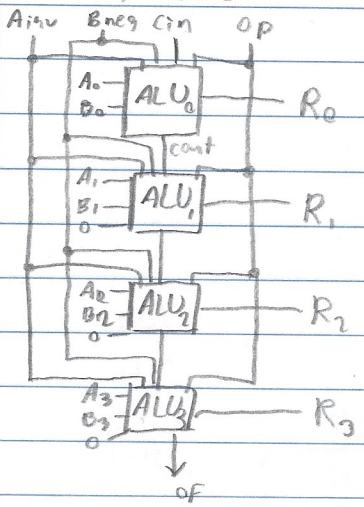
Carlo
Quitorio

CSCI 113 Midterm 2

1) 4 bit ALU



b) control signal for slt : 0111

get the correct data path

input for mux

e 0 ∅

10 AC ← AC + MD

01 AC ← AC − MD

11 ∅

c) Booth's multiplication

MD MQ

−5 * −7

0101 0111

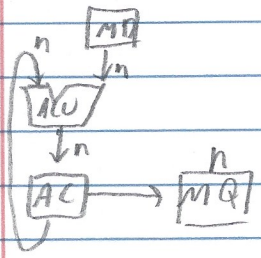
1010 1000

\+ 1 \+ 1

1011 1001

MD	AC	MQ	MQ-1	
1011	0000	1001	0	
	+1011			
	1011	1001	0	AC+MD
	1011	1100	1	>>
	+0101			
	0000	1100	1	AC−MD
	0000	0110	0	>>

d) Unsigned Hardware for division



e) 11/5 1011 ÷ 0101

MD MQ

non restore

if(AC<0)
  AC|MQ<<1
  AC ← AC+MD
else
  AC|MQ<<1
  AC ← AC-MD
if(AC<0)
  MQ=0
else
  MQ=1
if(AC<0)
  AC = AC+MD

MD	AC	MQ	
1011	0000	0101	
	0001	101	1st
	0101	101	
	0101	1011	
	1011	011	
	0110	011	2nd
	0110	0111	

1011
0100
+ 1
0101

2) Sub: don't worry about tap

6 + 3 + 5 + 3

9 + 8 = 17 ns

Lw: don't worry about tap

6 + 3 + 5 + 6 + 3

9 + 11 + 3

20 + 3 = 23 ns

beq: don't worry about tap

6 + 3 + 5

9 + 5 = 14 ns

b) Sub

Reg dest: 1

ALUSrc: 1

MemtoReg: 0

RegWrite: 1

3 a) compute speed up

Single cycle time: 23 ns

longest multi-cycle time is: 6ns

Sub: 4 clocks lw: 5 clocks OR: 4 clocks beq: 3 clocks

Speed up = $\frac{\text{single}}{\text{multi}}$ $\frac{23}{6*4}$ $\frac{23}{6*5}$ $\frac{23}{6*4}$ $\frac{23}{6*3}$

b) A <= Reg[IR[25:21]]

B <= Reg[IR[20:16]]

ALUOut <= PC + (sign extend [IR[15:0]] << 2)

c) beq

Reg dest: 1

ALU Src A: 1

ALU Src B: 0

d) sub

Mem to Reg: 1

Reg dest: 1

Reg Write: 1

e)