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1100
3210
8th=h

CSCI 113 Fall 2021 Final

1) M1: Rate = 500 MHz T=10 sec

M2: T=10 sec Speed up 2X clock rate = ? Clock cycle 2X fast

$$\text{Rate} = \frac{\#\text{times} \cdot 2(\text{clock rate})}{10} = \frac{2 \cdot 2(500\ \text{MHz})}{10} = \frac{2000\text{MHz}}{10} = 2000\ \text{MHz}$$

2) bne $s1, $s2, Label1;

I type op(6) rs(5) rt(5) offset(16)

	$s1	$s2	Label1
	5	17	18	0 0 0 1
000101	10001	10010	0 0 0 1
1	6	3	2	0 0 0 1

sll $s2, $s1, 4

R type op(6) rs(5) rt(5) rd(5) sft(5) func(6)

	0	0	17	18	4	
000000	00000	10001	10010	00100	000000
0	0	1	1	9	1	0	0

3) Booth's Multiplication

if MQ0/MQ-1 = 00 ∅

01 AC ← AC+MD

10 AC ← AC−MD

11 ∅

AC/MQ/MQ-1 >> 1

non restoring division

if (AC < 0)
  AC/MQ << 1
  AC ← AC + MD
else
  AC/MQ << 1
  AC ← AC - MD
if (AC < 0)
  MQ = 0
else
  MQ = 1
if (AC < 0)
  AC ← AC + MD

n

4. S_{ing}: 5ns Multi: 1 ns Pipeline: 1.2ns

Single cycle is slowest so all instructions take 5ns

6 instruc · 5 ns = **30 ns total**

Multi cycle

lw sll sw and beq j

5 + 4 + 4 + 4 + 3 + 3

5 + 12 + 6

5 + 18 = **23 ns**

Pipeline

depth = 5 + (IC - 1) · 1

5 + (6 - 1) · 1 = 10 clock cycles

$10\ cc \cdot \frac{1.2\ ns}{1\ cc} =$ **12 ns**

5. a) A, B, ALU_{out}, NPC

b) timing diagram

instruc	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
add $s3, $s1, $s2	IF	ID	EX	MEM	WB											
sub $s4, $s2, $s3		IF	ID	EX	MEM	WB										
and $s5, $s3, $s2			IF	ID	EX	MEM	WB									
lw $s6, 40($s3)				IF	ID	EX	MEM	WB								
add $s7, $s3, $s2					IF	ID	EX	MEM	WB							

11 execution cycles

6. a) increased block size pros: faster access time

cons: more misses & less hits

increased associativity pros: less misses & more hits

cons: slower access time

b) Write to memory directly, skip the cache and write to the memory for program to find it later.

Switch with value in the cache. Write the new value in the cache matching the tag, copy the old data and write to memory

7. 36 bit physical address direct map cache

256 KB data size

64 byte per block

36 bits

a	b	c (2 bits)

a+b+c = 34 bits

256 KB = 2^{18} bytes

64 bytes = 2^6 Byte

$\frac{\text{cache}}{\text{block}}$ = # of blocks → $\frac{2^{18}}{2^6} = 2^{12}$ blocks

B = 12 bits

22 bits left

$\frac{\text{block}}{\text{word}} = \frac{64B}{4B} = 16 = 2^4$ → C = 4 bits 22 − 4 = 18

A = 18 bits

b = $12 \cdot 2^{12}$ bytes

8. block size: 20 words
address transfer: 1 clock
DRAM access: 20 clocks
data transfer: 2 clocks

a) interleaved mem sys with 5 mem banks

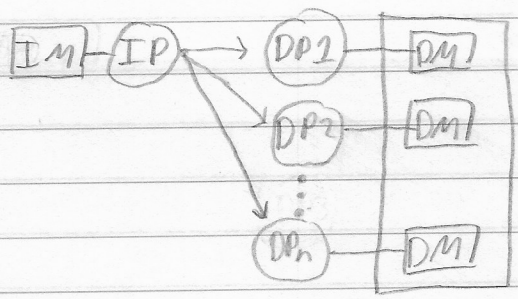
miss penalty = 1 + (20*5) + (20*2)
= 1 + 100 + 40
= 141 clock cycles

Bandwidth = $\frac{20 \cdot 5}{141}$ B/cycle

b) effective CPI = Ideal CPI + (Miss rate · miss penalty)
= 3 + (0.05 · 100) + ((0.4 · 0.10) · 100)
= 3 + 5 + (0.004 · 100)
= 8 + 0.4
= 8.4 CPI

0.04
x 0.10
000
+ 0040
0.0040

9. Shared Memory



b) Distributed memory is faster because it can divide tasks into pieces and run each thread/process on a processer.

distributed