	XOR TO
1	alzinget XOR
	A ADD
	B output
	b) $(A+B) \cdot (\overline{A} \cdot \overline{B}) = (A \cdot \overline{B}) + (\overline{A} \cdot B)$
<u> </u>	$((A+B)\cdot\overline{A})+(A+B)\cdot\overline{B})$
3	(A+B+A) + (A+B+B)
	(A · B) + (A · B)
	decoder Cin un Mux
	() ADID
	D) D) Ontput
	B-FI FI
	Cart
	23-8
	d) 109, 32 = 5 inputs 2"=16
	2-31

o.	7
to.	9
1.	6

Carto !

			C1 62		* * * * * * * * * * * * * * * * * * * *
2	C1: Rate = 500 M42	71: 20%	2 /		
	ez: Rate: 800 MHz	2 - 50%	ţ.		
		3: 30%		N -	
	a) CPU me, = IC * ((0.2 ×2) + (0,5 +	E11+10=+=11+	See 8	MC The Control of the	
7	= I(*(0,4+0.5+0.9).	19	37.10		
	§ KIC8	5 X 108			
			A	12.4 8x43	E. O. D.
	CPU = I(*((0,2 *1) +(0,5	*2) +(02 +4)	K super	1.8 5x108	times faster than C1
	= IC *(0,2+1+1,2)	2,4	1.6%	ZK10g	The CI
	8 Mg	8x108	19 11 11 11		
	b) MIPS C1 $\frac{510^8}{1.8 \times 10^6} = \frac{50}{1.8}$	0	rate 1 x106 = MIPS		
			1 XIG (17.6.)		
7	$C2 \frac{9x10^8}{24x10^6} = \frac{80}{2.0}$				
	Cr 24x16 = 2.1		•		
31	Rate 2 3 * ClockCycle,	South as			
	10 sec				
	Clock Cycle, = CPU Me, * Rate,				
	= 20 * 6x108				
	Rate = 3 * 20 × 6×10 = (	60×6×10			
	10	10			
4	7 124 29				
50	6 D3 4D		Long Marie		
	1	1 0			
			^		
400	- 10401/110				
	3 40 lwstr, 3(\$:	2 era) 1			
	128   t1=1A2830			P	
	0 1A 1t2-2B3C	4028			
Prof	1/1/				
	b) 5 accesses				

