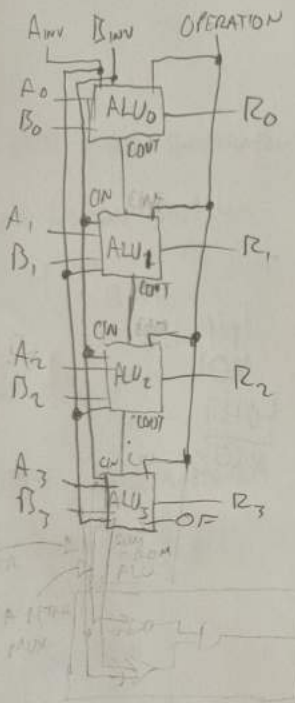
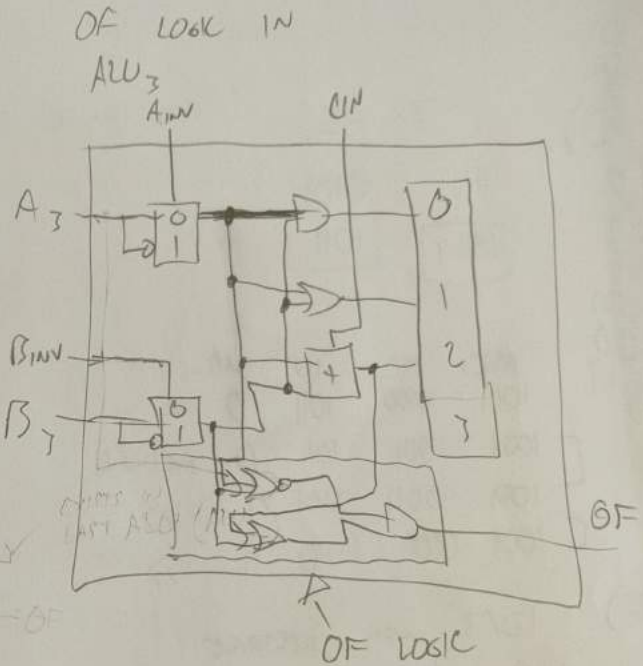
1)

A)





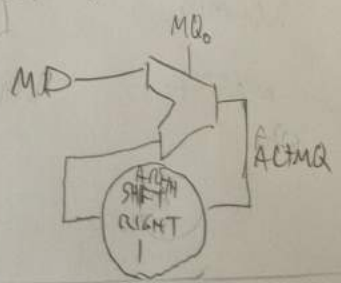
B) $NOR = \overline{(A+B)} = \bar{A} \cdot \bar{B}$

SIGNAL TO SELECT AND RESULT FROM MUX ← 11 00 ← CONTROL SIGNAL

B_{INV}, MUST INVERT B FOR OP

A_{INV}, MUST INVERT A FOR OP

C) DRAW BOOTH'S MULT HARDWARE



2)

A) LW

UPPER PATH OCCURS SIMULTANEOUSLY SO NO LOGIC

8ns + 4ns + 6ns + 8ns + 4ns

12+6

18+8

26+4ns

LW = 30ns

SW

UPPER PATH SIMULTANEOUSLY

8ns + 4ns + 6ns + 8ns

12ns + 6ns

18ns + 8ns

SW = 26ns

BEQ

UPPER PATH SIMULTANEOUS

8ns + 4ns + 6ns

12ns + 6ns

18ns

BEQ = 18ns

2B) LW

REG DEST = 0

ALU SRC = 1

MEM TO REG = 1

REG WRITE = 1

3A) LW IS LONGEST INST SO EACH INST TAKES 30ns

R-TYPE LW SW R-TYPE BEQ

MULTI CYCLED

LONGEST CYCLE IS 8ns SO 8ns PER CLOCK

ADD = 4 CLOCKS SO LW = 5 clocks SW = 4 clocks OR = 4 clocks BEQ = 3 clocks

8·4 = 32ns 8·5 = 40ns 8·4 = 32ns 8·4 = 32ns 8·3 = 24ns

SPEED UP ADD	SPEEDUP LW	SPEEDUP SW	SPEEDUP OR	SPEEDUP BEQ
30ns / 32ns	30ns / 40ns	30ns / 32ns	30ns / 32ns	30ns / 24ns

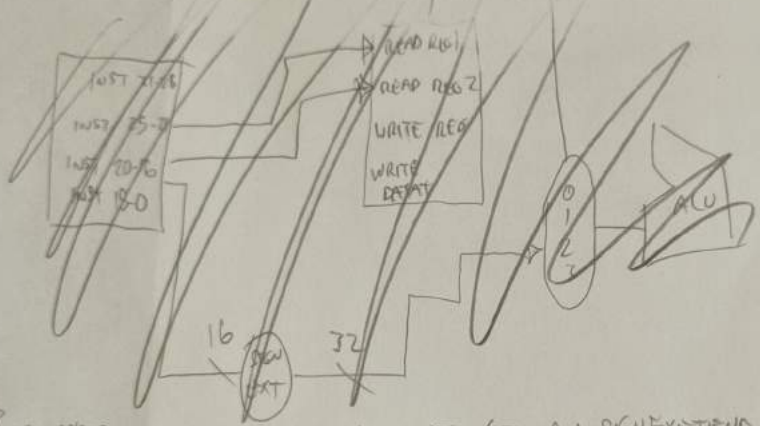
IN THIS INSTANCE THE SINGLE CYCLED CPU IS FASTER IN ALL INSTRUCTIONS EXCEPT FOR BEQ THAN THE MULTICYCLED CPU

3B) 2ND CYCLE OF BEQ

A <= REG [IR[25:21]]

B <= REG [IR[20:16]]

ALUOUT <= PC + (SIGN EXTEND (IR[15:0])) <<2)



3C) 3RD CYCLE OF LW = ALUOUT <= A + SIGNEXETEND (IR[15:0])

D) 5TH CYCLE OF LW CONTROL AND SIGNAL

REG WRITE = 1

MEM TO REG = 1

D) -7 · -5

0111 0101

1001 1011

1001
0110
0111

MD	AC	MQ	MQ-1	
1001	0000	1011	0	
1001	0111	1011	0	AC=MD
1001	0011	1101	1	>>>>
1001	0001	1110	1	>>

```
 111
 1101
+0111
-----
 0100
```

E) 12/3 NON RESTORE

1100 0011

1101

MD	AC	MQ		
0011	0000	1100		
0011	0001	1000	<<	
0011	1110	1000	AC=MD	
0011	1110	1000	MQ0=0	
0011	1101	0000	<<	
0011	0000	0000	AC+MD	
0011	0000	0001	MQ0=1	

```
  1
 0001
+1101
------
 1110
  111
 1101
+0011
------
 0000
```