CSCI 113 (Intro. Computer Organization) Exam 1 Spring 2021

//submit one email with photo files to jpark@csufresno.edu. //Write email title as CS113-Exam1-yourName.

(20pts)**1.** (a) Draw a schematic diagram of a 2x1 multiplexer using only basic gates (2 inputs each).
(b) What is the input width of the decoder used in a 16x1 multiplexer?
(c) Draw a schematic diagram of 1bit-ALU for {and, or, add, sub, nor, OF}. OF checking with cin/cout is not allowed.

(20pts)**2.** Consider the following instruction mix and CPI values for computers M1 (rate=600 MHz) and M2 (rate=500 MHz):
Type1 (30%): CPI_M1=2, CPI_M2 =2; Type2 (50%): CPI_M1=3, CPI_M2 =1; Type3 (20%): CPI_M1=1, CPI_M2 =4;
(a) Compute the CPU execution times of M1 and M2, and answer which computer is how much times faster than the other.
(b) Compute the MIPS rates of M1 and M2.

(10pts)**3.** Consider a computer M1(rate=600 MHz) on which a benchmark program execution takes 15 sec.
A design team is developing a new computer M2 aiming the triple performance (3 times faster) by increasing the clock rate with the cost of increased clock cycles with the factor of 2. What would be the clock rate of computer M2?

(15pts)**4.** MIPS ISA: Assume that data (23B4564D)hex and (B3C45D6E)hex are stored in memory at address 0 and 4, respectively.
Consider the following 3 consecutive instruction executions: lw $t1, 2($zero); sw $t1, 3($zero); lw $t2, 4($zero);
(a) Show the final contents of $t1 and $t2 in hex number.
(b) How many memory accesses are made?

(20pts) **5.** Consider the following MIPS assembly code segment for implementing a loop:

```
Label1: sll   $s1, $t1, 2;
        lw    $t0, 8($s1);
        bne   $s4, $t0, Label2;
        addi  $t1, $t1, 1;
        j     Label1;
Label2:
```

(a) What are addressing modes of the 2nd and the 3rd instructions?
(b) Write the MIPS machine code in hex number for the 1st instruction (sll…).
//use: opcode=0, function code=0, $s1(17), $t1(9)
(c) Write the MIPS machine code in hex number for the 3rd instruction (bne…).
//use: opcode=5, $t0(8), $s4(20)

(15pts) **6.** Consider the global pointer ($gp) value 10008000(hex).
(a) Write a MIPS assembly code for loading a word size data stored at memory address 10000080(hex) to register $t1.
(b) Compute and show the data address (in hex number) from the following store instruction: sw $t2, 8014h ($gp);