CSCI 113 (Intro. Computer Organization) Final Exam Spring 2020

Open book/lecture_note, but closed zoom video class sessions

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Submission guide:

* *Exam answers should be written on blank papers and please submit your answer sheets as scanned pdf or photo copy (pdf, png, or jpg);*
* *Please organize your answer sheets in the order of the question numbers; write your name and student ID on the first page, and write a page number on each page (right-upper corner);*
* *Please make a .zip file (do not use .rar) containing all your answer sheets; make your file name and email title as "CS113-final-exam-YourFirstName-YourLastName.zip"; and send it to me < jpark@csufresno.edu > within the exam session.*

(10 pts) 1. Performance

Consider the following instruction count and CPI values for machines M1 and M2:

	instruction-count	CPI on M1	CPI on M2
type-1:	30	1	2
type-2:	40	2	1
type-3:	10	3	3
type-4:	20	4	2

Assume that clock rates of machines M1 and M2 are 500MHz and 400 MHz, respectively.

(a) Which machine is more efficient in terms of CPU execution time? _____
Please show your computations of the CPU execution times (for M1 and M2).

(b) Which machine is more efficient in terms of MIPS rate? _____
Please show your computations of the MIPS rates (for M1 and M2).

(10 pts) 2. MIPS ISA

Consider the following MIPS assembly code segment for implementing a while loop:

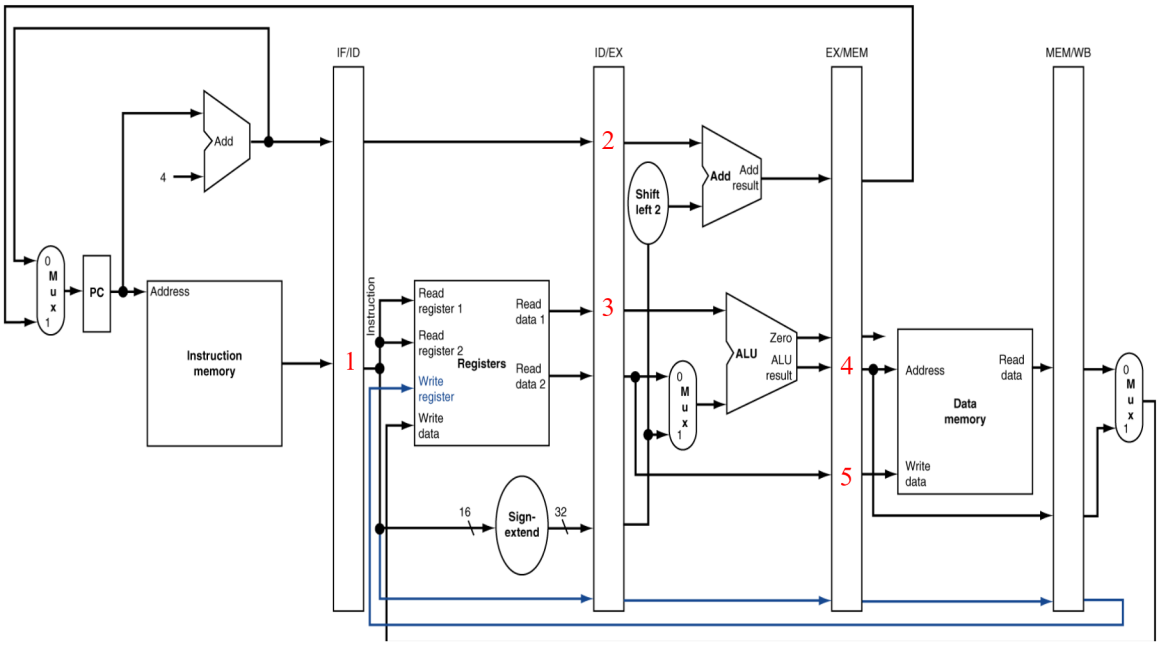
```
Start:  sll   $t2, $s2, 2
        lw    $t0, 8($t2)
        beq   $t0, $s5, Done
        addi  $s2, $s2, 2
subi  $s2, $s2, 1
        j   Start
 Done:
```

(a) Write the MIPS machine code (in hexadecimal number) for the 3rd instruction, i.e., bne $t0, $s5, Done.
Opcode for beq is 4 in decimal; register numbers for $t0 and $s5 are 8 and 21 in decimal, respectively.

(b) Assume that the first instruction (sll $t2, $s2, 2) is stored in the memory at starting byte address 80 in hexadecimal, and write the MIPS machine code (in hexadecimal number) for the last instruction, i.e., j Start.

(15 pts) 3. CPU – pipelined implementation

Consider the following diagram of the MIPS pipelined datapath and answer.



(a) Write the register names for RED color circled numbers, i.e., 1 2 3 4 5

(b) Write the micro operations done in the ID stage of a load instruction.

(c) Write the micro operations done in the EX stage of a branch (beq) instruction.

(15 pts) 4. MIPS pipeline more

Consider the following sequence of instructions for (a) and (b).

```
lw   $s2, 40($s1);
add  $s3, $s4, $s2;
sub  $s5, $s2, $s6;
and  $s7, $s2, $s3;
```

(a) If the system allows only stalling, what is the minimum total execution cycles needed? _____
Justify your answer (show the timing diagram).

(b) If the system allows all forwardings and 2phase clocking, what is the minimum total execution cycles needed? _____; Justify your answer (show the timing diagram).

(c) Assume that the branch instruction is resolved at the end of ID (2^{nd}) stage.

How many stall cycles are needed for a taken branch with Predict-not-Taken scheme? _____

How many stall cycles are needed for a not-taken branch with Predict-not-Taken scheme? _____

(15 pts) 5. Memory hierarchy

(a) Consider a set-associative cache system and describe the steps of operations for a cache read. Please include both hit and miss cases.

1. CPU issues a memory block address;
2.

. . . .

(b) Is the replacement policy needed for the direct-mapped cache? (Circle: yes, no)
Justify your answer, i.e., explain the reason.

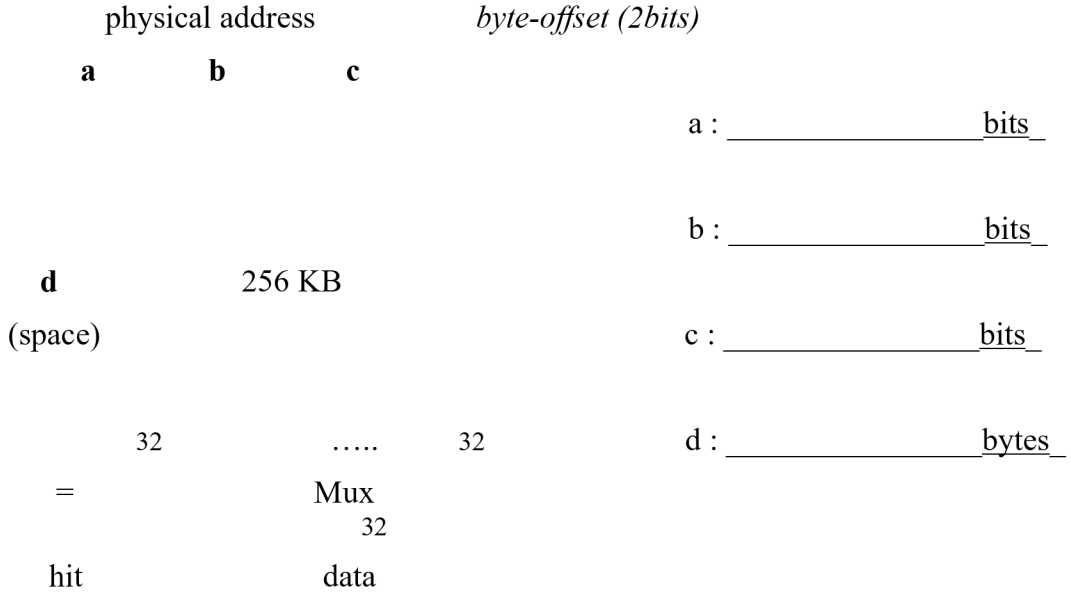
(c) When is the main memory updated in a system with WB cache?

(10 pts) 6. Memory hierarchy

Consider the following system:

Physical address: 34 bits total, right-most 2-bits are for byte-offset.
Cache: direct-mapped cache, 256KB total data size, 32 bytes data per block, no valid bit used.

Show sizes of labeled parts (a,b,c,d) in the following diagram.



a : _____bits_

b : _____bits_

c : _____bits_

d : _____bytes_

(20 pts) 7. Memory hierarchy more

(a) Assume that the cache block size is 20 words, and cache miss penalty consists of the followings:

address transfer: 1 clock cycle
DRAM access: 20 clock cycles
data transfer: 2 clock cycles

Compute the miss penalty in the interleaved memory system with 5 memory banks.
Also compute the memory bandwidth in this system.

(b) Consider the following series of word address references: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43
Assume that a 2-way set associative cache is used and the capacity of the entire cache is 8 words, with one word per block. The cache is initially empty, and the LRU replacement policy is used.

Answer how many hits are made: _____.

(c) Consider a virtual memory system with the following properties:

42-bit virtual address (byte address)
8-KB page size
32-bit physical address (byte address)

- What is the total size of the page table for each process on this machine?
  Assume that each entry of the page table contains a valid-bit and a physical page number.
- What is the total virtual memory size of each process?
- What is the total physical memory size for each process?

(5 pts) 8. Now, follow the submission guide shown in the first page and submit your file by 1:00 pm.

- Late submissions (1:00 pm – 1:10 pm) will be given some penalty points and submissions beyond 1:10 pm will not be considered for grading.