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CSCI 113 Assignment 10

1. 1, 4, 6, 5, 20, 17, 18, 56, 9, 11, 4, 43, 5, 6, 9, 17, 22, 27

0	
1	M[17]
2	M[18]
3	
4	M[4]
5	M[5]
6	M[22]
7	
8	M[56]
9	M[9]
10	
11	M[27]
12	
13	
14	
15	

Hit: 4

2. 1, 4, 6, 5, 20, 17, 18, 56, 9, 11, 4, 43, 5, 6, 9, 17, 22, 27

0	B 0	M[56]
	B 1	
1	B 0	M[9]
	B 1	M[17]
2	B 0	M[18]
	B 1	
3	B 0	M[27]
	B 1	M[43]
4	B 0	M[4]
	B 1	M[20]
5	B 0	M[5]
	B 1	
6	B 0	M[6]
	B 1	M[22]
7	B 0	
	B 1	

Hit: 5

3. 2^8 * (1+18+512) = 256 * 531 = 135936 bits

4.

A) Miss penalty = address time + memory latency + transfer time

Miss penalty = 1 + (20*20) + (2*20) = 440 clock cycles

Bandwidth = 16 bytes / clock cycles

Bandwidth = 16/440 = 0.03636 B/cycle

B) Miss penalty = address time + memory latency + transfer time

Miss penalty = 1 + 15 + 2 = 18 clock cycles

Bandwidth = 16 bytes / clock cycles

Bandwidth = 16/18 = 0.889 B/cycle

C) Miss penalty = address time + memory latency + transfer time

Miss penalty = 1 + 15 + (2*4) = 24 clock cycles

Bandwidth = 16 bytes / clock cycles

Bandwidth = 16/24 = 0.66667 B/cycle

5.