

$$\textcircled{1} \quad C_1 = 500 \text{ MHz} \quad T = 20 \text{ sec}$$

$$C_2 = ? \quad \text{SPEEDUP} = 2 \quad 1.5 \text{ CC NEEDED}$$

SPEEDUP OF 2 MEANS 2 TIMES CLOCK RATE

1,000MHz

1.5 TIMES CC MEANS 1.5 TIMES CLOCK RATE

$$C_2_{\text{CLK RATE}} = 1.5 \text{ GHz}$$

\textcircled{2} \quad 1-TYPE

OP	11	01	OP/SET		0 000
G	5	5	18	-8	10111
				1G	+1
BBBHTT	TTTT	TTTT	TTT	TTT	TTTT

$$\begin{array}{r} 0|000 \\ 10111 \\ +1 \\ \hline 11000 \end{array}$$

2ND MFT: 1 G 3 2 F F F 8

2-TYPE

6	5	5	5	5	6
OP	A3	A7	R0	SHARRY	FUNC

000000 000000 10001 10000 00100 000000

3RD MFT: 0011 9 | 00

I) A) IF $(AC < 0)$
 $AC/MQ \ll 1$
 $AC \leftarrow AC+MD$
 ELSE
 $AC/MQ \leq 1$
 $AC \leftarrow AC-MD$
 IF $(AC < 0)$
 $MQ_0 = 0$
 ELSE
 $MQ_0 = 1$

REPEAT
 N TIMES
 WHERE N IS
 THE NUMBER
 OF BITS IN
 MD OR MQ

IF $(AC < 0)$ } RESTORE AT END
 $AC \leftarrow AC+MD$

B) IF $MQ_0/MQ_{-1} == 00$ THEN $AC \leftarrow AC+0$
 $== 01$ THEN $AC \leftarrow AC+MD$
 $== 10$ THEN $AC \leftarrow AC-MD$
 $== 11$ THEN $AC \leftarrow AC+0$

4)

$$SC = 5\text{ ns} \quad MC = 1\text{ ns} \quad PL = 1.2\text{ ns}$$

SINGLE CYCLE IS AS SLOW AS SLOWEST INST SO ALL INST TAKE 5 ns; AS ONE CC IS ONE INST

$$6 \text{ insts, tot. } 5 \text{ ns} = 30 \text{ ns}$$

$$\frac{1}{MC} = \frac{1}{5}$$

MULTI CYCLE HAS DIFFERENT CC PER INST

$$\begin{array}{ccccccc}
 & \text{LL} & \text{SL} & \text{SW} & \text{AND} & \text{BTR} & \\
 \text{CC} & 5 & +4 & +4 & +4 & +3 & +3 \\
 & \backslash & / & / & / & \backslash & / \\
 & 13 & & & & 10 & \\
 & & \swarrow & \searrow & & & \\
 & & 23 \text{ CC} & & & & \\
 & & \cdot \frac{1\text{ ns}}{\text{cc}} = 23 \text{ ns} & & & &
 \end{array}$$

Pipeline CPU

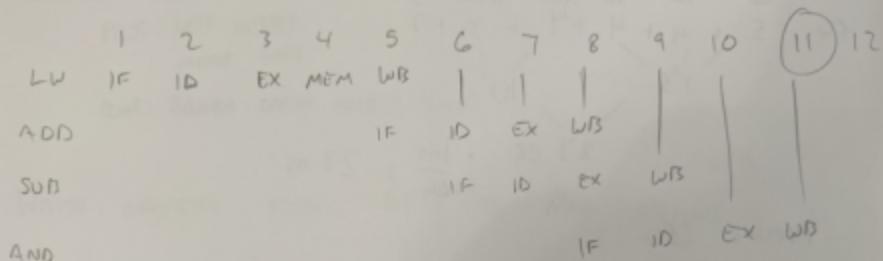
$$\begin{aligned}
 &\text{IT WOULD TAKE } 10 \text{ CC TO GET ALL INST THROUGH} \\
 &\text{PIPELINED CPU} \quad (\text{PIPELINE DEPTH} + (10-1)) = 5 + (6-1) = 10 \text{ cc}
 \end{aligned}$$

$$10 \text{ cc} \cdot \frac{1.2\text{ ns}}{\text{cc}} = 12\text{ ns}$$

5)

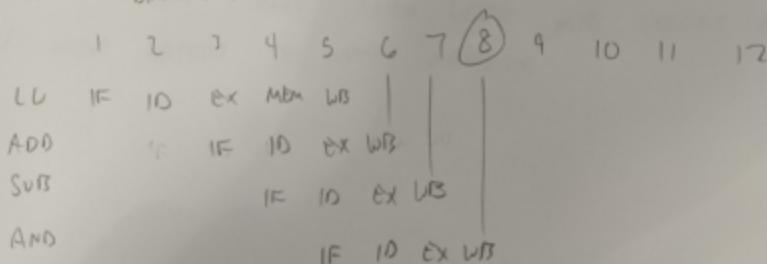
LW \$52, 40 (\$51)
ADD \$53, \$34, \$52
SUB \$55, \$52, \$56
AND \$57, \$52, \$53

A) TIMING DIAGRAM



11 CLOCK CYCLES USING ONLY STALLING

B) TIMING DIAGRAM



8 CLOCK CYCLES ARE NEEDED USING TWO PHASE
CLOCKING AND FORWARDING

Q)

INCREASED BLOCK SIZE

PROS: FASTER ACCESS TIME

CONS: MORE MISSES

LESS HITS

INCREASED ASSOCIATIVITY

PROS: LESS MISSES

MORE HITS

CONS: SLOWER CACHE ACCESS TIME

B) WRITE DIRECTLY FROM CPU TO MAIN MEMORY

WRITE TO CACHE, REPLACING A BLOCK w/ NEW DATA

C) MAIN MEMORY IS UPDATED ON WRITE BACK STAGE OF
A READ MISS AND WHEN WRITE MISS OCCURS AND
CPU WRITES DIRECTLY TO MAIN MEMORY.

⑦

36-BIT PHYS ADD

34-BIT 4/ 2 BYTE OFFSET

$T_4 = A + B + C$

256 KB = 2^{18} BYTES $\frac{\text{SIZE OF CACHE}}{\text{SIZE OF BLOCK}} = \# \text{ OF BLOCKS}$

64 MB = 2^6 BYTES

$$\frac{2^{18}}{2^6} = 2^{12} \text{ BLOCKS}$$

$$B = 12$$

22 BITS REMAINING

$$\frac{\text{WORD}}{\text{BLOCK}} = \frac{64}{4} = 16 = 2^4 \quad \begin{matrix} \text{WORD} \\ \text{OFFSET} \end{matrix} \quad C=4 \quad 22 - 4 = 18 \text{ BITS}$$

$$A = 18$$

D = 12 BIT · NUMBER OF BLOCKS

$$2^{12}$$

A)

$$A = 18 \text{ BITS}$$

$$B = 12 \text{ BITS}$$

$$C = 4 \text{ BITS}$$

$$D = 12 \cdot 2^{12} \text{ BYTES}$$

$$\begin{array}{r} 0000 \\ + 12 \\ \hline 0192 \\ + 11256 \\ \hline \end{array}$$

Q A)

$$5 \text{ mem banks} \cdot 32 \text{ bytes} = \boxed{160 \text{ bytes bandwidth}}$$

$$1 + \frac{(20 \text{ clocks} \cdot 20 \text{ words})}{400} + 2$$

$$\boxed{403 \text{ clock cycle miss penalty}}$$

$$13) \text{ideal CPI} = 3 \quad L/S \text{ INST: } 40^\circ \quad L-CACHE: 5.8^\circ \quad D-CACHE \text{ MISS RATE: } 10\% \\ \text{MISS PENALTY: } 100 \text{ clocks}$$

$$\text{EFFECTIVE CPI} = \text{IDEAL CPI} + \text{MISS RATE} \cdot \text{CACHE MISS PENALTY}$$

$$\begin{array}{rcl} 10^\circ \cdot 40^\circ & & 60^\circ \cdot 5.8^\circ \cdot \frac{60}{0.05} \\ 40^\circ & & 70^\circ \cdot 0.03 \cdot 100 \end{array}$$

$$0.04 \cdot 100 = 4$$

$$0.03 \cdot 100 = 3$$

$$3 + 4 + 3 = \boxed{10 \text{ effective CPI}}$$