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CSCI 113 Assignment 10

1. 1, 4, 6, 5, 20, 17, 18, 56, 9, 11, 4, 43, 5, 6, 9, 17, 22, 27

0	
1	M[17]
2	M[18]
3	
4	M[4]
5	M[5]
6	M[22]
7	
8	M[56]
9	M[9]
10	
11	M[27]
12	
13	
14	
15	

Hit: 4

2. 1, 4, 6, 5, 20, 17, 18, 56, 9, 11, 4, 43, 5, 6, 9, 17, 22, 27

0	B 0	M[56]
	B 1	
1	B 0	M[9]
	B 1	M[17]
2	B 0	M[18]
	B 1	
3	B 0	M[27]
	B 1	M[43]
4	B 0	M[4]
	B 1	M[20]
5	B 0	M[5]
	B 1	
6	B 0	M[6]
	B 1	M[22]
7	B 0	
	B 1	

Hit: 5

3. 2^8 * (1+18+512) = 256 * 531 = 135936 bits

4. Block size: 20 words

Width of organization: 4 words

Number of banks: 4

Send address delay = 1 cycle

Main mem latency for new access: 20 cycles

Transfer time: 2 cycles/word

A) Miss penalty = address time + memory latency + transfer time

Miss penalty = 1 + (20*20) + (2*20) = 441 clock cycles

Bandwidth = (20 * 4) bytes / clock cycles

Bandwidth = (20 * 4) /440 = 0.1814 B/cycle

B) Miss penalty = 1 + (20*5) + (2*20) = 111 clock cycles

Bandwidth = (20 * 4) bytes / clock cycles

Bandwidth = (20 * 4) /111 = 0.7207 B/cycle

C) Miss penalty = 1 + (20*5) + (20*2) = 141 clock cycles

Bandwidth = (20 * 4) bytes / clock cycles

Bandwidth = (20 * 4) /141 = 0.5673 B/cycle

5. 42 bit virtual address (byte address)

   8 KB page size

   32 bit physical address

Virtual address

V.P = 29 bits	Offset = 13 bits

8 KB = 2^{13} B/page becomes offset 13 bits

42 – 13 = 29 becomes V.P 29 bits

Physical address

P.P = 19 bits	Offset = 13 bits

VA offset = PA offset = 13 bits

32 – 13 = 19 bits

Page table

Each entry is 23 bits

1 bit	1 bit	1 bit	P.P = 19 bits

Total num of entries = $2^{V.P} = 2^{29}$ = 536870912 entries

Page table size = # of entries * (valid + protection + dirty + use + P.P) =

53687091 * (1 + 1+ 1+ 1+ 19) = 12348030976