MODEL NO. : G1599FP103FG-001

ISSUED DATE: 2018-02-22

VERSION : A0

■**Preliminary Specification**

□**Final Product Specification**

Customer : GV60FHGVRAAGVSOO01

Approved by	Notes

GVO Confirmed :

Prepared by	Checked by	Approved by

This technical specification is subjected to change without notice.

Table of Contents

Record of Revision

Rev	Issue Date	Description	Editor
A0	2018-03-22	Draft	Wei Rongrong

1 General Specifications

Feature		Spec	Remark
Display Spec	Screen Size (inch)	5.99	
	Display Mode	AMOLED	
	Resolution(dot)	1080(W) x 2160(H)	
	Active Area(mm)	68.04(W)×136.08 (H)	
	Pixel Pitch (um)	63.00(W) x 63.00 (H)	
	Pixel Configuration	V-Style4	
	Technology Type	LTPS	
	Color Depth	16.7M	
	Interface	MIPI 4 LANE	
	Surface Treatment	NONE	
Mechanical Characteristics	With TP/Without TP	With TP	
	Module Outline Dimension(W x H x D) (mm)	68.04 (W)x141.68 (H) x0.55(D)	
	Weight (g)	TBD	
Electronic	Driver IC(Type)	RM69297	
	Touch IC(Type)	mXT640U	

Note 1: Requirements on Environmental Protection: RoHS.

2 Input/output Terminals

2.1 Main FPC Pin Assignment

FPC connector: OK-23GM040-04(亚奇).

Main board recommended connector:. OK-23GF040-04(亚奇).

No	Symbol	I/O	Description
1	GND	GND	Ground
2	D0N	I/O	MIPI Data Lane
3	D0P	I/O	MIPI Data Lane
4	GND	GND	Ground
5	D1N	I	MIPI Data Lane
6	D1P	I	MIPI Data Lane
7	GND	GND	Ground
8	D2N	I	MIPI Data Lane
9	D2P	I	MIPI Data Lane
10	GND	GND	Ground
11	D3N	I	MIPI Data Lane
12	D3P	I	MIPI Data Lane
13	GND	GND	Ground
14	TCN	I	MIPI Clock Lane
15	TCP	I	MIPI Clock Lane
16	GND	GND	Ground
17	ELVSS	POWER	Negative power supply for OLED
18	ELVSS	POWER	Negative power supply for OLED
19	AVDD_EN	O	Enable DC-DC power IC,AVDD output
20	SWIRE	O	DC/DC Power IC S-Wire CTRL Pin
21	VSP	POWER	External Power Input for AVDD
22	VSP	POWER	External Power Input for AVDD
23	NC	NC	Not connected
24	NC	NC	Not connected
25	OTP	POWER	Power supply for MTP Programming or Erase. If it is not used please open it.

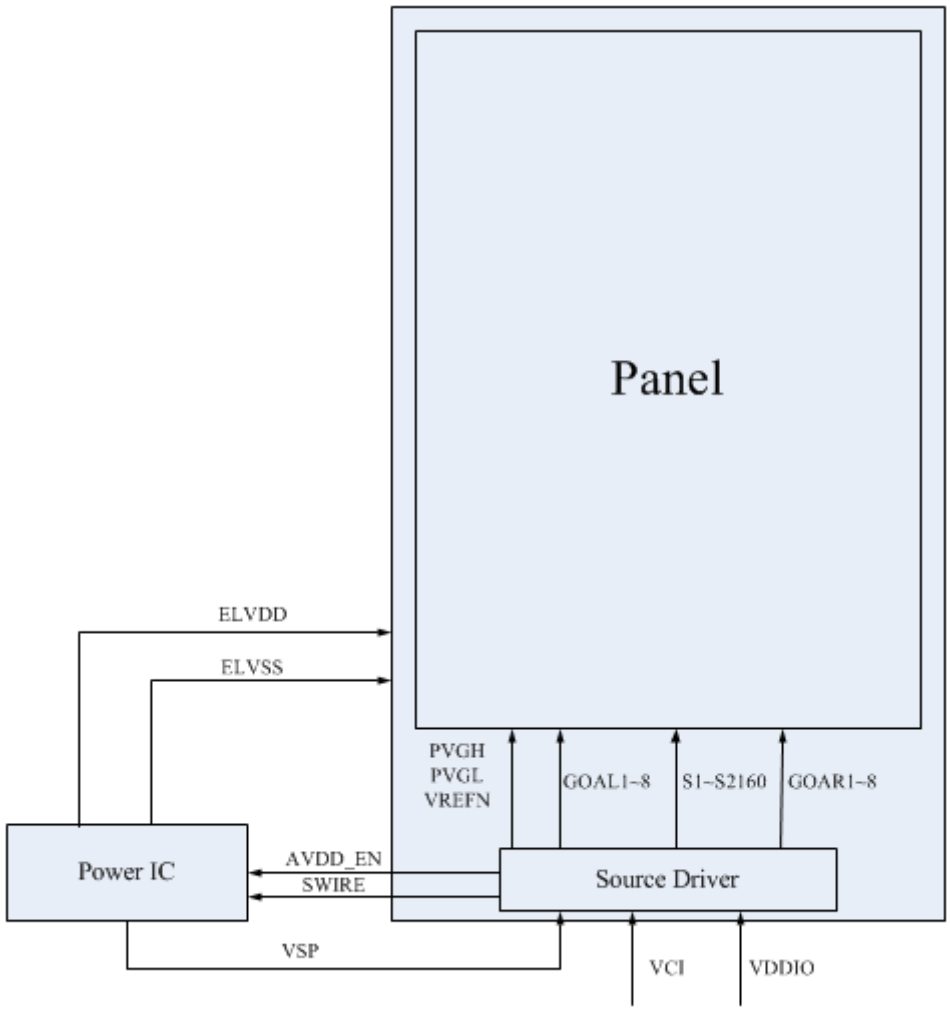
26	NC	NC	Not connected
27	NC	NC	Not connected
28	ELVDD	POWER	Positive power supply for OLED
29	ELVDD	POWER	Positive power supply for OLED
30	RESET	I	Display reset. Active low.
31	TE	O	Sync Signal for preventing Tearing Effect
32	VCI	POWER	Power supply for driver IC analog circuit
33	LCD_ID	O	Module ID check
34	VDDIO	POWER	Power supply for Driver IC digital circuits
35	GND	GND	Ground
36	I2C_SCL	I/O	SCL pin for TP
37	I2C_SDA	I/O	SDA pin for TP
38	TP_RESET	I/O	Reset Pin for TP, Active low
39	TP_INT	I/O	INT pin for TP
40	TP_VCC	I/O	Analog Power for TP

Note: I=Input; O=Output; P=Power; I/O=Input / Output

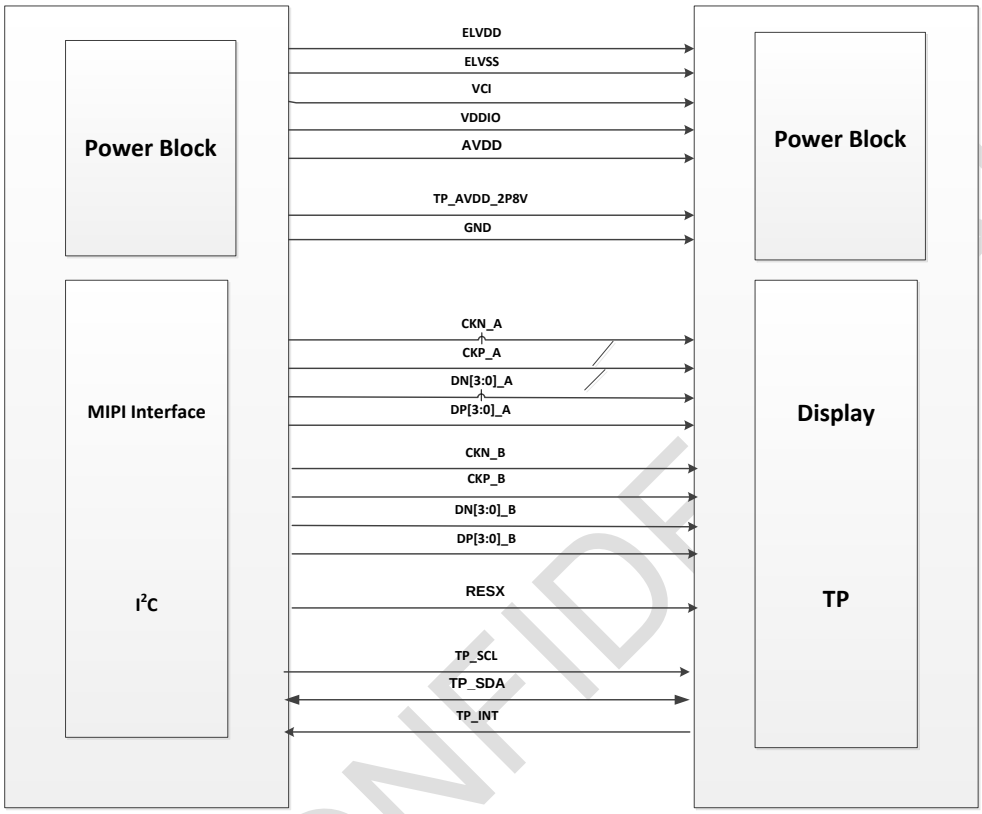
2.2 TP FPC Pin Assignment

No	Symbol	I/O	Description
1	TP_VCC	Power	Analog Power for TP
2	VDDIO	I/O	Digital IO interface power
3	TP_SDA	I/O	SDA pin for TP
4	TP_SCL	I/O	SCL pin for TP
5	TP_INT	I/O	INT pin for TP
6	TP_RESET	I	Reset Pin for TP, Active low
7	GND	GND	Ground

2.3 Circuit block diagram (Display)



2.4 MCU and Display Module Interface Conflagration



3 Absolute Maximum Ratings

3.1 Driving AMOLED Panel

Maximum Ratings (Voltage Referenced to VSS) Vss=0V, Ta=25°C

Item	Symbol	MIN	MAX	Unit
Analog Power supply	VCI	-0.3	+5.0	V
Logic Power supply	VDDIO	-0.3	+4.0	V
Positive power for OLED	ELVDD	+4.0	+5.0	V
Negative power for OLED	ELVSS	-1.0	-5.0	V
Source Analog Power	AVDD	+3.5	+6.5	V
D0P/N D1P/N D2P/N D3P/N TCP/N	Differential Input	-0.3	+1.5	V
Touch analog power supply	TP_VCC	-0.3	+4.0	V
Touch IC input current at any pin		—	±100	mA

Note: Functional operation should satisfy the limits in the Electrical Characteristics tables or Pin Description section. If the module exceeds the absolute maximum ratings, permanent damage may occur. Besides, if the module is operated with the absolute maximum ratings for a long time, the reliability may also drop.

4 Electrical Characteristics

4.1 Driving AMOLED Panel

Test Conditions: VDDIO=1.8V, VCI=2.8V, ELVSS=-3V, ELVDD=4.6V, AVDD=6.4V

Ta=25℃

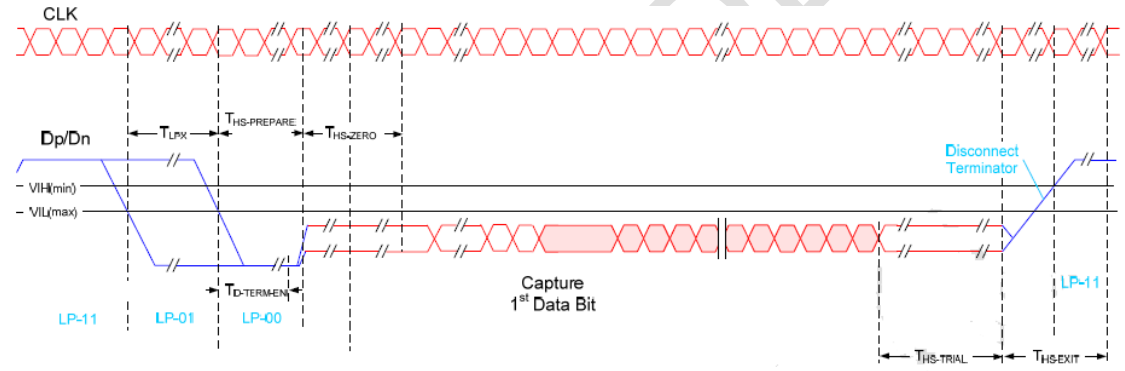
Item		Symbol	MIN	TYP	MAX	Unit
Logic Power supply		VDDIO	1.65	1.80	3.30	V
Analog Power supply		VCI	2.70	2.80	3.60	V
Source Analog Power		AVDD	6.30	6.40	6.50	V
Default Positive Output Voltage		ELVDD	-	4.60	-	V
Positive Output voltage total variation			-0.80	-	+0.80	%
Default Negative Output voltage		ELVSS	-1.00	-	-5.00	V
Negative output voltage total variation			-1.00	-	+1.00	%
Touch analog power supply		TP_VCC	2.70	3.00	3.60	V
Input Signal Voltage	High Level	VIH	0.80*VDDIO	-	VDDIO	V
	Low Level	VIL	0.00	-	0.20*VDDIO	V

Output Signal Voltage	High Level	VOH	0.80*VDDIO	-	VDDIO	V
	Low Level	VOL	0.00	-	0.20*VDDIO	V
Normal		I_{ELVDD} /I_{ELVSS}	-	-	291	mA
		I_{VCI}	-	2.93	-	mA
		I_{VDDIO}	-	20.5	-	mA
		I_{AVDD}	-	17.5	-	mA
Stand-by		I_{VCI}	-	1	-	uA
		I_{VDDIO}	-	1	-	uA

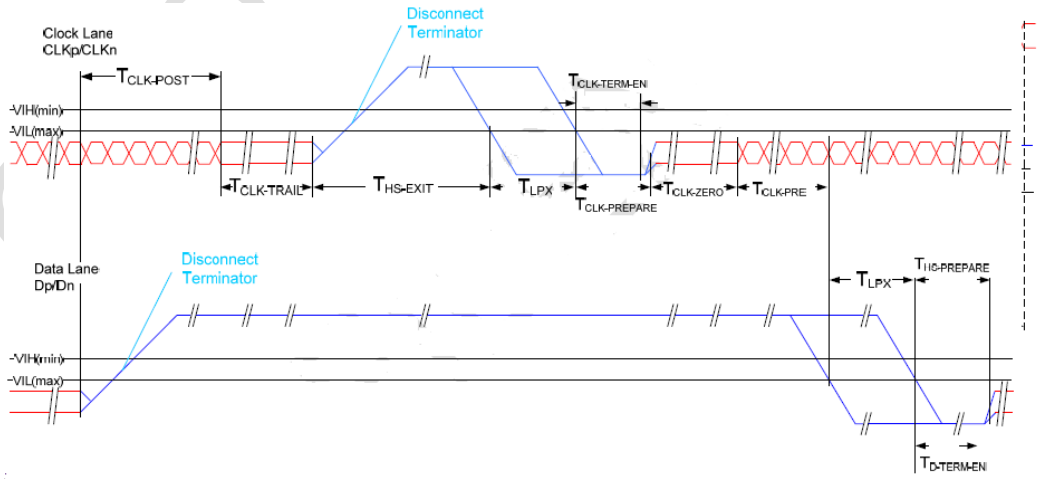
5 AC Characteristics

5.1 MIPI Interface Characteristics

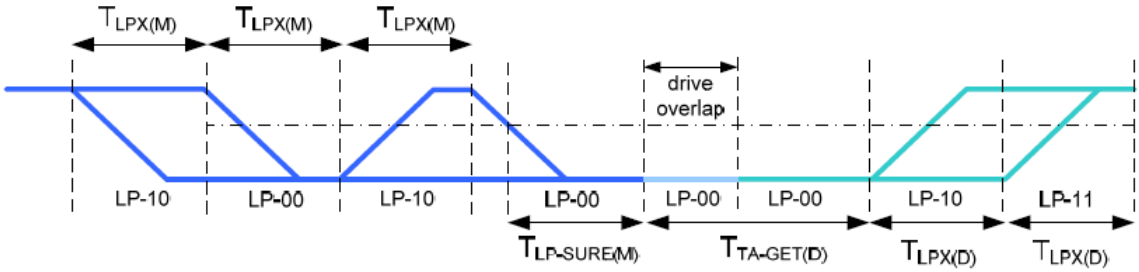
HS Data Transmission Burst



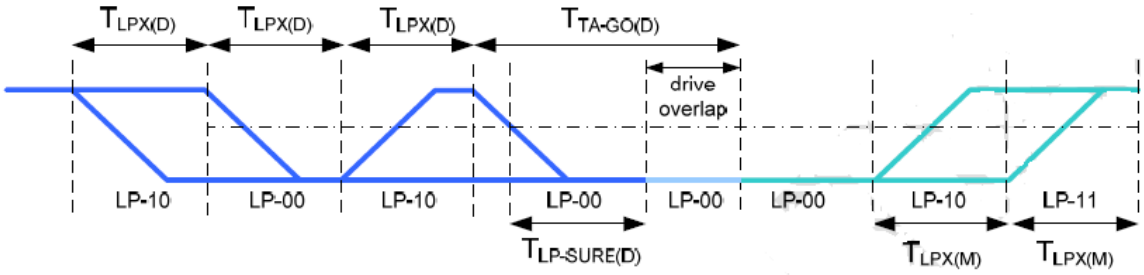
HS clock transmission



Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



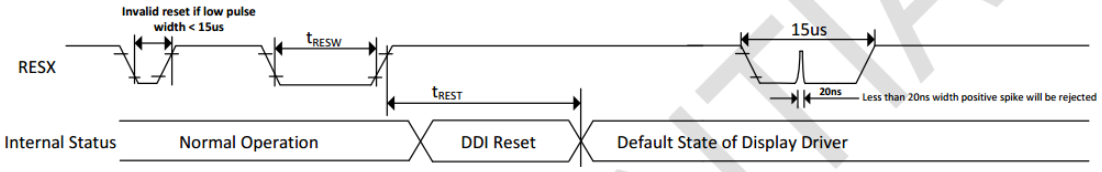
Timing Parameters：

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

5.2 Display RESET Timing Characteristics

Reset input timing:



VDDIO=1.65 to 1.98V, VCI=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Timing Parameters

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	Reset low pulse width	15	-	-	1. Shorter than 5us, Reset rejected 2. Longer than 15μs, IC reset 3. Between 5μs and 15μs, It depends on voltage and temperature condition.	μs
t_{REST}	Reset complete time	-	-	10	When reset applied at sleep-in mode	ms
		-	-	120	When reset applied at sleep-out mode	ms

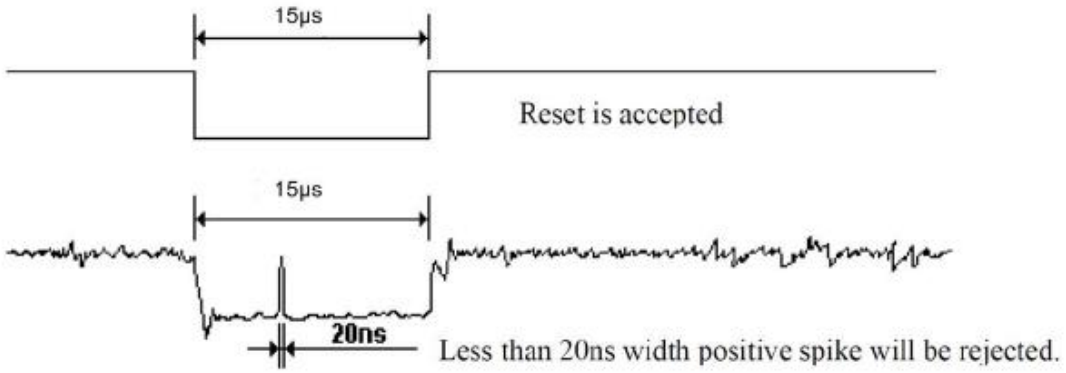
Note1.Spike caused by an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 15μs	Reset
Between 5μs and 15μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blank (The display is entering blanking sequence, whose maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains blank in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

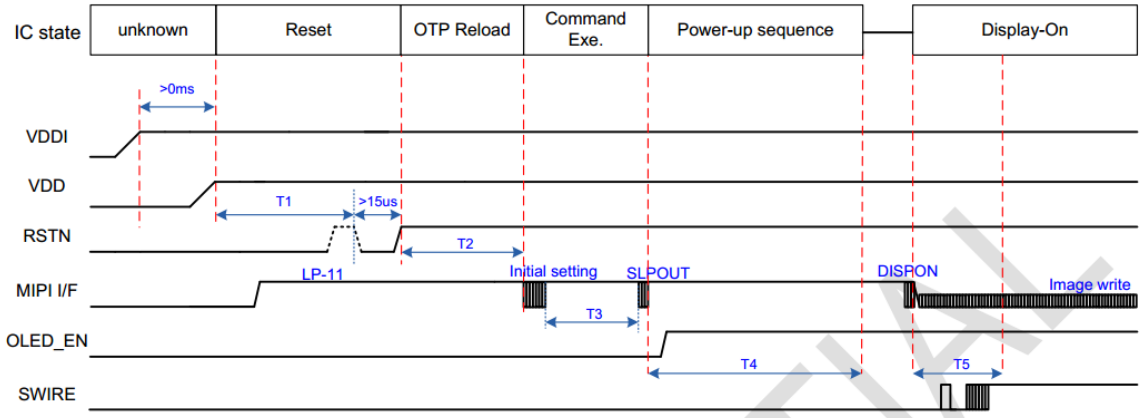


Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

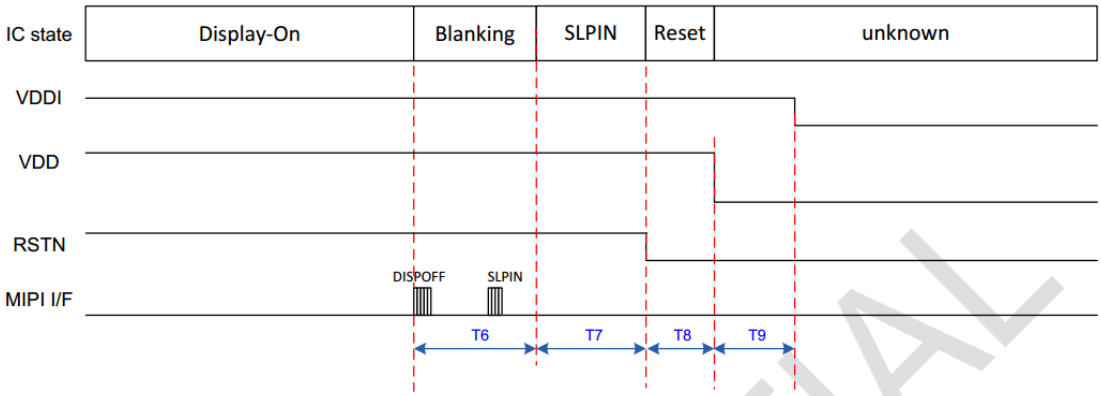
6 Recommended Operating Sequence

6.1 Display Power on / off Sequence

6.1.1 Power On Sequence



6.1.2 Power Off Sequence



6.2 Brightness control

Use "command 5100h, data xxh" to adjust the Manual Brightness value of the display: In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

	WRDISBV												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRDISBV	W	51h	5100h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF

7 Optical Characteristics Optical Specification

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angle		θT	CR≥10	75	85		Degree	Note 2 Test Equipment：CS2000A
		θB		75	85			
		θL		75	85			
		θR		75	85			
Contrast Ratio		CR	θ=0°	10000				Note1 Note3 Test Equipment：CS2000A
Response Time		T_{ON}	25℃			1	ms	Note1 Note4 Test Equipment：Admesy MSE
		T_{OFF}						
Chromaticity	White	x		(0.280)	(0.300)	(0.320)		Test Equipment：CS2000A Note: Chromaticity can be modified according to customer demand
		y		(0.300)	(0.320)	(0.340)		
	Red	x		(0.625)	(0.655)	(0.685)		
		y		(0.315)	(0.345)	(0.375)		
	Green	x		(0.210)	(0.250)	(0.290)		
		y		(0.670)	(0.710)	(0.750)		
	Blue	x		(0.105)	(0.135)	(0.165)		
		y		(0.030)	(0.060)	(0.090)		
Uniformity		U		75			%	Note1 Note6 luminance of center point is 350±70nits Test Equipment：CS2000A
NTSC				85	100		%	Note5
Luminance		L		280	350	420	Cd/m^2	Note1 Note7 Test Equipment：CS2000A
Cross-talk						1.5	%	Note8 L≤350nits Test Equipment：

							CS2000A
Gamma			2.0	2.2	2.4		Gamma=2.2±0.2（L≤350nits）； Gamma Self-adjustment (L＞350nits) Test Equipment：CS2000A

Test Conditions:

1. the ambient temperature is 25℃.
2. The test systems refer to Note1 and Note2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the AMOLED screen. All input terminals AMOLED panel must be ground when measuring the center area of the panel.

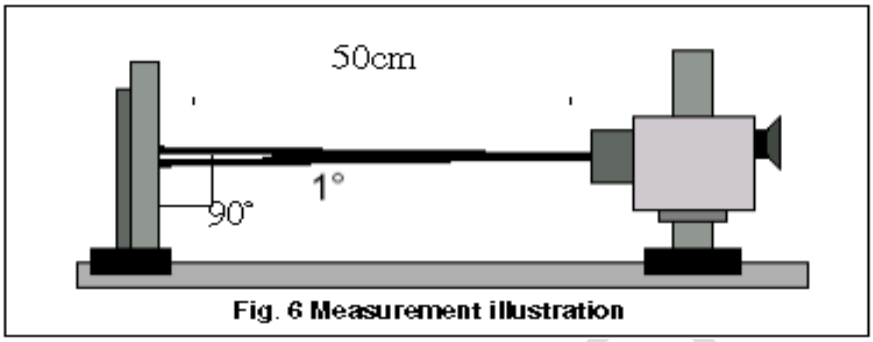


Fig. 6 Measurement illustration

Note 2: Definition of viewing angle range and measurement system.

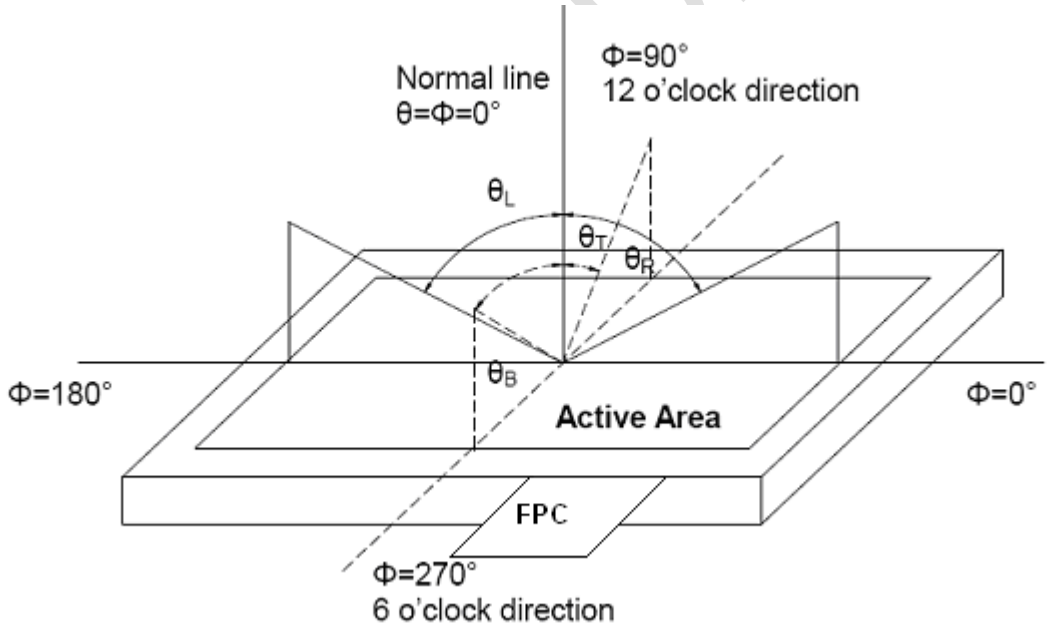


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

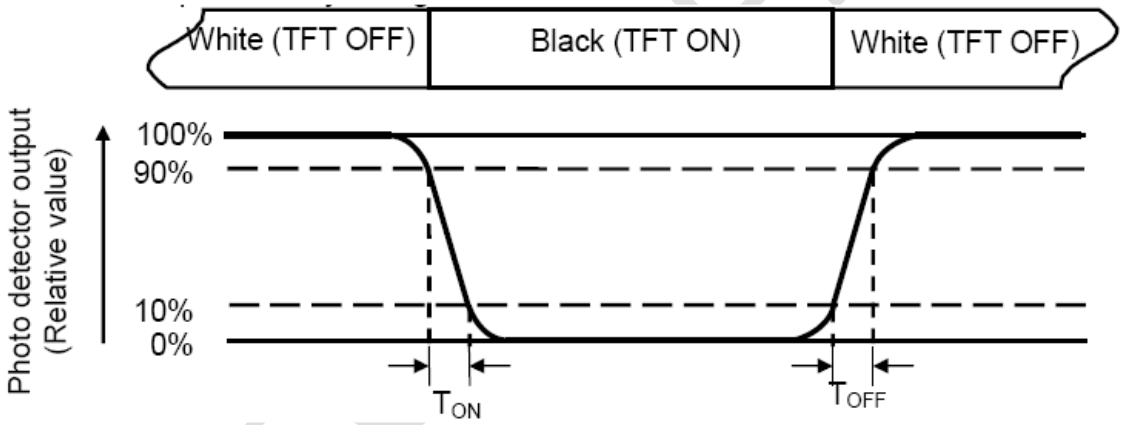
$$\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when LCD is on the "white" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “: A state where the AMOLED should be driven by Vwhite.

“Black state”: A state where the AMOLED should be driven by Vblack.

Note 4: Definition of response time

The response time is defined as the AMOLED optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changing from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changing from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of AMOLED.

Note 6: Definition of luminance uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length W----- Active area width

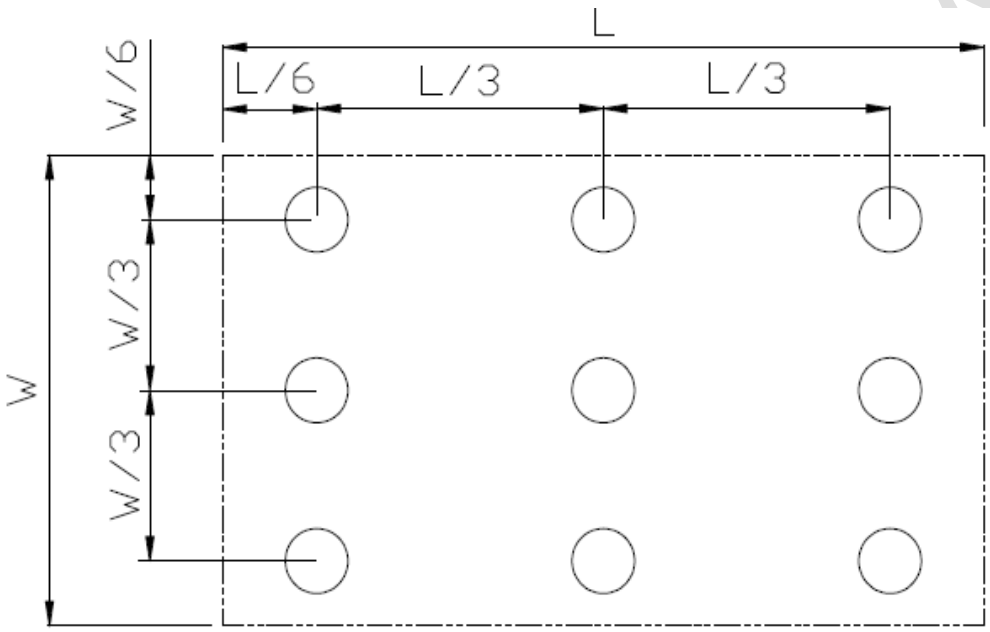


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of luminance:

Measure the luminance of white state at center point.

Note 8: Cross Talk

A. Measure luminance at the position, P0.

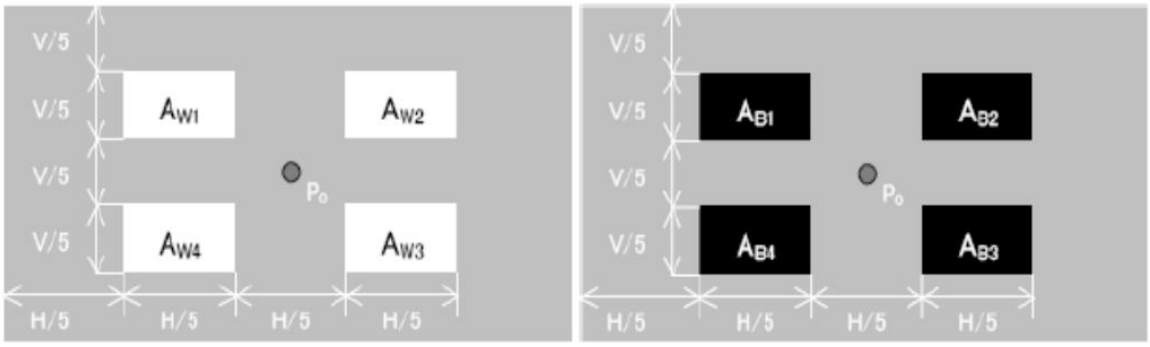
B. Calculate cross talk as below equation.

$$L_{W\_OFF} = \frac{L_{W1} + L_{W2} + L_{W3} + L_{W4}}{4}$$

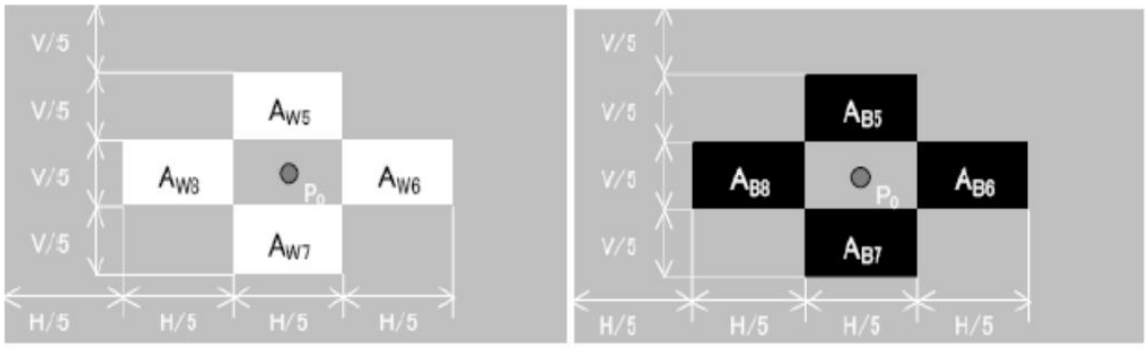
$$L_{B\_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$crosstalk = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\% \qquad (i = 5 \text{ to } 8)$$

$$crosstalk = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\% \qquad (i = 5 \text{ to } 8)$$



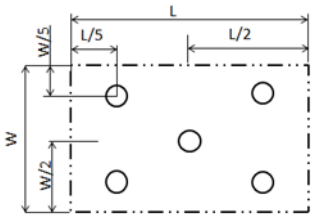
(a) L_{W_OFF}, L_{B_OFF} measuring pattern



(b) L_{W_ON}, L_{B_ON} measuring pattern

8 Environmental / Reliability Test

The following test items are based on module products with 3D coverglass. The products Withnot 3D Cover glass don't do any test on reliability.

No	Test Item	Condition	Remark
1	High Temperature Operation	+70℃, 120hrs	IEC60068-2-2,GB2423.2
2	Low Temperature Operation	-20℃, 120hrs	IEC60068-2-1 GB2423.1
3	High Temperature Storage	+80℃, 120hrs	IEC60068-2-2 GB2423.2
4	Low Temperature Storage	-40℃, 120hrs	IEC60068-2-1 GB2423.1
5	High Temperature & High Humidity Operation	60℃, 90% RH,120hrs	IEC60068-2-78 GB/T2423.3
6	Thermal Shock (Non-operation)	-40℃(60 min)~+85℃(60 min), 30Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14,GB2423.22
7	Electro Static Discharge (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times; (Environment: 15℃~35℃, 30%~60%, 86Kpa~106Kpa).  	IEC61000-4-2 GB/T17626.2

Note: refer to reliability verification results with cover len.

9 Quality Level

9.1 AMOLED Module of Characteristic Inspection

The environmental condition and visual inspection shall be conducted as below:

(1) Ambient temperature: 22± 3℃

(2) Humidity: 55 ± 10%RH

(3) Ambient light intensity of visual inspection: 800 ~ 1200 lux

(4) Ambient light intensity of function inspection: ≤200lux

(5) Viewing Distance: 35 ± 5cm

(6) Viewing angle (tolerance): the front side 90° (Z) ±30°

(7) Inspection time: 10 ±2 sec

9.2 Sampling Procedures for each item acceptance table

Defect type	Sampling Procedures	AQL
Major defect	GB/T2828.1-2003 Inspection level Ⅱ normal inspection single sample inspection	0.65
Minor defect	GB/T2828.1-2003 Inspection level Ⅱ normal inspection single sample inspection	1.0

Major defect:

Any defect may result in functional failure, or reduce the usability of product for its purpose. For example, electrical failure, deformation and etc.

Minor defect

A defect does not reduce the usability of product for its intended purpose and un-uniformity, such as dot defect and etc.

The criteria on major and/or minor judgment will be according with the classification of defects.

9.3 Inspection Item

No.	Item	Area	Criterion of Defect			Defect type
1	Dot Defect	AA	Type	DS	Acceptable number	
			Bright Dot	≥10mm	0	Major
			Dark Dot	≥10mm	4	

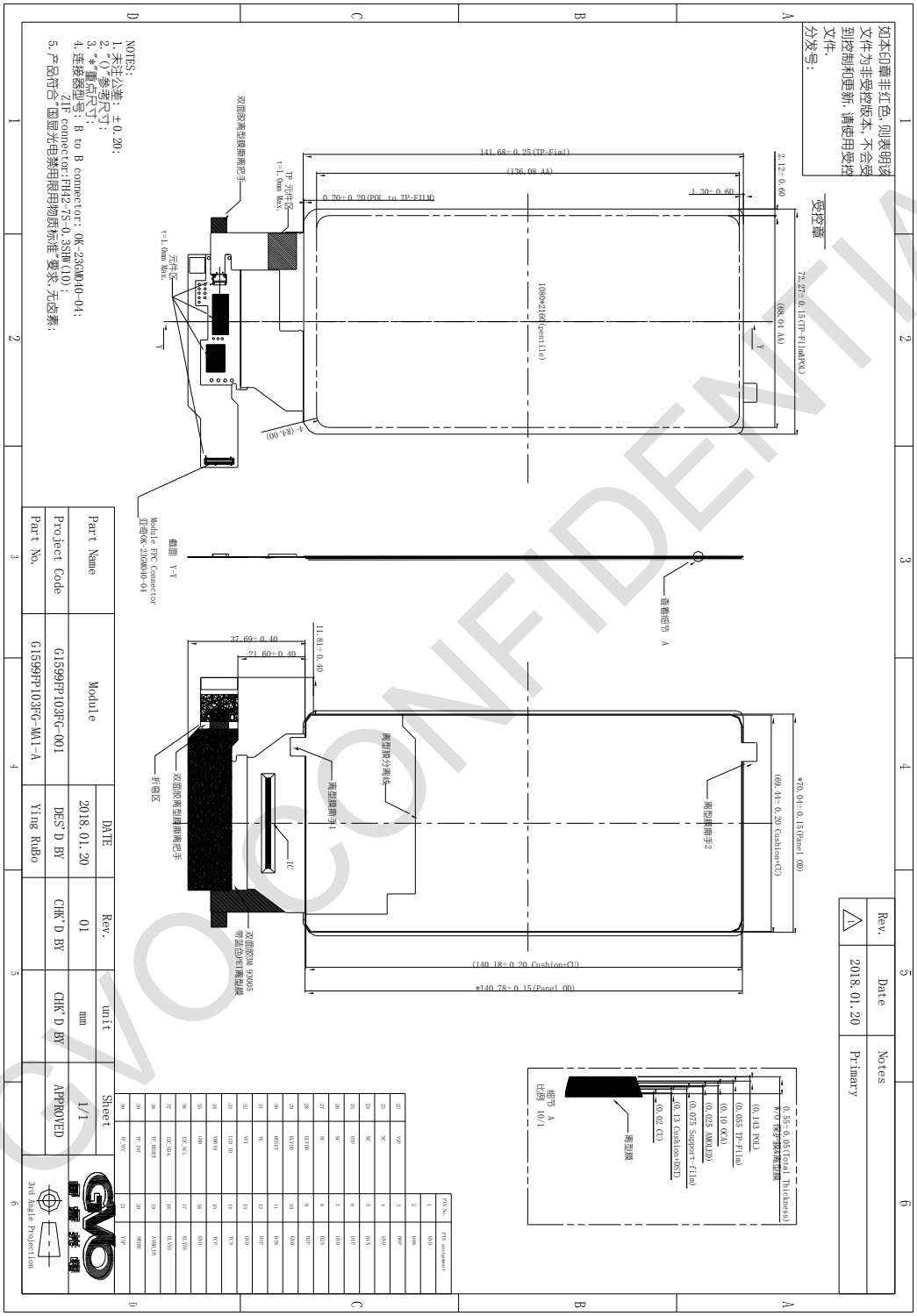
			Dark Dot（≥two connections）	≥10mm		2	
2	No Display	AA	/			Not allowed	Fatal
3	Abnormal Display	AA	/			Not allowed	Fatal
4	Normally white(can't switch)	AA	/			Not allowed	Fatal
5	Line Defect	AA	single line	Bright line		Not allowed	Fatal
				Dark line		Not allowed	
			Multiple lines	Bright line		Not allowed	
				Dark line		Not allowed	
			Half-Line	Bright line		Not allowed	
				Dark line		Not allowed	
6	Color & Edge Mura	AA	See limit sample(under 255 gray-scale white screen)				Major
7	Color Mura	AA	See limit sample(under full white screen)				Major
8	Water Ripple	AA	See limit sample(under 64 gray-scale white screen)				Major
9	Other mura(water stains、Low gray-scale white spot、S-Line Mura)	AA	See limit sample				Major
10	TP function	AA	TP function NG/TP parameters is different with sample parameters		Not allowed		Fatal
11	Glass crack	AA、OA	/		Not allowed		Fatal
12	Screen bump dot	AA、OA	0.15mm＜D≤0.3mm，N≤3，DS≥10mm				Minor
13	Line defects (linear foreign body、scratch)	AA	W（mm）	L（mm）	AA	Not AA	Minor
			W≤0.03	L≤10.0	Ignore		
			0.03＜ W≤0.05	L≤10.0	2	5	
			W>0.08	-	0		
			-	L>10.0	0		
			Feel scratch is not allowed				
14	Point defects(white and	AA	D(mm)	DS(mm)	Acceptable number		Minor
			D≤0.1	-	Ignore		

	black dot、foreign body point)		0.1＜D≤0.15	≥10		2	
				10≤DS＜50		5	
				10≤DS＜50		2	
				DS＞50		3	
			D>0.3	-		0	
15	Polarizer crease / indentation	AA	See limit sample				Minor
16	Polarizer starved/overflow glue	Except AA	W≤0.3mm Don't control				Minor
17	Polarizer bump point	Whole area	0.15mm＜D≤0.3mm，N≤3，DS≥10mm				Minor
18	Polarizer surface Scratches /	Whole area	If the body isn't damage, don't control				Minor
19	Glass Edge/corner breakage	Whole area	Other area except two corners on LTPS below and four corners of encap	Z(mm)	Y(mm)	X(mm)	Accept limit	Minor
				≤ T	Can't stretch leading area/frit area	≤2.0	Total breakage is less than 5(crack isn't allowed)	
			Two corners on LTPS below and four corners of Encap	Refer to mobilephone common testing standard accessary				
20	Surface seal glue	Pin area	Height of seal glue≤1.13mm					Minor
			Glue break on circuit area circuit bareness aren't allowed, bubble diameter≤1mm					
			IC covered completely for COG					
21	Back lineation	Pin area	Height of lineation≤0.25mm					Minor
22	Composite glue	LTPS	No breakage, winkle can't leak light, can't affect combination and thickness, no leaking paste					Minor
			Left and right offsets≤0.2mm					
23	ACF	Bondin	The length of attachment is more than both ends of					Minor

		g Area	FPC, which should be range from 0.2 to 1.5mm. Don't go beyond the edge of panel. Effective lap width of wiring ACF is more than 2/3, which is compared with the width of the gold finger of FPC. Don't have bubble or wrinkle.			
24	Seating bubble	Whole area	D(mm)	DS（mm）	N	Minor
			D≤0.2	/	Ignore	
			0.2＜D≤0.3	DS＞10	3	
			D＞0.3	/	Not allow	
25	FPCA	FPC	capacitor and inductance polarity welding reversely /wrong package dimension/wrong direction not allowed			Major
			Component wrong/creak/damage/fall off/offset not allowed			
			Incline component don't affect function and assemble not control			
			FPC should not have serious crease which destroy the line, prick and spots damage. Scratch is not allowed if Cu layer is exposed.			
			The component of FPC should be the same as BOM list. Wrong component/more component/less component not allowed			
			Connector with joint Solder or residual Solder Ball not allowed; pin with Solder spatter not allowed			
			FPC surface dirty not allowed			
			Bonding wire area without visible impurity and foreign body			
			FPC rough edge not control			
			FPC silkscreen bad: content mistake not allowed			
			FPC appearance break: can't exceed 1/2 of the distance between side and conductor or <2.5mm			
			FPC cutting bad: location hole missing / break through and offset not allowed,			
			FPC indentation: circuit wipe off indentation resulting in the back of cover film turn pale not allowed, indentation can't result in FPC damage out circuit area			
			FPC Reinforcing plate bubble area<10%			
			FPC green oil /coverfilm: bubble resulting in metal conductor exposure and connection not allowed			
			FPC Solder: joint Solder/vain Solder/missing solder not allowed			
			Solder Ball and Solder spatter residual: the area should no Solder Ball and Solder spatter of golden finger isn't allowed residual			
			FPC Reinforcing plate is bad: damage (W≤0.3mm，L≤1mm)			

			Reinforcing plate missing paste/reversing paste resulting in FPC separation, reinforcing color is different from samples, that isn't allowed.	
			Reinforcing plate convex point: D≤0.25mm,Don't affect overall thickness	
		FPC golden finger	Golden finger coating layer arcus/visible surface concave convex not allowed	Major
			Golden finger crack: top crack ≤0.3mm, other parts crack not allowed	
			Appearance damage/ concave point not allowed	
			Golden finger offset: positive and negative golden finger offset and mark offset W≤0.1mm	
			Golden finger exposed Cu: W≤1/3 line width, L≤1/3 line width,3 or more golden finger exposed Cu not allowed	
			Golden finger gap: gap and circuit gap≤1/3 line width	
			Golden finger crush: visible crush not allowed	
			Golden finger wrinkle/dart: sharp corner wrinkle/dart not allowed	
			Golden finger crack/dirty not allow	
			The gold fingers should not be oxidized, scraped, folded, impressed, broken, spotted or dissymmetry.	
			Golden finger turn black, scald, turn brown not allowed, electrode layer oxidized and color not allowed	
26	Package	other	Products should put into the anti-static trays, with non-overlapping, and the trays should be staggered placed.	Minor
			Different products cannot be mixed into the same inner package.	
			The package should not have obvious deformation or breakage .The printing labels type and quantity are correct.	
			The package should have QC signature. ROHS label is needed if the product is under ROHS control.	

10 Mechanical Drawing



Packing Drawing

TBD

11 Precautions for Use of AMOLED Modules

11.1 Handling Precautions:

11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from height.

11.1.2 Do not press down the screen or the adjoining areas too hard because the color tone may be shifted.

11.1.3 The polarizer covering the display surface of the AMOLED module is soft and easily scratched. Handle this polarizer carefully.

11.1.4 If the display surface is contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear, moisten the cloth with ethyl alcohol.

11.1.5 Solvents may damage the polarizer. Do not use water, ketone or aromatic solvents except ethyl alcohol.
Do not attempt to disassemble the AMOLED Module.

11.1.6 If the logic circuit power is off, do not apply the input signals.

11.1.7 To prevent destruction from static electricity, be careful to maintain an optimum working environment.

11.1.8 Be sure to make yourself in contact with the ground when handling with the AMOLED Modules.

11.1.9 Tools required for assembly, such as soldering irons, must be properly ground.

11.1.10 To reduce the generation of static electricity, do not conduct assembly or other work under dry conditions.

11.1.11 To protect the display surface, the AMOLED Module is coated with a film. Be careful when peeling off this protective film, because static electricity may generate.

11.2 Storage Precautions:

11.2.1 When storing the AMOLED modules, be sure that they are not directly exposed to the sunlight or the light of fluorescent lamps.

11.2.2 The AMOLED modules should be stored under the storage temperature range. If the AMOLED modules will be stored for a long time, the recommended condition is:
Temperature: 0℃~40℃ Relatively humidity: ≤80%

11.2.3 The AMOLED modules should be stored in the room without acid, alkali or harmful gas.

11.3 Transportation Precautions:

11.3.1 The AMOLED modules should not be suffered from falling and violent shocking during transportation. Besides, excessive press, water, damp and sunshine, should be avoided.