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| i2c address = 0001\_111x when INT=0 during reset |
| i2c address = 0011\_111x when INT=1 during reset |

Void **RS1**() {

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| --- |
| // Initialization for Stand-by (RS1) |
| // Software Reset |
| i2c1\_h2cpd\_write16(0x0004,0x0004); // ConfCtl |
| i2c1\_h2cpd\_write16(0x0002,0x7F80); // SysCtl |
| i2c1\_h2cpd\_write16(0x0002,0x0000); // SysCtl |
| // PWR Island block Reset |
| i2c1\_h2cpd\_write16(0x0002,0x0001); // SysCtl |
| i2c1\_h2cpd\_write16(0x0004,0x8004); // ConfCtl |
| Waitx1us(10); |
| i2c1\_h2cpd\_write16(0x0004,0x0004); // ConfCtl |
| i2c1\_h2cpd\_write16(0x0002,0x0000); // SysCtl |
| // Disable Interrupt |
| i2c1\_h2cpd\_write16(0x0016,0x07BF); // TOP\_INTM |
| // HDMI Interrupt Control |
| i2c1\_h2cpd\_write8(0x8502,0xFF); // SYS\_INTS\_C |
| i2c1\_h2cpd\_write8(0x850B,0x3F); // MISC\_INTS\_C |
| i2c1\_h2cpd\_write16(0x0014,0x07BF); // TOP\_INTS\_C |
| i2c1\_h2cpd\_write8(0x8512,0xFE); // SYS\_INTM |
| i2c1\_h2cpd\_write8(0x851B,0x3D); // MISC\_INTM |
| // HDMI PHY |
| i2c1\_h2cpd\_write8(0x8532,0x80); // PHY CTL1 |
| i2c1\_h2cpd\_write8(0x8536,0x40); // PHY\_BIAS |
| i2c1\_h2cpd\_write8(0x853F,0x0A); // PHY\_CSQ |
| i2c1\_h2cpd\_write8(0x8537,0x02); // PHY\_EQ |
| // HDMI SYSTEM |
| i2c1\_h2cpd\_write8(0x8543,0x32); // DDC\_CTL |
| i2c1\_h2cpd\_write8(0x8544,0x10); // HPD\_CTL |
| i2c1\_h2cpd\_write8(0x8545,0x31); // ANA\_CTL |
| i2c1\_h2cpd\_write8(0x8546,0x2D); // AVM\_CTL |
| // HDCP Setting   |  | | --- | |  | | i2c1\_h2cpd\_write8(0x85D1,0x01); // | | i2c1\_h2cpd\_write8(0x8560,0x24); // HDCP\_MODE | | i2c1\_h2cpd\_write8(0x8563,0x11); // | | i2c1\_h2cpd\_write8(0x8564,0x0F); // | |
| // HDMI Audio REFCLK |
| i2c1\_h2cpd\_write8(0x8531,0x01); // PHY\_CTL0 |
| i2c1\_h2cpd\_write8(0x8532,0x80); // PHY\_CTL1 |
| i2c1\_h2cpd\_write8(0x8540,0x8C); // SYS\_FREQ0 |
| i2c1\_h2cpd\_write8(0x8541,0x0A); // SYS\_FREQ1 |
| i2c1\_h2cpd\_write8(0x8630,0xB0); // LOCKDET\_REF0 |
| i2c1\_h2cpd\_write8(0x8631,0x1E); // LOCKDET\_REF1 |
| i2c1\_h2cpd\_write8(0x8632,0x04); // LOCKDET\_REF2 |
| i2c1\_h2cpd\_write8(0x8670,0x01); // NCO\_F0\_MOD |
| // HDMI Audio Setting |
| i2c1\_h2cpd\_write8(0x8600,0x00); // AUD\_Auto\_Mute |
| i2c1\_h2cpd\_write8(0x8602,0xF3); // Auto\_CMD0 |
| i2c1\_h2cpd\_write8(0x8603,0x02); // Auto\_CMD1 |
| i2c1\_h2cpd\_write8(0x8604,0x0C); // Auto\_CMD2 |
| i2c1\_h2cpd\_write8(0x8606,0x05); // BUFINIT\_START |
| i2c1\_h2cpd\_write8(0x8607,0x00); // FS\_MUTE |
| i2c1\_h2cpd\_write8(0x8620,0x22); // FS\_IMODE |
| i2c1\_h2cpd\_write8(0x8640,0x01); // ACR\_MODE |
| i2c1\_h2cpd\_write8(0x8641,0x65); // ACR\_MDF0 |
| i2c1\_h2cpd\_write8(0x8642,0x07); // ACR\_MDF1 |
| i2c1\_h2cpd\_write8(0x8652,0x02); // SDO\_MODE1 |
| i2c1\_h2cpd\_write8(0x8665,0x10); // DIV\_MODE |
| i2c1\_h2cpd\_write8(0x85AA,0x50); // FH\_MIN0 |
| i2c1\_h2cpd\_write8(0x85AF,0xC6); // HV\_RST |
| i2c1\_h2cpd\_write8(0x85AB,0x00); // FH\_MIN1 |
| // Info Frame Extraction |
| i2c1\_h2cpd\_write8(0x870B,0x2C); // NO\_PKT\_LIMIT |
| i2c1\_h2cpd\_write8(0x870C,0x53); // NO\_PKT\_CLR |
| i2c1\_h2cpd\_write8(0x870D,0x01); // ERR\_PK\_LIMIT |
| i2c1\_h2cpd\_write8(0x870E,0x30); // NO\_PKT\_LIMIT2 |
| i2c1\_h2cpd\_write8(0x9007,0x10); // NO\_GDB\_LIMIT |
| // EDID |
| i2c1\_h2cpd\_write8(0x85C7,0x01); // EDID\_MODE |
| i2c1\_h2cpd\_write8(0x85CA,0x00); // EDID\_LEN1 |
| i2c1\_h2cpd\_write8(0x85CB,0x01); // EDID\_LEN2 |
| // EDID Data |
| i2c1\_h2cpd\_write8(0x8C00,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C01,0xFF); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C02,0xFF); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C03,0xFF); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C04,0xFF); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C05,0xFF); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C06,0xFF); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C07,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C08,0x52); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C09,0x62); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C0A,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C0B,0x88); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C0C,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C0D,0x88); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C0E,0x88); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C0F,0x88); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C10,0x1C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C11,0x15); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C12,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C13,0x03); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C14,0x80); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C15,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C16,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C17,0x78); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C18,0x0A); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C19,0x0D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C1A,0xC9); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C1B,0xA0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C1C,0x57); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C1D,0x47); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C1E,0x98); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C1F,0x27); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C20,0x12); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C21,0x48); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C22,0x4C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C23,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C24,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C25,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C26,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C27,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C28,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C29,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C2A,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C2B,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C2C,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C2D,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C2E,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C2F,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C30,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C31,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C32,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C33,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C34,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C35,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C36,0x02); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C37,0x3A); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C38,0x80); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C39,0x18); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C3A,0x71); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C3B,0x38); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C3C,0x2D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C3D,0x40); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C3E,0x58); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C3F,0x2C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C40,0x45); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C41,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C42,0xC4); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C43,0x8E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C44,0x21); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C45,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C46,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C47,0x1E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C48,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C49,0x1D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C4A,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C4B,0x72); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C4C,0x51); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C4D,0xD0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C4E,0x1E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C4F,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C50,0x6E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C51,0x28); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C52,0x55); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C53,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C54,0xC4); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C55,0x8E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C56,0x21); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C57,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C58,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C59,0x1E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C5A,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C5B,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C5C,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C5D,0xFC); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C5E,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C5F,0x54); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C60,0x37); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C61,0x34); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C62,0x39); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C63,0x2D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C64,0x66); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C65,0x48); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C66,0x44); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C67,0x37); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C68,0x32); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C69,0x30); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C6A,0x0A); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C6B,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C6C,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C6D,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C6E,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C6F,0xFD); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C70,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C71,0x14); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C72,0x78); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C73,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C74,0xFF); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C75,0x1D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C76,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C77,0x0A); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C78,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C79,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C7A,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C7B,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C7C,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C7D,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C7E,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C7F,0x7B); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C80,0x02); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C81,0x03); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C82,0x1A); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C83,0x71); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C84,0x47); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C85,0x90); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C86,0x04); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C87,0x02); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C88,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C89,0x11); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C8A,0x22); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C8B,0x05); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C8C,0x23); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C8D,0x09); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C8E,0x07); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C8F,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C90,0x83); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C91,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C92,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C93,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C94,0x65); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C95,0x03); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C96,0x0C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C97,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C98,0x10); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C99,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C9A,0x8C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C9B,0x0A); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C9C,0xD0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C9D,0x8A); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C9E,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8C9F,0xE0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA0,0x2D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA1,0x10); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA2,0x10); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA3,0x3E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA4,0x96); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA5,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA6,0x13); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA7,0x8E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA8,0x21); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CA9,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CAA,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CAB,0x1E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CAC,0xD8); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CAD,0x09); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CAE,0x80); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CAF,0xA0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB0,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB1,0xE0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB2,0x2D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB3,0x10); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB4,0x10); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB5,0x60); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB6,0xA2); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB7,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB8,0xC4); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CB9,0x8E); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CBA,0x21); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CBB,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CBC,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CBD,0x18); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CBE,0x8C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CBF,0x0A); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC0,0xD0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC1,0x90); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC2,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC3,0x40); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC4,0x31); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC5,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC6,0x0C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC7,0x40); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC8,0x55); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CC9,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CCA,0x48); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CCB,0x39); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CCC,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CCD,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CCE,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CCF,0x18); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD0,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD1,0x1D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD2,0x80); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD3,0x18); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD4,0x71); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD5,0x38); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD6,0x2D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD7,0x40); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD8,0x58); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CD9,0x2C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CDA,0x45); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CDB,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CDC,0xC0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CDD,0x6C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CDE,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CDF,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE0,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE1,0x18); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE2,0x01); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE3,0x1D); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE4,0x80); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE5,0x18); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE6,0x71); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE7,0x1C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE8,0x16); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CE9,0x20); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CEA,0x58); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CEB,0x2C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CEC,0x25); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CED,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CEE,0xC0); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CEF,0x6C); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF0,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF1,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF2,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF3,0x18); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF4,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF5,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF6,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF7,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF8,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CF9,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CFA,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CFB,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CFC,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CFD,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CFE,0x00); // EDID\_RAM |
| i2c1\_h2cpd\_write8(0x8CFF,0x32); // EDID\_RAM |
| // Enable Interrupt |
| i2c1\_h2cpd\_write16(0x0016,0x05BF); // TOP\_INTM |
| // Enter Sleep |
| i2c1\_h2cpd\_write16(0x0002,0x0001); // SysCtl  }  void **RS\_int** { |
| // Interrupt Service Routine(RS\_Int) |
| // Exit from Sleep |
| i2c1\_h2cpd\_write16(0x0002,0x0000); // SysCtl |
| Waitx1us(10); |
| // Check Interrupt  // checking if bit[9]=1 for HDMI-RX interrupt |
| rdata16=i2c1\_h2cpd\_read16(0x0014); // TOP\_INTS\_C    // checking bit[0]=1 for 5V DDC power change interrupt] |
| rdata8=i2c1\_h2cpd\_read8(0x8502); // SYS\_INTS\_C  // check bit[1]=1 for HDMI sync change interrupt |
| rdata8=i2c1\_h2cpd\_read8(0x850B); // MISC\_INTS\_C    // check bit[0] for 5V DDC status , bit[7] for HDMI vsync status |
| rdata8=i2c1\_h2cpd\_read8(0x8520); // MISC\_INTS\_C |
| i2c1\_h2cpd\_write16(0x0016,0x07BF); // TOP\_INTM |
| i2c1\_h2cpd\_write8(0x8502,0xFF); // SYS\_INTS\_C |
| i2c1\_h2cpd\_write8(0x850B,0x3F); // MISC\_INTS\_C |
| i2c1\_h2cpd\_write16(0x0014,0x07BF); // TOP\_INTS\_C  }  Void **RS2**() { |
| // Initialization for Ready (RS2) |
| // Enable Interrupt |
| i2c1\_h2cpd\_write16(0x0016,0x05BF); // TOP\_INTM |
| // Let HDMI Source start access |
| i2c1\_h2cpd\_write8(0x854A,0x01); // INIT\_END  } |
| Void **RS3\_check\_resolution**() { |
| // MIPI Output Enable(RS3) |
| // Check HDMI resolution/format |
| Waitx1ms(1000); |
| // Check HDMI resolution |
| rdata8=i2c1\_h2cpd\_read8(0x852E); // PX\_FREQ0 |
| rdata8=i2c1\_h2cpd\_read8(0x852F); // PX\_FREQ1 |
| rdata8=i2c1\_h2cpd\_read8(0x858A); // H\_SIZE0 |
| rdata8=i2c1\_h2cpd\_read8(0x858B); // H\_SIZE1 |
| rdata8=i2c1\_h2cpd\_read8(0x8582); // DE\_WIDTH\_H0 |
| rdata8=i2c1\_h2cpd\_read8(0x8583); // DE\_WIDTH\_H1 |
| rdata8=i2c1\_h2cpd\_read8(0x858C); // V\_SIZE0 |
| rdata8=i2c1\_h2cpd\_read8(0x858D); // V\_SIZE1 |
| rdata8=i2c1\_h2cpd\_read8(0x8588); // DE\_WIDTH\_V0 |
| rdata8=i2c1\_h2cpd\_read8(0x8589); // DE\_WIDTH\_V1 |
| // Check HDMI format |
| rdata8=i2c1\_h2cpd\_read8(0x8528); // VI\_STATUS3 |
| rdata8=i2c1\_h2cpd\_read8(0x8522); // VI\_STATUS |
| rdata8=i2c1\_h2cpd\_read8(0x8525); // VI\_STATUS2 |
| rdata8=i2c1\_h2cpd\_read8(0x8526); // CLK\_STATUS  }  Void **RS3\_enable\_CSI\_for\_60fps**() { |
| // MIPI Output Setting |
| // Stop Video and Audio |
| i2c1\_h2cpd\_write16(0x0004,0x0CD4); // ConfCtl |
| // Reset CSI-TX Block |
| i2c1\_h2cpd\_write16(0x0002,0x1200); // SysCtl |
| i2c1\_h2cpd\_write16(0x0002,0x0000); // SysCtl |
| // PLL Setting |
| i2c1\_h2cpd\_write16(0x0022,0x0200); // PLLCtl1 |
| i2c1\_h2cpd\_write16(0x0020,0x508A); // PLLCtl0 |
| i2c1\_h2cpd\_write16(0x0022,0x0203); // PLLCtl1 |
| Waitx1us(10); |
| i2c1\_h2cpd\_write16(0x0022,0x0213); // PLLCtl1 |
| // Video Setting |
| i2c1\_h2cpd\_write8(0x8573,0xC1); // VOUT\_SET2 |
| i2c1\_h2cpd\_write8(0x8574,0x08); // VOUT\_SET3 |
| i2c1\_h2cpd\_write8(0x8576,0xA0); // VI\_REP |
| // Misc Setting |
| i2c1\_h2cpd\_write16(0x0006,0x012C); // FIFO Ctl |
| i2c1\_h2cpd\_write16(0x0060,0x0001); // CSI-2TX\_MISC |
| i2c1\_h2cpd\_write16(0x7080,0x0000); // DB\_Ctl |
| // Data ID Setting |
| // CSI Lane Enable |
| i2c1\_h2cpd\_write32(0x0140,0x00000000); // CLW\_CNTRL |
| i2c1\_h2cpd\_write32(0x0144,0x00000000); // D0W\_CNTRL |
| i2c1\_h2cpd\_write32(0x0148,0x00000000); // D1W\_CNTRL |
| i2c1\_h2cpd\_write32(0x014C,0x00000000); // D2W\_CNTRL |
| i2c1\_h2cpd\_write32(0x0150,0x00000000); // D3W\_CNTRL |
| // CSI Transition Timing |
| i2c1\_h2cpd\_write32(0x0210,0x00001770); // LINEINITCNT |
| i2c1\_h2cpd\_write32(0x0214,0x00000005); // LPTXTIMECNT |
| i2c1\_h2cpd\_write32(0x0218,0x00001505); // TCLK\_HEADERCNT |
| i2c1\_h2cpd\_write32(0x021C,0x00000001); // TCLK\_TRAILCNT |
| i2c1\_h2cpd\_write32(0x0220,0x00000105); // THS\_HEADERCNT |
| i2c1\_h2cpd\_write32(0x0224,0x0000332C); // TWAKEUP |
| i2c1\_h2cpd\_write32(0x0228,0x00000008); // TCLK\_POSTCNT |
| i2c1\_h2cpd\_write32(0x022C,0x00000002); // THS\_TRAILCNT |
| i2c1\_h2cpd\_write32(0x0230,0x00000005); // HSTXVREGCNT |
| i2c1\_h2cpd\_write32(0x0234,0x0000001F); // HSTXVREGEN |
| i2c1\_h2cpd\_write32(0x0238,0x00000000); // TXOPTIONACNTRL |
| i2c1\_h2cpd\_write32(0x023C,0x00050004); // BTACTRL1 |
| i2c1\_h2cpd\_write32(0x0204,0x00000001); // STARTCNTRL |
| i2c1\_h2cpd\_write32(0x0518,0x00000001); // CSI-2\_START |
| i2c1\_h2cpd\_write32(0x0500,0xA3008087); // CSI-2\_CONFW |
| i2c1\_h2cpd\_write32(0x0100,0x00000203); // CLW\_DPHYCONTTX |
| i2c1\_h2cpd\_write32(0x0104,0x00000203); // D0W\_DPHYCONTTX |
| i2c1\_h2cpd\_write32(0x0108,0x00000203); // D1W\_DPHYCONTTX |
| i2c1\_h2cpd\_write32(0x010C,0x00000203); // D2W\_DPHYCONTTX |
| i2c1\_h2cpd\_write32(0x0110,0x00000203); // D3W\_DPHYCONTTX |
| // VIP |
| // VIP Main Controls |
| // De-Interlacer IP Controls |
| // LCD Controler |
| // YCbCr to RGB |
| // VIP coeff |
| // Enable Interrupt |
| i2c1\_h2cpd\_write8(0x8502,0xFF); // SYS\_INTS\_C |
| i2c1\_h2cpd\_write8(0x850B,0x3F); // MISC\_INTS\_C |
| i2c1\_h2cpd\_write16(0x0014,0x07BF); // TOP\_INTS\_C |
| i2c1\_h2cpd\_write16(0x0016,0x05BF); // TOP\_INTM |
| // Start CSI output |
| i2c1\_h2cpd\_write16(0x0004,0x0CD7); // ConfCtl  } |
|  |
| Void RS5() {   |  | | --- | | // MIPI Output Disable(RS5) | | // Stop CSI output | | i2c1\_h2cpd\_write16(0x0004,0x0CD4); // ConfCtl | | // Enable Interrupt | | i2c1\_h2cpd\_write16(0x0016,0x053F); // TOP\_INTM  Void RS6() { | | // MIPI Output Disable & Sleep(RS6) | | // Stop CSI output | | i2c1\_h2cpd\_write16(0x0004,0x0CD4); // ConfCtl | | // Enable Interrupt | | i2c1\_h2cpd\_write16(0x0016,0x053F); // TOP\_INTM | | // Enter Sleep | | i2c1\_h2cpd\_write16(0x0002,0x0001); // SysCtl  } | |  | |
|  |
|  |
| Void **RS3\_enable\_CSI\_for\_30fps**() {  // for 30fps progressive mode or 1080 interlace mode |
| |  | | --- | | // MIPI Output Setting | | // Stop Video and Audio | | i2c1\_h2cpd\_write16(0x0004,0x0CD4); // ConfCtl | | // Reset CSI-TX Block | | i2c1\_h2cpd\_write16(0x0002,0x1200); // SysCtl | | i2c1\_h2cpd\_write16(0x0002,0x0000); // SysCtl | | // PLL Setting | | i2c1\_h2cpd\_write16(0x0022,0x0600); // PLLCtl1 | | i2c1\_h2cpd\_write16(0x0020,0x306D); // PLLCtl0 | | i2c1\_h2cpd\_write16(0x0022,0x0603); // PLLCtl1 | | Waitx1us(10); | | i2c1\_h2cpd\_write16(0x0022,0x0613); // PLLCtl1 | | // Video Setting | | i2c1\_h2cpd\_write8(0x8573,0xC1); // VOUT\_SET2 | | i2c1\_h2cpd\_write8(0x8574,0x08); // VOUT\_SET3 | | i2c1\_h2cpd\_write8(0x8576,0xA0); // VI\_REP | | // Misc Setting | | i2c1\_h2cpd\_write16(0x0006,0x015E); // FIFO Ctl | | i2c1\_h2cpd\_write16(0x0060,0x0001); // CSI-2TX\_MISC | | i2c1\_h2cpd\_write16(0x7080,0x0000); // DB\_Ctl | | // Data ID Setting | | // CSI Lane Enable | | i2c1\_h2cpd\_write32(0x0140,0x00000000); // CLW\_CNTRL | | i2c1\_h2cpd\_write32(0x0144,0x00000000); // D0W\_CNTRL | | i2c1\_h2cpd\_write32(0x0148,0x00000000); // D1W\_CNTRL | | i2c1\_h2cpd\_write32(0x014C,0x00000000); // D2W\_CNTRL | | i2c1\_h2cpd\_write32(0x0150,0x00000000); // D3W\_CNTRL | | // CSI Transition Timing | | i2c1\_h2cpd\_write32(0x0210,0x00001388); // LINEINITCNT | | i2c1\_h2cpd\_write32(0x0214,0x00000002); // LPTXTIMECNT | | i2c1\_h2cpd\_write32(0x0218,0x00000F02); // TCLK\_HEADERCNT | | i2c1\_h2cpd\_write32(0x021C,0x00000000); // TCLK\_TRAILCNT | | i2c1\_h2cpd\_write32(0x0220,0x00000002); // THS\_HEADERCNT | | i2c1\_h2cpd\_write32(0x0224,0x00004268); // TWAKEUP | | i2c1\_h2cpd\_write32(0x0228,0x00000006); // TCLK\_POSTCNT | | i2c1\_h2cpd\_write32(0x022C,0x00000000); // THS\_TRAILCNT | | i2c1\_h2cpd\_write32(0x0230,0x00000005); // HSTXVREGCNT | | i2c1\_h2cpd\_write32(0x0234,0x0000001F); // HSTXVREGEN | | i2c1\_h2cpd\_write32(0x0238,0x00000000); // TXOPTIONACNTRL | | i2c1\_h2cpd\_write32(0x023C,0x00020001); // BTACTRL1 | | i2c1\_h2cpd\_write32(0x0204,0x00000001); // STARTCNTRL | | i2c1\_h2cpd\_write32(0x0518,0x00000001); // CSI-2\_START | | i2c1\_h2cpd\_write32(0x0500,0xA3008087); // CSI-2\_CONFW | | i2c1\_h2cpd\_write32(0x0100,0x00000203); // CLW\_DPHYCONTTX | | i2c1\_h2cpd\_write32(0x0104,0x00000203); // D0W\_DPHYCONTTX | | i2c1\_h2cpd\_write32(0x0108,0x00000203); // D1W\_DPHYCONTTX | | i2c1\_h2cpd\_write32(0x010C,0x00000203); // D2W\_DPHYCONTTX | | i2c1\_h2cpd\_write32(0x0110,0x00000203); // D3W\_DPHYCONTTX | | // VIP | | // VIP Main Controls | | // De-Interlacer IP Controls | | // LCD Controler | | // YCbCr to RGB | | // VIP coeff | | // Enable Interrupt | | i2c1\_h2cpd\_write8(0x8502,0xFF); // SYS\_INTS\_C | | i2c1\_h2cpd\_write8(0x850B,0x3F); // MISC\_INTS\_C | | i2c1\_h2cpd\_write16(0x0014,0x07BF); // TOP\_INTS\_C | | i2c1\_h2cpd\_write16(0x0016,0x05BF); // TOP\_INTM | | // Start CSI output | | i2c1\_h2cpd\_write16(0x0004,0x0CD7); // ConfCtl | |  | |
| } |
|  |
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|  |