B 441 – Digital Design

Fall 2017

Lab No:	01	Title:	**Vivado and Basys3 Tutorial**
Issued:	Monday, Aug 21, 2017	Due:	Thursday, Aug 24, 2017

This lab shows the steps in a digital design project using Xilinx Vivado design suite and Digilent Basys 3 FPGA board. You will learn how to use Vivado tool to create a digital design and implement the design on an FPGA circuit located on the Basys3 board. You are expected to demonstrate that you successfully performed the design steps, from setting up a project to implementing the project on the FPGA board.

The tutorial also gives you basic background on electrical engineering and digital circuits. This is a starter project with very little hands-on work, but it is a good reference if you ever forget how to start and complete a lab project.

Description

The use of the word 'circuit' in this context comes from the idea that electric power must flow from the positive terminal of a power source through one or more electronic devices and back to the negative terminal of a power source, thereby forming a circuit. If the connections between an electronic device and either the positive or negative terminals of a power supply are interrupted, the circuit will be broken and the device will not function.

In this project we will design and implement a circuit which consists of power supply, a slide switch, a light emitting diode (LED), and a ground. If the slide switch connects LED to the power supply, the LED will light (will be turned on). If the slide switch connects to the ground, the LED will be turned off.

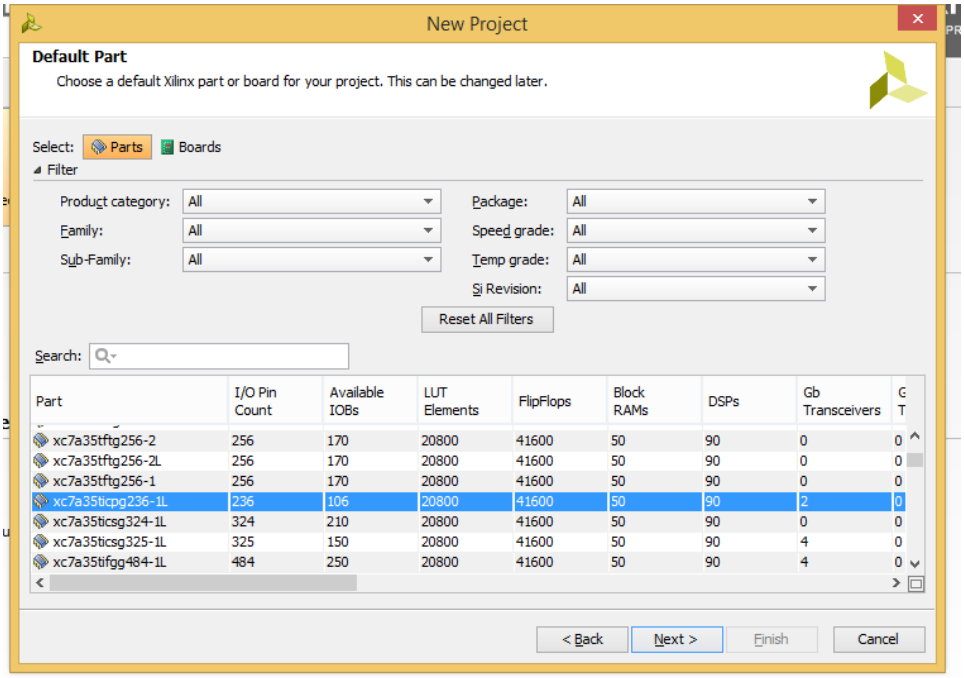
Create project

- Start Vivado and create a new project.

- Follow the wizard. Browse and select a folder in which your project will be created.
- Give a name to your project, for example *Lab01*.
- Check "*Create project subdirectory*."
- For Project Type, select "*RTL Project*." Check "*Do not specify sources at this time*."

Default Part

- Select "*Parts*."
- Select part "*xc7a35ticpg236-1L*."



New Project Summary

A new RTL project will be created in the directory that you specified. You can have a look at the directory and make sure that the project directory was created together with 3 subdirectories and a Vivado project file.

Create design source file

- Right click into the Sources window and select “Add Sources.”
- Check “Add or create design sources”, then “Next.”
- Click “+” on the left hand menu, and select “Create file.” In the dialog box enter the name of the file, to make it easier give it a name “main.”
- Click “Finish.”
- File “main.v” is in Design Sources -> Non-module Files.

Create Verilog code

- Double click on “*main.v*” is in *Design Sources -> Non-module Files*.
- Enter the following Verilog statements:

```
module main(
    output led,
    input sw
    );
    assign led = sw;
endmodule
```

- Save the file (`Ctrl^S`)
- Your *“main.v”* file should be in Design Sources directory.

Create Constraints file

- Right click on “*Constraints*”, select “*Add Sources*.”
- Select “*Add or create constraints*” hit Next.
- Click + on the left hand menu, and select “*Create file*.” In the dialog box enter the name of the file, to make it easier give it a name “*main*.”
- Click “*Finish*.”
- File “*main.xdc*” is in *Constraints -> constrs_1*.

Create Constraints

- Right click on "*Constraints*", select "*Add Sources*."
- Enter the constraints:

```
set_property PACKAGE_PIN V17 [get_ports {sw}]
      set_property IOSTANDARD LVCMOS33 [get_ports {sw}]
set_property PACKAGE_PIN U16 [get_ports {led}]
      set_property IOSTANDARD LVCMOS33 [get_ports {led}]
```

- Save the file (`Ctrl^S`)

Hardware Synthesis

- On the left hand menu select "*Run Synthesis*."
- After the Synthesis is complete, select "*Run Implementation*."
- After the Implementation is complete, select "*Generate Bitstream*."

Creating local host

- On the left hand menu select "*Hardware Manager*."
- In the Hardware Manager window, select "*Open target -> Open New Target*"
- In the "*Open Hardware Target*" wizard click "*Next*".
- Connect *Basys3* card to the USB port.
- Select Connect "*Local server*."
- The wizard should find target type "*xilinx_tcf*", name "*Digilent*" with the hardware device "*xc7a35t_0*." Click *Finish*.

Programming FPGA

- In the Hardware window select "*xc7a35t_0*".
- In the window "*Hardware Device Properties*" select the bitstream file which is used to program FPGA chip.
- Browse to find the bistream file *main.bit*, it should be in the directory: *project_name/project_name.runs/impl_1*
- In the "*Hardware*" window, right click on the FPGA chip name and select "*Program Device*."

Test your implementation

If you successfully completed all steps, slide switch 0 (*sw0*):

- If you slide it up, LED is on.
- If you slide it down, LED is off.