

**University of Southern California**

**Viterbi School of Engineering**

**EE477L**

**MOS VLSI Circuit Design**

**Phase 1 Project Report:  
Multiplier and Divider Design**

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**Professor: Dr. Shahin Nazarian**

**Due Date: 10/31/2023**

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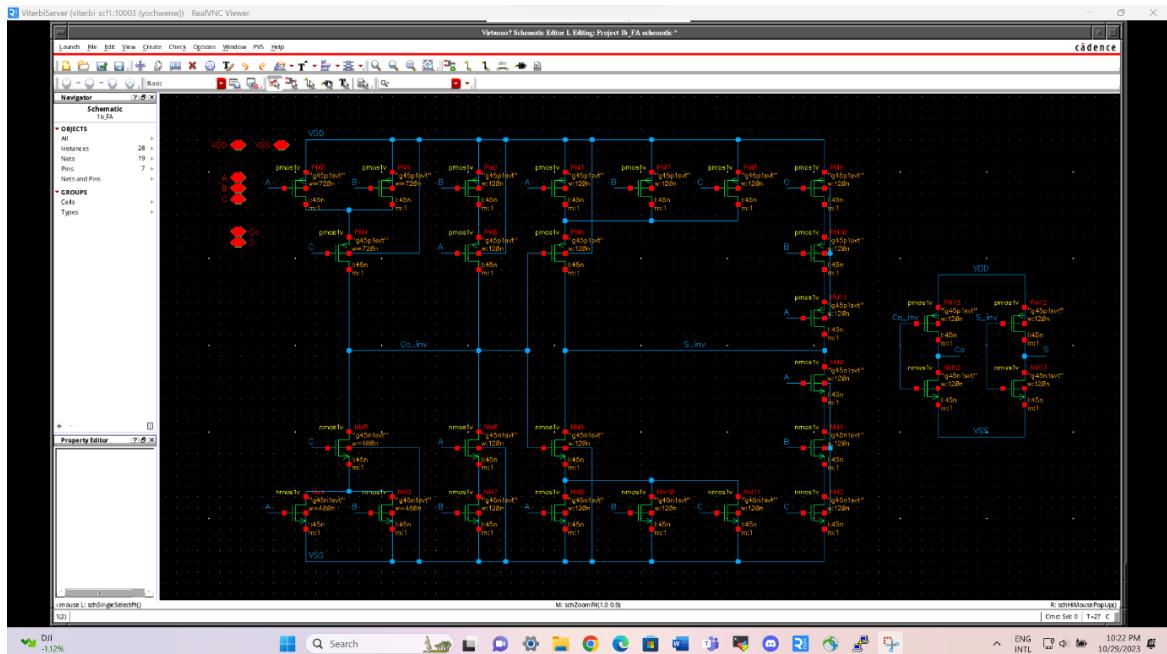
# Part 1: Full-Adder Design

## Part 1: (1 Point)

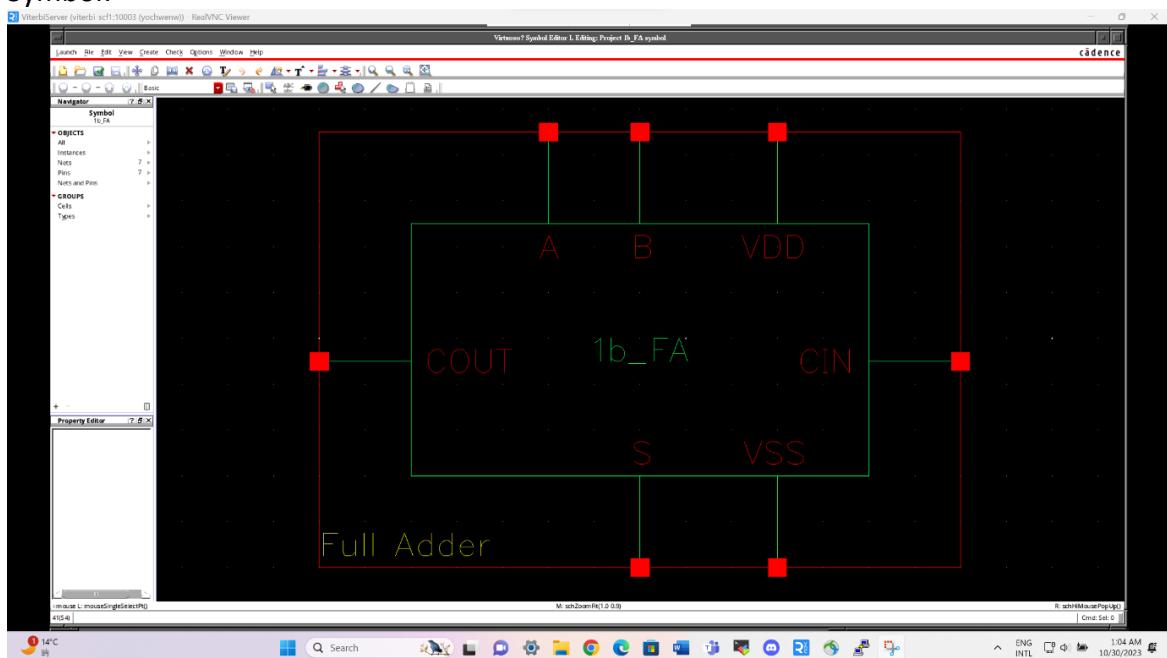
- Schematic and Symbol of the 1-bit FA
- Functional Verification of the 1-bit FA

## 1-bit Full Adder (FA) Design:

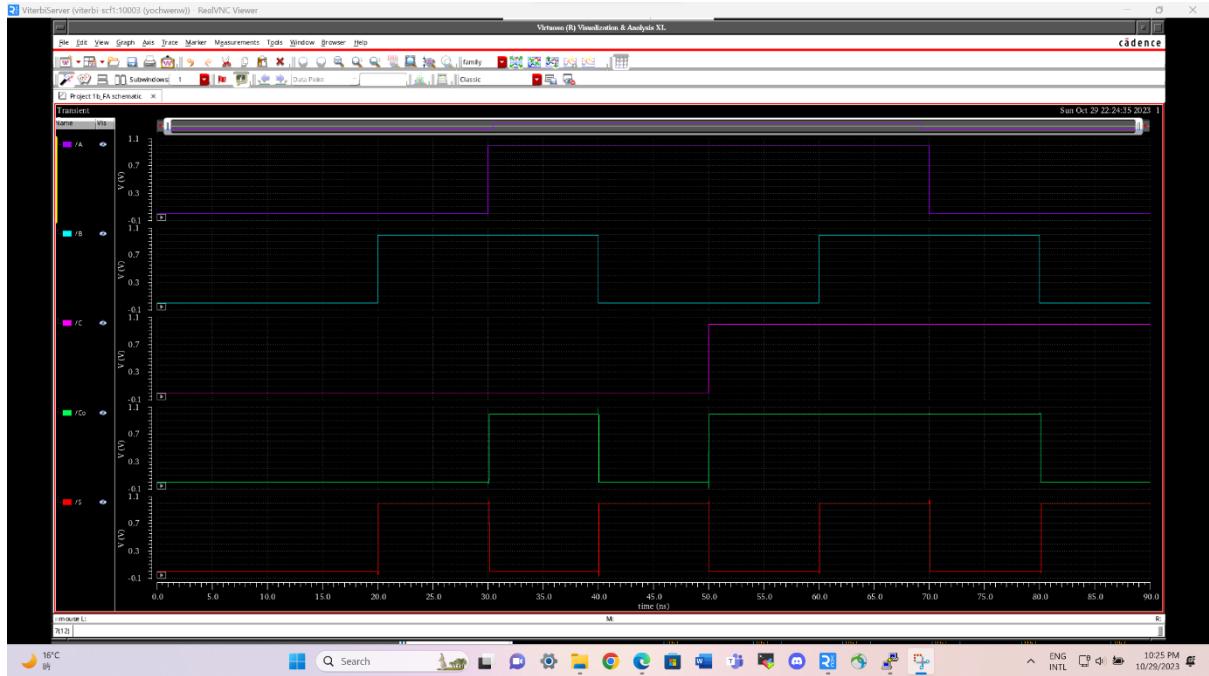
Schematic:



Symbol:



## Functional Verification of 1-bit FA:



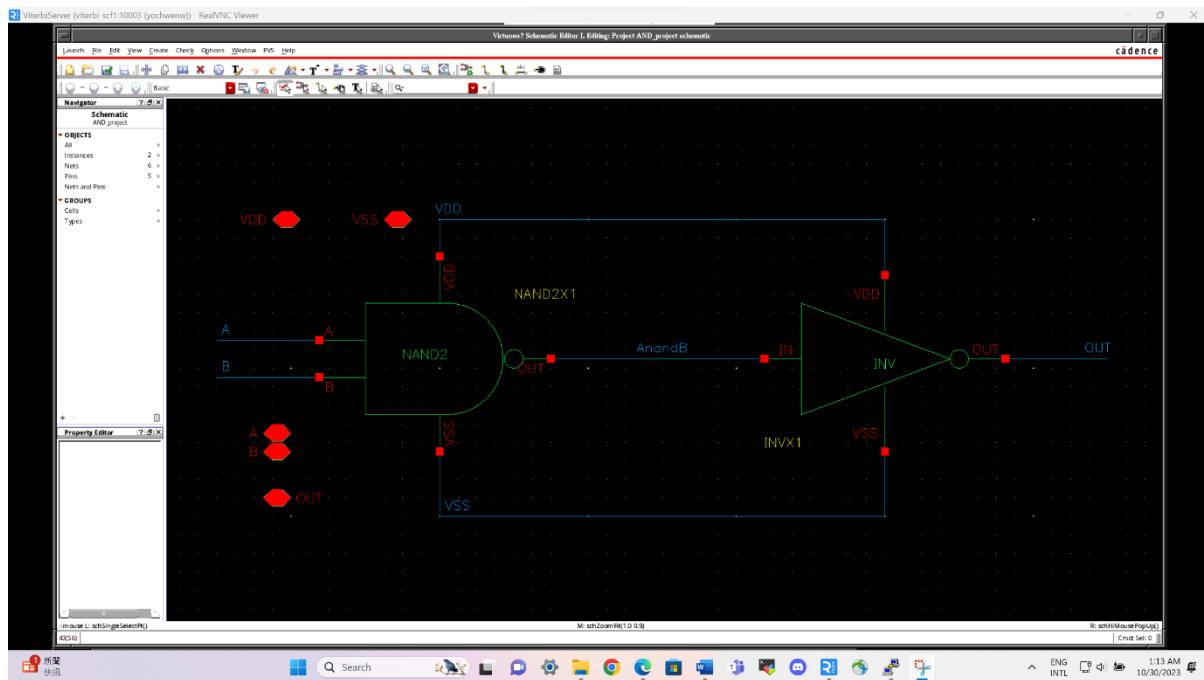
# Part 2: Multiplier Design

## Part 2: (2 Points)

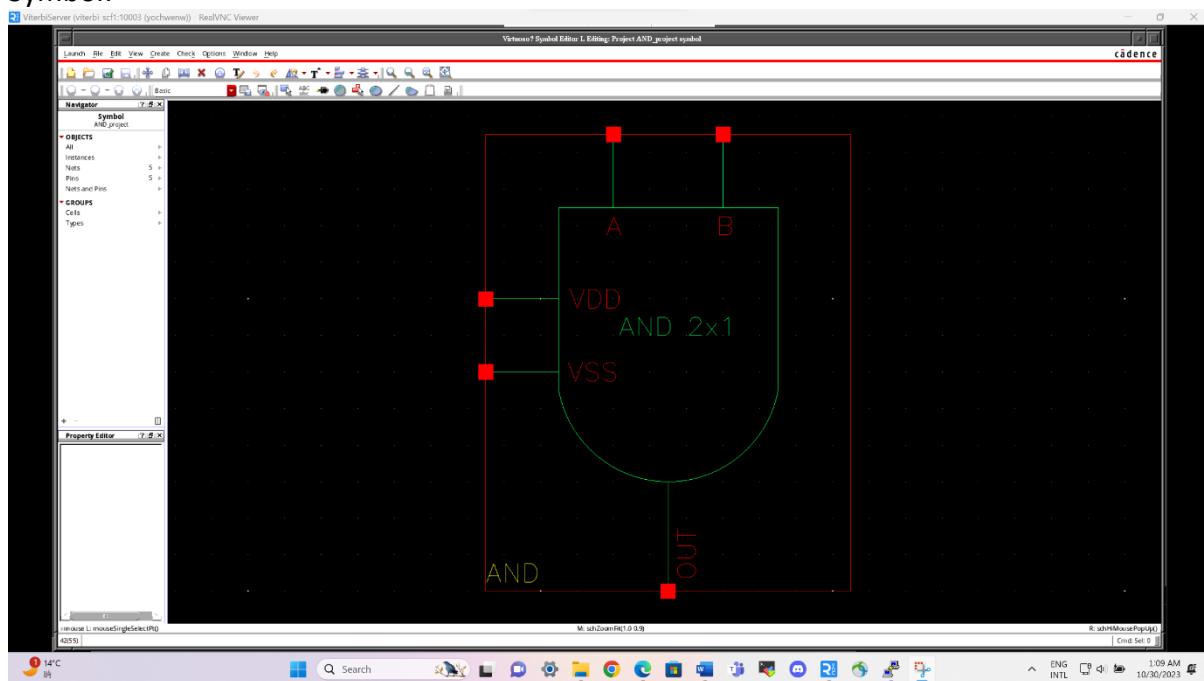
- Schematic and Symbol of AND gate. If you use subcircuits (e.g., NAND, INV, etc.), also provide screenshots of those subcircuits.
- Schematic and Symbol of HA. If you use subcircuits (e.g., XOR, AND, etc.), also provide screenshots of those subcircuits.
- Schematic and Symbol of the multiplier design.
- Functional verification for all 8 test cases using the delay testbench (multiple screenshots showing transient A, B, and Z signals with hex values).
- Delay measurement

## AND gate Design:

Schematic:

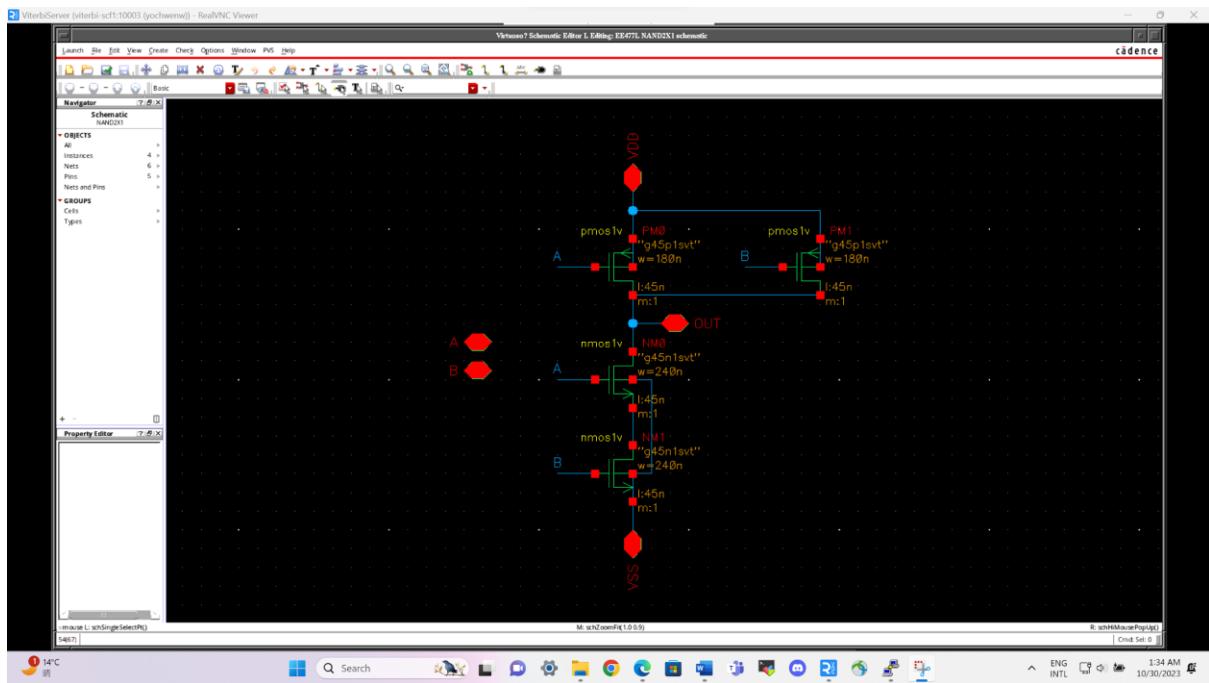


Symbol:

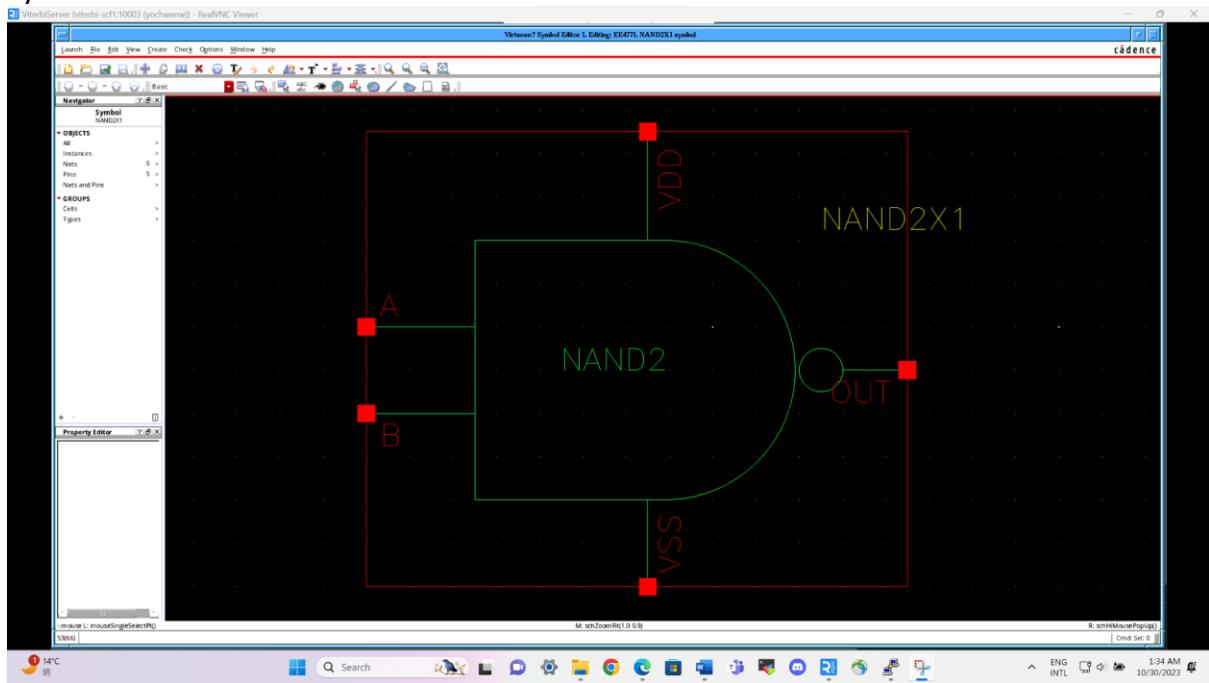


## NAND gate Design:

Schematic:

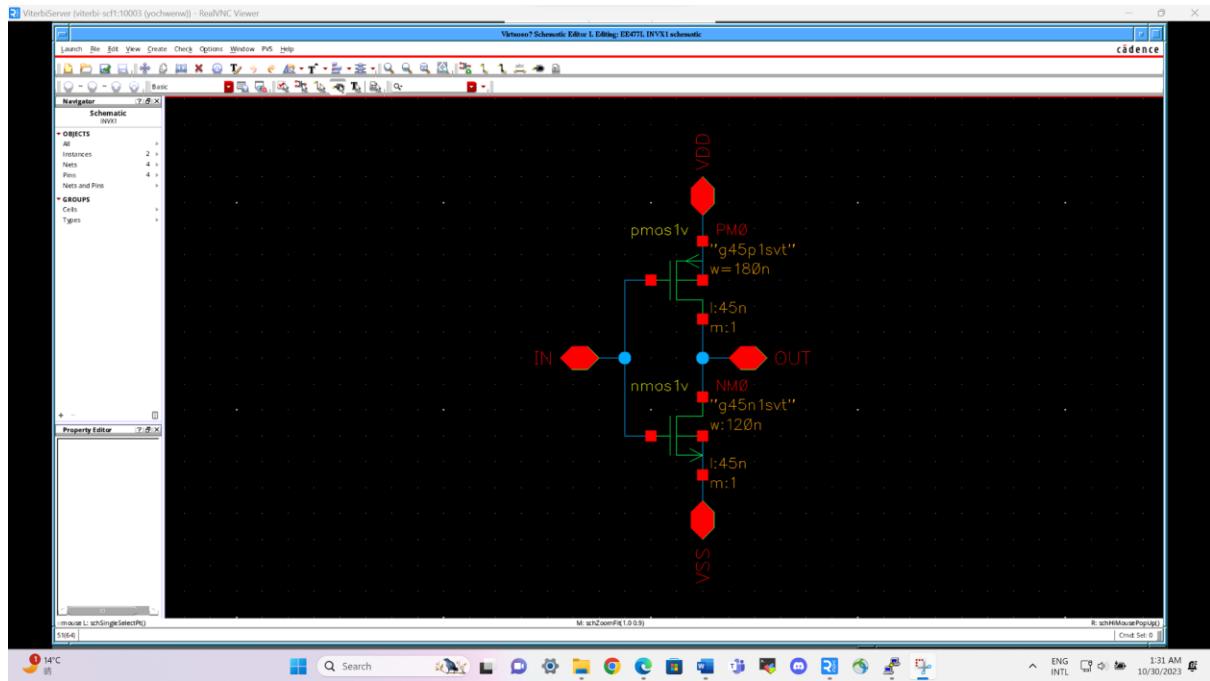


Symbol:

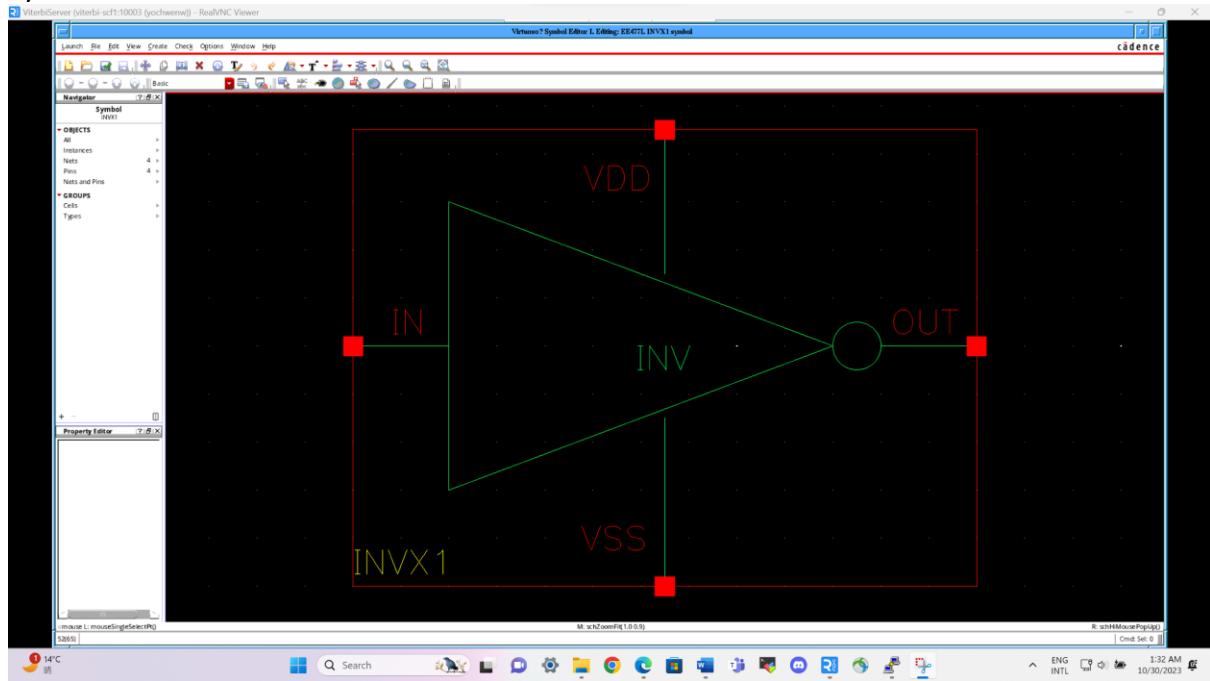


## INV gate Design:

### Schematic:

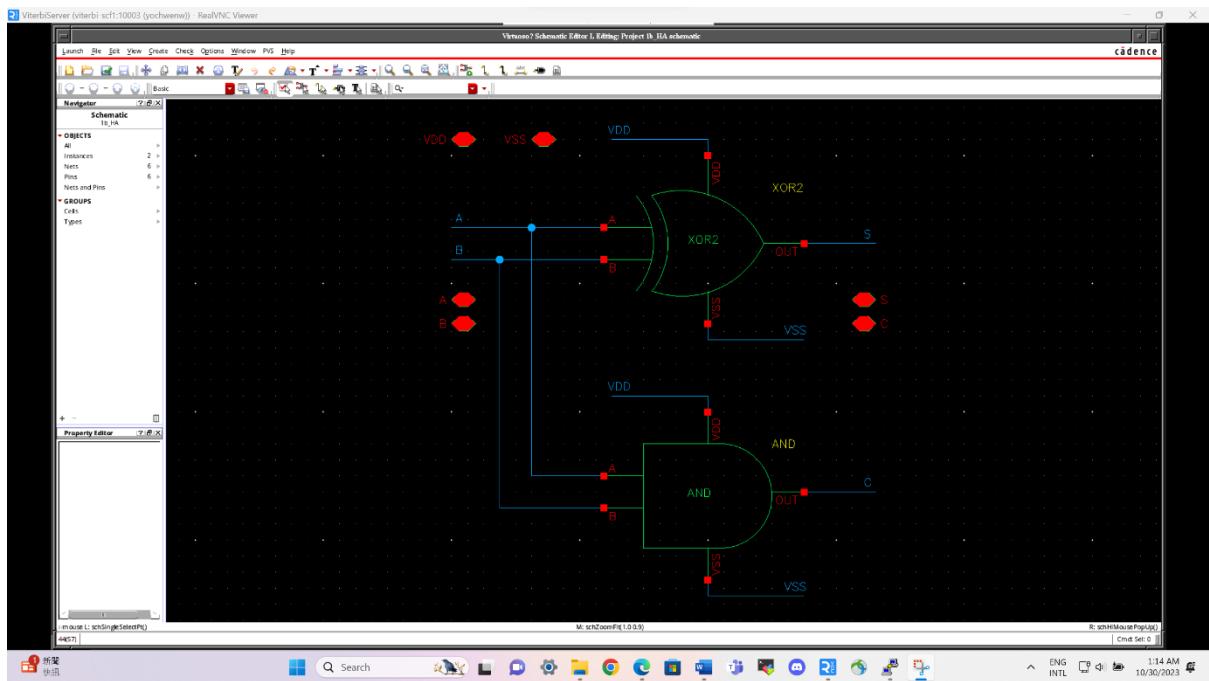


### Symbol:

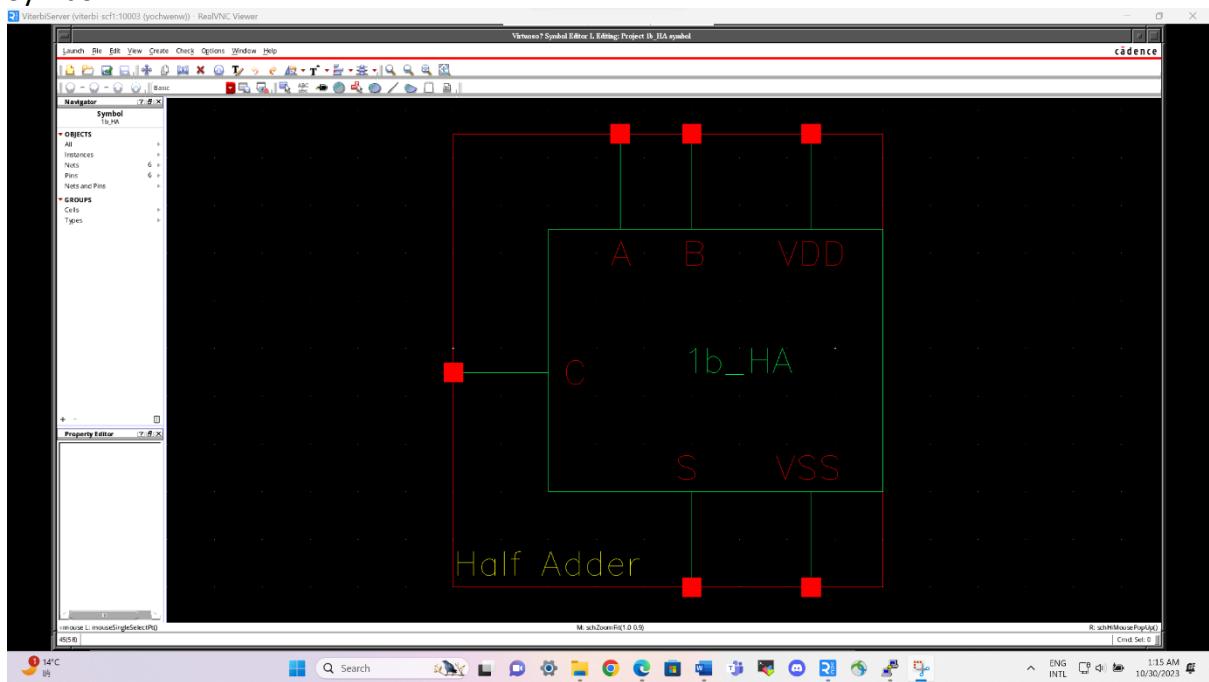


## Half Adder (HA) Design:

### Schematic:

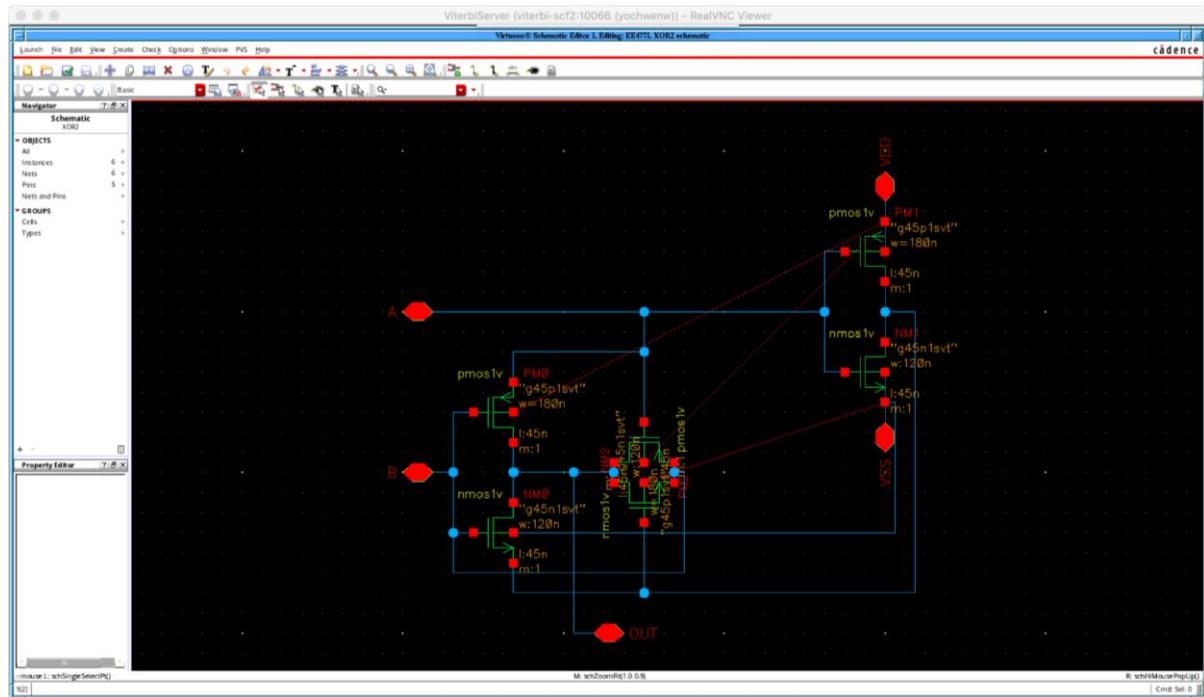


### Symbol:

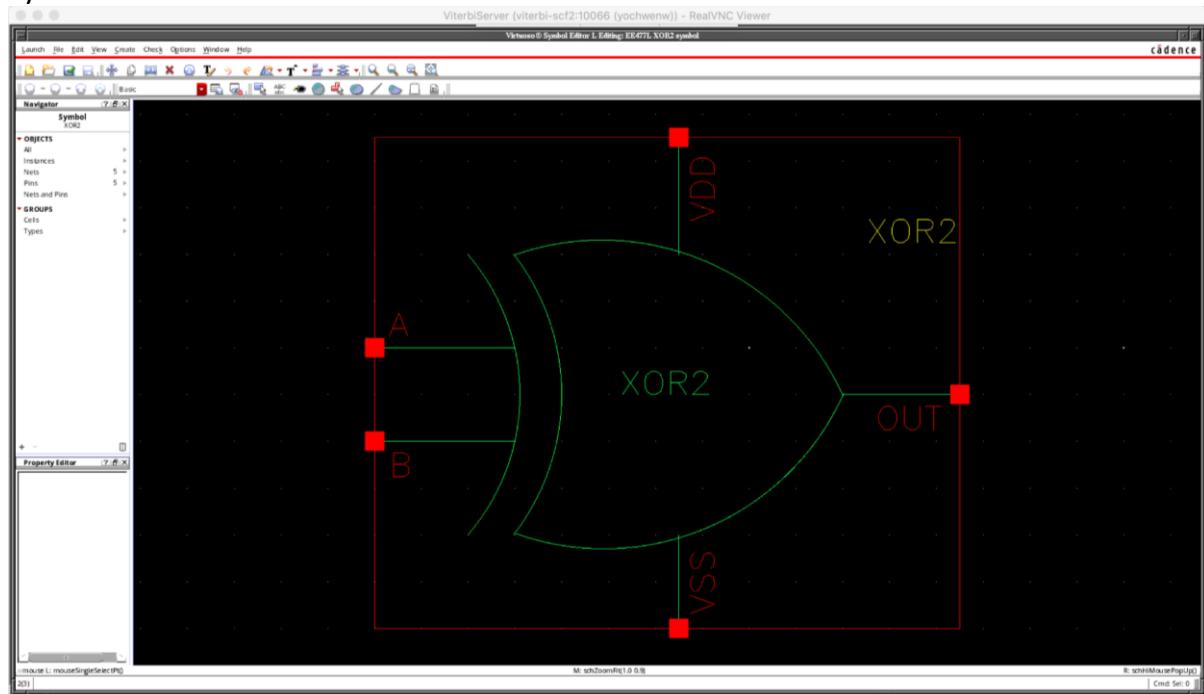


## XOR gate Design:

Schematic:

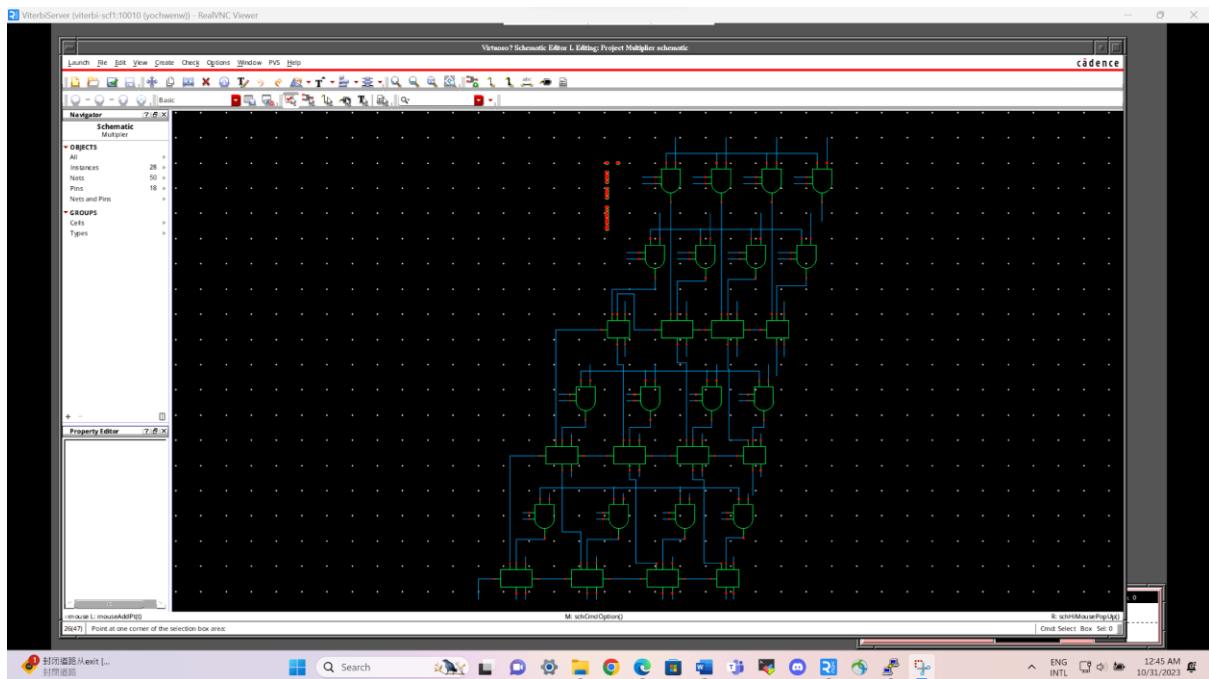


Symbol:

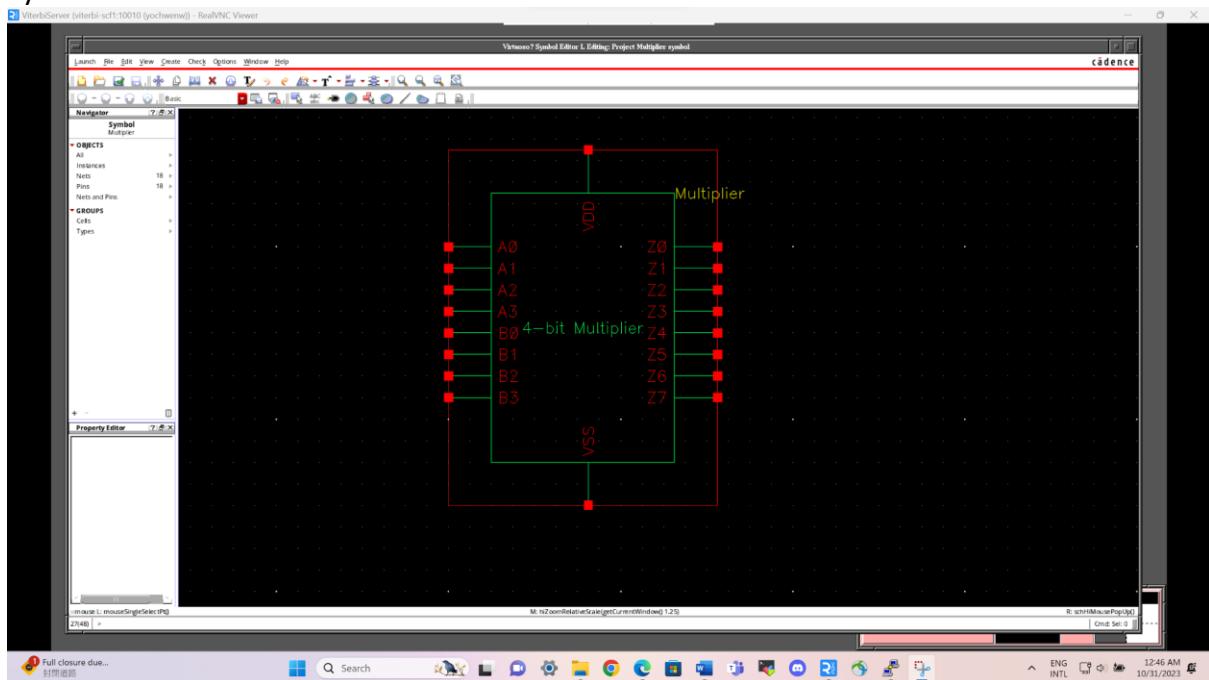


## 4-bit Multiplier Design:

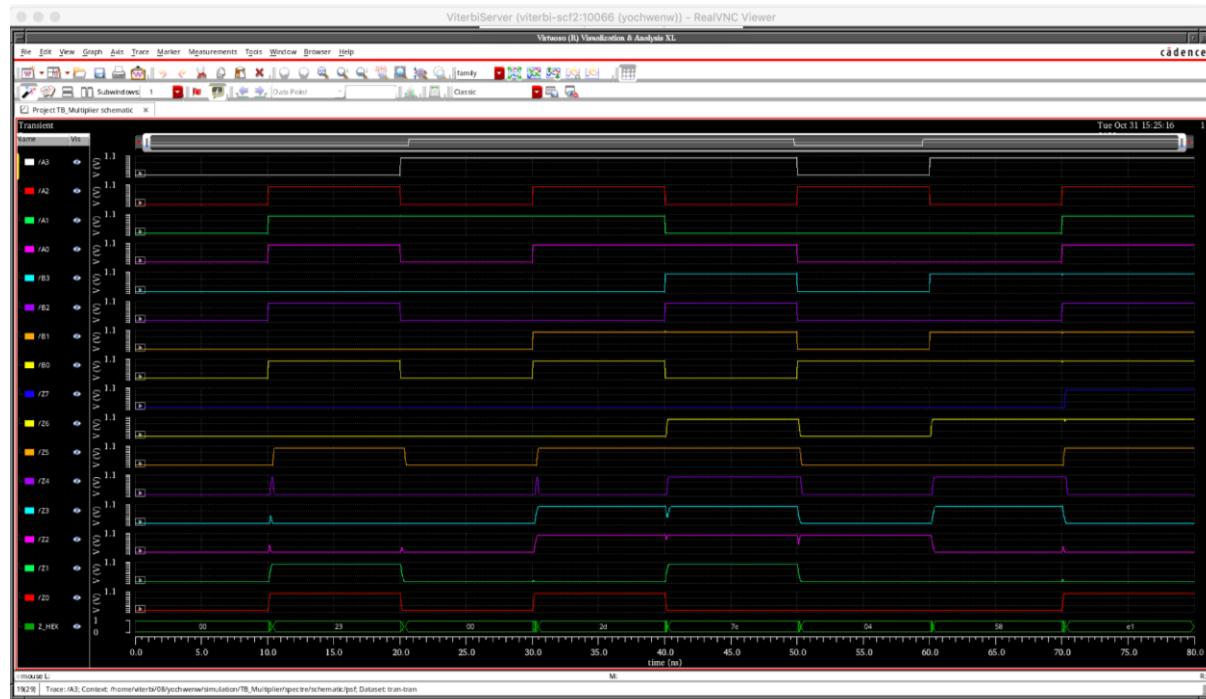
### Schematic:



### Symbol:



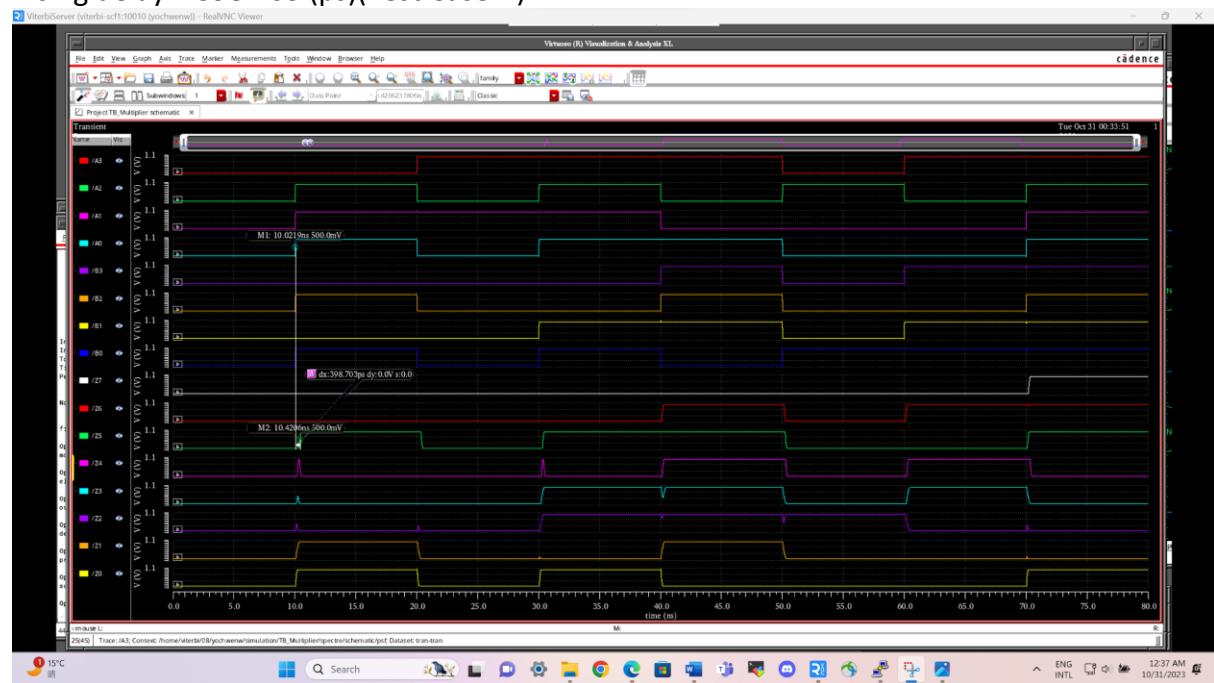
**Functional verification for all 8 test cases using the delay testbench:**



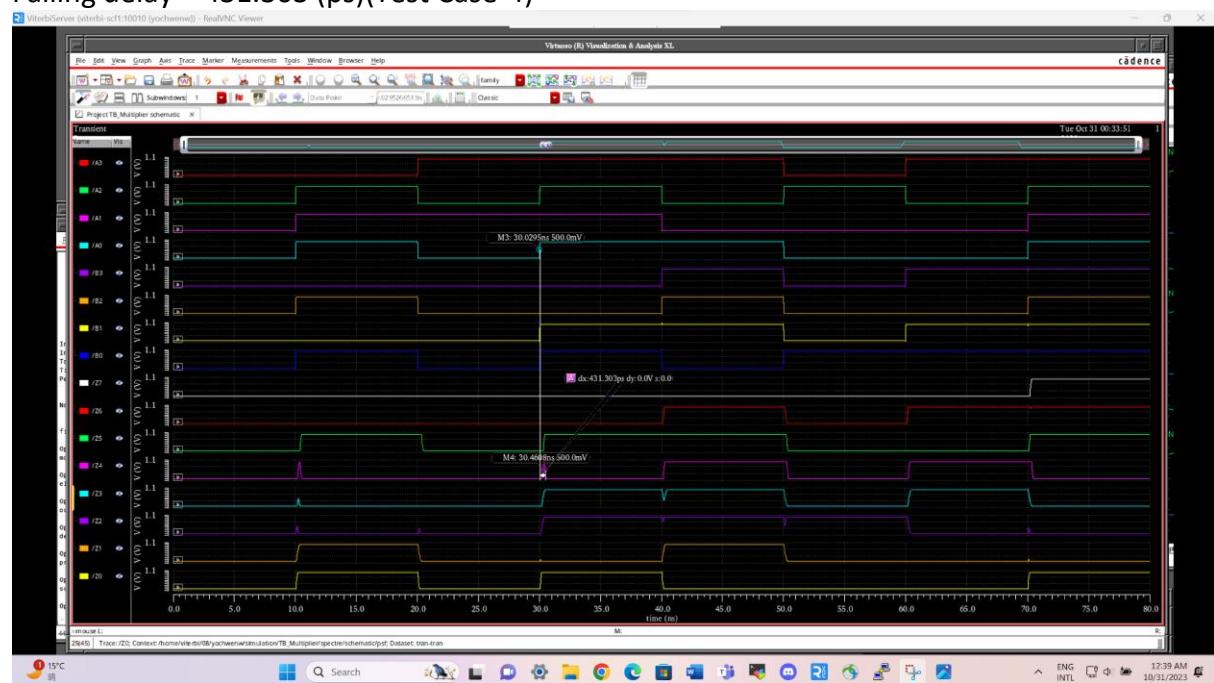
A[3:0]	B[3:0]	Z	A'	B'
0	0	<b>00 = 00000000</b>	F	F
7	5	<b>23 = 00100011</b>	8	A
A	0	<b>00 = 00000000</b>	5	F
F	3	<b>2D = 00101101</b>	0	C
9	E	<b>7E = 01111110</b>	6	1
4	1	<b>04 = 00000100</b>	B	E
8	B	<b>58 = 01011000</b>	7	4
F	F	<b>E1 = 11100001</b>	0	0

## Delay measurement:

Rising delay = 398.703 (ps)(Test Case-2)



Falling delay = 431.303 (ps)(Test Case-4)



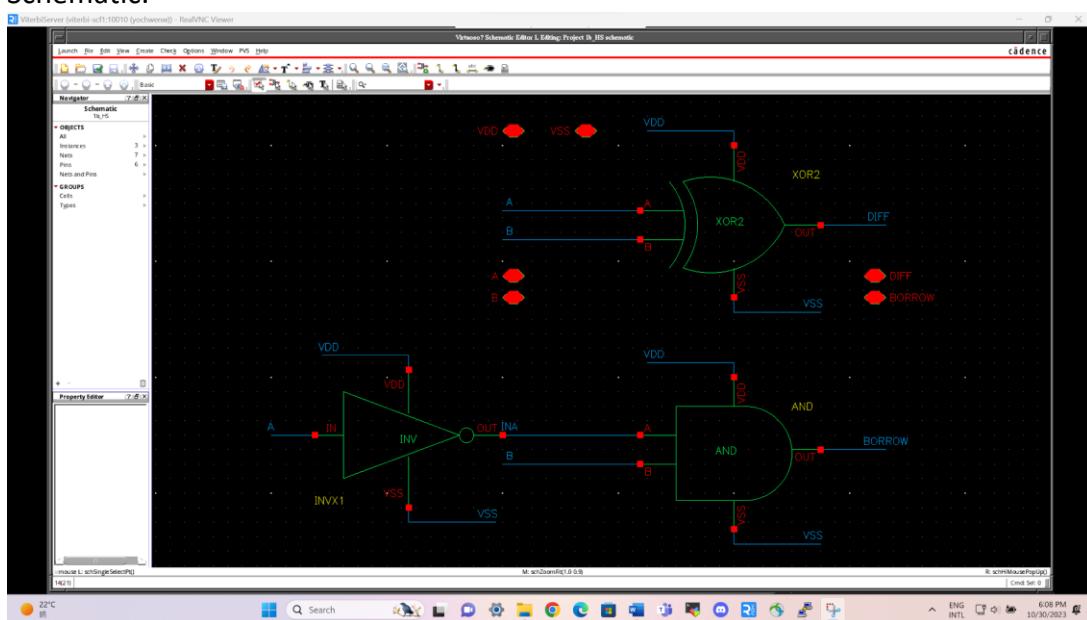
# Part 3: Divider Design

## Part 3: (3 Points)

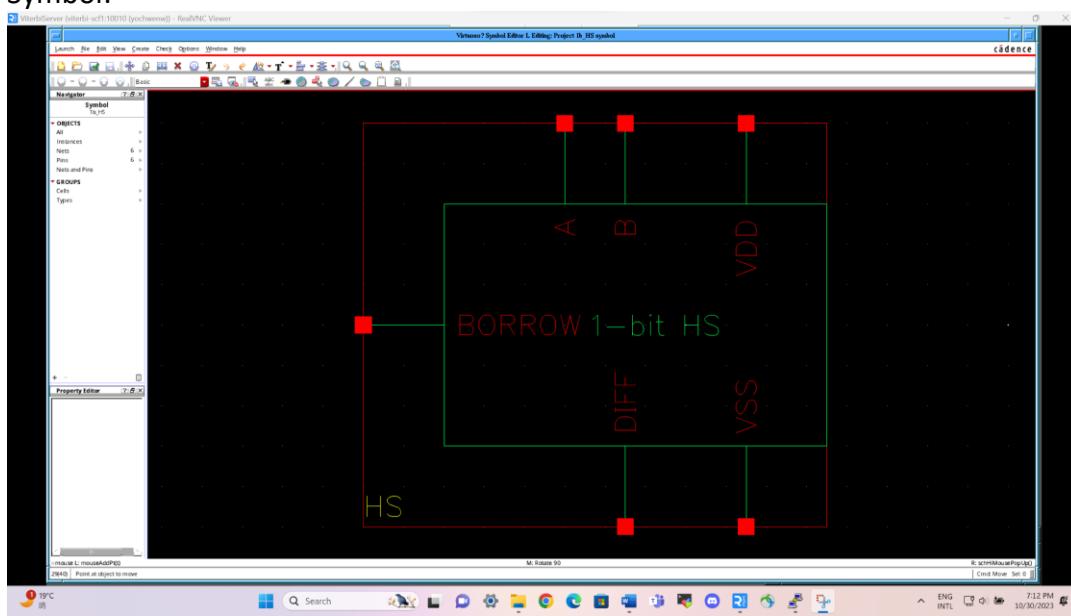
- Schematic, Symbol, and Functional Verification of Half-Subtractor (HS) circuit. Also, provide screenshots of any subcircuits used to design the HS.
- Schematic, Symbol, and Functional Verification of Full-Subtractor (FS) circuit. Also, provide screenshots of any subcircuits used to design the FS.
- Schematic, Symbol, and Functional Verification of 2-to-1 MUX circuit. Also, provide screenshots of any subcircuits used to design the MUX circuit.
- Schematic, Symbol, and Functional Verification of FS\_MUX circuit. Also, provide screenshots of any subcircuits used to design the FS\_MUX.
- Schematic, Symbol, and Functional Verification of HS\_MUX circuit. Also, provide screenshots of any subcircuits used to design the HS\_MUX.
- Schematic and Symbol of the divider design.
- Functional verification for all 8 test cases using the delay testbench (multiple screenshots showing transient D, d, Q, and R signals with hex values).
- Delay measurement

## Half-Subtractor (HS) Design:

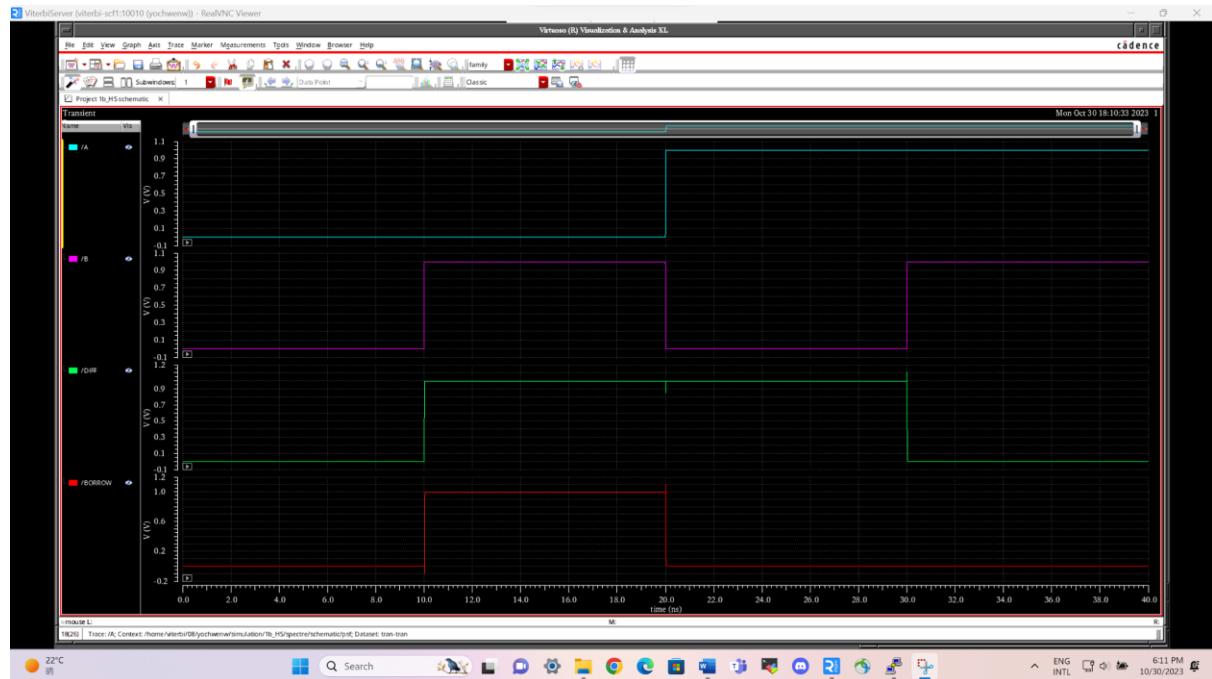
Schematic:



Symbol:

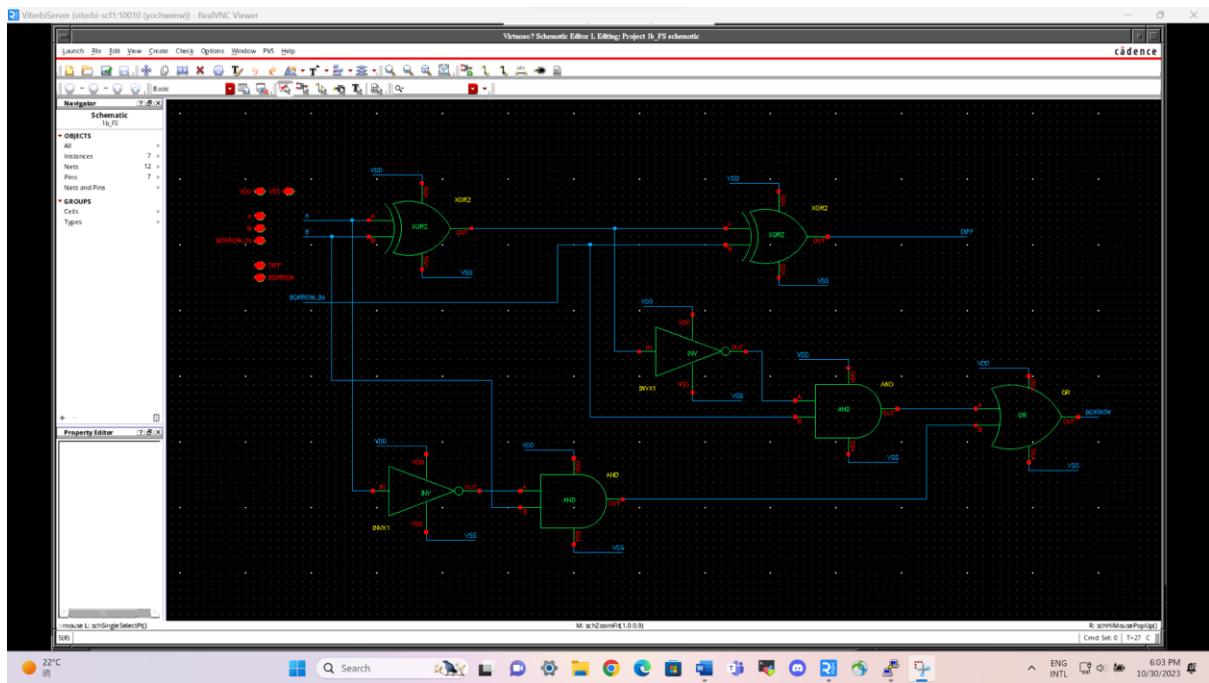


## Functional Verification of Half Subtractor:

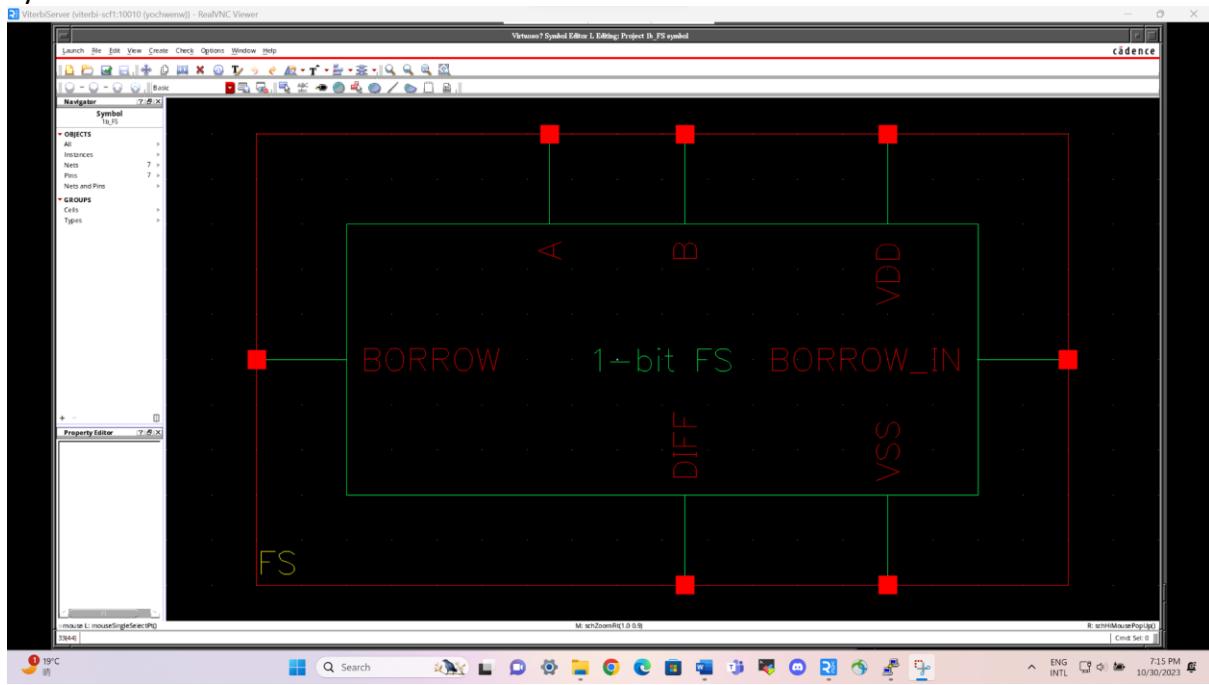


## Full-Subtractor (FS) Design:

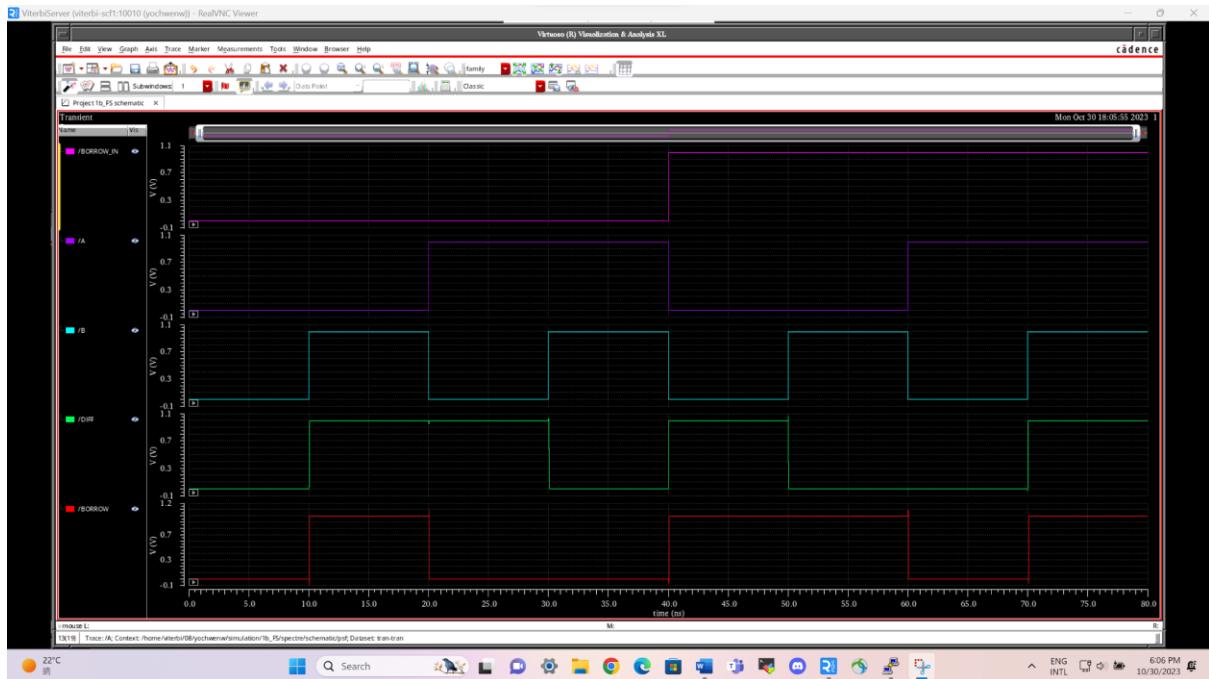
Schematic:



Symbol:

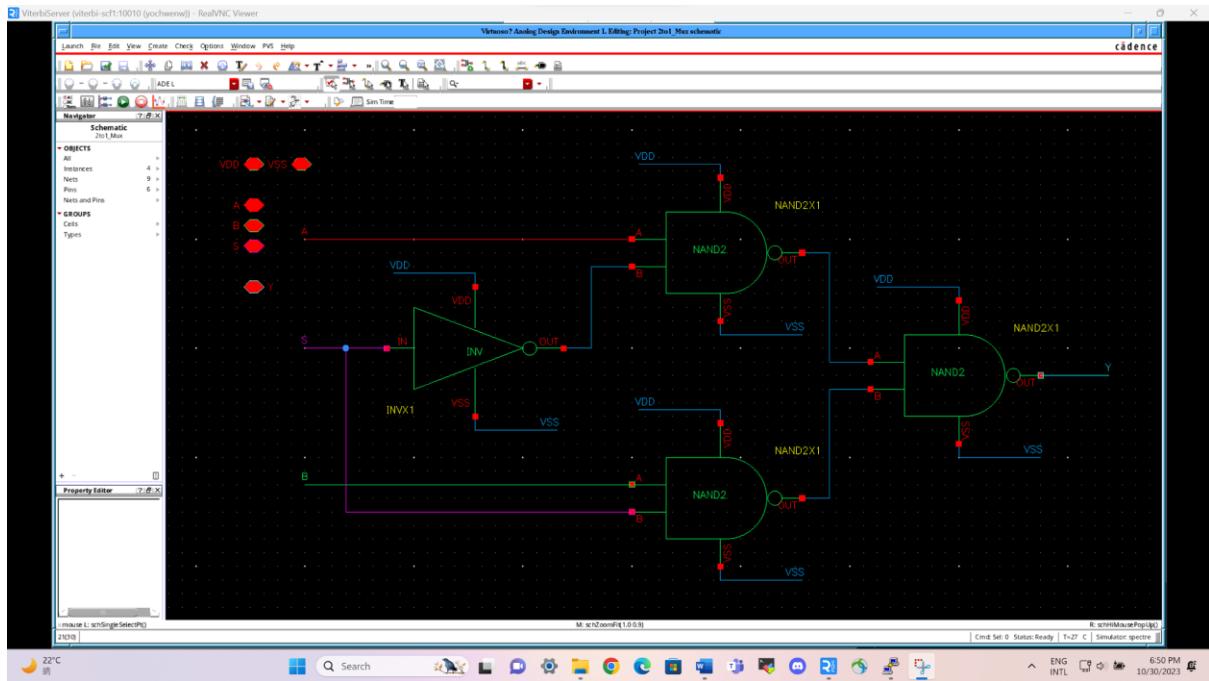


## Functional Verification of Full Subtractor:

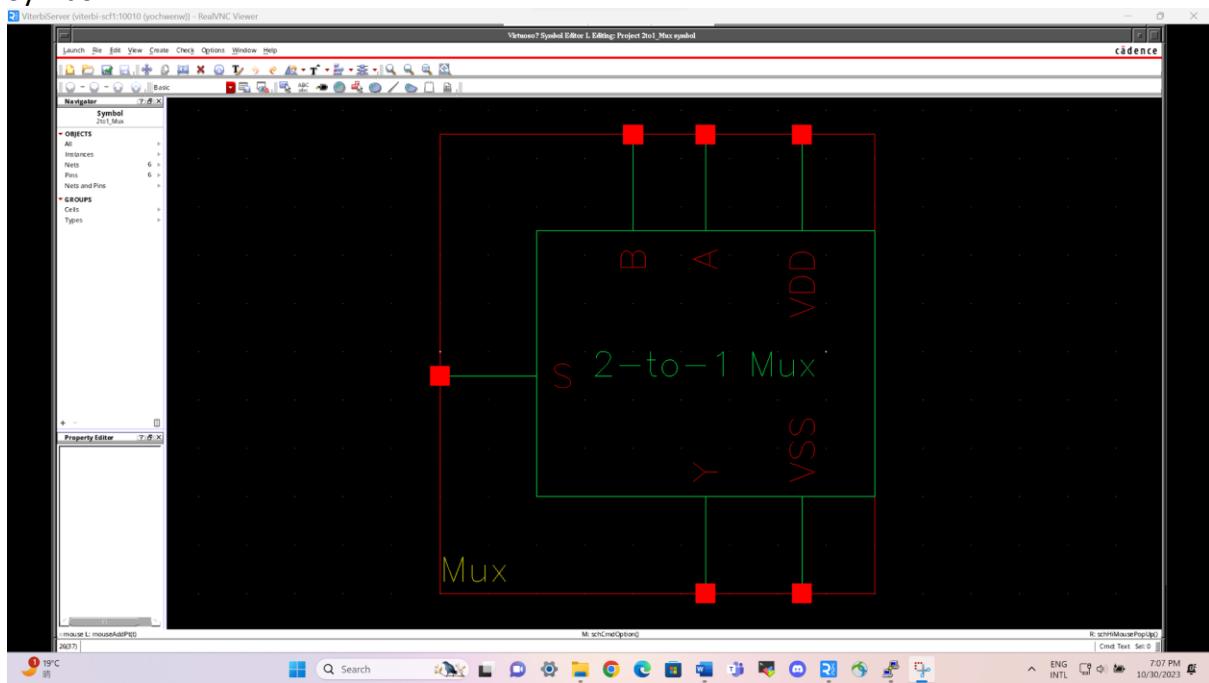


## 2-to-1 MUX Design:

Schematic:



Symbol:

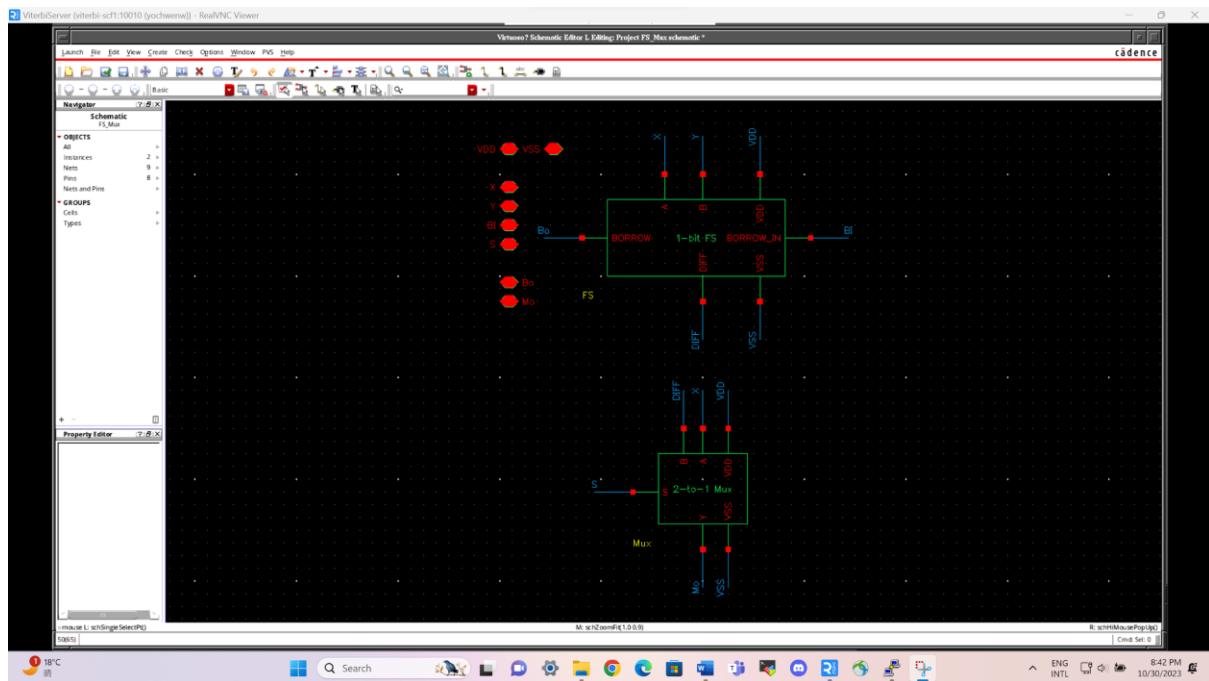


## Functional Verification of 2-to-1 mux:

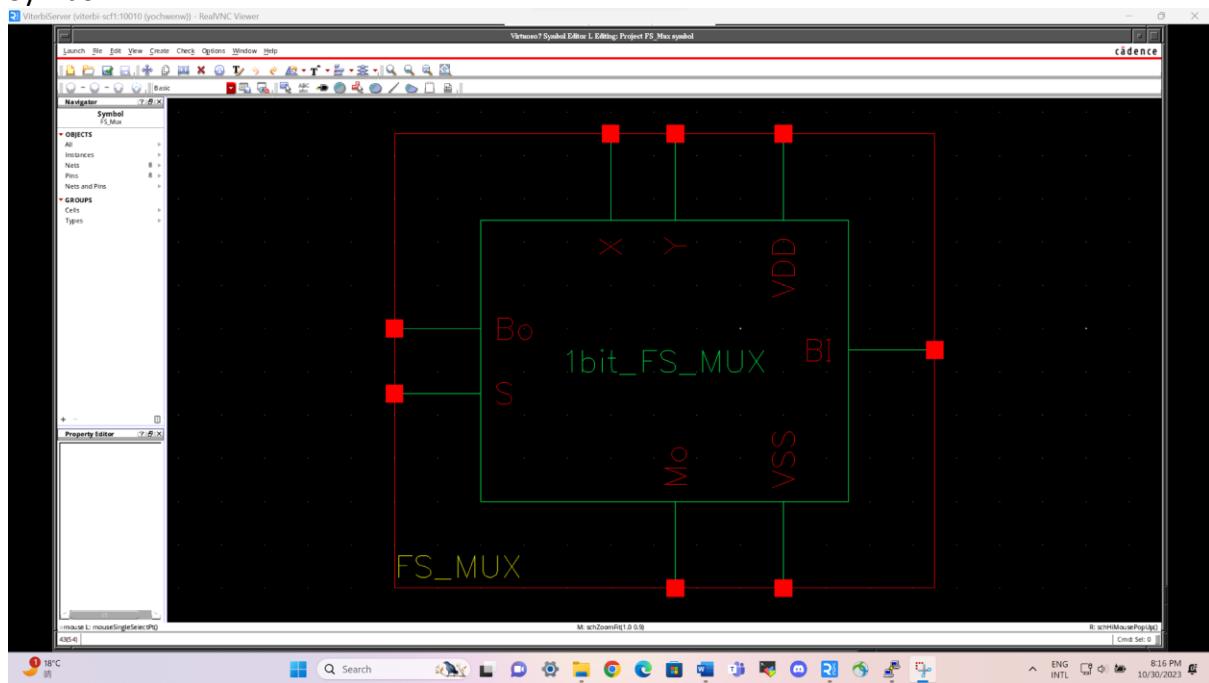


## **FS\_MUX circuit Design:**

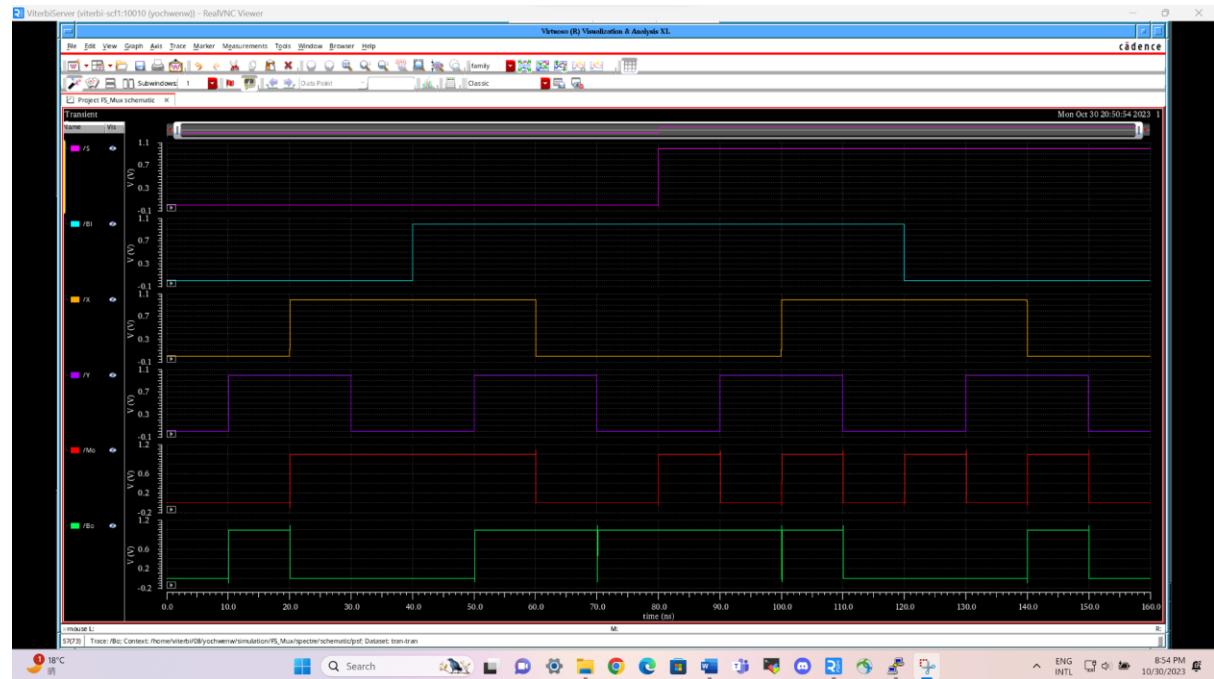
### Schematic:



### Symbol:

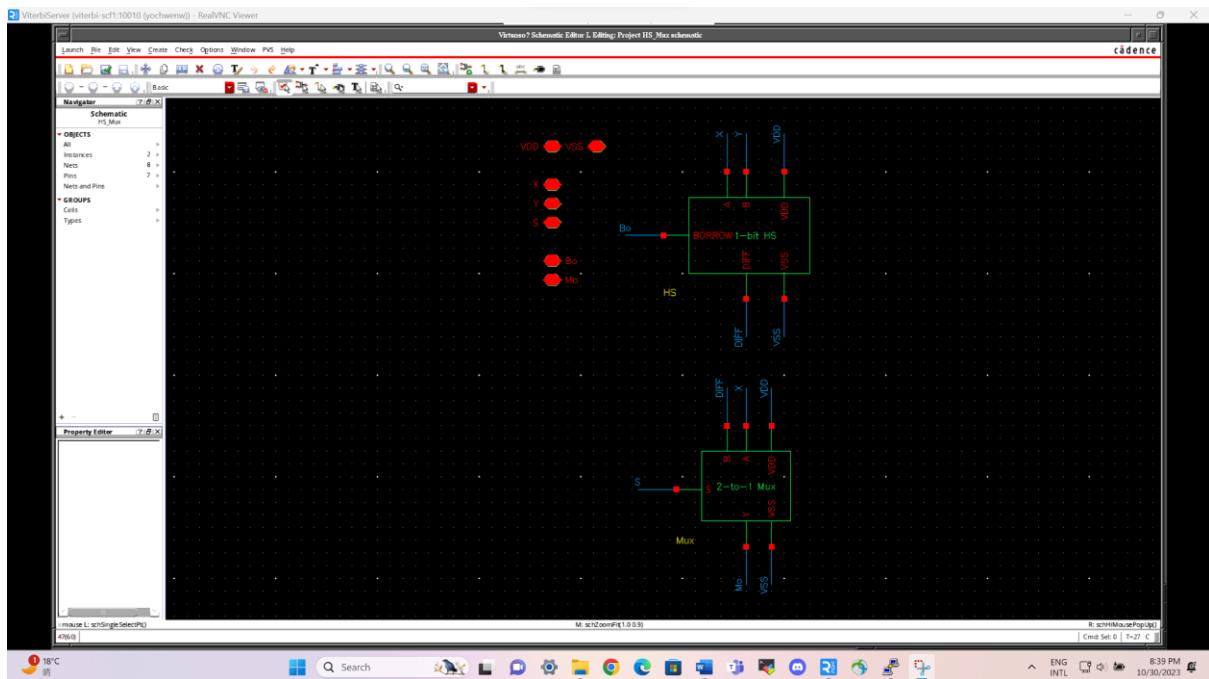


## Functional Verification FS mux:

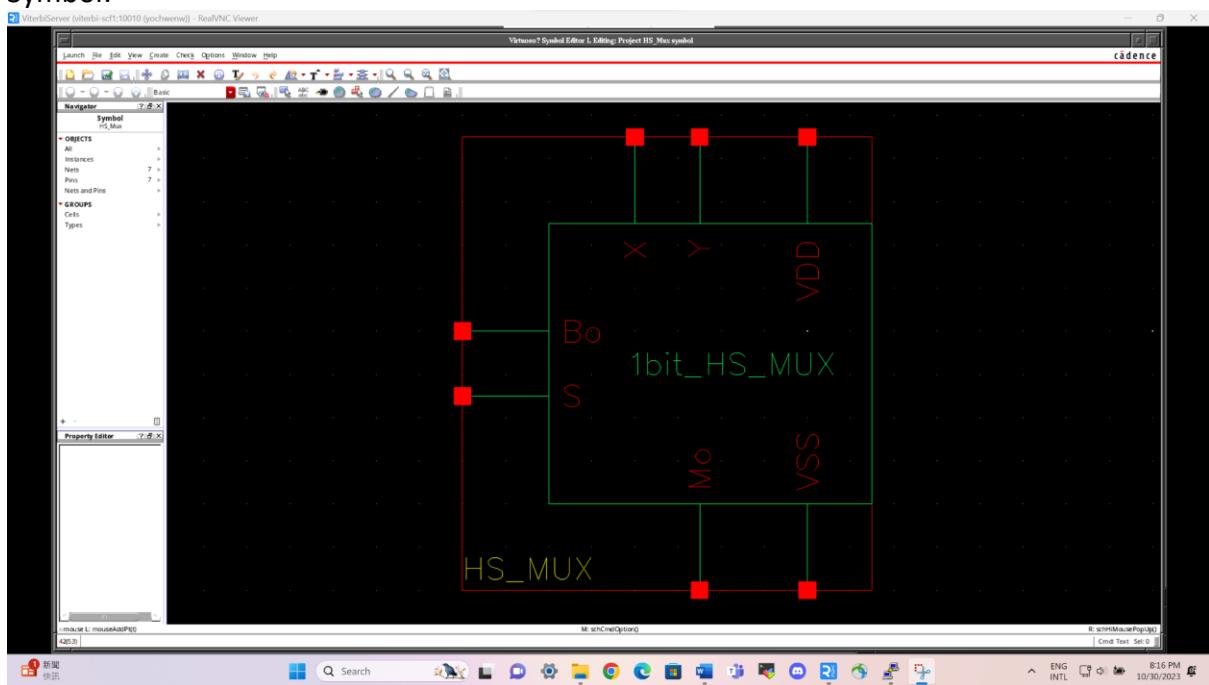


## HS\_MUX circuit Design:

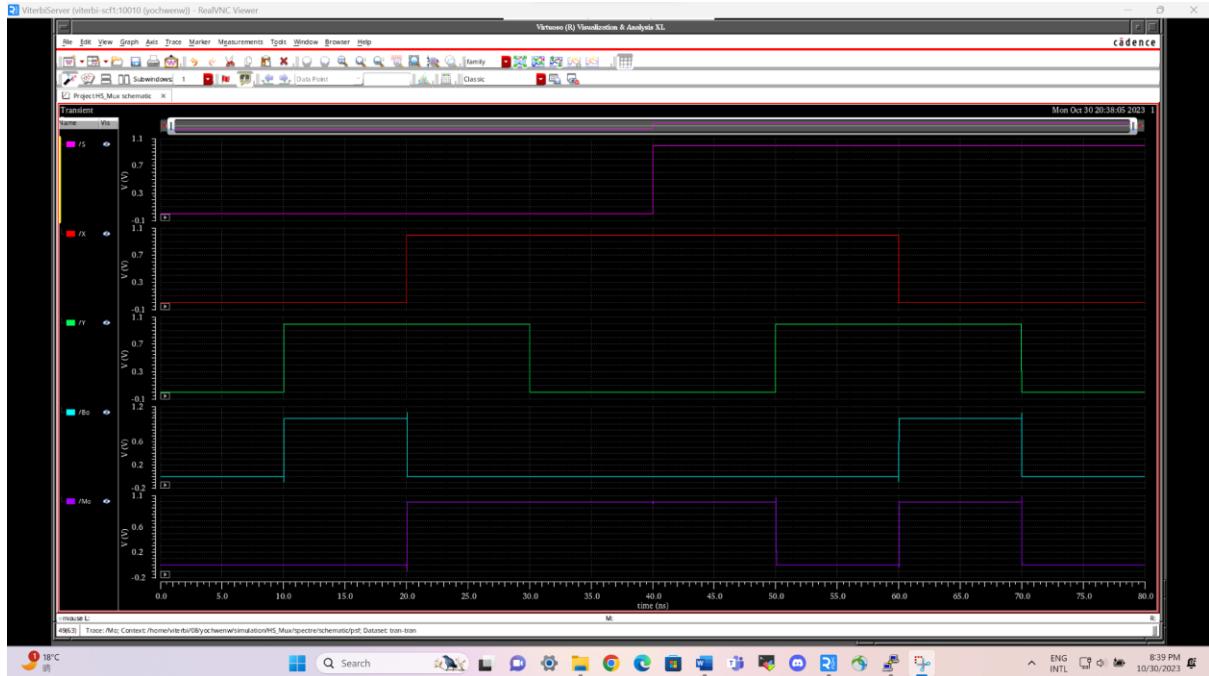
Schematic:



Symbol:

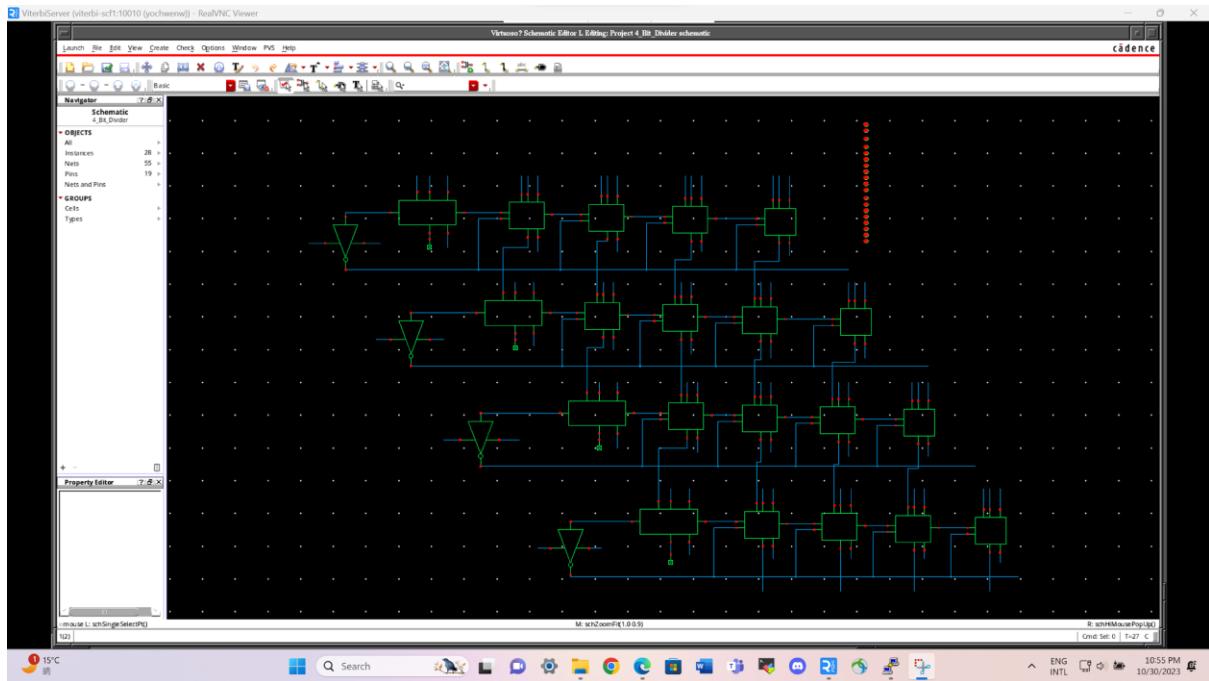


## Functional Verification of HS\_mux:

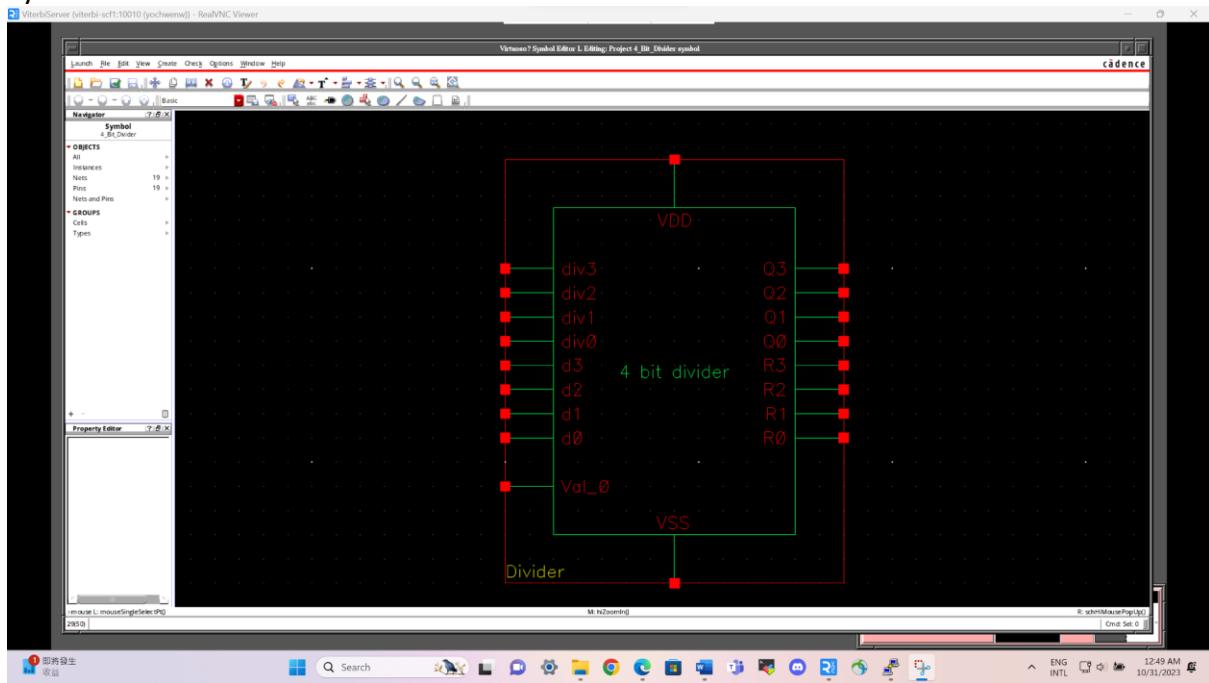


## 4-bit Divider Design:

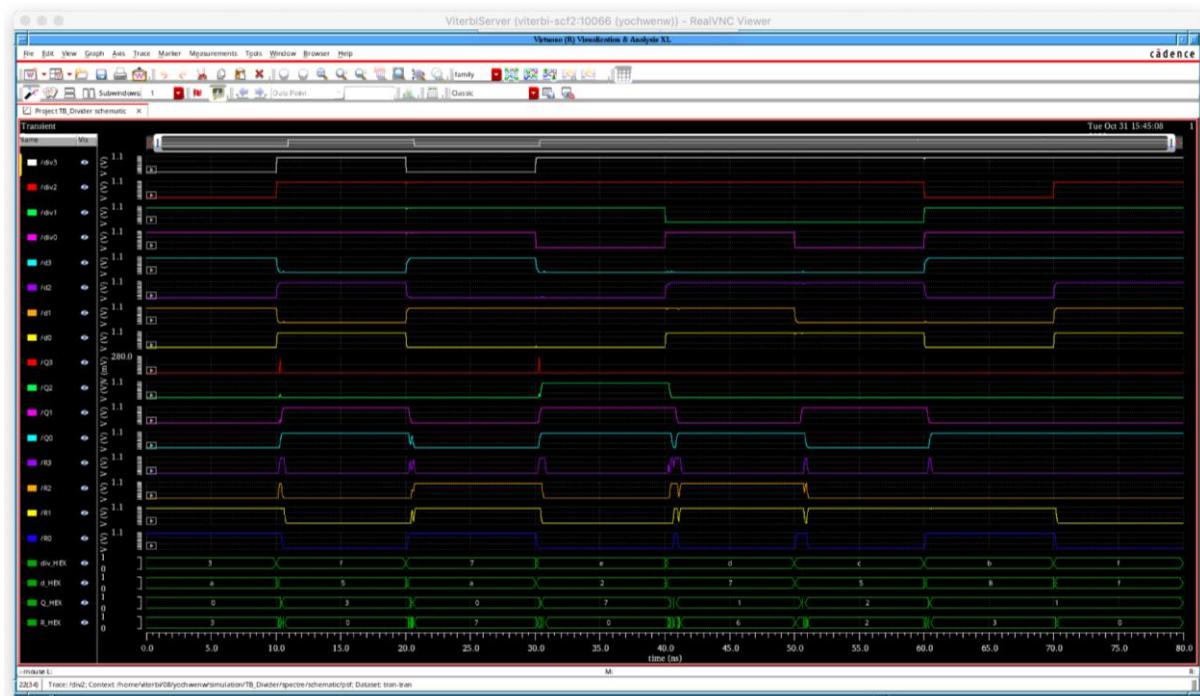
Schematic:



Symbol:



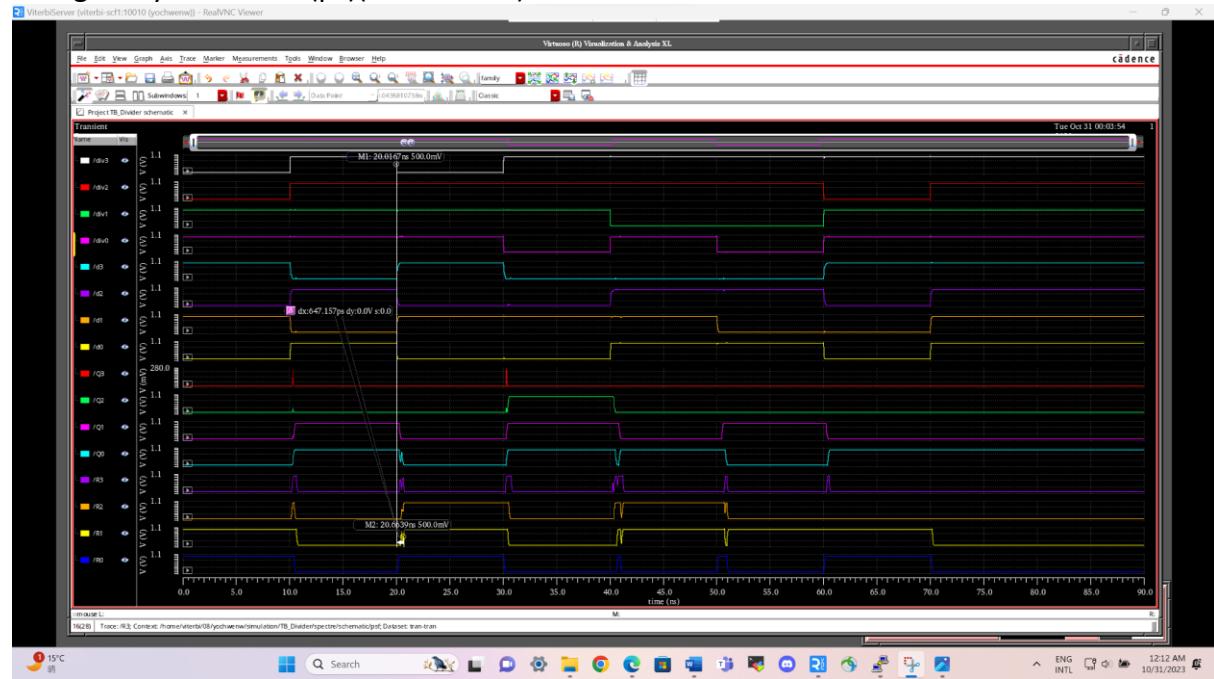
## Functional verification for all 8 test cases using the delay testbench:



<b>div[3:0]</b>	<b>d[3:0]</b>	<b>Q</b>	<b>R</b>
<b>3</b>	<b>A</b>	<b>0 = 0000</b>	<b>3 = 0011</b>
<b>F</b>	<b>5</b>	<b>3 = 0011</b>	<b>0 = 0000</b>
<b>7</b>	<b>A</b>	<b>0 = 0000</b>	<b>7 = 0111</b>
<b>E</b>	<b>2</b>	<b>7 = 0111</b>	<b>0 = 0000</b>
<b>D</b>	<b>7</b>	<b>1 = 0001</b>	<b>6 = 0110</b>
<b>C</b>	<b>5</b>	<b>2 = 0010</b>	<b>2 = 0010</b>
<b>B</b>	<b>8</b>	<b>1 = 0001</b>	<b>3 = 0011</b>
<b>F</b>	<b>F</b>	<b>1 = 0001</b>	<b>0 = 0000</b>

## Delay measurement:

Rising delay = 647.157 (ps)(Test Case-3)



Falling delay = 1.24897 (ns)(Test Case-5)

