

University of Southern California

Viterbi School of Engineering

EE477L

MOS VLSI Circuit Design

**Phase 3 Project Report:
Multiplier and Divider Design**

**Li-Wei (Richard) Liu 5297015518
Hung-Ting (Andrew) Tsai 4995041703
Yo-Chwen Wang 8331269140**

Professor: Dr. Shahin Nazarian

Due Date: 11/28/2023

Performance Metrics Number

PAD Table:

metal layer used: 5

| | Schematic | Extracted |
|--------------|------------------|------------------------|
| Power | 163.1 uW | 123.2 uW |
| Area | x | 0.00116 mm^2 |
| Delay | 1.4 ns | 1.4 ns |

PAD number:

$$\text{PAD} = \text{Power (P)} * \text{Area (A)} * \text{Delay (D)} = 123.2 \text{ uW} * 0.00116 \text{ mm}^2 * 1.4 \text{ ns}$$

$$\text{PAD} = \textbf{0.200} (\text{uW} * \text{mm}^2 * \text{ns})$$

Work Distribution Table:

Throughout the project, tasks were evenly distributed to each teammate, and we were able to help each other while doing functional verification and merging each subpart.

| Hung-Ting (Andrew) Tsai | Li-Wei Liu | Yo-Chwen Wang |
|--|--|--|
| Phase 1 | | |
| HA/FA design | 2-1 mux | Half Subtractor/ Full Subtractor |
| Multiplier Design | Functional Verification for Multiplier and Divider | Divider Design |
| Delay Measurement | Delay Measurement | Delay Measurement |
| Phase 2 | | |
| FSM design | FSM design | FSM design |
| 1-bit DFF | Arbiter | Arbiter |
| Complete System Schematics (draw, confirm, functional verification, and time delay measurements) | Complete System Schematics (draw, confirm, functional verification, and time delay measurements) | Complete System Schematics (draw, confirm, functional verification, and time delay measurements) |
| Phase 3 | | |
| DFF, 8 bit DFF | And/OR gate | Half adder |
| 2-1 mux, 8 bit 2-1 mux | Full adder | Half Subtractor, Full Subtractor/ FS Mux |
| Full adder | Multiplier | Divider |
| Functional Verification for past design, Complete System Layout | Complete system layout | Complete system layout |
| PAD, complete system verification | PAD, complete system verification | PAD, complete system verification |

Table of Contents

| | |
|---|-----------|
| Performance Metrics Number | 2 |
| Table of Contents | 4 |
| Part 0: System Overview | 5 |
| Part 1: Layout Design and Post-Layout Verification | 6 |
| Multiplier design: | 6 |
| 1-bit Half Adder (HA) Design: | 6 |
| 1-bit Full Adder (FA) Design: | 8 |
| AND Design: | 9 |
| Multiplier Design: | 11 |
| Divider design: | 13 |
| 1-bit Half Subtractor (HS) Design: | 13 |
| 1-bit Full Subtractor (FS) Design: | 14 |
| 2-to-1 MUX Design: | 16 |
| HS_MUX Design: | 17 |
| FS_MUX Design: | 19 |
| OR Design: | 20 |
| Divider Design: | 22 |
| Arbiter Design: | 24 |
| 1-bit DFF: | 25 |
| 8-bit DFF: | 27 |
| 8-bit 2-to-1_MUX Design: | 28 |
| Complete system Design: | 30 |
| Part 1.5: Post-Layout Verification | 32 |
| Post-layout functional verification: Multiplier: | 32 |
| Post-layout functional verification: Divider: | 33 |
| Post-layout functional verification: Arbiter: | 34 |
| Post-layout functional verification: DFF: | 34 |
| Post-layout functional verification: Complete System: | 35 |
| Part 2: Performance Metrics Calculation | 36 |
| Area measurement: | 36 |
| Average Delay measurement: | 37 |
| Average power measurement: | 38 |
| PAD Table: | 39 |
| PAD number: | 39 |
| Appendix | 40 |
| Vector files for post layout functional verification testing: | 40 |
| Work Distribution Table: | 43 |

Part 0: System Overview

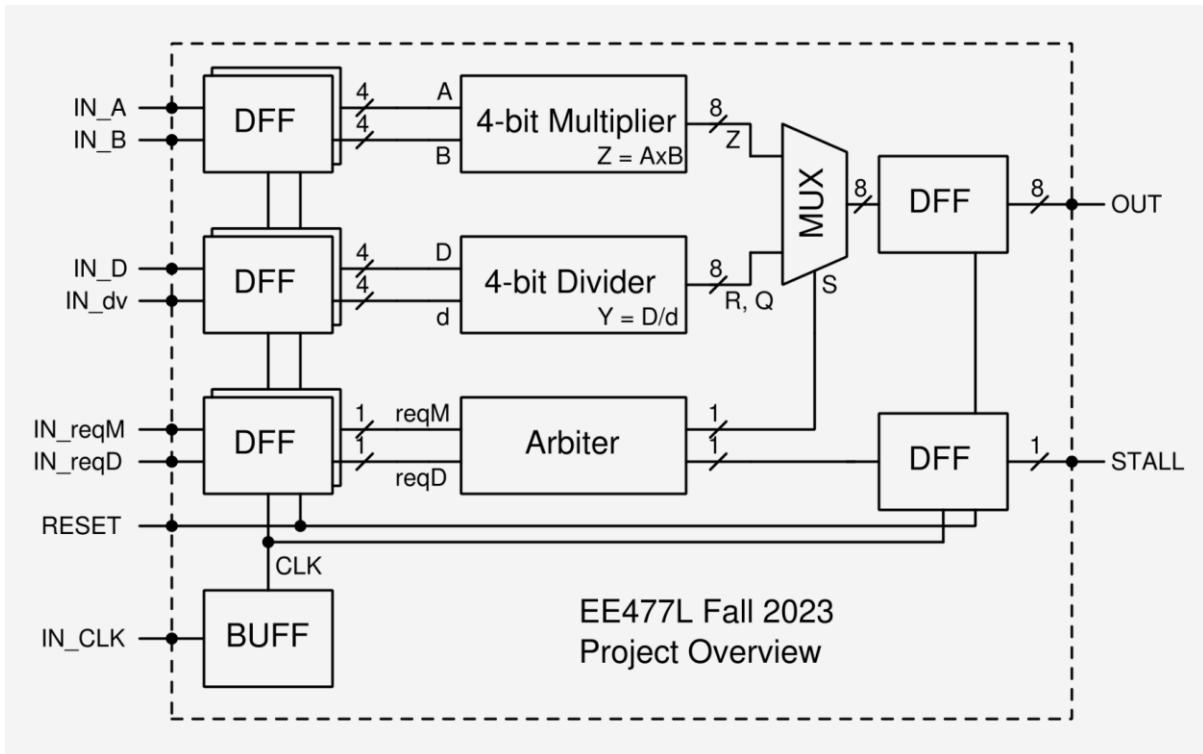


Figure 0: Overall System Block Diagram

Part 1: Layout Design and Post-Layout Verification

Part 1: (7 Point)

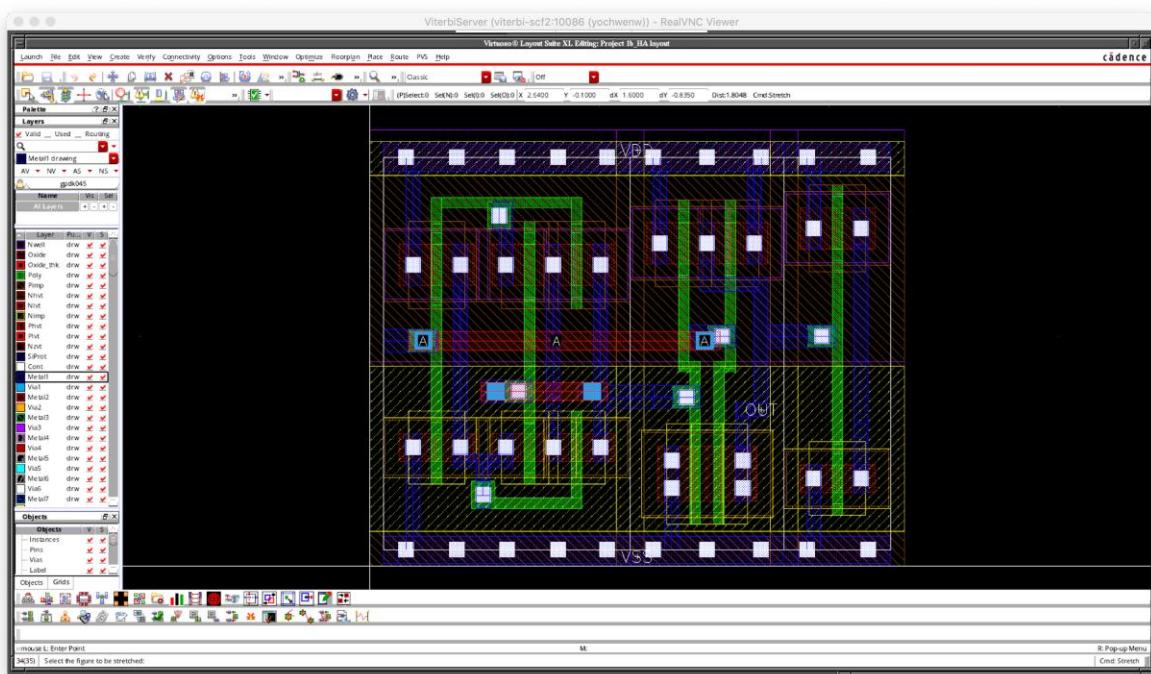
- Screenshots of the layout, DRC, and LVS window for each subblock (e.g., HA, FA, AND, etc.) of the multiplier.
- Screenshots of the layout, DRC, and LVS window of the multiplier.
- Post-layout functional verification of the multiplier.
- Screenshots of the layout, DRC, and LVS window for each subblock (e.g., HS, FS, MUX, HS_MUX, FS_MUX, OR, etc.) of the divider.
- Screenshots of the layout, DRC, and LVS window of the divider.
- Post-layout functional verification of the divider.
- Screenshots of the layout, DRC, and LVS window of the arbiter.
- Post-layout functional verification of the arbiter.
- Screenshots of the layout, DRC, and LVS window of the other subblocks (e.g., DFF, MUX, Buffer, etc.).
- Screenshots of the layout, DRC, and LVS window of the complete system.
- Post-layout (extracted) functional verification of the complete system.

Note: If you make any changes to optimize any of the subblocks, then please attach screenshots of the layout, DRC, and LVS window for each subblock.

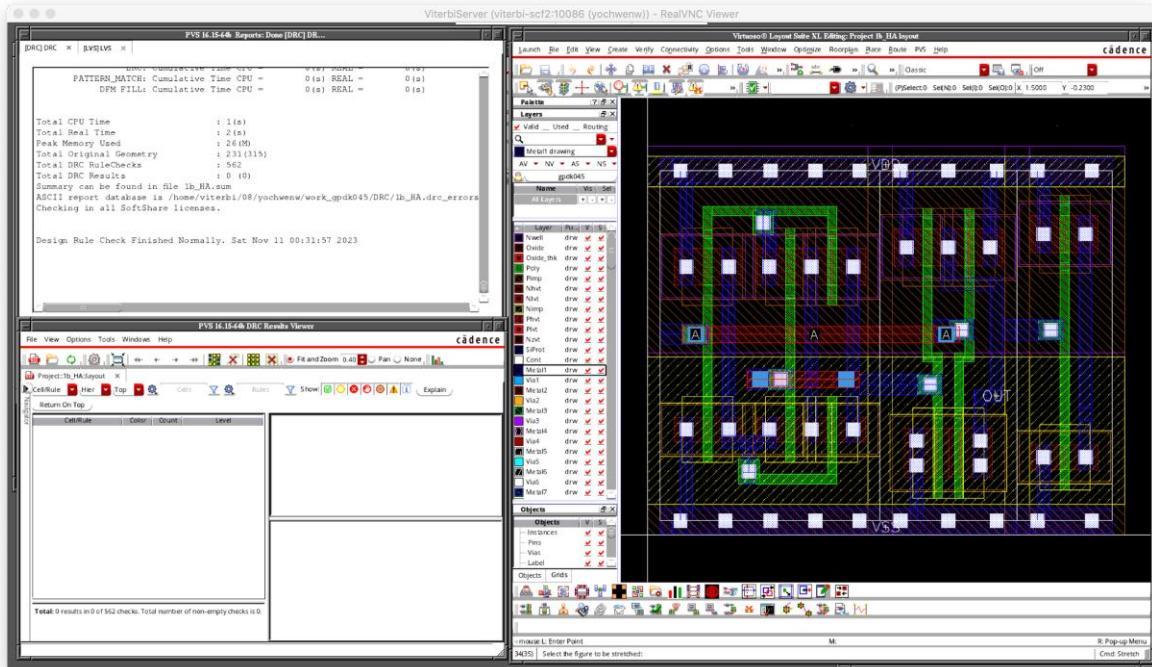
Multiplier design:

1-bit Half Adder (HA) Design:

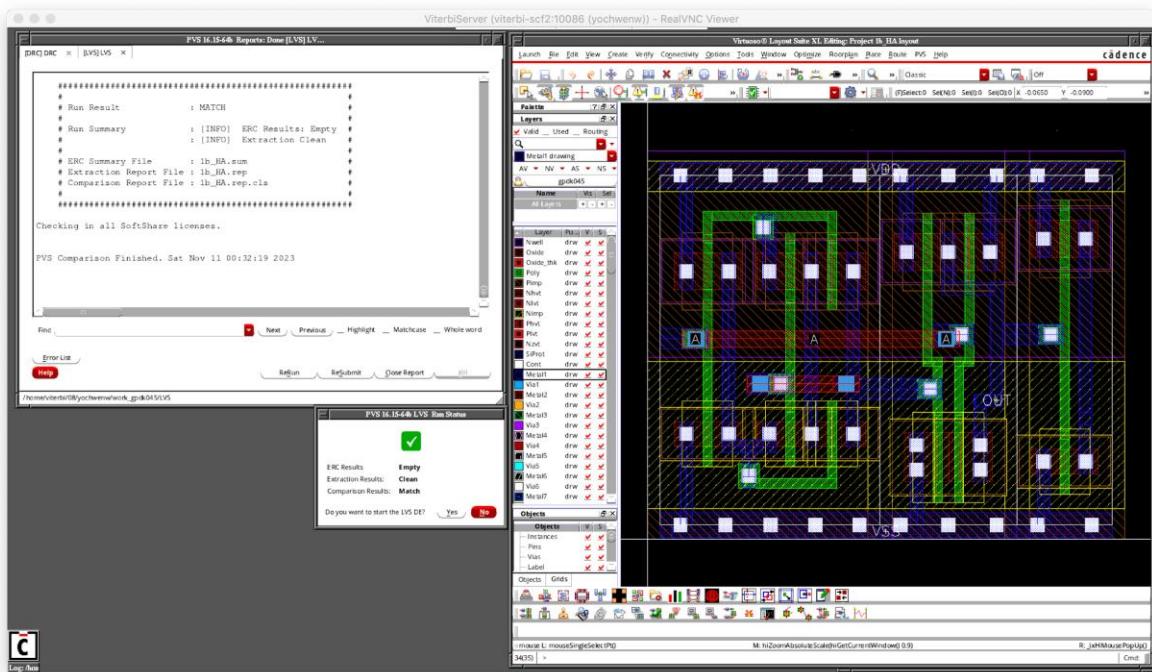
Layout:



DRC:

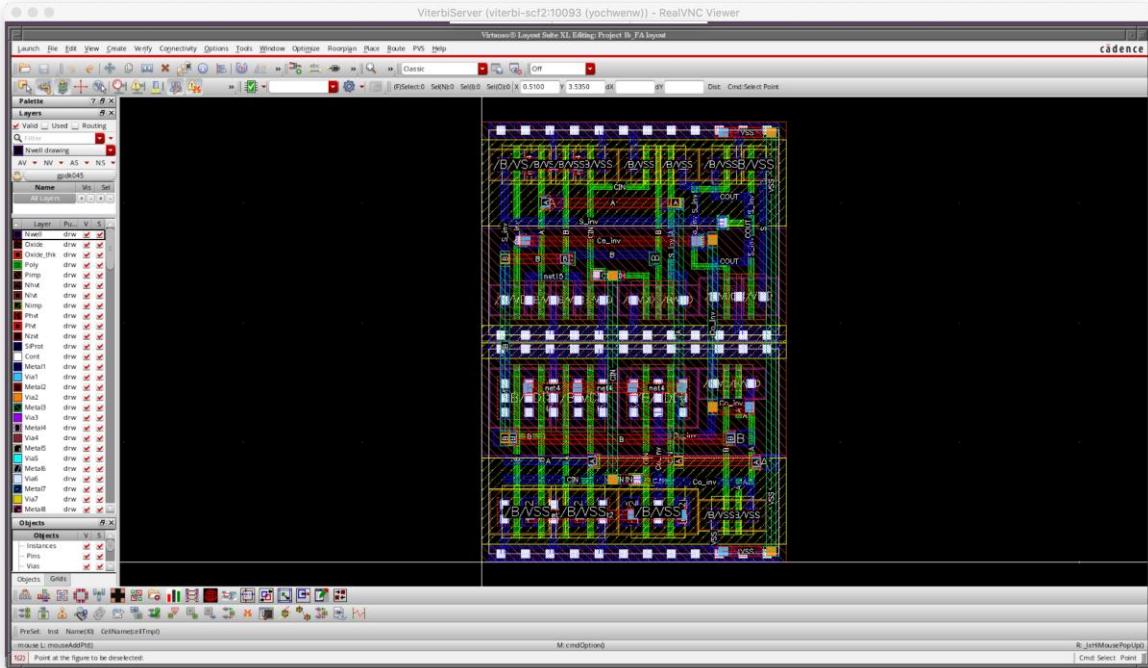


LVS:

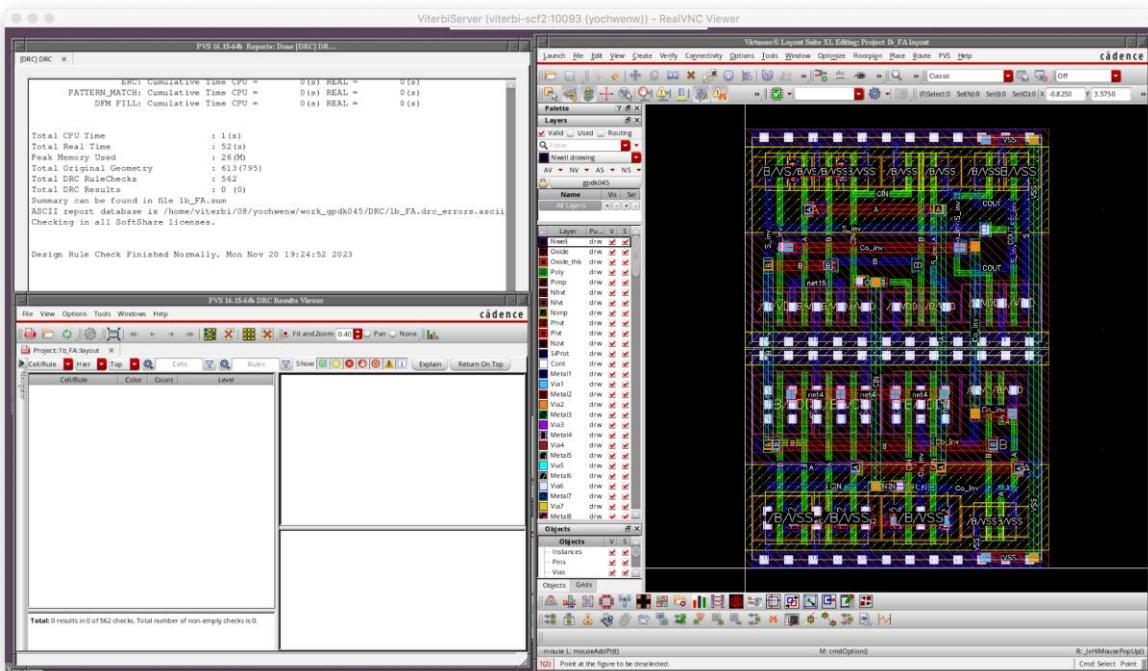


1-bit Full Adder (FA) Design:

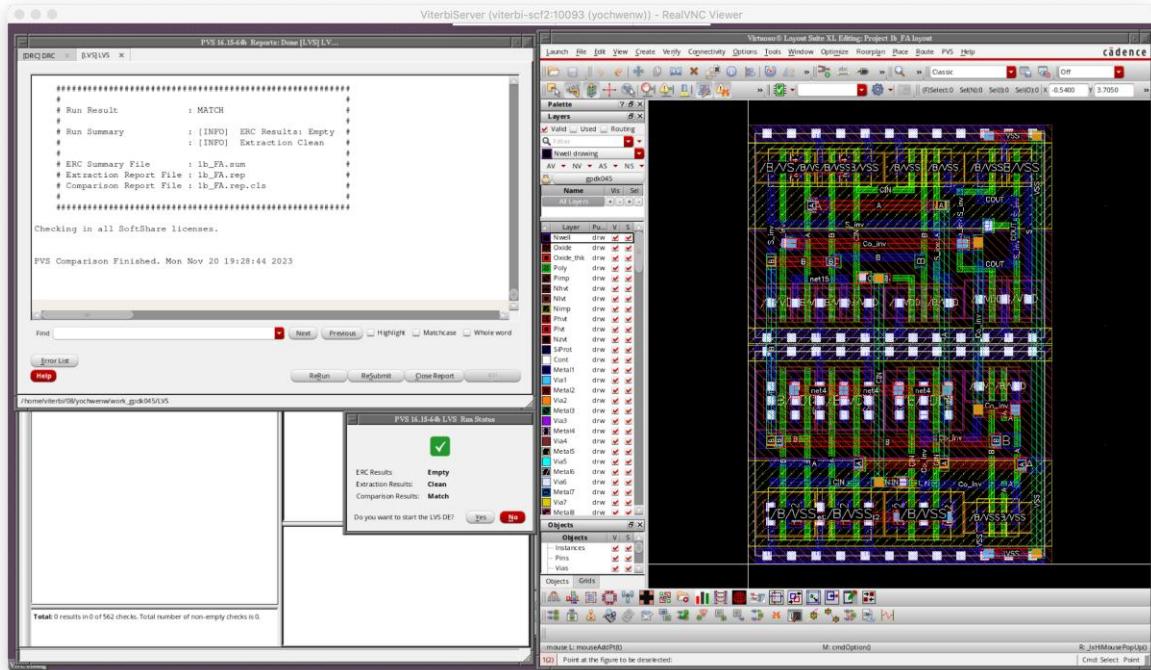
Layout:



DRC:

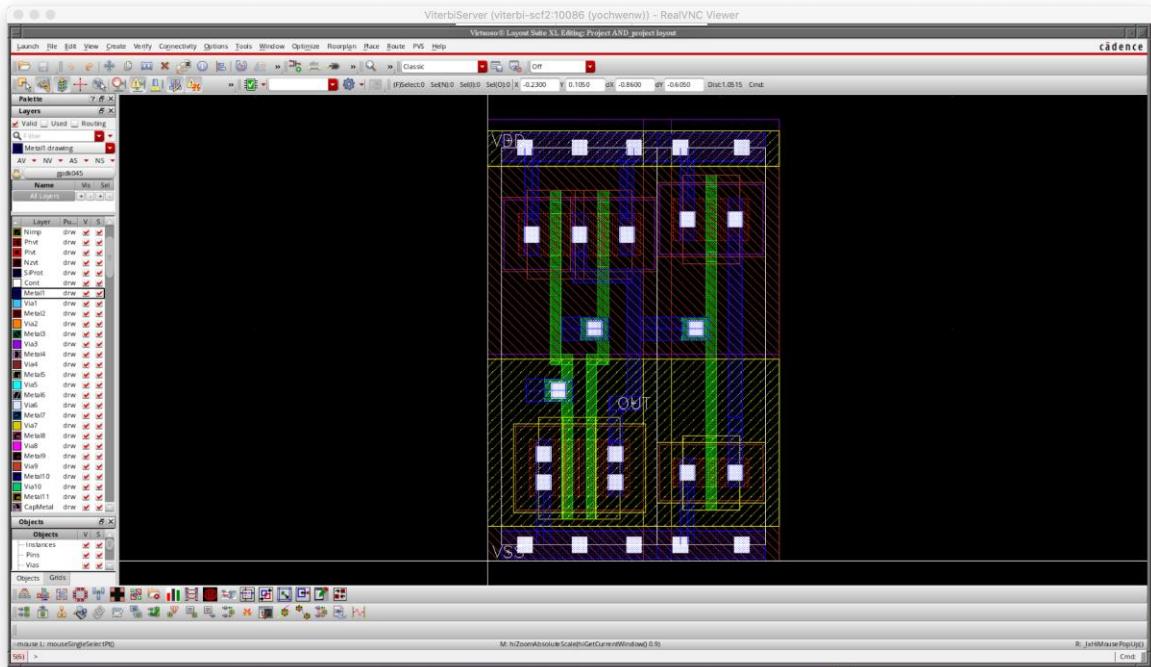


LVS:

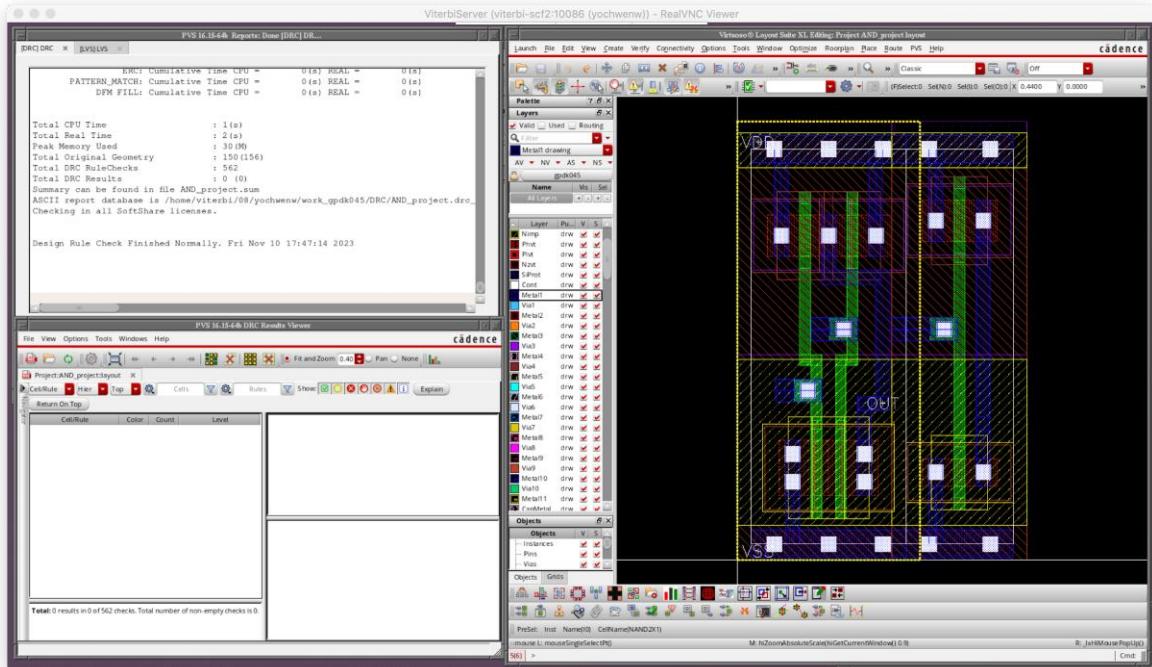


AND Design:

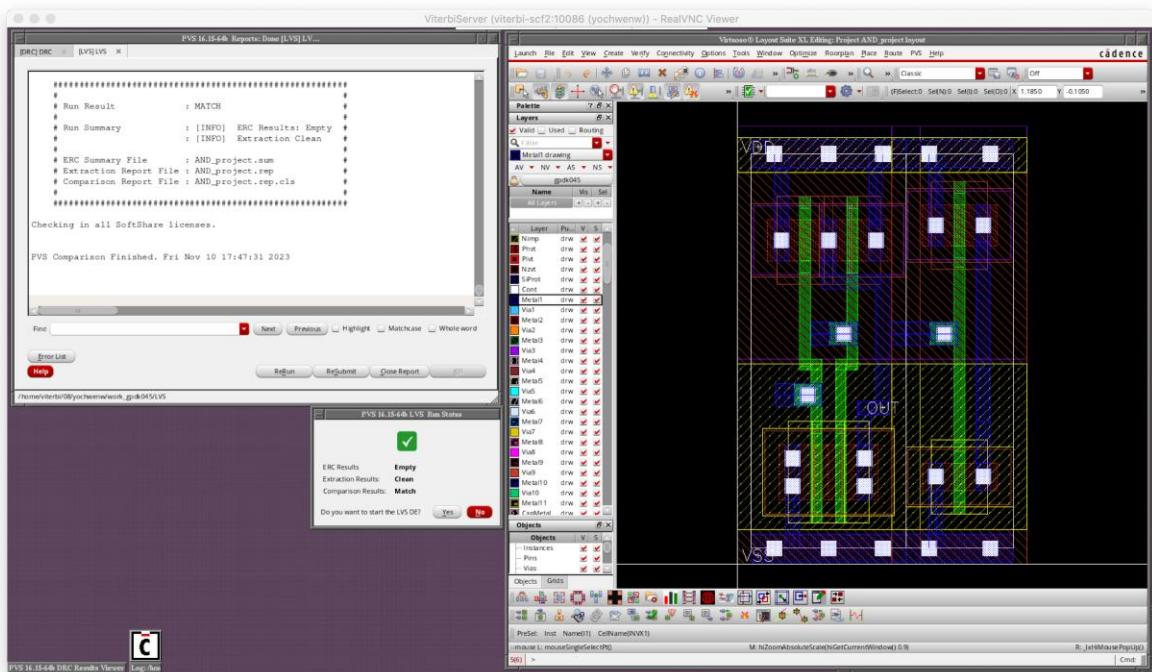
Layout:



DRC:

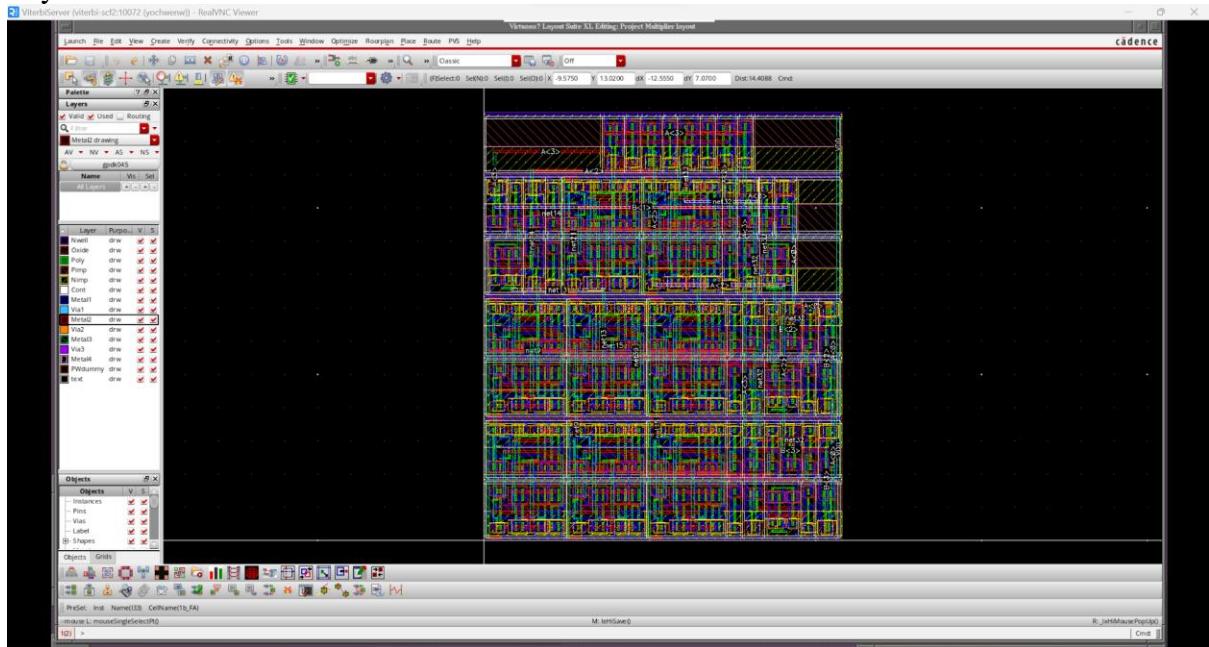


LVS:

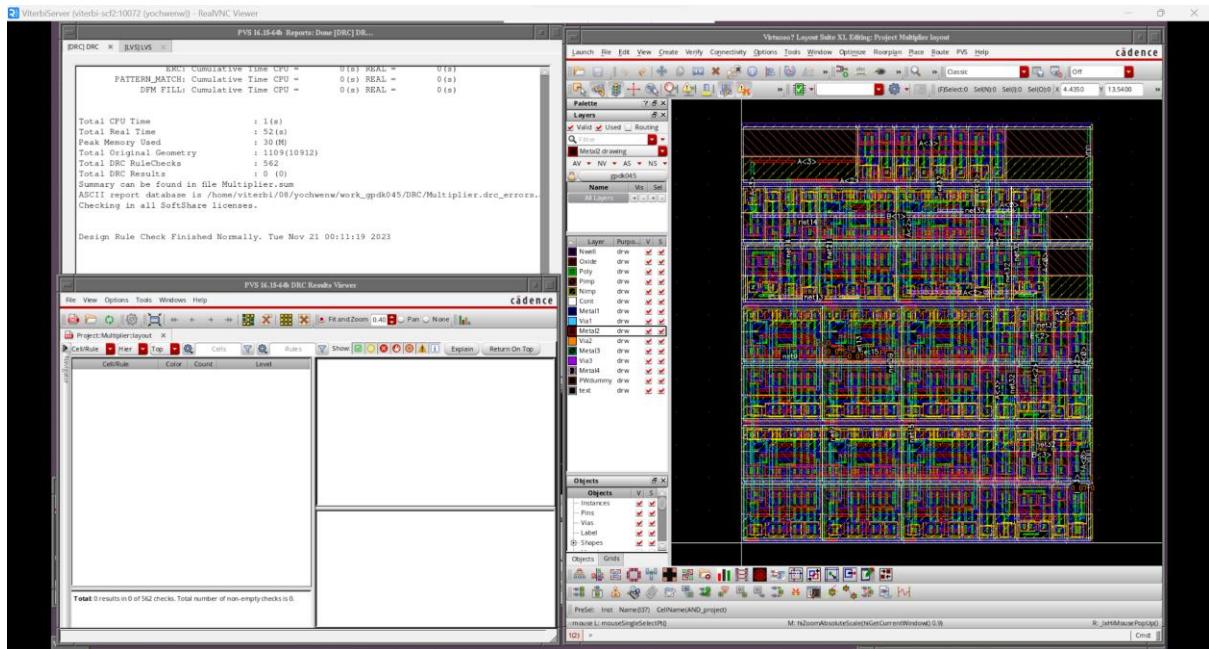


Multiplier Design:

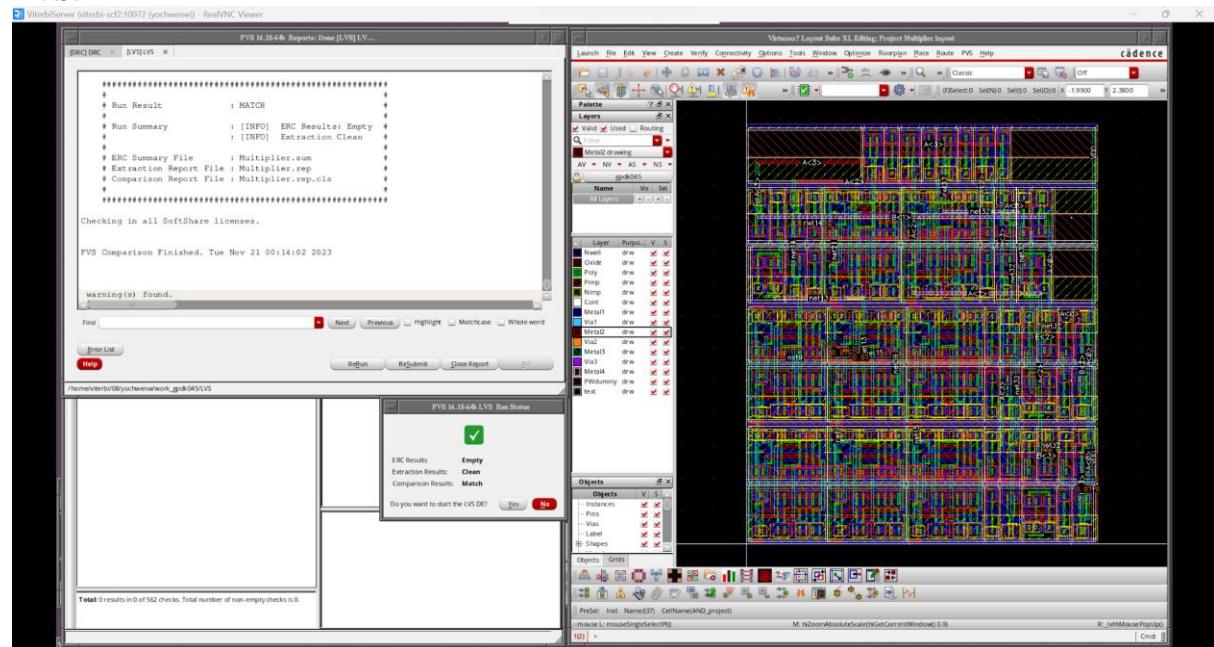
Layout:



DRC:



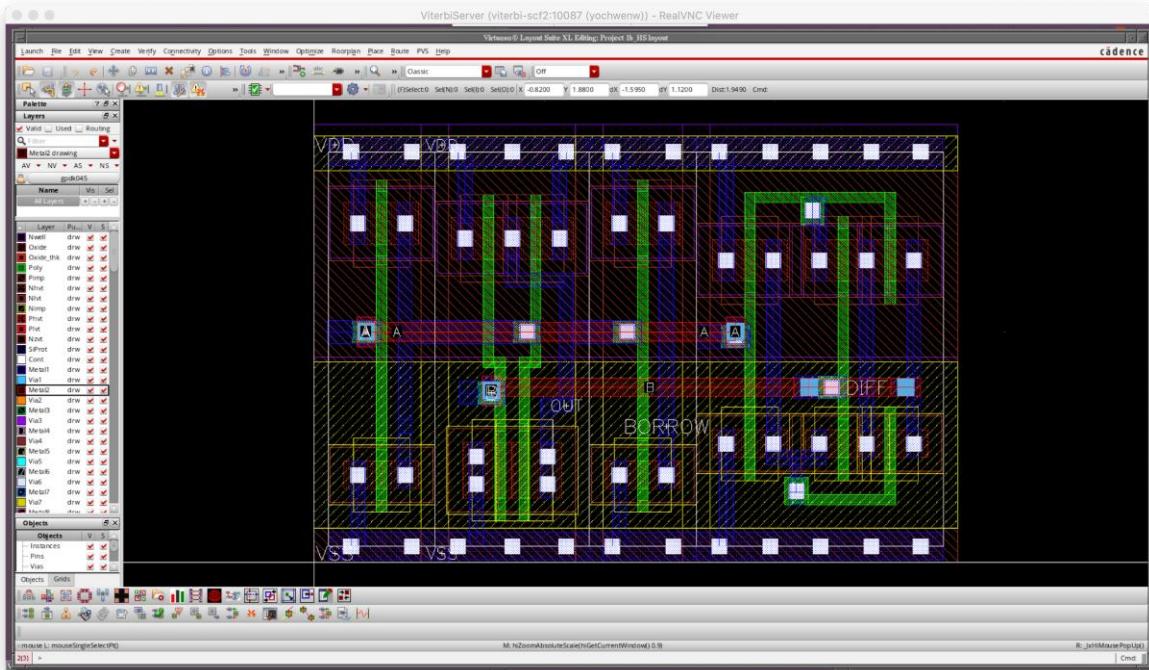
LVS:



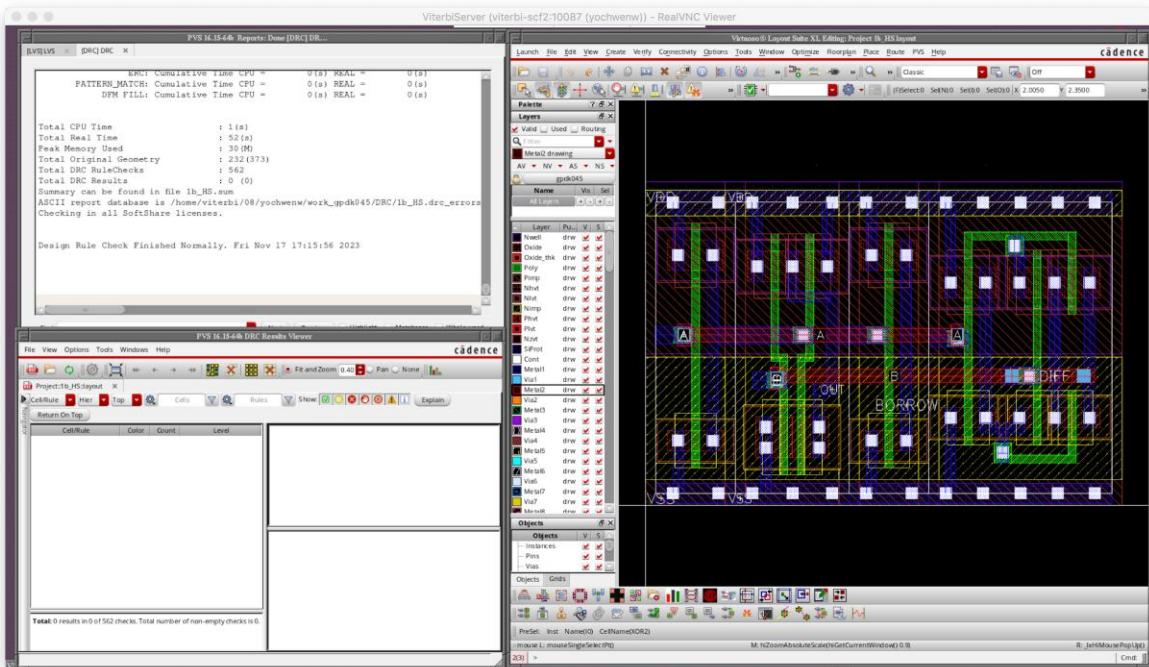
Divider design:

1-bit Half Subtractor (HS) Design:

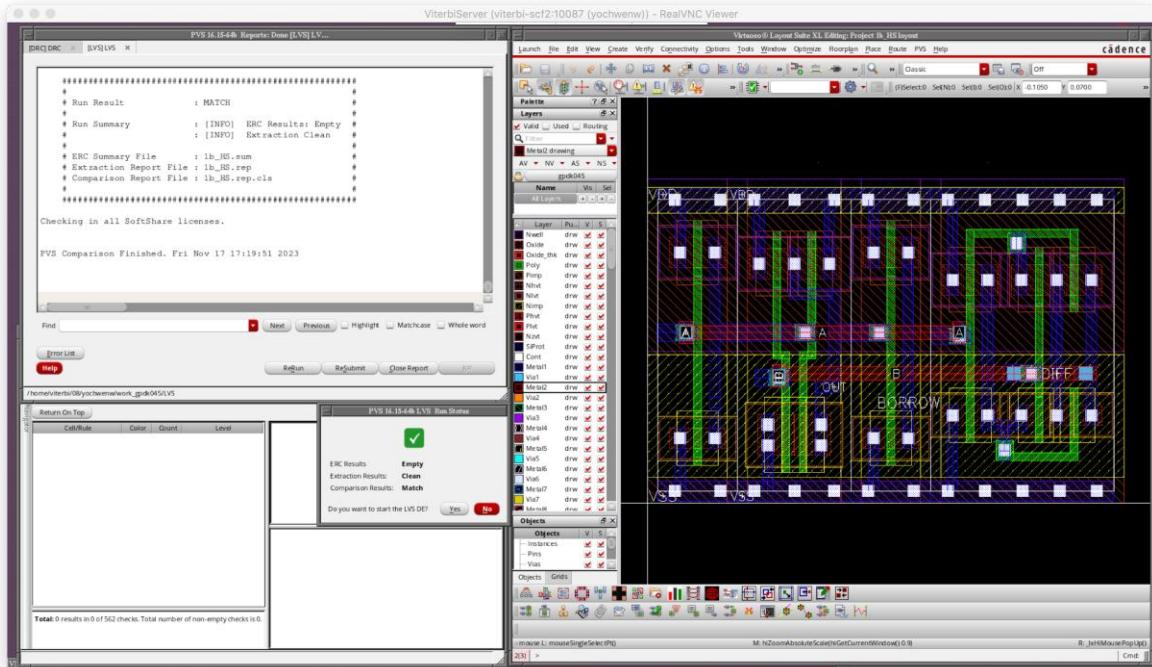
Layout:



DRC:

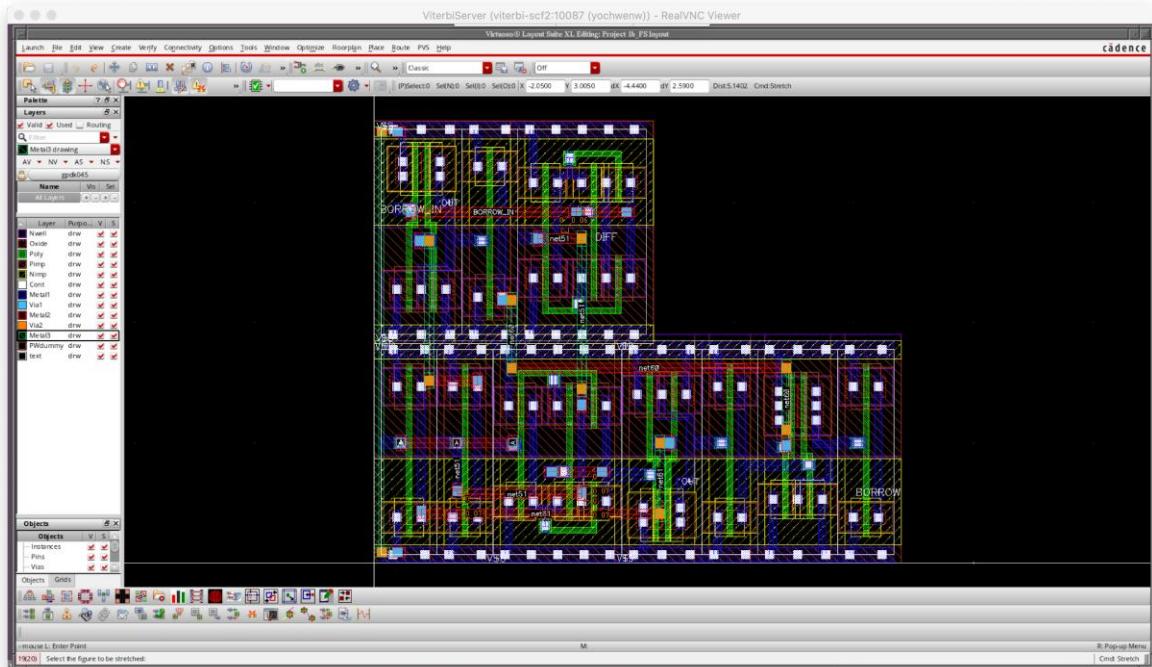


LVS:

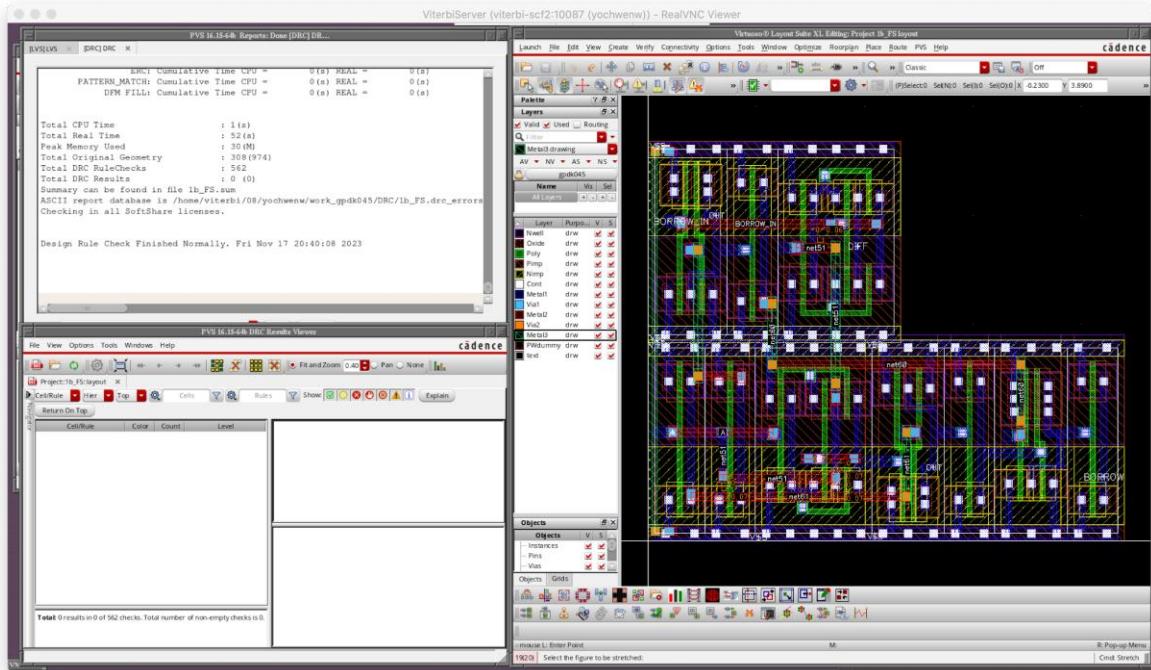


1-bit Full Subtractor (FS) Design:

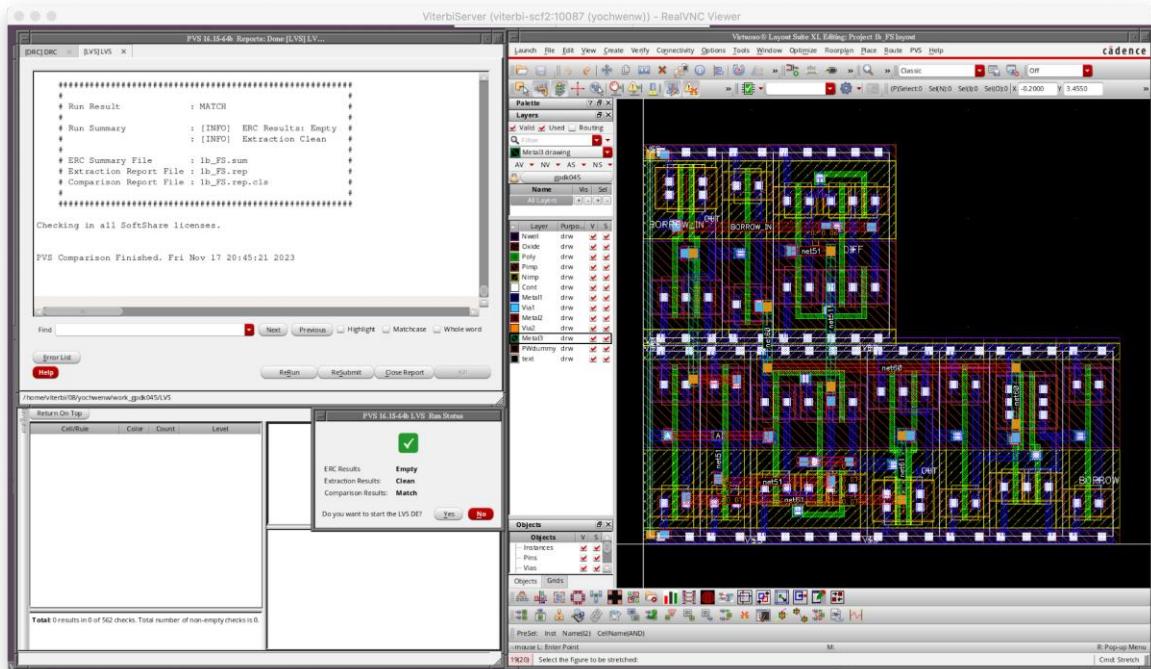
Layout:



DRC:

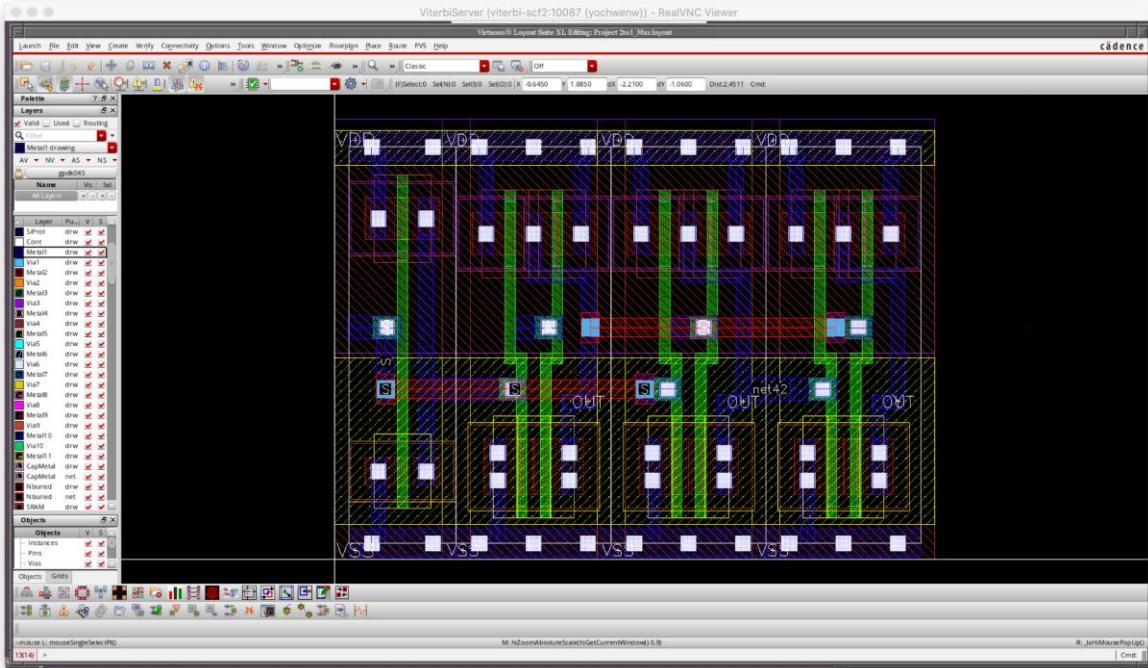


LVS:

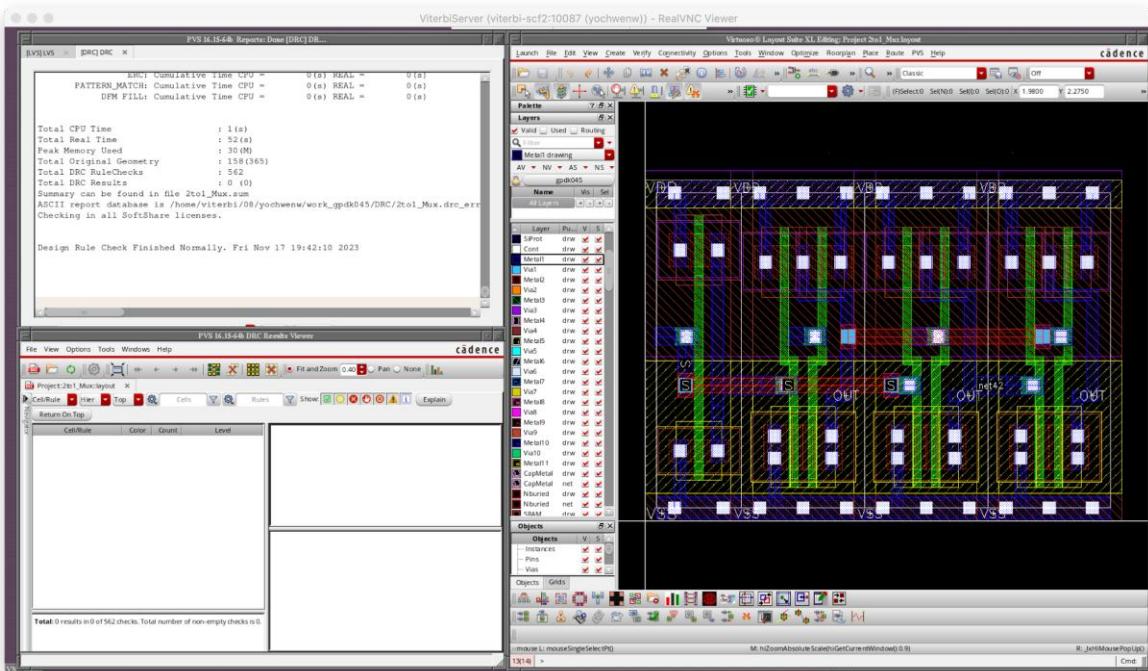


2-to-1 MUX Design:

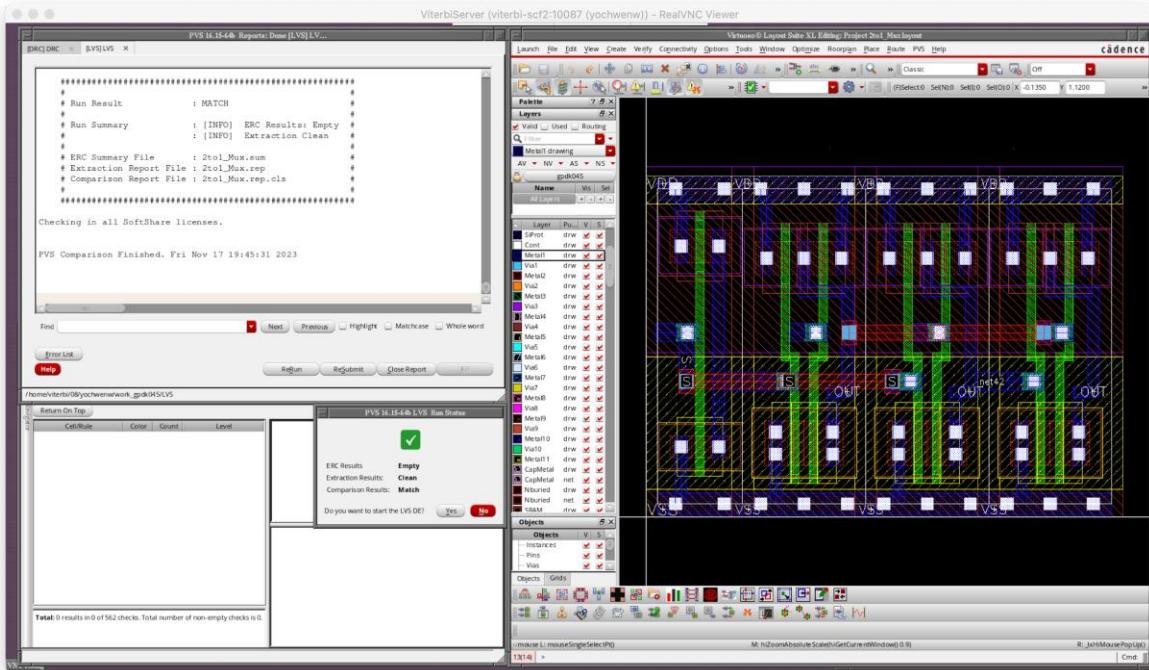
Layout:



DRC:

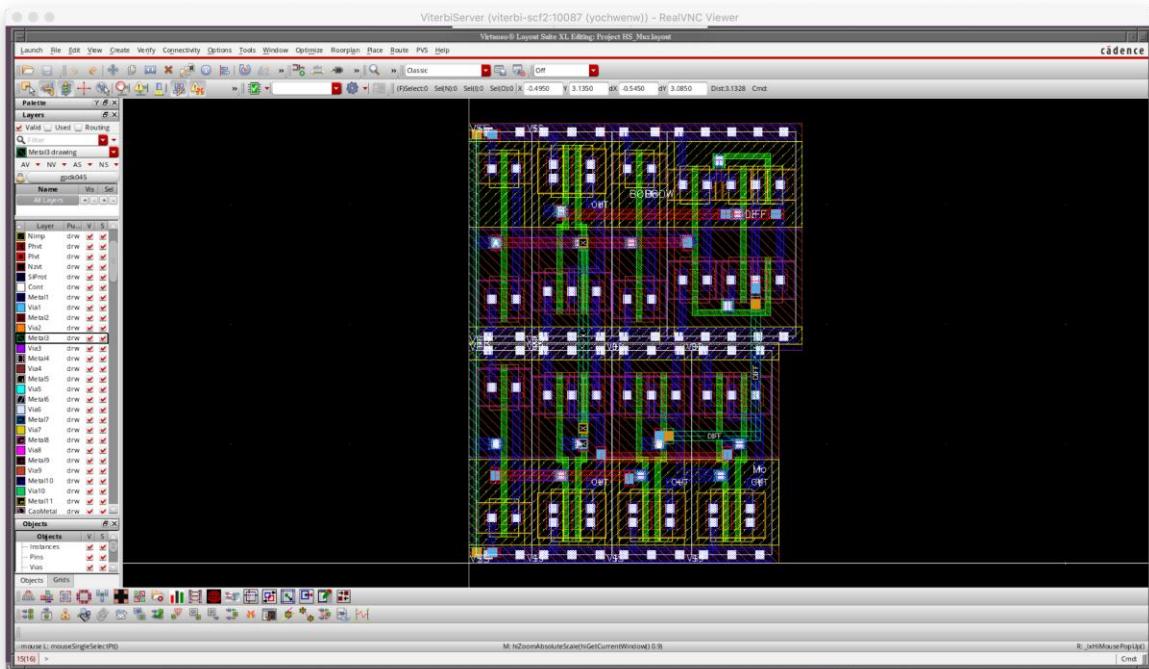


LVS:

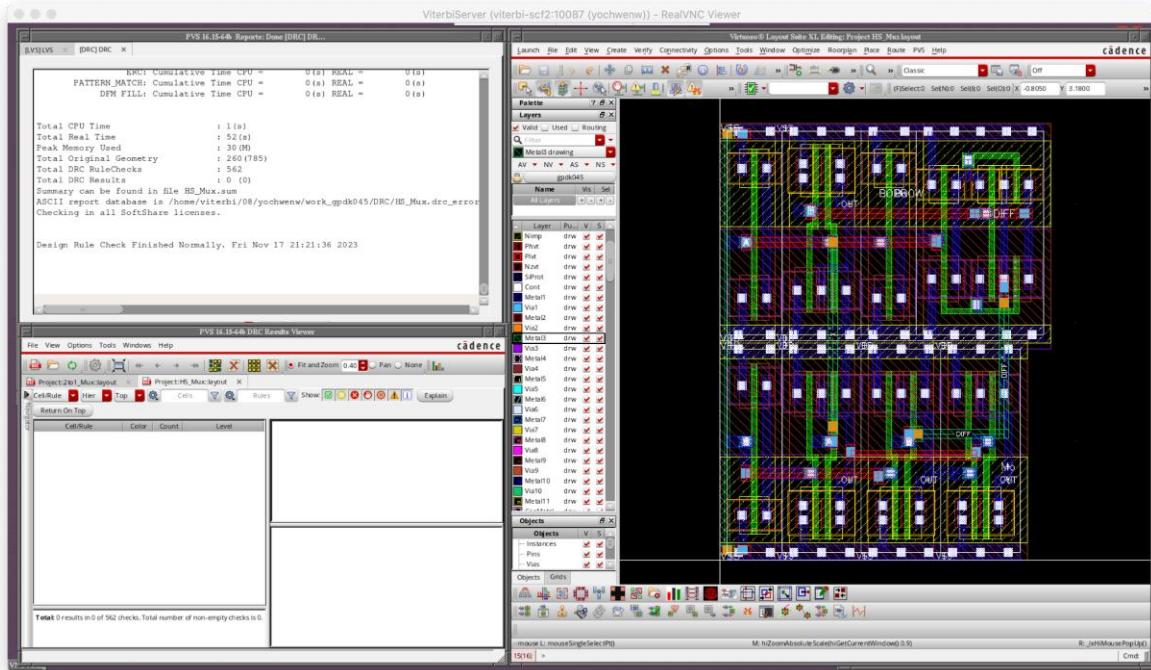


HS_MUX Design:

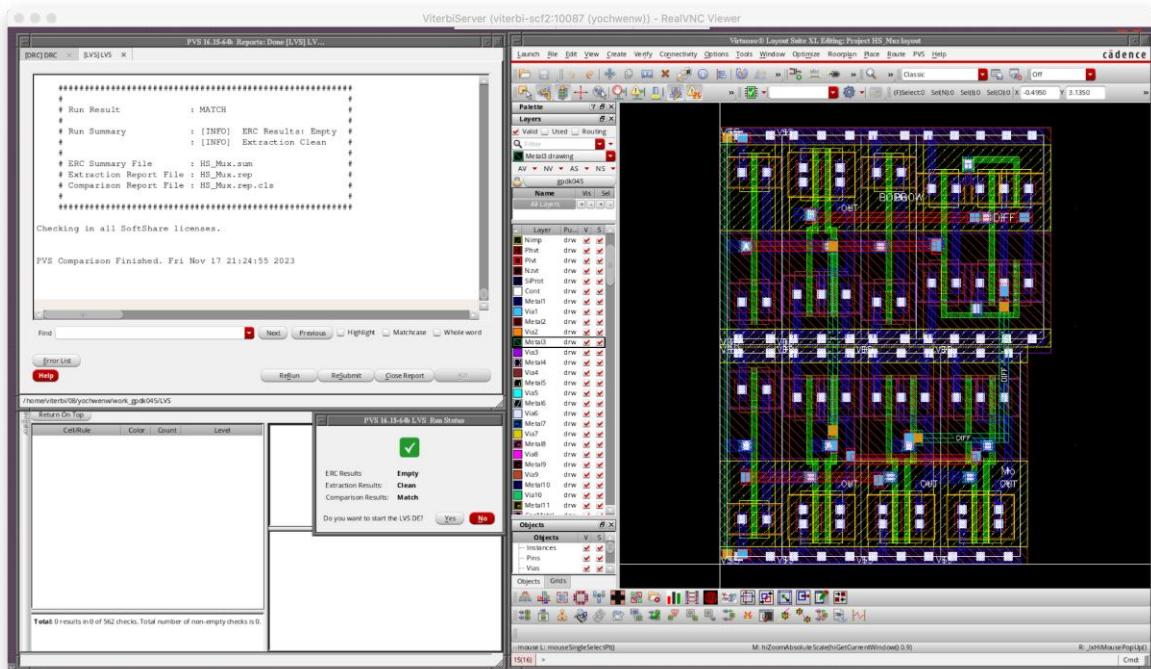
Layout:



DRC:



LVS:

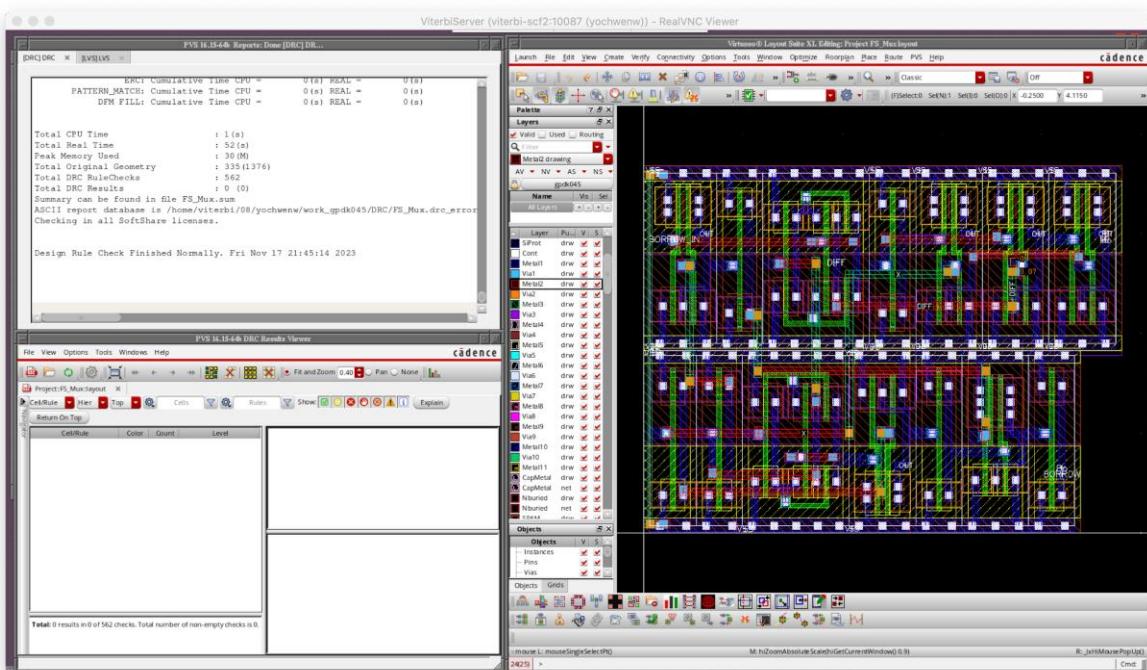


FS_MUX Design:

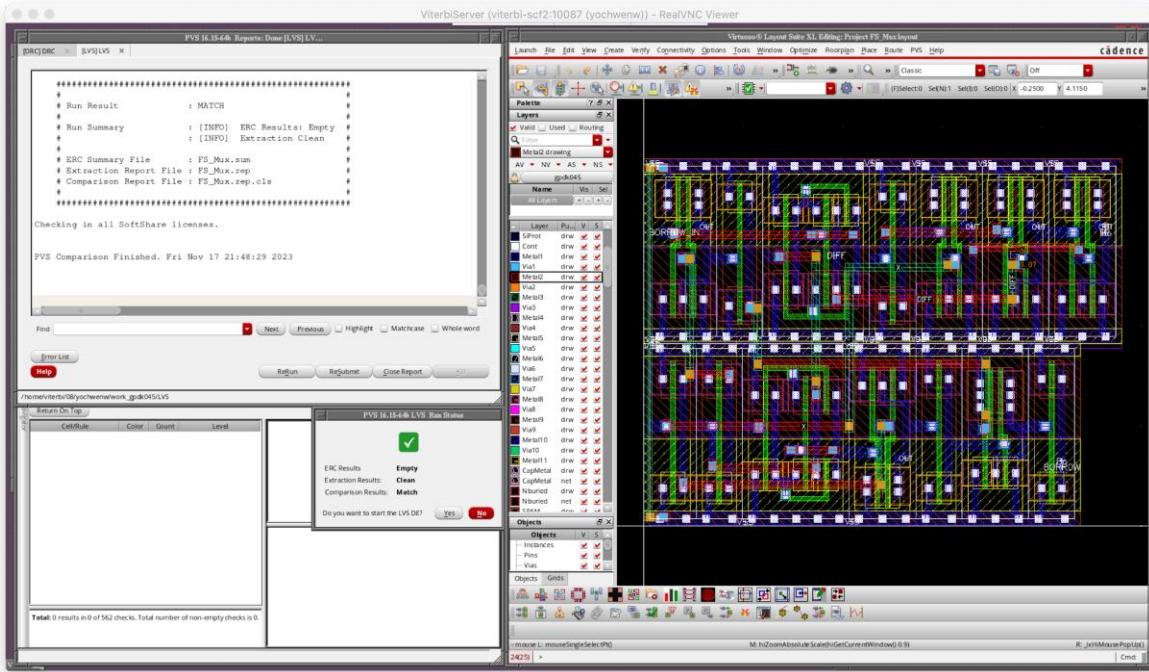
Layout:



DRC:

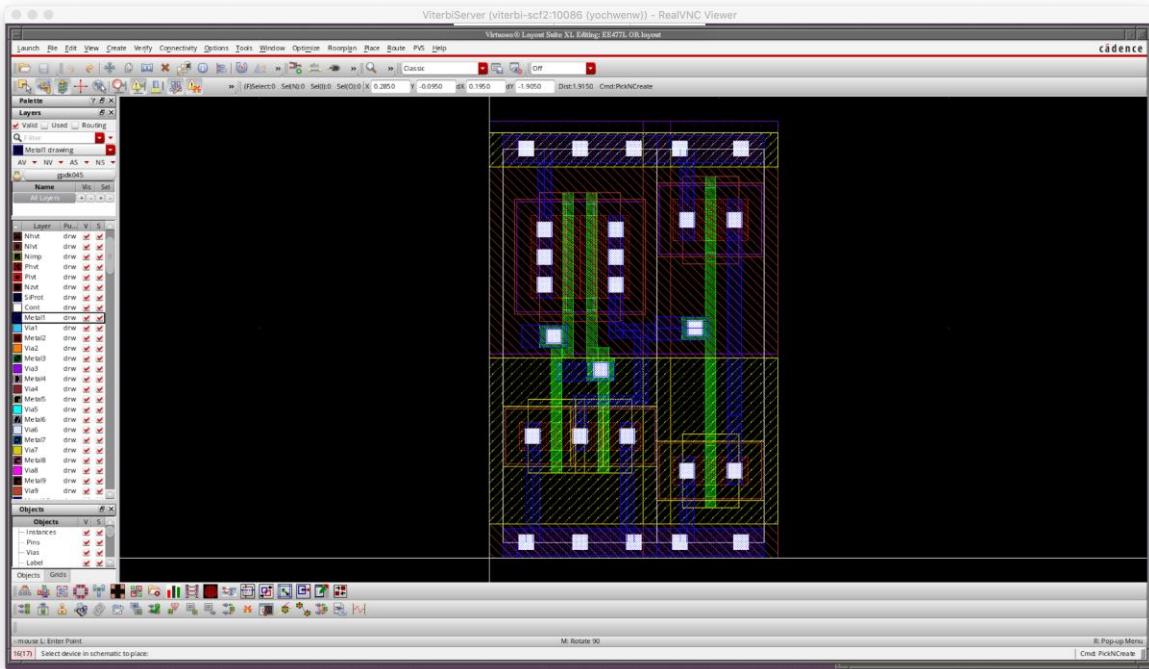


LVS:

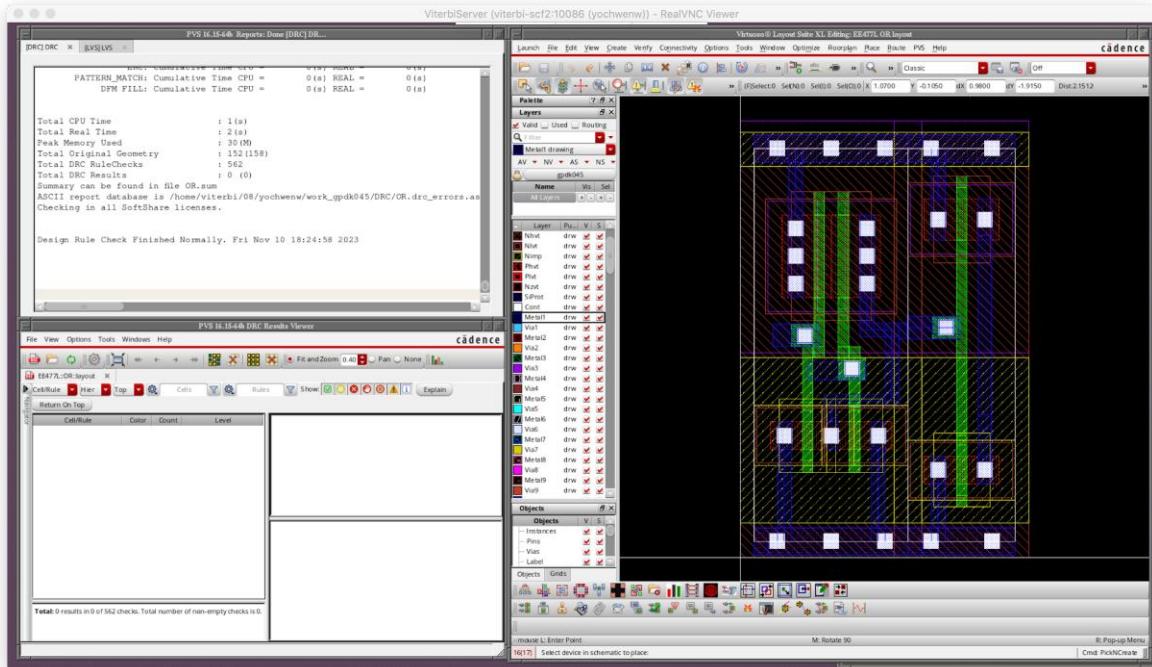


OR Design:

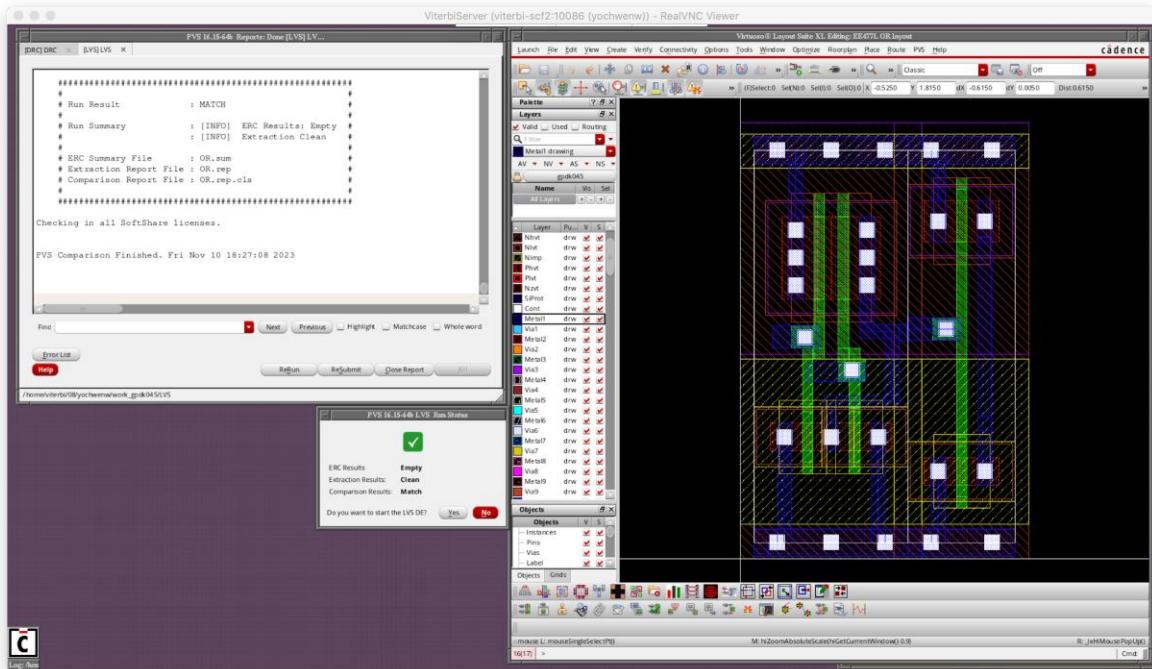
Layout:



DRC:

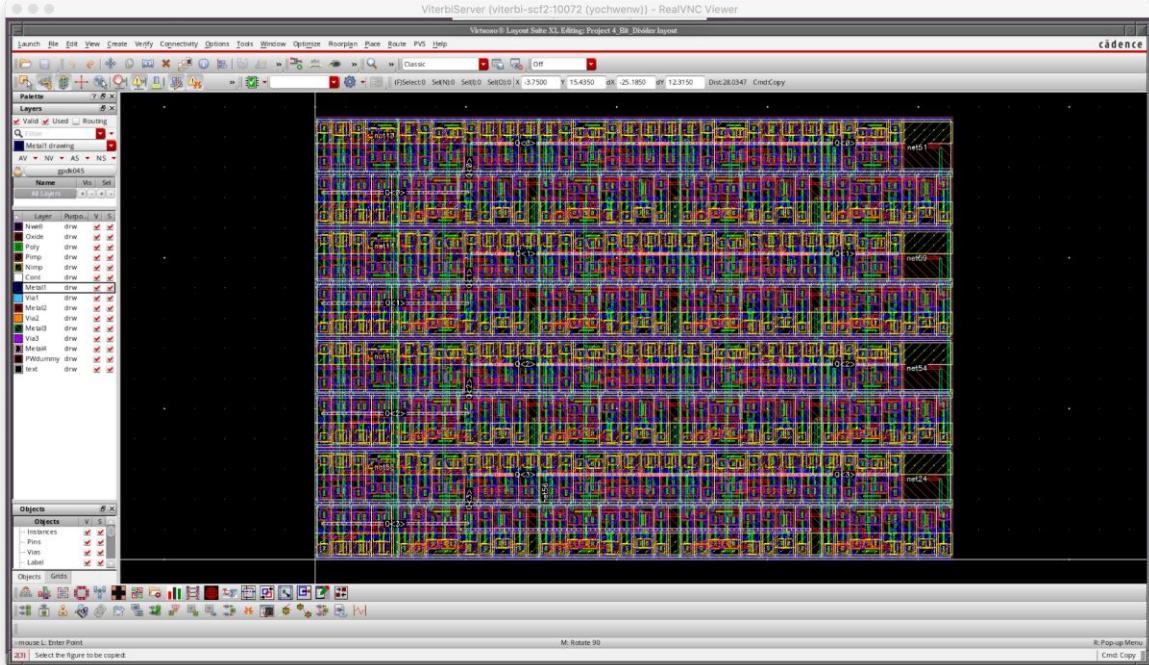


LVS:

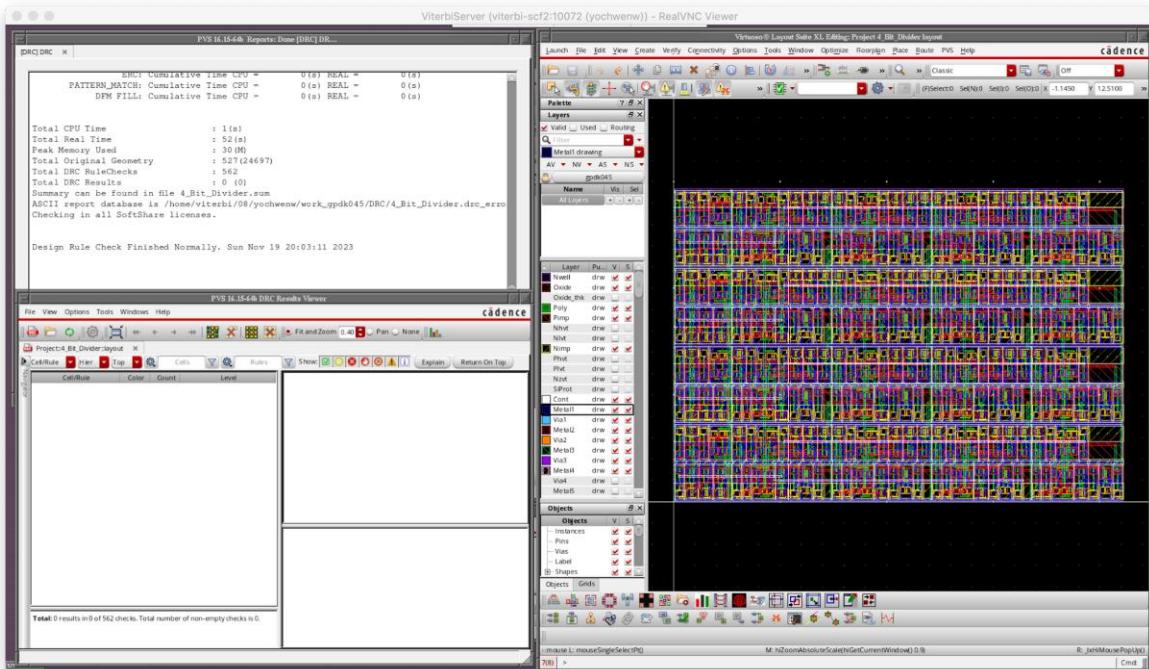


Divider Design:

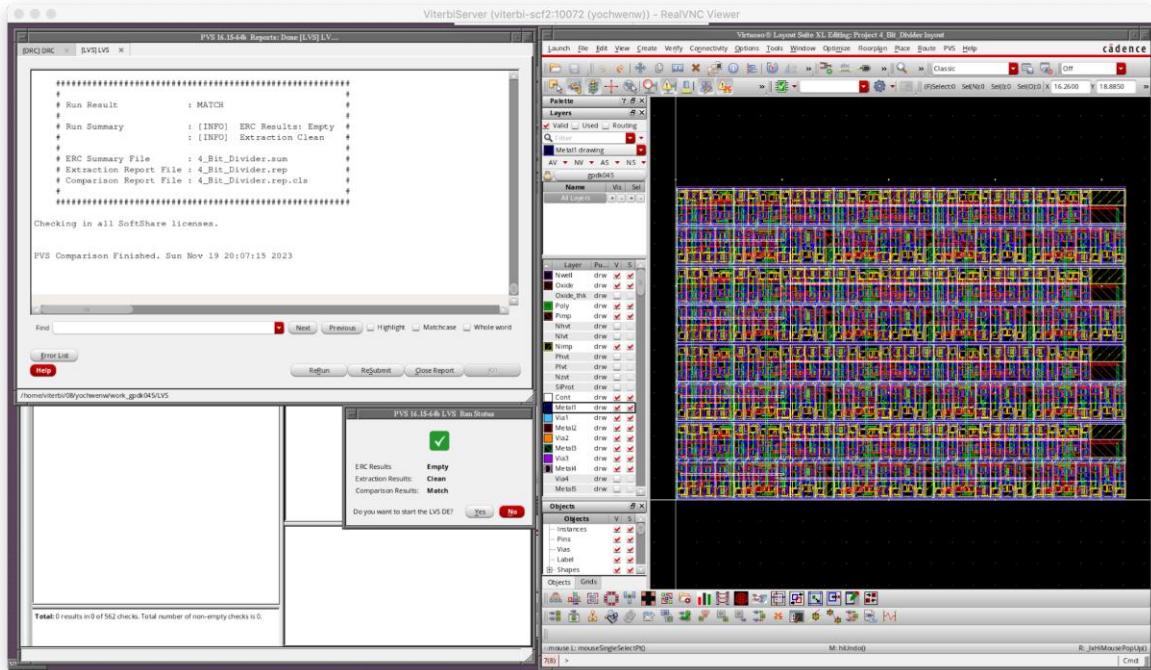
Layout:



DRC:

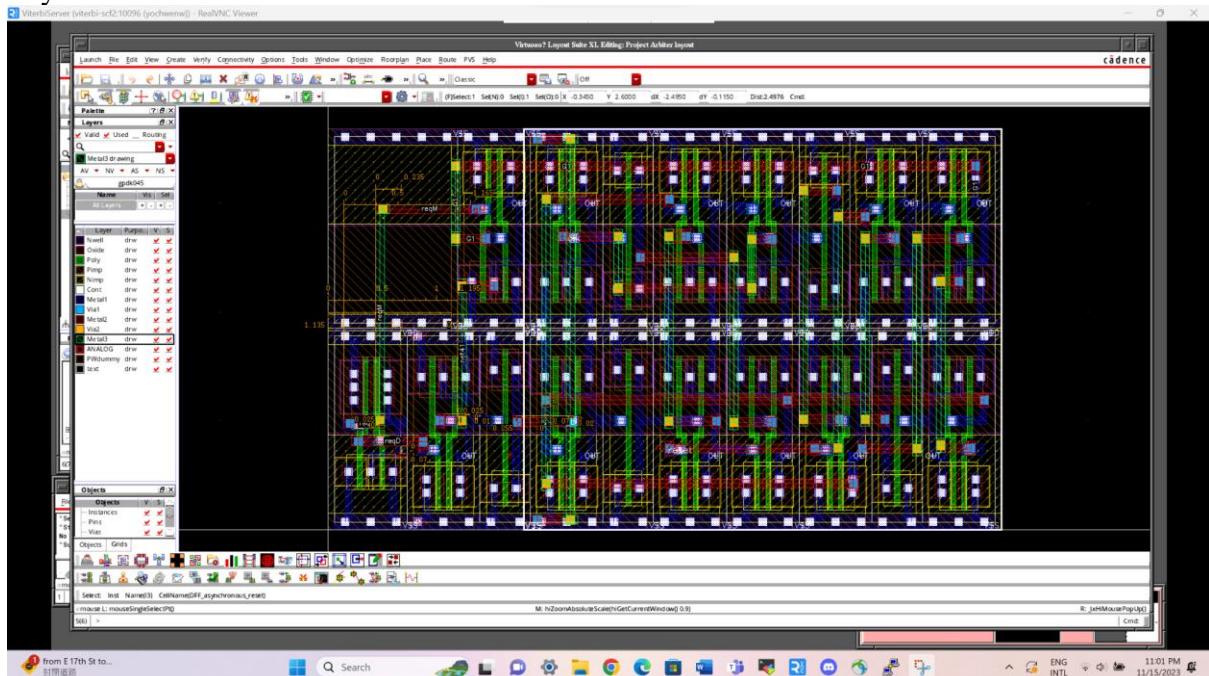


LVS:

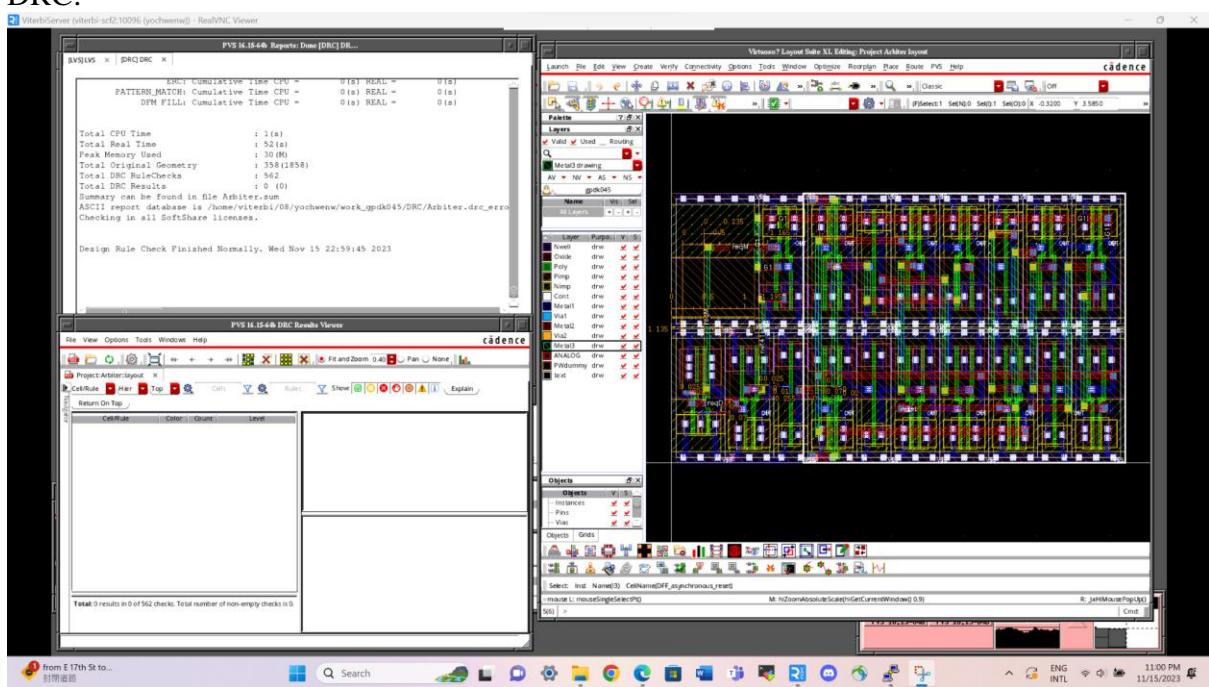


Arbiter Design:

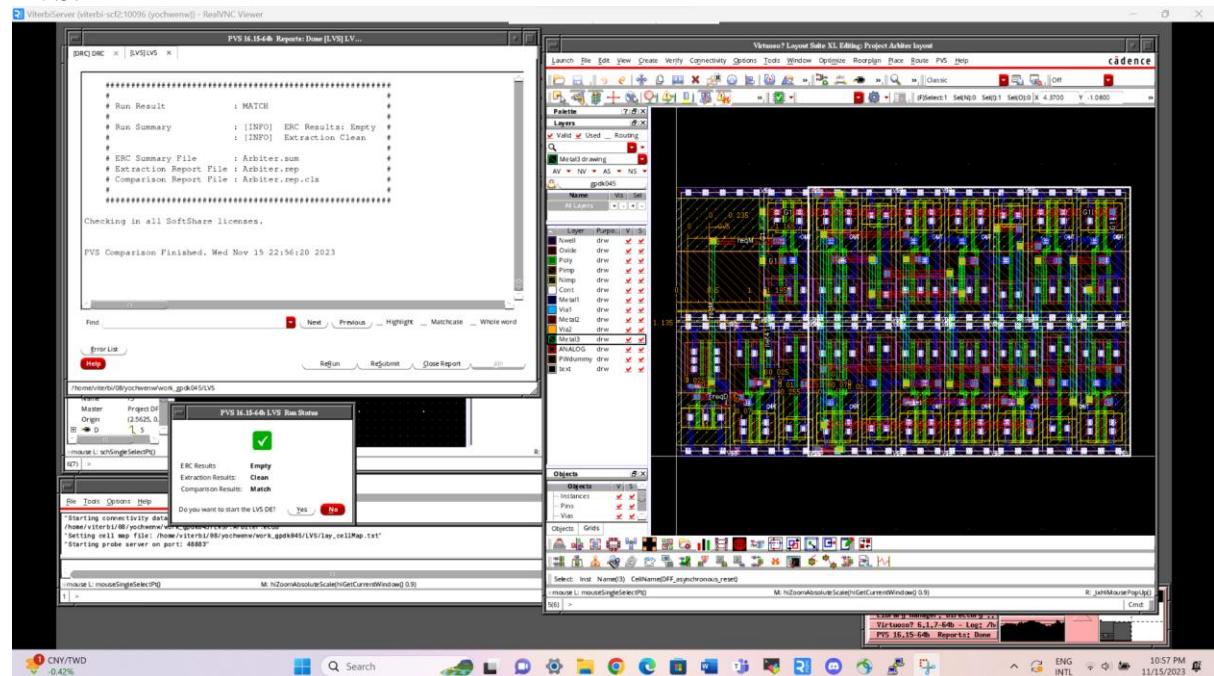
Layout:



DRC:

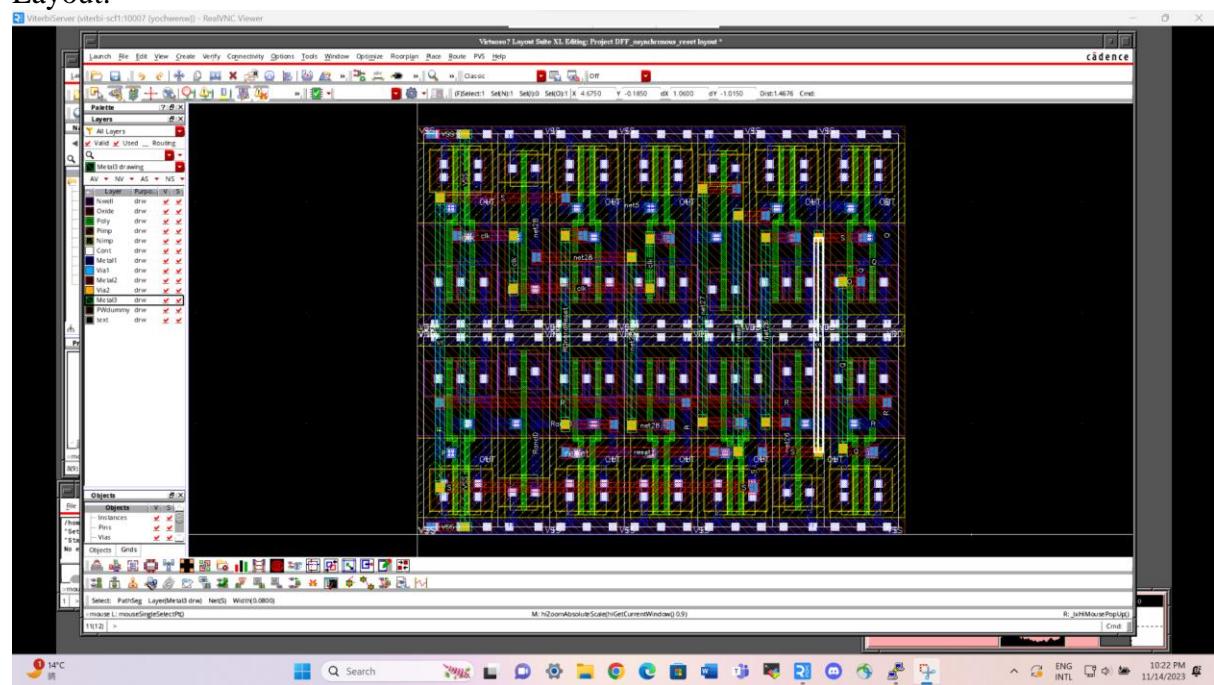


LVS:

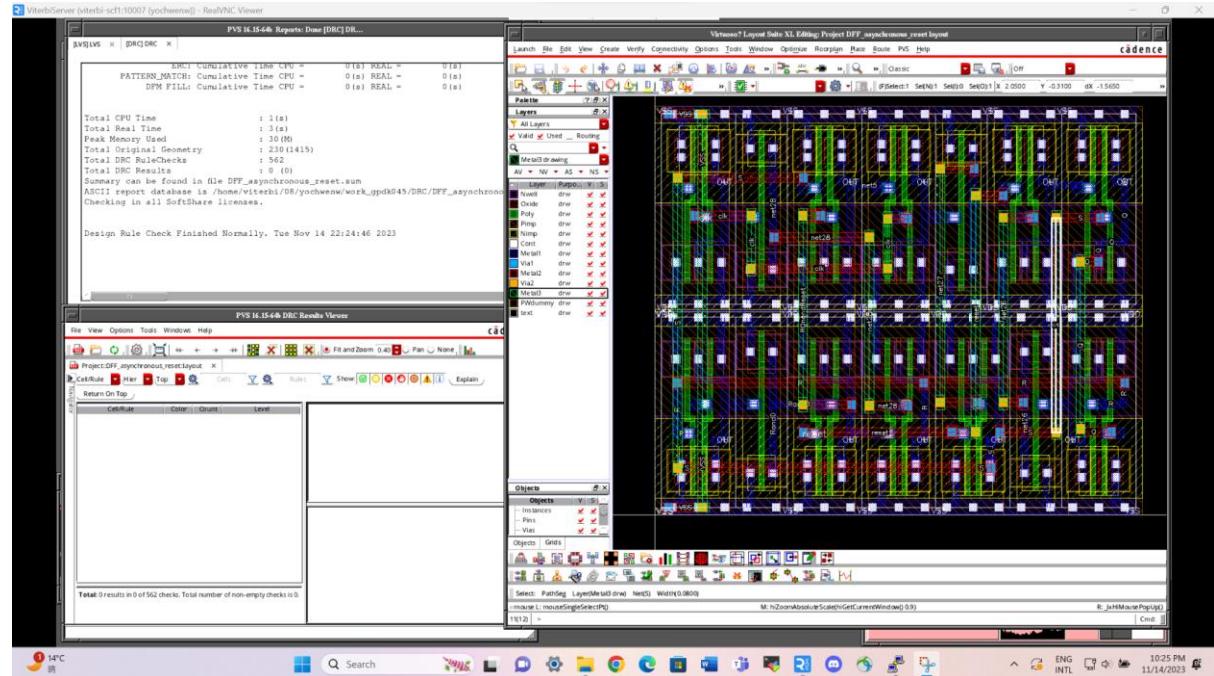


1-bit DFF:

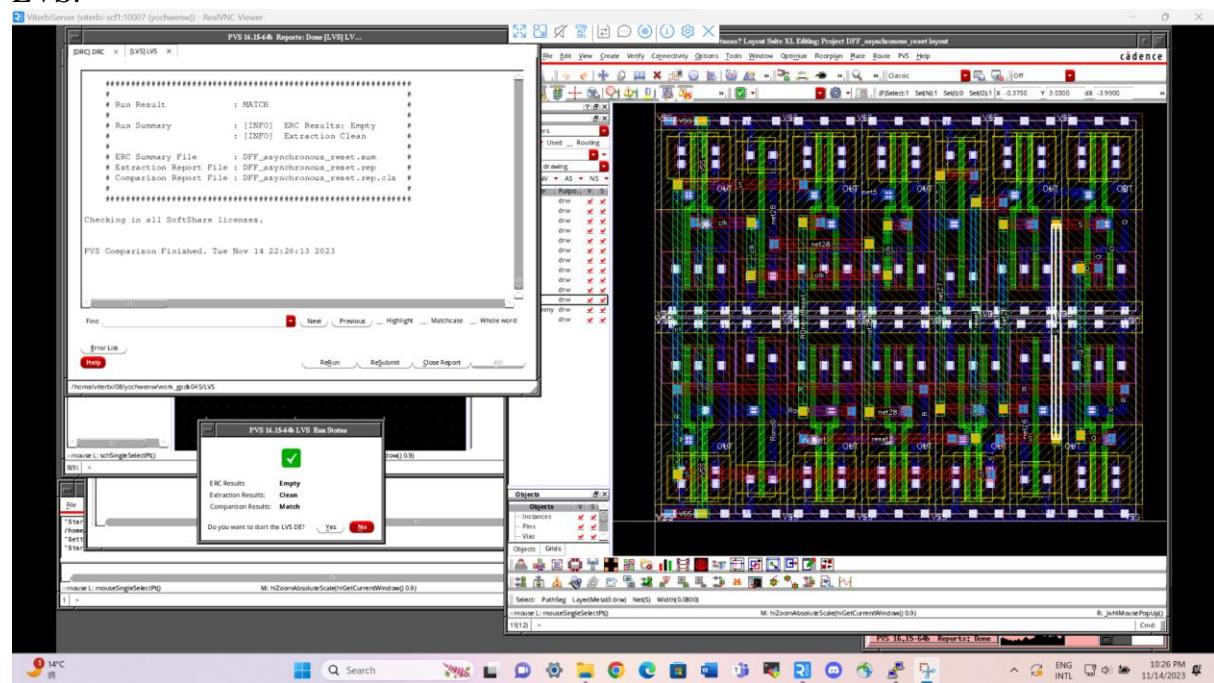
Layout:



DRC:

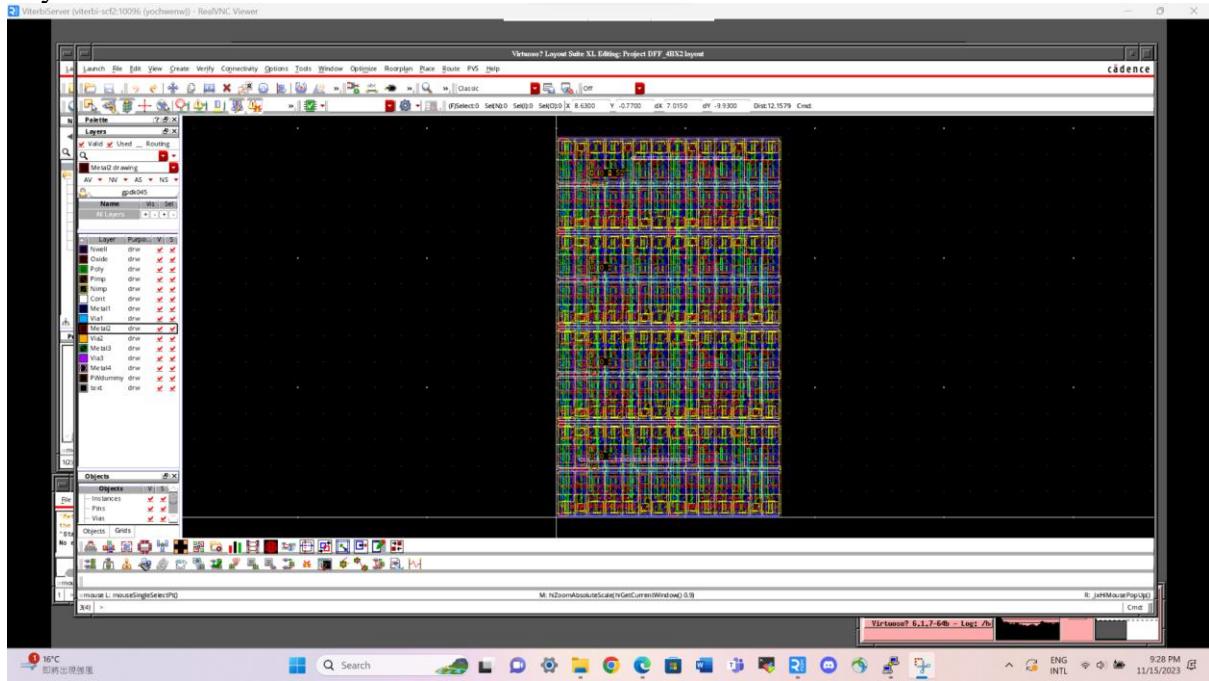


LVS:

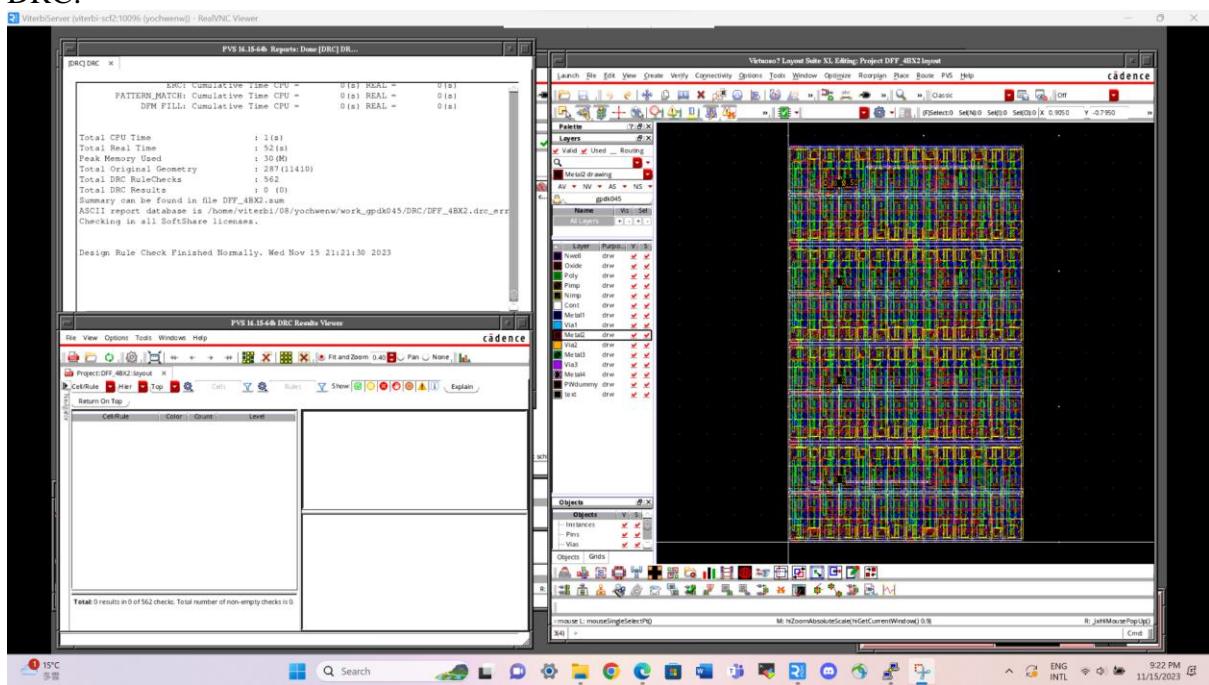


8-bit DFF:

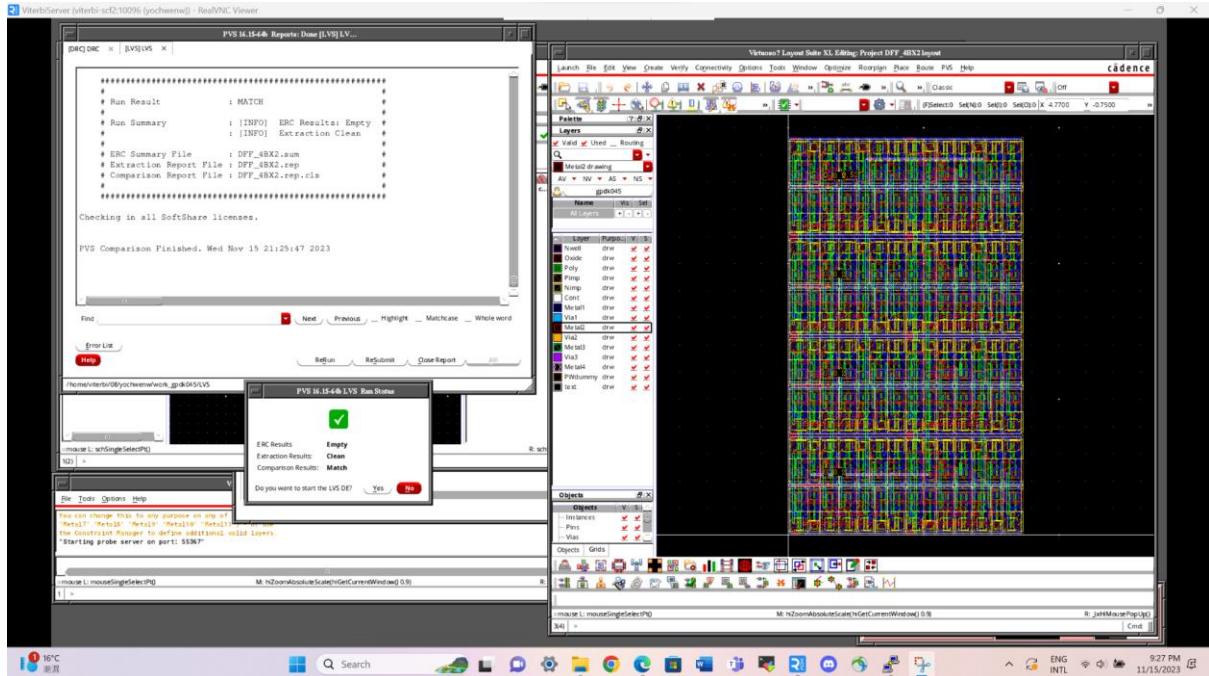
Layout:



DRC:

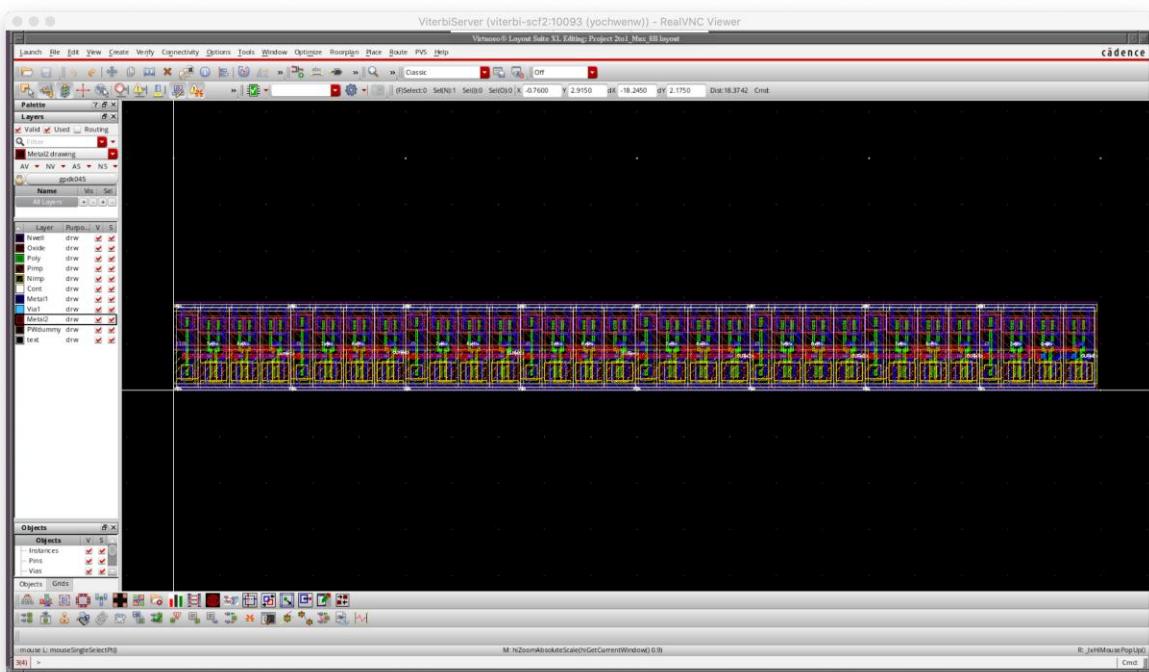


LVS:

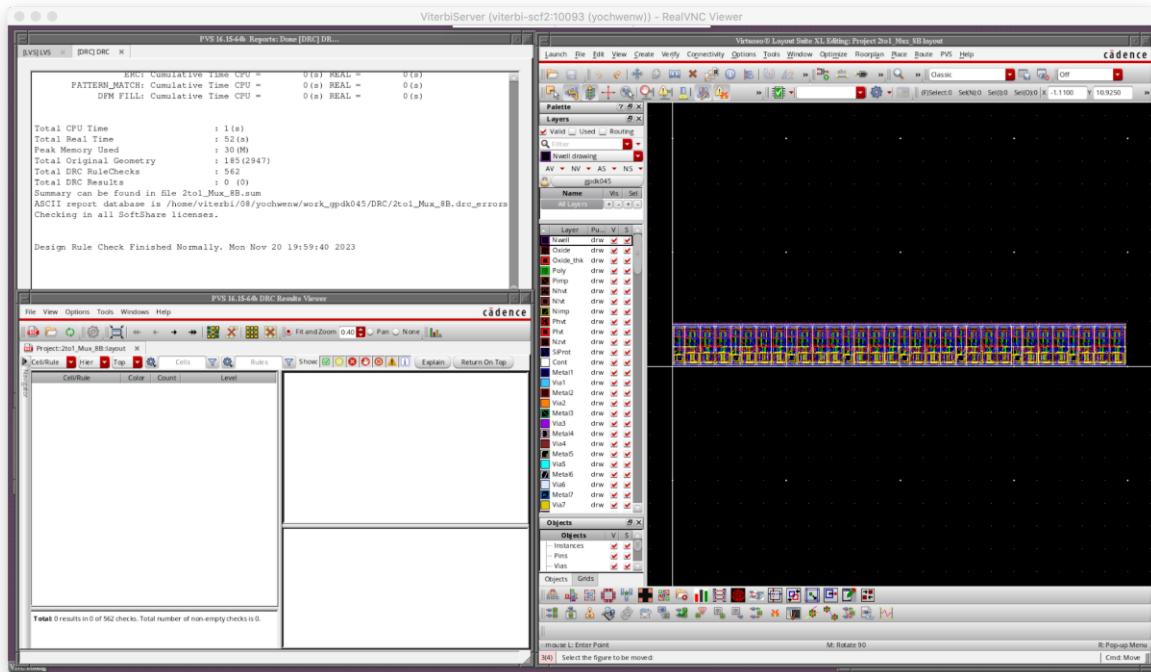


8-bit 2-to-1_MUX Design:

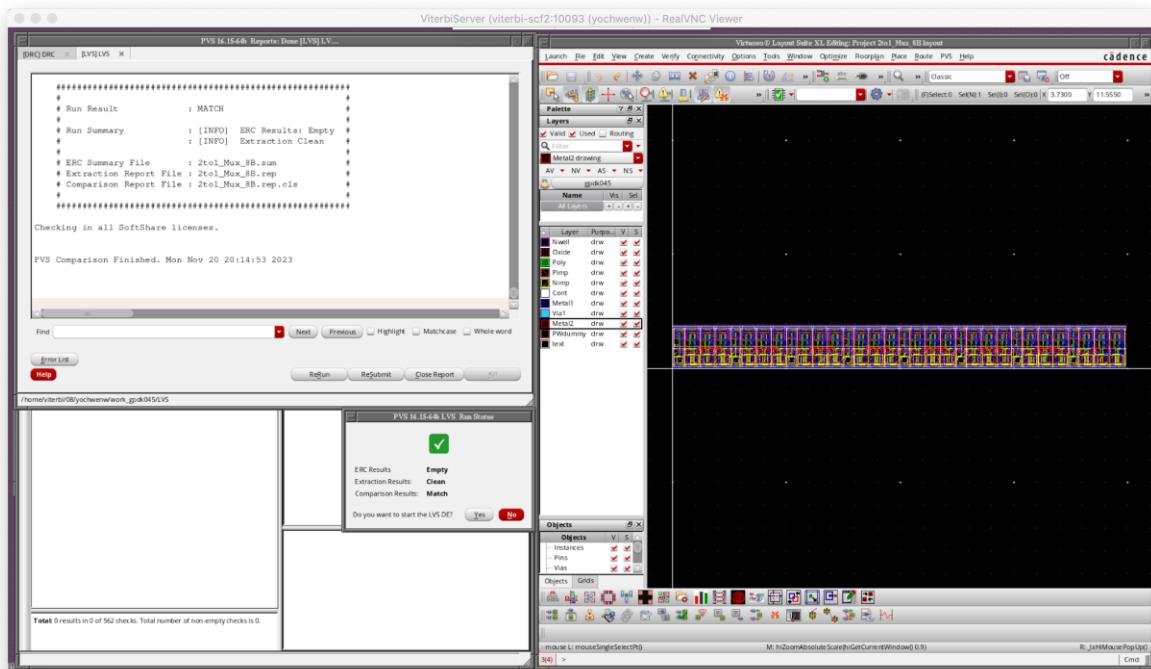
Layout:



DRC:



LVS:

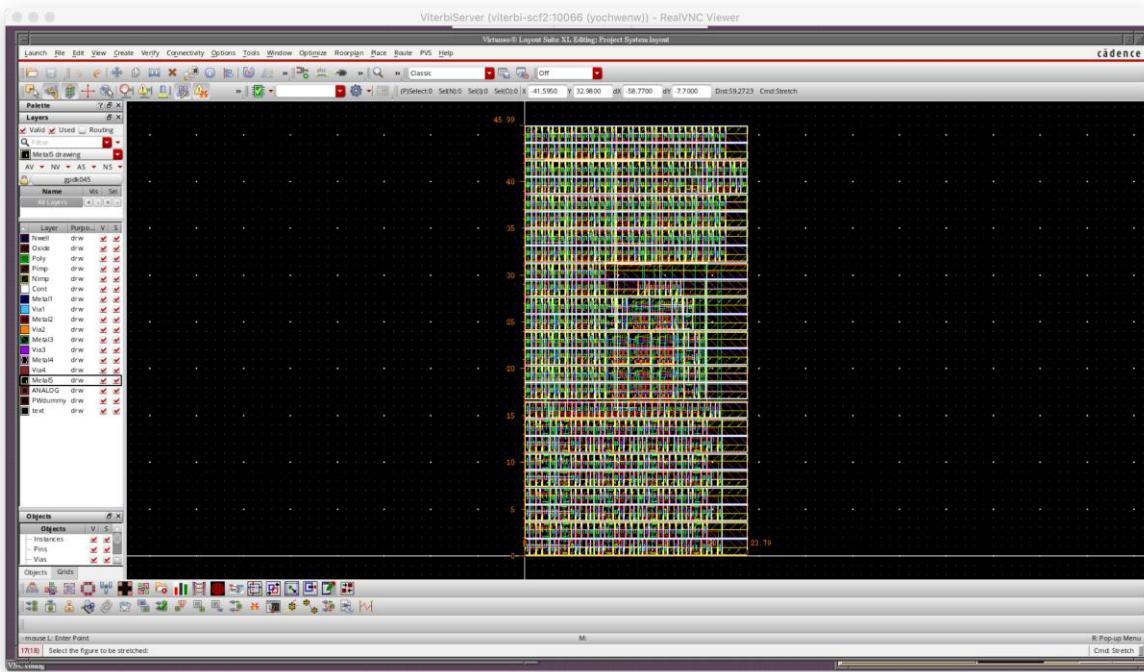


Complete system Design:

Note: Buffer is merged in complete system design.

Note: Total amount of metal layer used: 5

Layout:



DRC:



LVS:



Part 1.5: Post-Layout Verification

Post-layout functional verification: Multiplier:



Expected output

| A[3:0] | B[3:0] | Z | A' | B' |
|--------|--------|---------------|----|----|
| 0 | 0 | 00 = 00000000 | F | F |
| 7 | 5 | 23 = 00100011 | 8 | A |
| A | 0 | 00 = 00000000 | 5 | F |
| F | 3 | 2D = 00101101 | 0 | C |
| 9 | E | 7E = 01111110 | 6 | 1 |
| 4 | 1 | 04 = 00000100 | B | E |
| 8 | B | 58 = 01011000 | 7 | 4 |
| F | F | E1 = 11100001 | 0 | 0 |

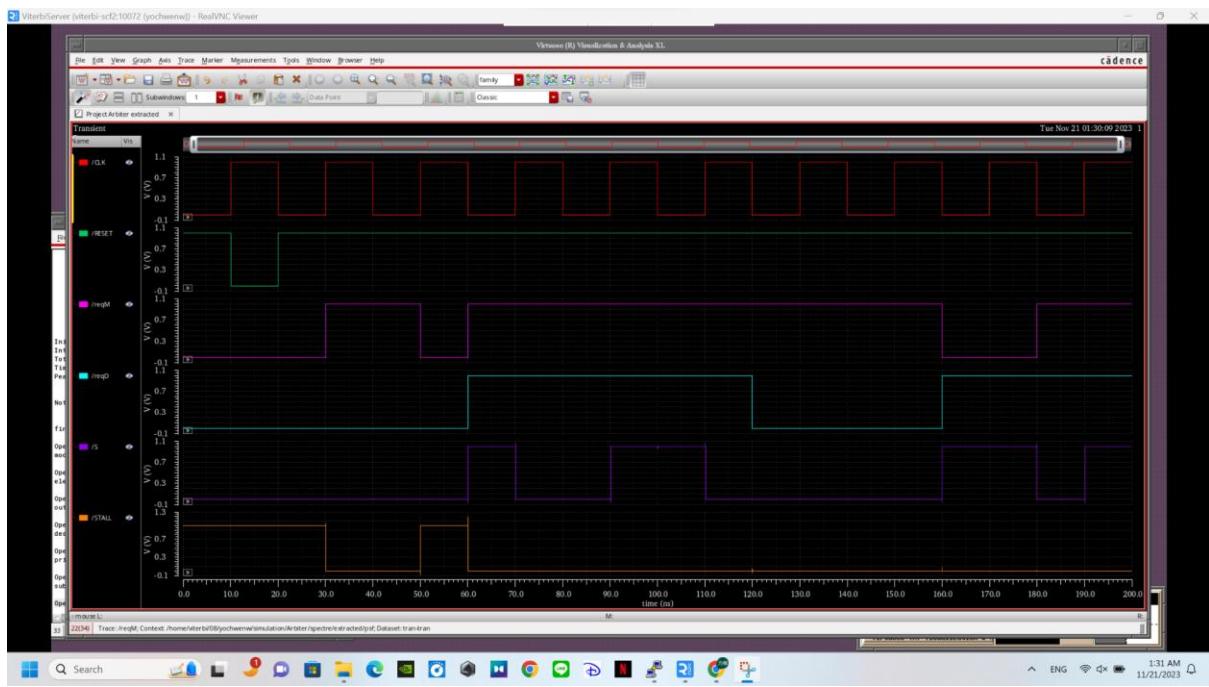
Post-layout functional verification: Divider:



Expected output

| div[3:0] | d[3:0] | Q | R |
|----------|--------|----------|----------|
| 3 | A | 0 = 0000 | 3 = 0011 |
| F | 5 | 3 = 0011 | 0 = 0000 |
| 7 | A | 0 = 0000 | 7 = 0111 |
| E | 2 | 7 = 0111 | 0 = 0000 |
| D | 7 | 1 = 0001 | 6 = 0110 |
| C | 5 | 2 = 0010 | 2 = 0010 |
| B | 8 | 1 = 0001 | 3 = 0011 |
| F | F | 1 = 0001 | 0 = 0000 |

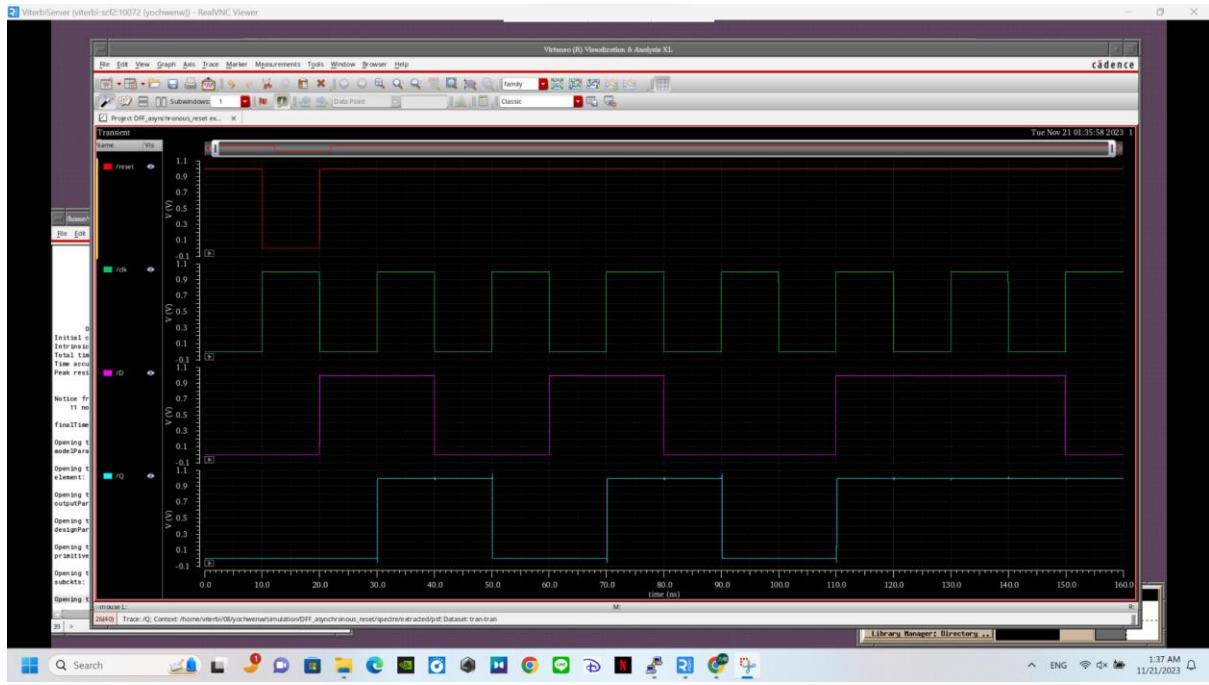
Post-layout functional verification: Arbiter:



Expected S: 0000 0010 0110 0000 1101

Expected Stall signal: 1110 0100 0000 0000 0000

Post-layout functional verification: DFF:



Expected output: Q = D

Post-layout functional verification: Complete System:

Expected output: 00 61 2A 2D 63 17 80 02 0D 04

Note: As we only need to check the first 10 results, 5A of the end of the output is not valid because the arbiter will oscillate ($\text{reqD} = 1$, $\text{reqM} = 1$) and it will keep reproducing the last result with either multiplier or divider.

Expected stall signal: 1000 1001 00

Schematic Functional Verification



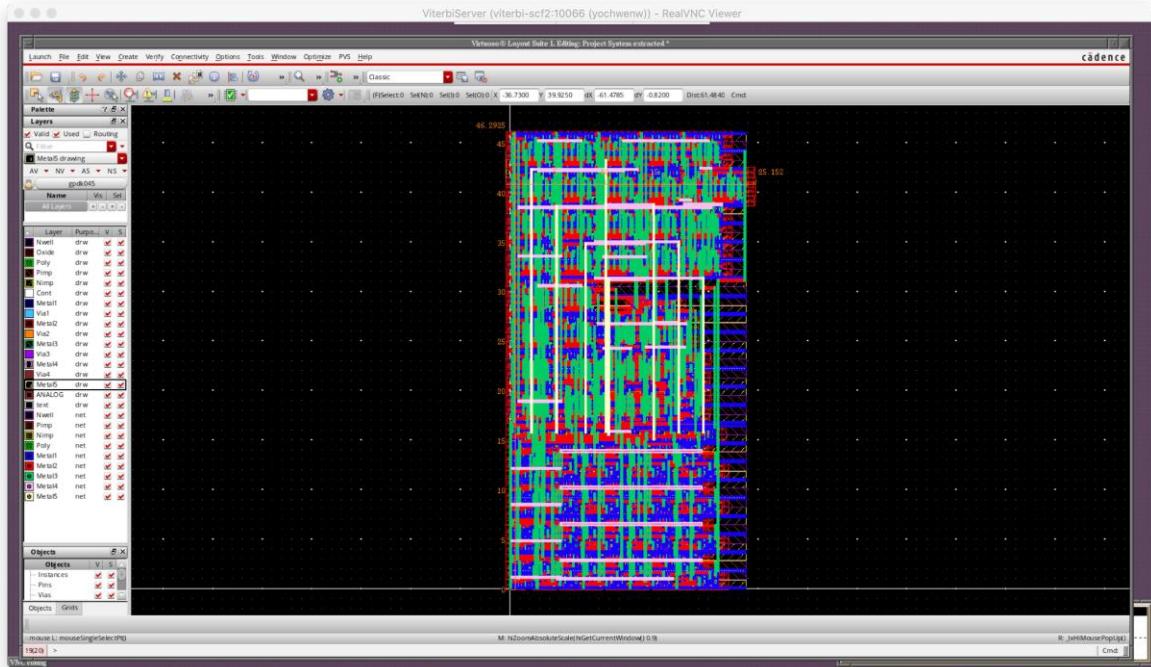
Extracted Layout Functional Verification



Part 2: Performance Metrics Calculation

Area measurement:

Extracted Layout



Extracted area: $25.152 \times 46.2925 = 1164.35 \mu\text{m}^2 = 0.00116 \text{ mm}^2$

Average Delay measurement:

Schematic:



Minimum clock period = 1.4 ns

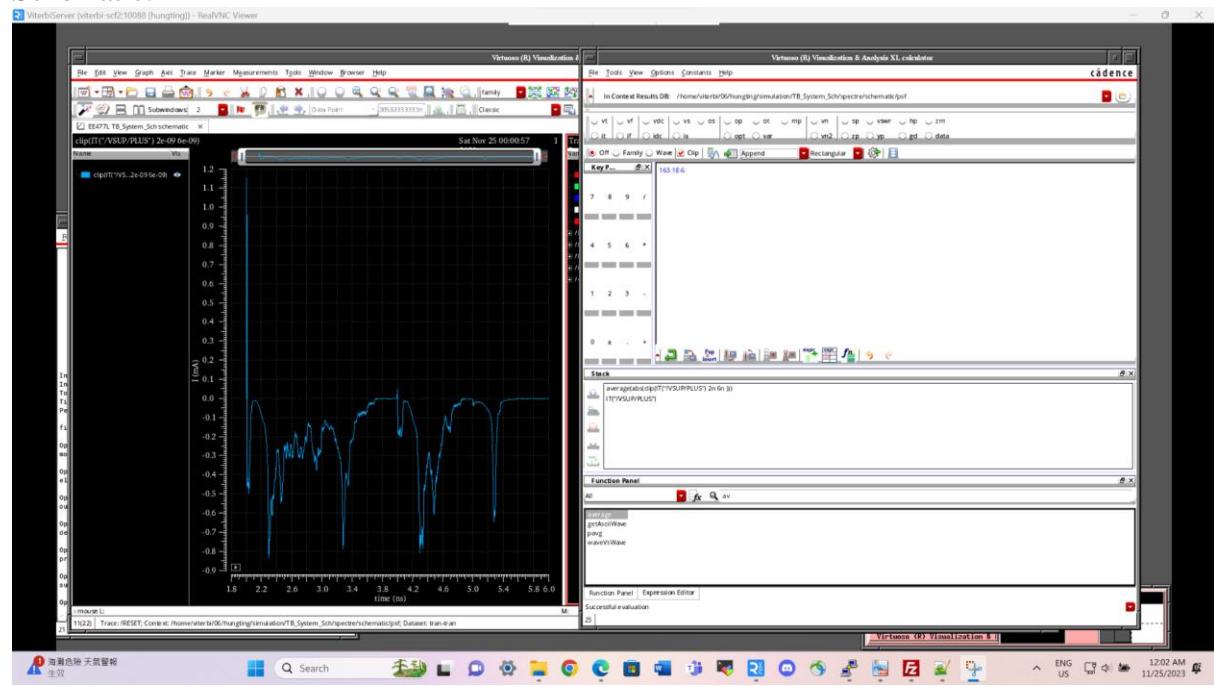
Extracted:



Minimum clock period = 1.4 ns

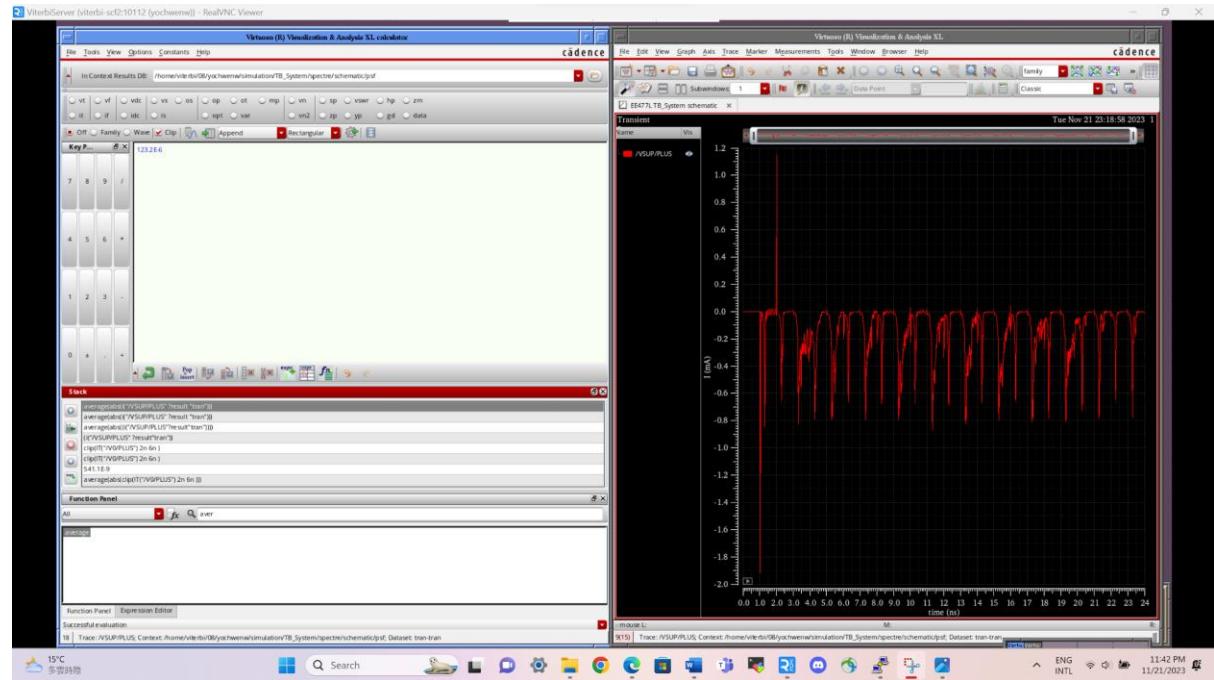
Average power measurement:

Schematic:



$$I = 163.1 \times 10^{-6} \text{ A}, P = VI = 163.1 \mu\text{W}$$

Extracted:



$$I = 123.2 \times 10^{-6} \text{ A}, P = VI = 123.2 \mu\text{W}$$

PAD Table:

metal layer used: 5

| | Schematic | Extracted |
|--------------|------------------|------------------------|
| Power | 163.1 uW | 123.2 uW |
| Area | x | 0.00116 mm^2 |
| Delay | 1.4 ns | 1.4 ns |

PAD number:

$$\text{PAD} = \text{Power (P)} * \text{Area (A)} * \text{Delay (D)} = 123.2 \text{ uW} * 0.00114 \text{ mm}^2 * 1.4 \text{ ns}$$

$$\text{PAD} = 0.211 (\text{uW} * \text{mm}^2 * \text{ns})$$

Appendix

Vector files for post layout functional verification testing:

Multiplier:

```
radix 4 4
io i i
vname A<[3:0]> B<[3:0]>
tunit ns
slope 0.01
vih 1.0
vil 0.0

0 0 0
10 7 5
20 A 0
30 F 3
40 9 E
50 4 1
60 8 B
70 F F
```

Divider:

```
radix 4 4
io i i
vname div<[3:0]> d<[3:0]>
tunit ns
slope 0.01
vih 1.0
vil 0.0

0 3 A
10 F 5
20 7 A
30 E 2
40 D 7
50 C 5
60 B 8
70 F F
```

Arbiter:

```
radix 4 4 4 4  
io i i i i  
vname IN_A<[3:0]> IN_B<[3:0]> IN_D<[3:0]> IN_dv<[3:0]>  
tunit ns  
slope 0.01  
vih 1.0  
vil 0.0
```

```
0 0 0 0 0  
1 0 0 0 0  
2 7 5 4 2  
3 7 5 4 2  
4 A 0 5 2  
5 A 0 5 2  
6 F 3 8 6  
7 F 3 8 6  
8 9 E 7 4  
9 9 E 7 4  
10 4 1 A 5  
11 4 1 A 5  
12 8 B B 6  
13 8 B B 6  
14 F F C 6  
15 F F C 6  
16 F F D 5  
17 0 0 0 1  
18 0 0 0 1  
19 7 5 4 2  
20 7 5 4 2  
21 A 0 5 2  
22 A 0 5 2  
23 F 3 8 6
```

Complete system:

radix 4 4 4 4

io i i i i

vname IN_A<[3:0]> IN_B<[3:0]> IN_D<[3:0]> IN_dv<[3:0]>

tunit ns

slope 0.01

vih 1.0

vil 0.0

0 F F F F

1.4 4 9 d 7

2.8 6 7 5 b

4.2 F 3 7 2

5.6 B 9 A 7

7 C B F 2

8.4 3 3 8 A

9.8 5 A A 5

11.2 D 1 E 1

12.6 F 6 8 2

Work Distribution Table:

| Hung-Ting Tsai | Li Wei Liu | Yo-Chwen Wang |
|--|--|--|
| Phase 1 | | |
| HA/FA design | 2-1 mux | Half Subtractor/ Full Subtractor |
| Multiplier Design | Functional Verification for Multiplier and Divider | Divider Design |
| Delay Measurement | Delay Measurement | Delay Measurement |
| Phase 2 | | |
| FSM design | FSM design | FSM design |
| 1 bit DFF | Arbiter | Arbiter |
| Complete System Schematics (draw, confirm, functional verification, and time delay measurements) | Complete System Schematics (draw, confirm, functional verification, and time delay measurements) | Complete System Schematics (draw, confirm, functional verification, and time delay measurements) |
| Phase 3 | | |
| DFF, 8bit DFF | And/OR gate | Half adder |
| 2-1 mux, 8bit- 2-1 mux | Full adder | Half Subtractor, Full Subtractor/ FS Mux |
| Full adder | Multiplier | Divider |
| Functional Verification for past design, Complete System Layout | Complete system layout | Complete system layout |
| PAD, complete system verification | PAD, complete system verification | PAD, complete system verification |

