

Improving the coherence time of superconduct- ing qubits by de- sign

A procedure to cal-
culate participa-
tion ratios

R.A. Koster

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Improving the coherence time of superconducting qubits by design

A procedure to calculate participation ratios

by

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Preface

Preface...

R.A. Koster
Delft, January 2016

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Introduction

Since the introduction of the transmon quantum bit (transmon qubit) by Koch et al. in 2007 [3] as a promising candidate of qubits there have been investigations into sources of decoherence of these qubits. C. Wang et al. found that surface dielectric dissipation is probably still the major limiting factor for the coherence time of transmon qubits [5]. The different surface dielectrics introduced to the system during production have distinct material compositions [1] and as a result will have a different impact on the coherence time [5]. Qubit structure design itself will dictate how the Electric field is distributed through the dielectrics.

The goal of this research is to determine this distribution and to use this information to design a transmon qubit in such a way as to be able to avoid concentrating the Electric field in regions containing more lossy dielectric material. Being able to do so may better the ability to design transmon qubits with longer coherence times.

The following section will provide necessary background information to substantiate the above. Information particularly relevant to this research will be provided in the next chapter.

Quantum computing and quantum bits

In order to understand the importance of this research a minimal understanding of a quantum computer is necessary.

A classical computer uses binary digits (or bits) for computation and storage. Every bit can be in one of two states, usually denoted by zero or one. A quantum computer however uses what has been named quantum bits, or qubits for short, instead. These qubits can represent a zero or a one, or any superposition of these two states. The superposition of the qubits combined with the right algorithms allows a quantum computer to perform certain tasks significantly faster than is currently possible using classical computers. Prominent examples are those that deal with large sets of data such as querying of information in large sets of data, and optimization problems such as the travelling salesman problem [2].

There are multiple types of qubits which use different methods to achieve a state of superposition. Examples are the photon polarization qubit and the electron spin qubit. The qubit under investigation in this research is the transmon qubit. Further information about this type of qubit will be given in the next chapter.

A common necessity for these qubits is that they must maintain their state of superposition for as long as any calculation is running. In other words, their coherence time must be sufficiently long.

-General information about quantum computing. Benefits, application etc. -quantum bits; importance of longer coherence time

Restatement of the problem -Role of dielectric lossy materials -why is this research important?!

-Knowing how design choices influence the participation ratio of lossy layers.

Restatement of the response - "In order to address this problem, I will ...".

Roadmap -How will the thesis proceed

2

Theory

Electric fields

Perfect Electric Conductor

As the qubit is supercooled to temperatures of only a few mK, the metal in the qubit is treated as a Perfect Electric Conductor (PEC).

Continuity rules

Stored energy

The energy stored in the Electric field in a material can be calculated using equation (2.1)

$$W = \frac{\epsilon}{2} \int |E|^2 dV \quad (2.1)$$

Where ϵ is the permittivity of the material and V is the volume occupied by the material.

The transmon qubit

The qubit under investigation during this project is the so called transmon qubit. A traditional transmon qubit consists of a pair of Josephson junctions connected to two superconducting pads. The structure is surrounded by a grounded metal plane. Other parts of the structure are the transmission line resonator, the quantum bus resonator and the

LC-circuits

The transmon qubit can be treated as a simple LC-circuit. The Josephson junction is replaced by an inductor and the different capacitors are replaced by an single equivalent capacitor. The resulting simplified system can be seen in figure 2.1.

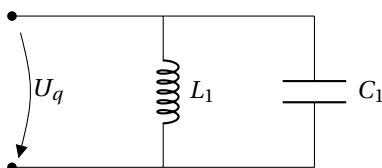


Figure 2.1: A simple parallel LC-circuit

Energy in an LC-circuit

In order to determine the participation ratio of the lossy layers in storing energy in the system, the total energy must be known. The total energy stored in an LC-circuit at any time can be calculated as follows:

$$W = \frac{1}{2} CV^2 \quad (2.2)$$

Where C is the total capacitance of the system and V the voltage over the systems.

Resonance frequency of an LC-circuit

Sources of decoherence

In order for the qubit to be coherent for a sufficiently long time period, sources of decoherence must be eliminated. Sources include spontaneous emission, the Purcell Effect, quasiparticle tunnelling and flux coupling [3]. The source in question during this project is the loss through dielectric materials in the system. It is believed to be a prominent, if not limiting source of decoherence [4][3].

Dielectric loss

During production of qubits, different procedures introduce lossy materials to the structure. An important property of each of these materials is their permittivity. It will determine the strength of the field and the energy stored inside the layers.

Two-Level Systems

The participation ratio

To determine what kind of structure design may improve coherence time the participation ratio of lossy layers can be calculated. If the assumption is made that the Electric field remains constant inside the lossy layer equation (2.1) can be rewritten as follows:

$$W = \frac{\epsilon}{2} t \int |E|^2 dA \quad (2.3)$$

Where ϵ is the permittivity of the material and t is the thickness of the lossy layer. Furthermore, A is the surface area of the lossy layer.

Model of the system

In order to calculate the participation ratio of the different lossy layers in an arbitrary structure, it is simulated using 3D EM simulation software called Computer Simulation Technology Studio Suite (CST). Certain assumptions and simplifications are made to allow for simulation within CST. These are discussed below. A step-by-step guide for setting up a simulation in CST can be found in appendix A.

The qubit as an LC-circuit

In order to obtain the energy contained in the complex transmon qubit system, it can be reduced to a simple LC-circuit. The capacitances created by the pads and the ground plane can be reduced to a single equivalent capacitor representing the capacitance of the entire system. The Josephson junction is represented by an inductor. What is left is an LC-circuit where the inductance can be adjusted by changing its value directly and the capacitance can be changed by changing the geometry of the system (the pads more specifically). The total energy contained in the system is then given by formula (2.2)

Materials and dimensions

Certain choices of materials and dimensions are valid for all qubit designs in this project. They are listed in table 3.1 below.

Lossy layers

The material layers present on the different material interfaces are assumed to have an equal thickness of around 3 nm [6]. Different layers do have distinct material compositions. The dominant materials are Niobium Oxides (NbO), Silicon Oxides (SiO), and Silicon Nitrides (SiN) for the Metal-Air (MA), Substrate-Air (SA), and Metal-Substrate (MS) interfaces respectively. An overview is given in table 3.1. A simple representation of the structure can be seen in figure 3.1. The relatively small thickness of the layers suggests that the impact they have on the electric field is small. During simulation their impact is neglected and the layers are therefore omitted. The exclusion of thin lossy layers prevents the necessity for mesh elements with sub-nano meter size. This significantly reduces the number of mesh elements and allows for the simulation on the system in its entirety.

SOURCE needed?

	Material	Thickness	Dielectric constant
Pads	PEC	10 μm	1
Substrate	Silicon	520 μm	11.45
Ground	PEC	-	1
MA	NbO	~3 nm	10
MS	SiN	~3 nm	7.5
SA	SiO	~3 nm	3.9

Table 3.1: Parameters that are valid for all qubit designs used in this research

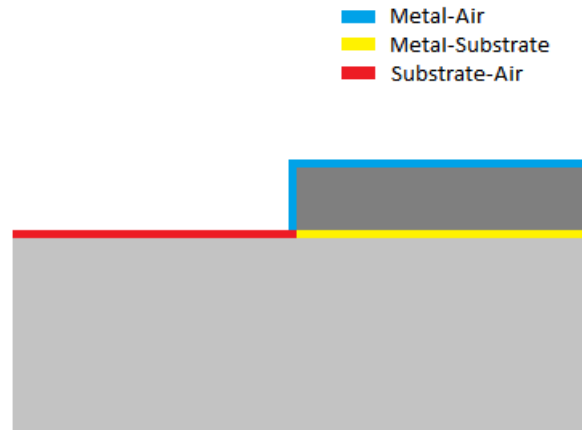


Figure 3.1: Simplification of the system including three lossy layers. The substrate and metal are depicted in light and dark grey respectively

Meshing

To reduce simulation times the initial mesh is of critical importance. After each mesh refinement the fields are simulated anew. While CST is able to select regions of importance in the system where it should further refine the mesh, it can only do so after having simulated the fields. When establishing the initial mesh the importance of different regions of the system must be taken into account. Two important steps taken to improve the initial mesh during this project are described below.

Ground

To reduce the number of mesh elements, the ground pad is replaced by a sheet of PEC with zero thickness. Considering the field in the ground region is small compared to the field at the edges of the pads its contribution to the participation ratio is also small. Investing more computation time on the ground plane region by increasing the density of mesh elements there, would therefore also have limited impact on the participation ratio.

Pads

The pads being the source of the electric field, it is to be expected that the intensity will be greatest in this region. Furthermore, electric field lines tend to have a higher density at the edges of a metal. Considering this, the intensity of the electric field in the entire system is expected to be greatest around the edges of the metal pads. The initial mesh should reflect this by being very fine in these regions. In order to achieve this the edges of the metal pads are rounded as in figure 3.2. A comparison between the resulting mesh and a standard initial mesh is depicted in figure 3.3. The difference is significant; an increase of mesh element count from 10776 to 590570. It would take CST around 8 iterations to achieve similar mesh element counts. The exact steps taken to achieve this in CST can be found in appendix A.

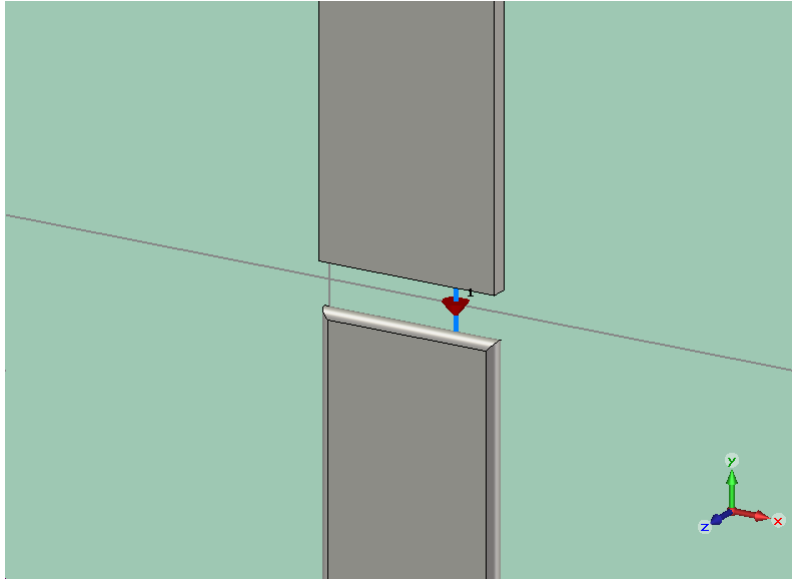
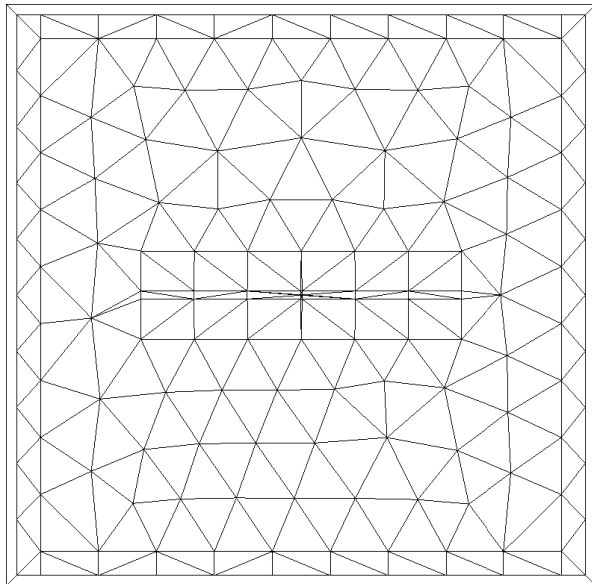
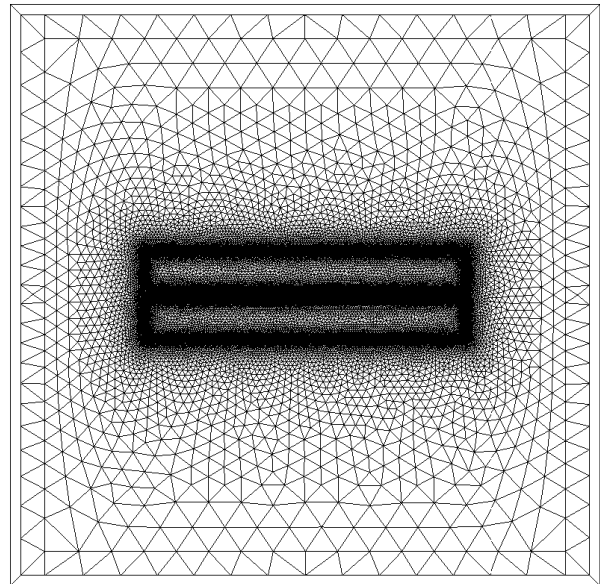


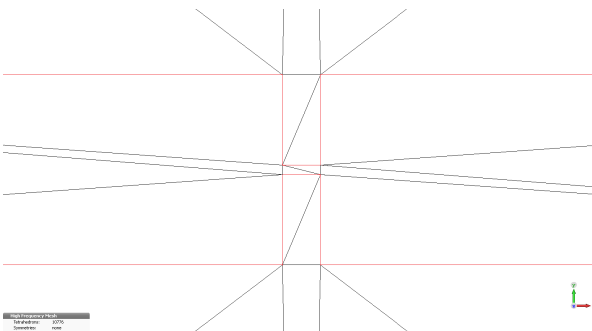
Figure 3.2: An illustration of the blending of the pad edges. The bottom pad has been blended whereas the top pad has not.



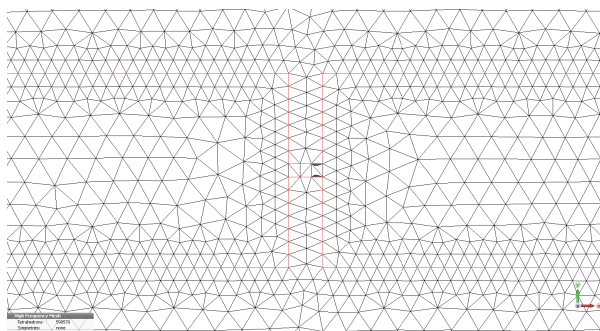
(a) Simple mesh



(b) Refined mesh



(c) Simple mesh, junction



(d) Refined mesh, junction

Figure 3.3: A comparison of the initial mesh before (a and c) and after (b and d) blending of the pad edges. (c) and (d) show the region close to the junction leads which are in the very centre in (a) and (b). The edges of the pads are highlighted in red. The total mesh element count is 10776 and 590570 for the simple and refined mesh respectively.

Results and Discussion

The starting point of this project was the familiar interdigitated qubit (see figure 4.1). This chapter will start with a discussion of the results gathered on this design.

First, the influence of different parameters on the capacitance of structures was determined. This knowledge enables designing structures with a specific capacitance necessary for a qubit with a certain frequency (see equation (??)). The target capacitance is 60 fF . With an inductor having an inductance of 10 nH this result in a resonance frequency of around 6.5 GHz .

Secondly, the participation ratio of the lossy layers is determined. This will give insight into what design decisions can be made to reduce these participation ratios. Taking these insights into account, a second qubit design was investigated in similar fashion.

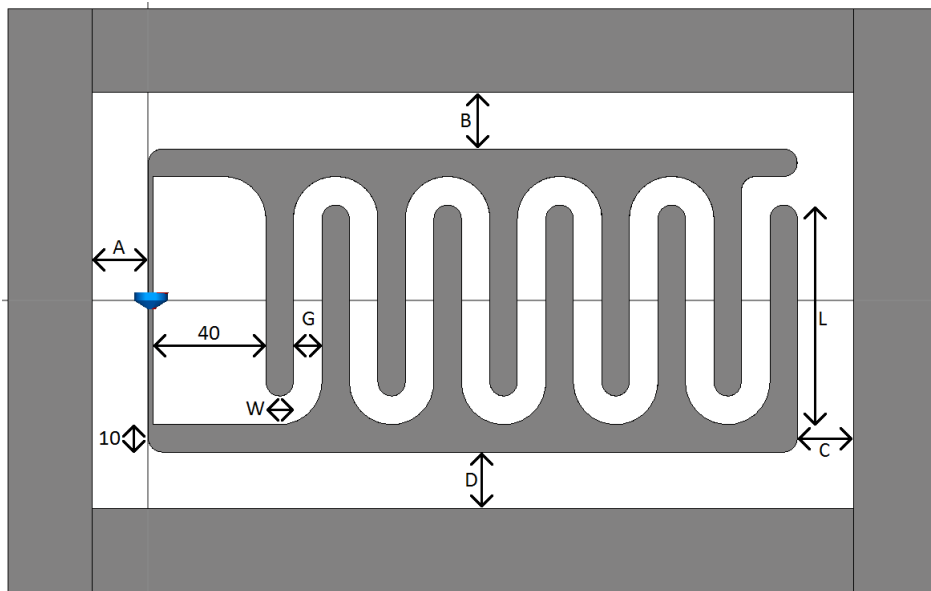


Figure 4.1: The interdigitated qubit design including parameters and dimensions valid for all iterations of the design. Dimensions are in micrometers.

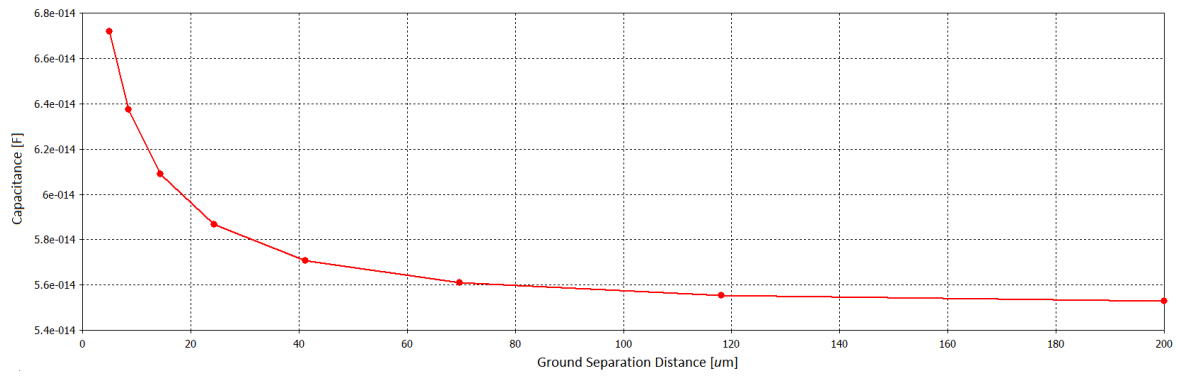


Figure 4.2: Capacitance of the system as a function of ground plane separation

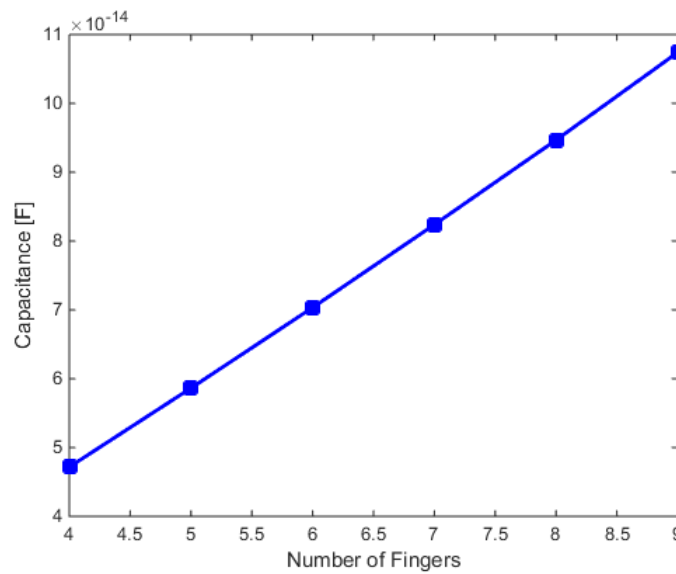


Figure 4.3: Capacitance as a function of the amount of fingers in the interdigitated qubit design. Finger width and length are equal in all qubits.

Interdigitated qubit

As the name suggests the interdigitated qubit consists of two pads having a certain amount of fingers. The pads are positioned such that the fingers are at an equal distance from each other. The distance between the inductor and the first finger was set to 40 μm for all interdigitated qubit designs. An overview of the design with its parameters is depicted in figure 4.1

The capacitance

To better determine the influence of the pad design on the capacitance of the system, the influence of the ground plane is determined as a function of separation distance. Figure 4.2 indicates that the influence of the ground plane on the capacitance of the system decreases rapidly with increasing separation distance. The influence of the ground plane becomes insignificant only at a separation distance of around 100 μm . So, in order to determine the influence of changes in pad design on the capacitance (and participation ratio) of the system, the separation distance of the ground plane should be carefully kept equal among pad designs.

For the interdigitated pad design specifically, the first parameter under investigation is the amount of 'fingers' in the qubit. The capacitances of qubits with 4 to 9 fingers were determined. The finger length, width and separation were not changed. As can be seen in figure 4.3, the relationship appears to be linear. This can be explained by viewing the addition of a finger as the addition of an extra capacitor in parallel.

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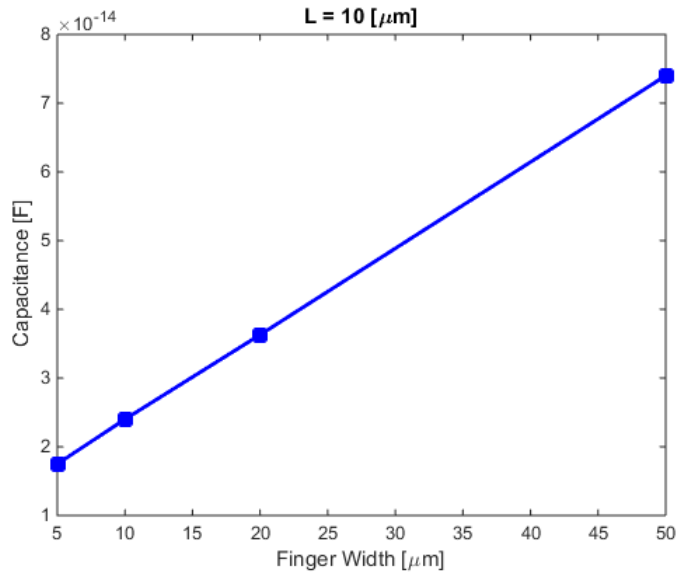


Figure 4.4: Capacitance as a function of finger width in the interdigitated qubit design. All qubit have five fingers and equal finger length.

Next the influence of the finger width is determined. The finger separation is kept equal to the finger width. For a design with five fingers the results are depicted in figure 4.4.

Having determined the dependencies, qubits can be designed to have specific capacitances. Keeping all other parameters equal, the capacitance of earlier systems was tuned by adjusting the length of the fingers. For qubits with 5 fingers and a finger width of 5 to 50 μm the finger length was adjusted between 10 and 100 μm .

The results are combined in figure 4.5. From the figure it is possible to determine the finger length needed to achieve the target capacitance of 60 $f\text{F}$. For qubits with a finger width of 5 μm , 10 μm , and 20 μm , their length must be 87 μm , 76 μm , and 56 μm respectively.

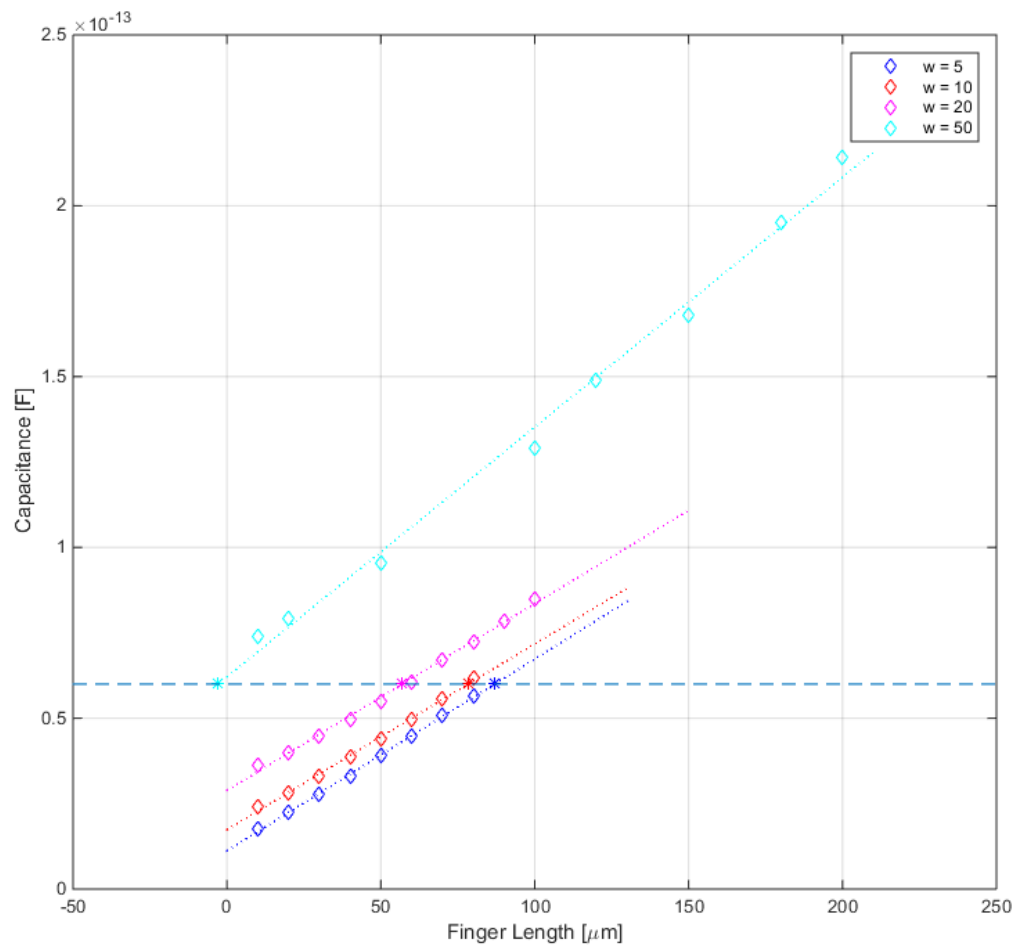


Figure 4.5: A plot of the capacitance as a function of finger length for several finger widths. dotted lines represent linear fits of the data. The horizontal dashed line is a guideline for the eye showing the necessary finger length to make a 60 fF capacitor; $87\text{ }\mu\text{m}$, $76\text{ }\mu\text{m}$, and $56\text{ }\mu\text{m}$ for qubits with a finger width of $5\text{ }\mu\text{m}$, $10\text{ }\mu\text{m}$, and $20\text{ }\mu\text{m}$ respectively.

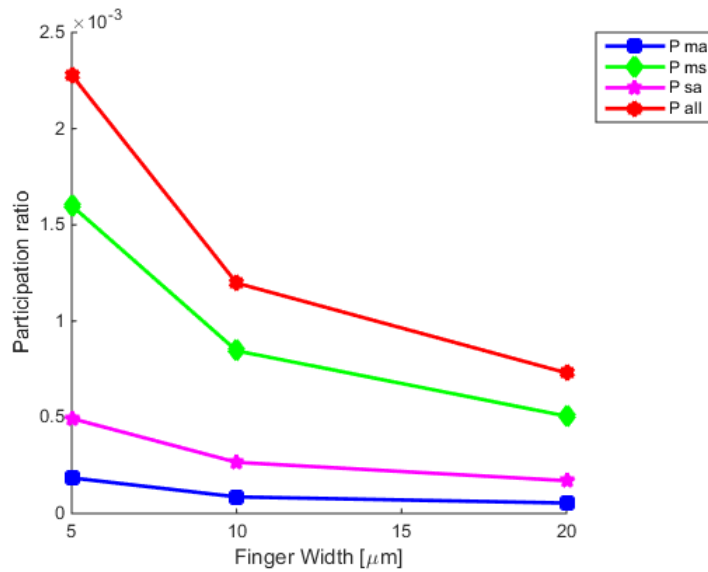


Figure 4.6: A plot of the different ratios for qubits with five fingers. The length of the fingers has been adjusted for each qubit to reach a capacitance of 60 fF. For qubits with a finger width of 5 μm , 10 μm , and 20 μm , their lengths are 87 μm , 76 μm , and 56 μm respectively.

Fingers	Finger Width [μm]	Finger Length [μm]	P ma	P ms	P sa	P all
5	5	87	1.85e-04	1.60e-03	4.94e-04	2.28e-03
5	10	76	8.62e-05	8.45e-04	2.66e-04	1.20e-03
5	20	56	5.43e-05	5.06e-04	1.70e-04	7.31e-04
10	5	36	1.36e-04	1.30e-03	4.12e-04	1.85e-03
10	10	26	7.56e-05	7.33e-04	2.46e-04	1.06e-03

Table 4.1: The relevant parameters for interdigitated qubit and the resulting participation ratios. For all designs the finger length has been tuned to result in a qubit with a capacitance of 60 fF.

The participation ratios

Using the previous results several interdigitated qubits were designed to have a capacitance of 60 fF. An overview of the relevant parameters can be seen in table 4.1. The resulting participation ratios of the different lossy layers can be seen in the same table and are plotted in figure 4.6 for those qubits with 5 fingers. As the finger width is increased and the finger length decreased, all participation ratios decrease.

By default the corners of the fingers were rounded (as in figure 4.1). As this was not standard practice the influence of doing so was determined retroactively. To do so the corner radius of the fingers (with a width of 20 μm) was changed between 1 and 10 μm (10 μm making semi-circles at the finger tips). The resulting participation ratios can be seen in table 4.2 and figure 4.7. All participation ratios tend to decrease as the corner radius is increased.

The influence of the ground plane separation distance on the participation ratios was also determined. The distance was changed between 10 μm and 200 μm . The resulting participation ratios can be found in table 4.3 and figure 4.8. Again, all participation ratios show a downward trend with increasing separation

Corner radius [μm]	P ma	P ms	P sa	P all
1	6.30e-05	6.04e-04	1.83e-04	8.50e-04
2	6.57e-05	6.00e-04	1.82e-04	8.47e-04
5	6.62e-05	5.76e-04	1.78e-04	8.20e-04
8	6.18e-05	5.93e-04	1.80e-04	8.34e-04
10	5.43e-05	5.06e-04	1.70e-04	7.31e-04

Table 4.2: The participation ratios for different corner radii.

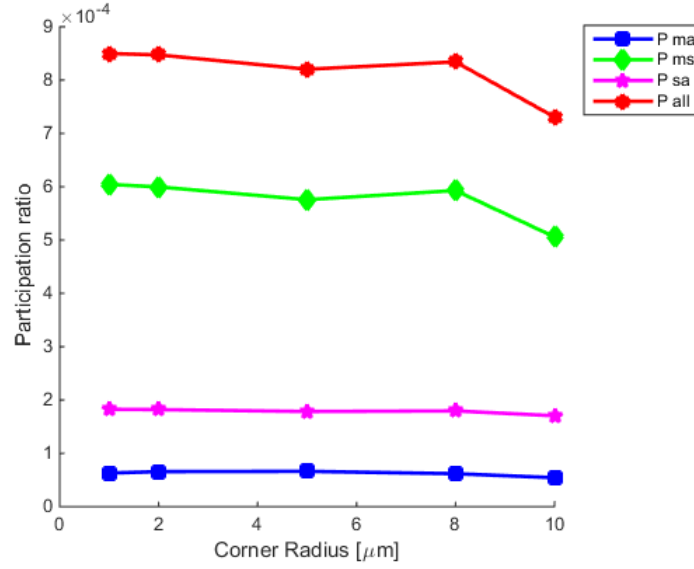


Figure 4.7: A plot of the different participation for several corner radii. However slowly, all ratios tend to decrease with increasing radius.

Ground Separation [μm]	P ma	P ms	P sa	P all
10	5.71e-05	5.31e-04	1.78e-04	7.67e-04
20	5.43e-05	5.06e-04	1.70e-04	7.31e-04
50	5.22e-05	5.04e-04	1.61e-04	7.17e-04
100	4.82e-05	4.92e-04	1.54e-04	6.94e-04
200	5.10e-05	4.90e-04	1.59e-04	7.00e-04

Table 4.3: The participation ratios for different ground separation distances.

distance. The influence of increasing the the separation beyond 100 μm is very small.

Looking at these results for the interdigitated qubit design it can be seen that the most significant change in participation ratios was achieved by making the fingers shorter and separating them further. Extrapolating these changes would indicate that a qubit consisting of two parallel rectangular pads would have even smaller participation ratios.

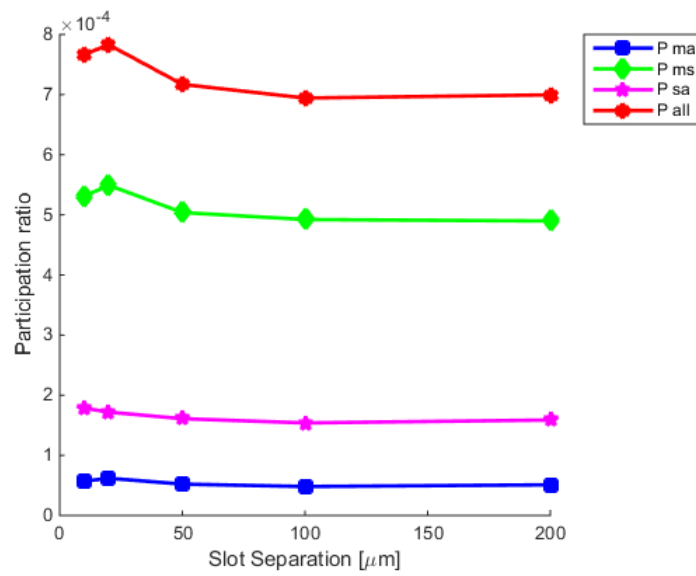
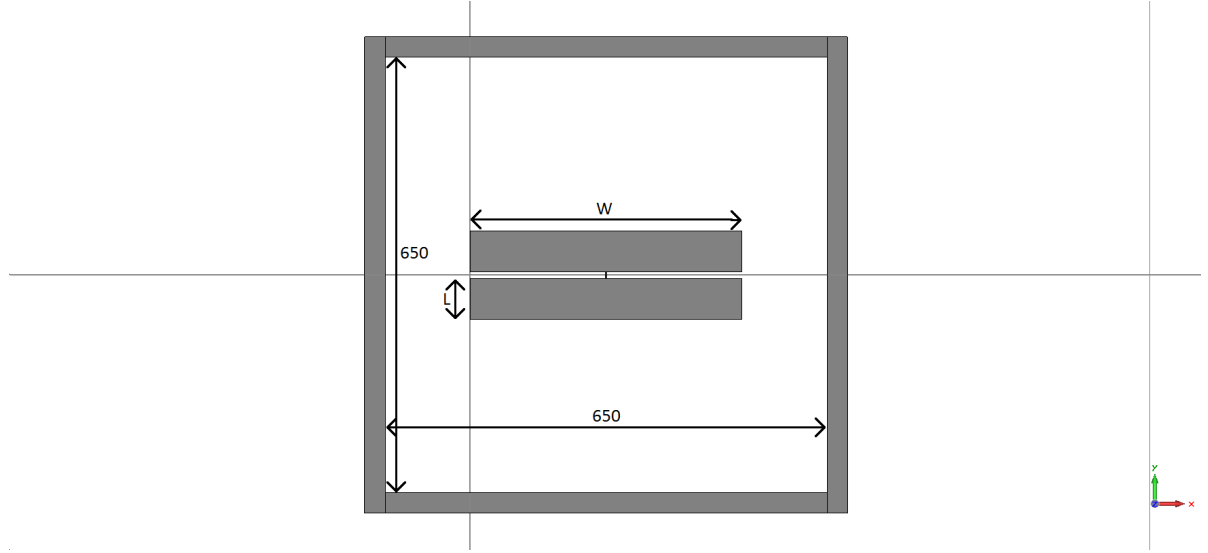


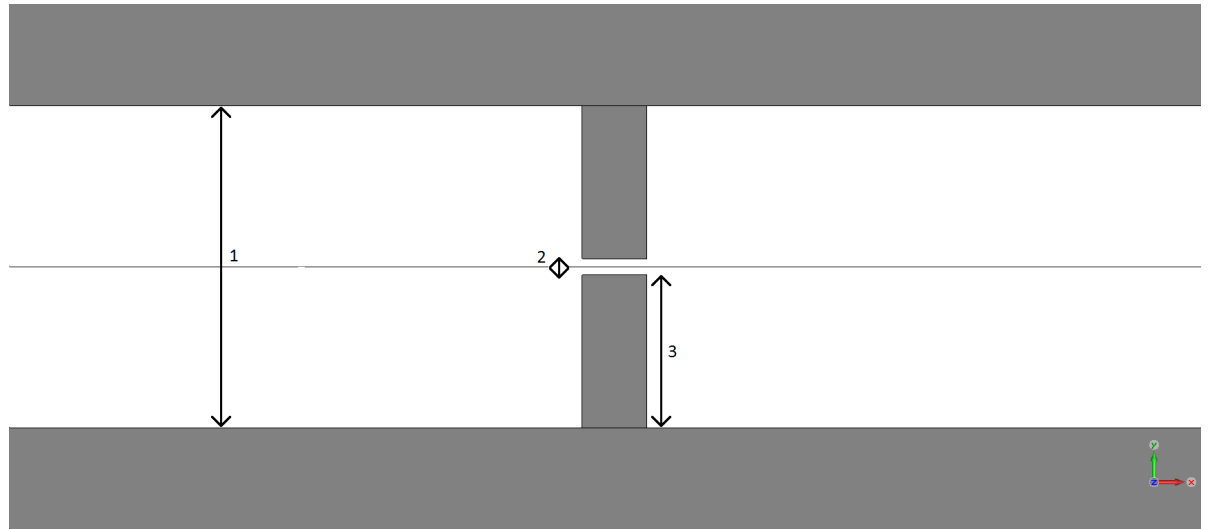
Figure 4.8: A plot of the different participation ratios for several separation distances to the ground plane. However slowly, all ratios tend to decrease with increasing separation.

Parallel pad qubit

The resulting qubit design can be seen in figure 4.9. It consists of two large parallel pads which are connected two smaller pads with the inductor in-between. The ground plane consist of a square slot at a relatively large distance from the qubit. Due to its simplicity, there are fewer ways of changing the qubit. The parameters under consideration are the pad separation, the pad width, and the radius of the corners. Again, first, the influence different parameters have on the capacitance of the system was determined. Afterwards the participation ratios of different configurations were calculated.



(a) Overview of the parallel pad qubit



(b) Zoomed in view of the center of the qubit.

Figure 4.9: The parallel pad qubit design including parameters and dimensions valid for all iterations of the design. (a) W is the width of the pads, L is the length of the pad, the size of the grounded slot here is $650 \mu\text{m}$. (b) 1 is the pad separation distance. 2 is the junction separation distance which is $0.5 \mu\text{m}$ for all qubits. 3 is the length of the junction lead which depends only on the separation distance of the qubit.

The capacitance

Similar to adding extra fingers to the interdigitated qubit, widening the pad width is expected to linearly increase the capacitance of the system. The pad width was changed between 300 and $500 \mu\text{m}$. The data shown in figure 4.10 indeed shows a linear proportionality.

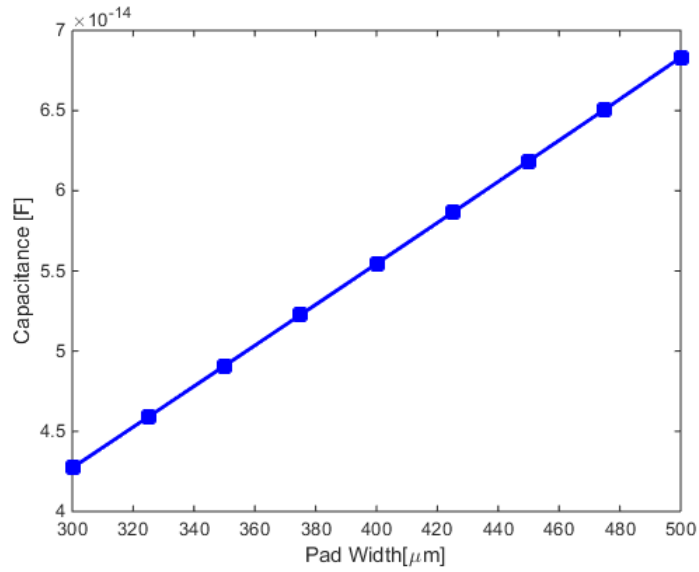


Figure 4.10: The capacitance of parallel pad qubits with different pad widths.

The capacitance of a standard parallel plate capacitor is inversely proportional to the plate separation. Similar proportionality is expected for the parallel pad qubit system. The pad separation was set between 5 and 60 μm . The resulting capacitances can be seen in figure 4.11.

Finally the radius of pads' corners are changed. They were set between 5 and 30 μm . The resulting capacitances are shown in figure 4.12.

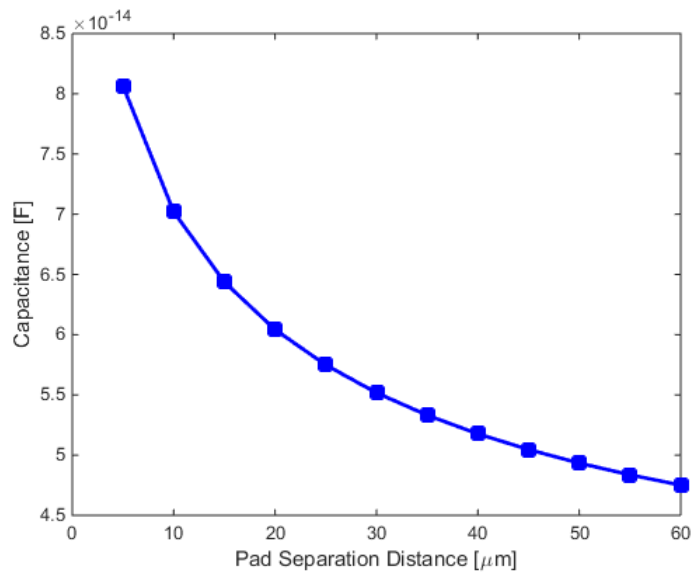


Figure 4.11: The capacitance of parallel pad qubits with different pad separation distances.

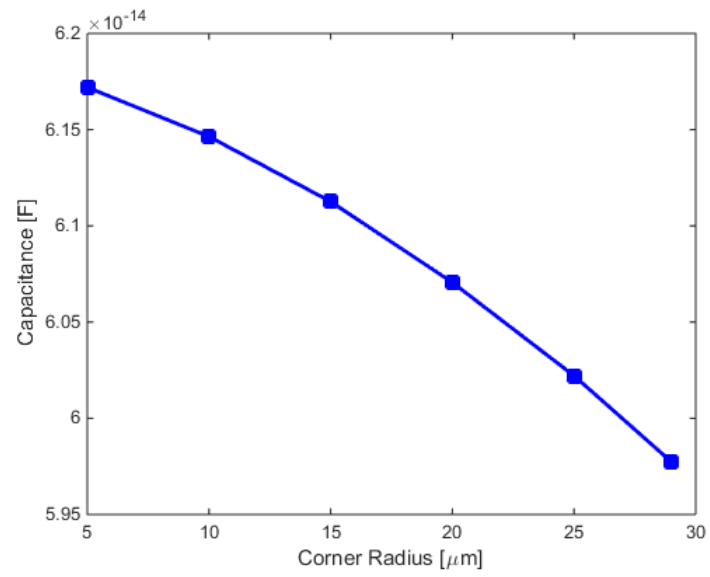


Figure 4.12: The capacitance of parallel pad qubits with different corner radii.

Pad Width [μm]	P ma	P ms	P sa	P all
300	4.71e-05	3.51e-04	1.08e-04	5.06e-04
350	4.29e-05	3.44e-04	1.04e-04	4.91e-04
400	4.27e-05	3.38e-04	1.02e-04	4.82e-04
450	4.17e-05	3.32e-04	1.01e-04	4.74e-04
500	4.04e-05	3.28e-04	9.92e-05	4.68e-04

Table 4.4: The participation ratios of parallel pad qubits with different pad widths.

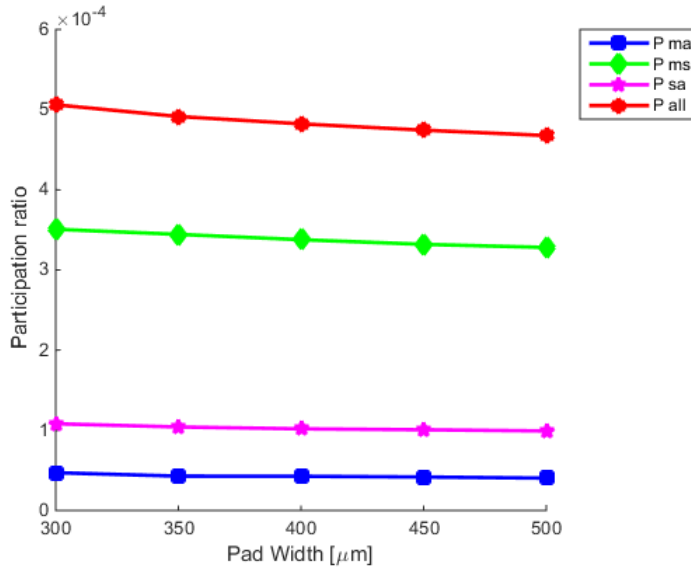


Figure 4.13: The participation ratios of parallel pad qubits with different pad widths.

The participation ratios

Comparing the two qubit designs; increasing the finger width (and separation) in the interdigitated qubit can be seen as increasing the pad separation and pad width in the parallel pad qubit. Therefore the participation ratios are expected to decrease when increasing pad width or separation. The influence of three parameters on the participation ratios were investigated separately: the pad separation, the pad width, and the corner radius. Contrary to what was done during the investigation of the interdigitated qubit, the resonance frequencies of all parallel pad qubits were kept equal by changing the value of the inductance (see formula (??)).

Starting with the pad width which was again changed between 300 and 500 μm . Table 4.4 and figure 4.13 show the resulting ratios, all of them decreasing with increasing width.

Secondly, the separation between the two pads was changed between 5 and 60 μm . The results in table 4.5 and figure 4.14 again show decreasing ratios for all layers with increasing separation.

Finally, the radius of the corners was changed between 5 and 30 μm , where a radius of 30 μm results in an semi-circle on the sides. Although the resulting ratios in table 4.6 and figure 4.15 show a decreasing trend, the change is much less significant compared to that of the interdigitated qubit.

Pad Separation [μm]	P ma	P ms	P sa	P all
5	6.42e-05	5.59e-04	1.82e-04	8.42e-04
10	4.65e-05	4.26e-04	1.28e-04	6.00e-04
20	4.02e-05	3.21e-04	9.67e-05	4.58e-04
50	3.35e-05	2.55e-04	7.70e-05	3.65e-04

Table 4.5: The participation ratios of parallel pad qubits with different pad separation distances.

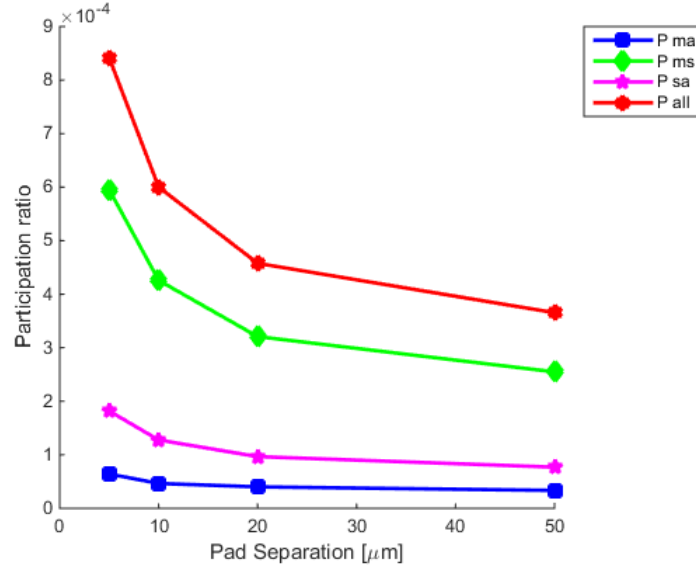


Figure 4.14: The participation ratios of parallel pad qubits with different pad separation distances.

Corner Radius [μm]	P ma	P ms	P sa	P all
5	3.74e-05	3.03e-04	9.53e-05	4.35e-04
10	3.56e-05	3.01e-04	9.47e-05	4.31e-04
15	3.67e-05	2.98e-04	9.60e-05	4.31e-04
20	3.37e-05	3.00e-04	9.51e-05	4.29e-04
25	3.47e-05	2.97e-04	9.41e-05	4.26e-04
29	3.49e-05	2.99e-04	9.47e-05	4.28e-04

Table 4.6: The participation ratios of parallel pad qubits with different corner radii.

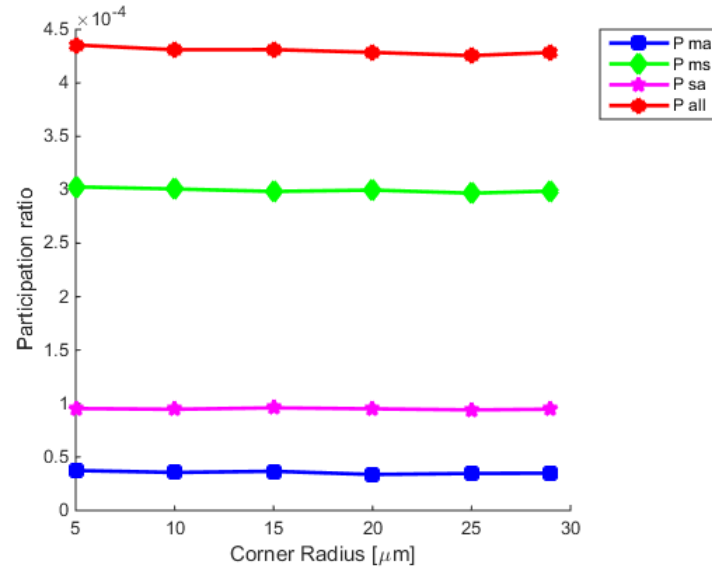


Figure 4.15: The participation ratios of parallel pad qubits with different corner radii.

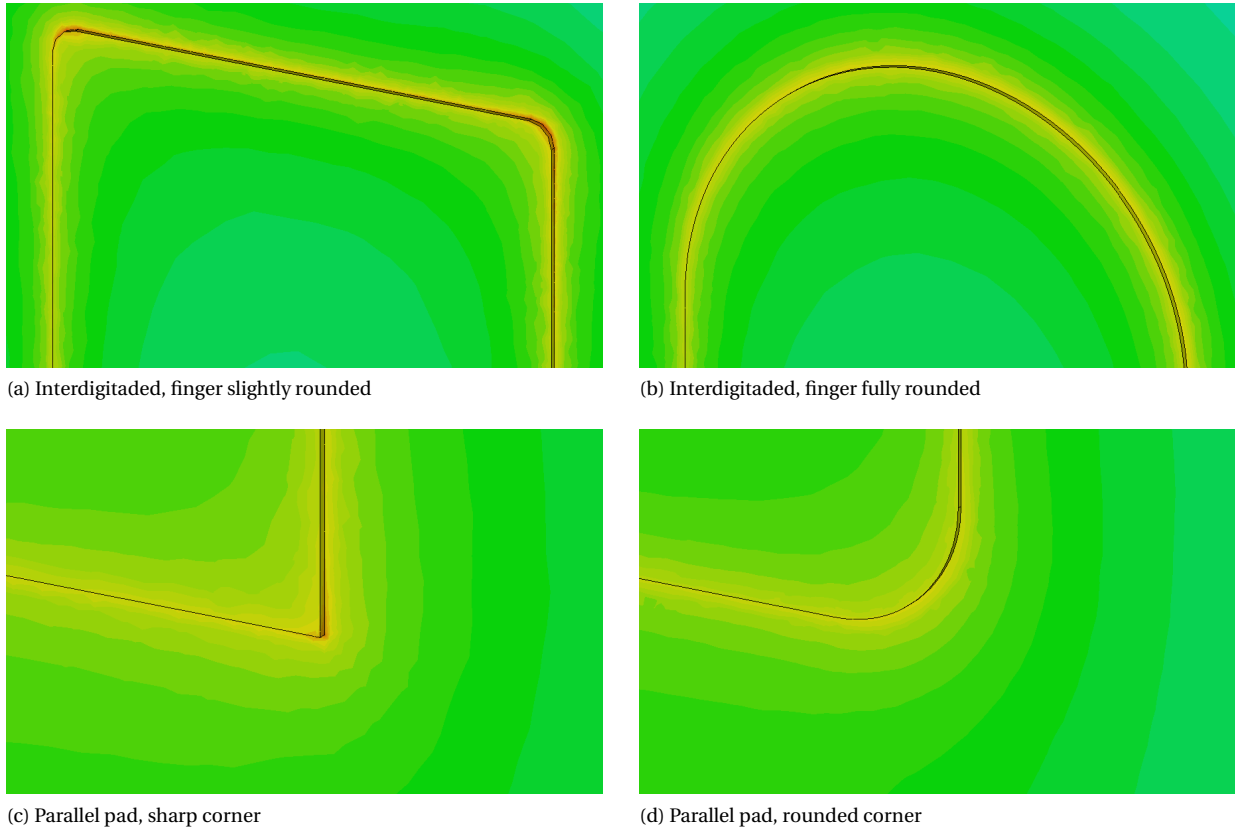


Figure 4.16: The absolute value of the electric field in the area around corners. The rounding of the corners results in less concentrated electric fields.

Further Discussion

Finally, to explain some of the results, the simulated electric fields can be looked at. Figure 4.16 shows the absolute value of the electric field around the corners of the interdigitated (a and b) and parallel pad qubits (c and d). The electric field is less concentrated when the corners are rounded. It appears these highly concentrated electric fields at the corners are a cause for higher participation ratios. The reduction of the participation ratios is most apparent for the interdigitated qubit which simply has more corners.

Figure ?? shows a the electric field on a cross-section of the parallel pad qubit with different pad separation distances, XXX μm away from the junction.

5

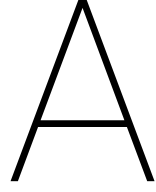
Conclusion

The largest reduction in participation ratios was achieved by elimination of the 'fingers' entirely. Further reduction can be achieved by increasing the separation of the pads. Both adjustments to the qubit design decrease the capacitance of the system. To compensate, the overall size of the capacitor pads can be increased.

In future qubit design, the capacitor pads should have a shape such that the electric field is spread out equally across as large an area as possible. The biggest constraint is the overall size of the resulting qubit system. With this in mind, the results in this research show that the rounding of corners is a promising adjustment to the qubit design.

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CST procedure

This appendix will detail the steps that should be taken to easily set up a qubit simulation in CST. First a project template needs to be created.

Creating a new project

When a new project is started, CST asks which module is going to be used. Most settings can be changed at a later time.

- After clicking '*Create project*' choose '*MW & RF & Optical*'.
- Choose '*Antennas*' and click '*Next >*'.
- Choose '*Waveguide (Horn, Cone, etc.)*'.
- Choose '*Frequency Domain*'.
- Select the units to be used, the default settings are sufficient.
- Choose a frequency domain. This can be left blank and changed at a later time.
- Click '*Next*' to see an overview of the created template.
- Click '*Finish*'.

Qubit designs can now be imported or created in CST.

The estimation of the capacitance of the qubit and the electric fields in the structure will be treated separately as the second process is more complex. Both simulations make use of the Frequency Domain Solver. Settings applicable to both processes are the frequency range and the boundaries.

- Under '*Simulation*' click '*Frequency*' and set the desired values.
- Again under '*Simulation*' click '*Boundaries*' and set the fields as in figure A.1
- Click '*Open Boundary...*' and under '*Automatic minimum distance to structure*' select '*Fraction of wavelength*' and set to 8. Click '*OK*'.

The capacitance

As shown in equation (A.1) the capacitance of the structure must be known to calculate the total energy in the qubit. The value of the capacitance converges very quickly as the mesh is refined. This simulation should always include a Discrete Port connected to the capacitor pads.

$$W = \frac{1}{2} CV^2 \quad (\text{A.1})$$

Where C is the total capacitance of the system and V the voltage over the systems.

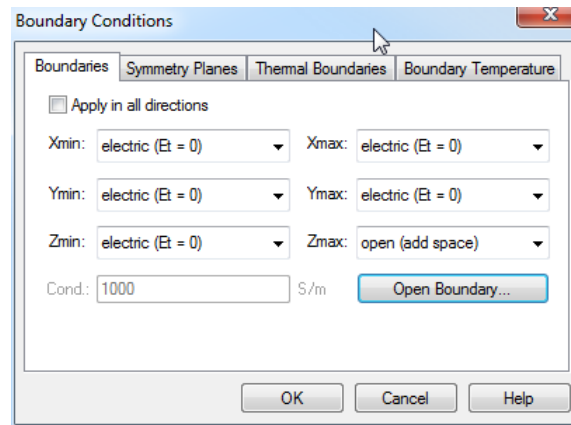


Figure A.1: Settings for the boundary conditions of the simulations. All except 'Zmax' are set to 'electric ($E_t = 0$)'. 'Zmax' is set to 'open(add space)'.

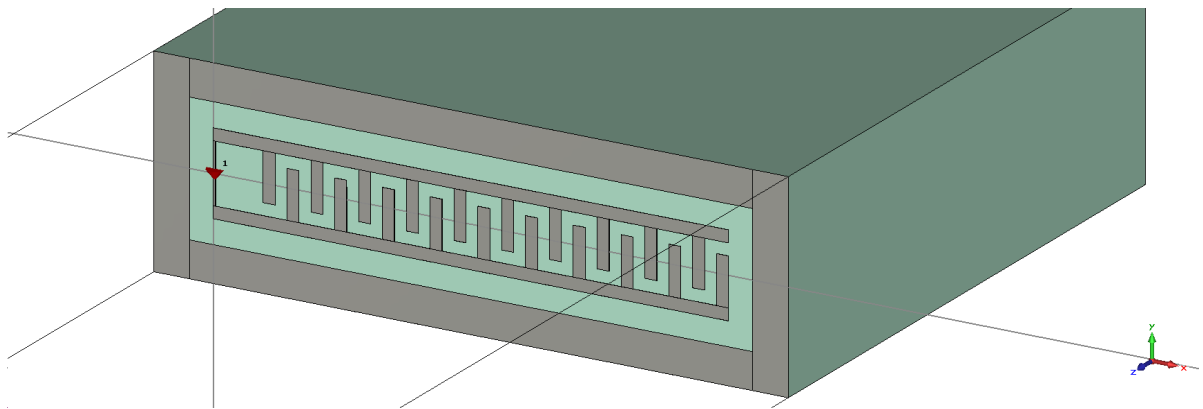


Figure A.2: An example of a qubit design with the substrate in green, the metal parts in grey and the port indicated by the red cone. No lumped element representing the Josephson junction is present in the model.

Modeling

The qubit design can be imported to CST or created in CST itself. Figure A.2 shows a qubit designed in CST. It includes two perfectly electrical conducting (PEC) pads connected by a discrete port. The pads must be modelled using their actual thickness in order to include the lossy layers on their sides. A discrete port can be added as follows:

- Under 'Simulation' click 'Discrete Port'.
- Now select the location in the model or input the coordinates numerically. Ensure that the discrete port connects the two PEC pads.
- Leave all other settings as default.

The pads are surrounded by a PEC ground sheet. For the determination of the capacitance, the inductor representing the Josephson junction should be omitted from the simulation.

Meshing

The default settings for the tetrahedral meshing can be used during calculation of the capacitance. This will yield a very rough initial mesh with few mesh elements and will ensure short simulation times.

Post processing

In the post processing templates window, the capacitance of the simulated structure can be retrieved;

- Under 'Post Processing' select 'Template Based Post Processing'.

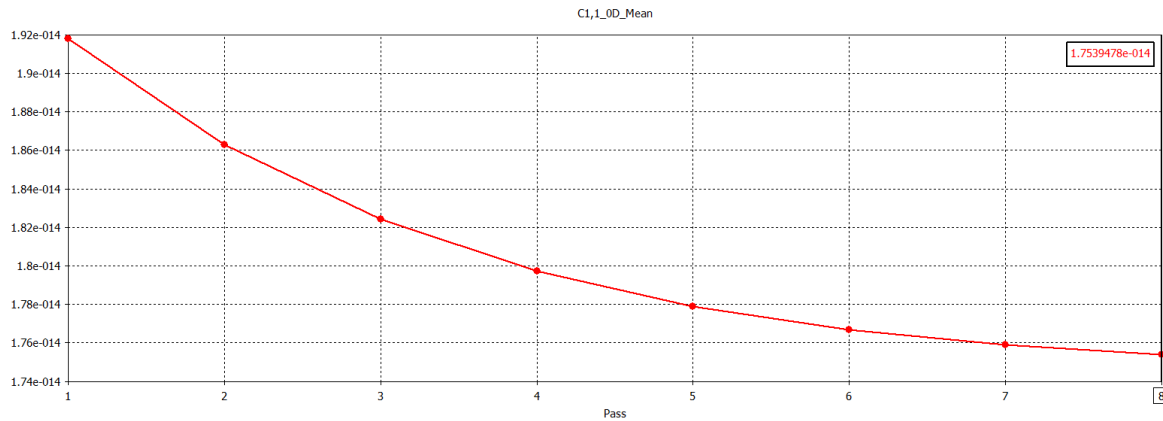


Figure A.3: An example of the data retrieved on the capacitance of a qubit design. On the y-axis is the capacitance in Farad. On the x-axis is the number of mesh refinement passes. Highlighted is the value of the capacitance after 8 passes.

- In the pop-up window, in the first selection box choose '*S-Parameters*'.
- In the second selection box choose '*Z-parameter*'.
- In the pop-up window check the '*C*' option and click '*OK*'.

This will yield a 2D graph showing the capacitance of the structure as a function of frequency. Now include a second template;

- In the first selection box choose '*General 1D*'.
- In the second selection box choose '*0D or 1D Results from 1D Result (Rescale, Derivation, etc)*'.
- In the pop-up window select '*y at given x*' and set '*Evaluate at x =*' to the desired frequency. Click '*OK*'.

After simulation, the result should be a single value of the capacitance at the required frequency.

Simulation setup

To ensure convergence of the capacitance, results from the post processing templates can be used as targets for the simulation;

- Under '*Simulation*' choose '*Setup Solver*'.
- Under '*Adaptive mesh refinement*' make sure the '*Adaptive tetrahedral mesh refinement*' is checked and click '*Properties*'.
- In the pop-up window under '*Number of passes*' set the maximum to at least 8.
- Under '*Check after broadband calculation*:' mark the '*0D result Template...*' as active and select the 0D result of the capacitance from the post processing template above.
- Set the required Threshold and Checks as desired and click '*OK*'.

This will ensure the simulation keeps refining the mesh until your demands on accuracy are met or until maximum amount of mesh refinement passes is reached. After every mesh refinement pass the results are updated and can be checked. In the Navigation Tree click '*Tables*' → '*0D Results*' → '*C1,1_0D_yAtX*'. The first result will be viewable once the first pass of the simulation is completed. When the simulation is finished the capacitance of the structure can be extracted from the plot. An example is given in figure A.3.

The electric field

Now that the capacitance of the structure is known the more extensive simulation of the electric field can be set up.

Modeling

Using equation (A.2) the inductance needed to reach a certain resonance frequency can be calculated.

$$L = \frac{1}{(2\pi)^2 f_0^2 C} \quad (\text{A.2})$$

Where f_0 is the required qubit frequency and C its capacitance.

Now to include such an inductor;

- In the simulation menu add a '*Lumped element*'.
- Set the element '*Type*' to be '*RLC parallel*'
- Set the value of the inductance as calculated and leave the other values at zero.
- Make sure the '*Monitor voltage and current*' is checked.
- Set the location as desired or use picked points.

Next, to ensure a fine initial mesh, the edges on the side of the pads are rounded. In order to make this possible each pad must be a single object. To achieve this the '*Boolean*' operation can be used to combine multiple object into one;

- In the Navigation Tree, under '*Components*' select all objects pertaining to one pad.
- Under '*Modeling*' click '*Boolean*'.

Now that the pad consists of a single object, its side edges can be rounded.

- Under '*Modeling*' click '*Picks*' and choose '*Pick Edge Chain*' (or use Shift+E)
- Select all the edges laying in the xy -plane.

Figure A.4 show what the selection should look like. Once the right edges are selected they can be rounded;

- Under '*Modeling*' click '*Blend*'.
- Set the '*radius*' to be half the height of the pad.

The result should be as in figure A.4.

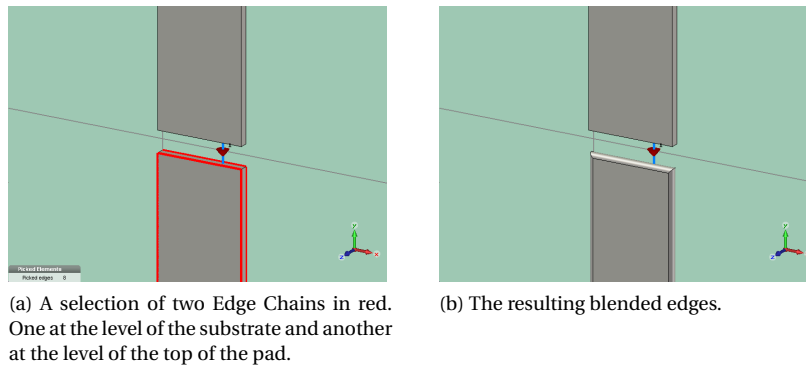


Figure A.4: Before and after blending the edges

Meshing

In order to obtain a fine initial mesh the *Global mesh properties* can be changed;

- Under '*Simulation*' click '*Global mesh properties*'.
- In the pop-up window click '*Specials*'.
- Under the '*Mesh Control*'-tab set '*Smooth mesh with equilibrate ratio*' to around 1.15. Use this value to fine tune the number of mesh elements in the initial mesh.
- Set '*Normal tolerance*' to 1 degree.
- **Uncheck** the '*Anisotropic curvature refinement*'.
- Click '*OK*' and '*Update*' to see the resulting mesh.

Again, use the '*Smooth mesh with equilibrate ratio*' to tune the amount of mesh elements in the initial mesh. See figure A.5 for the settings.

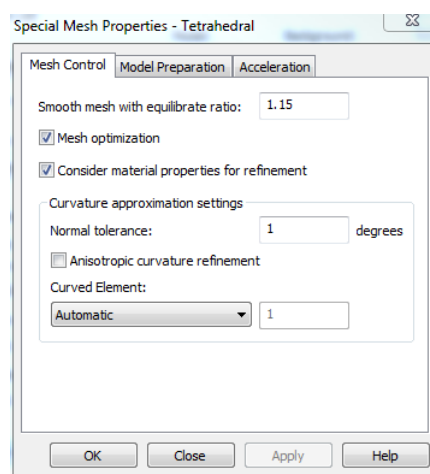


Figure A.5: The required settings for the Mesh Properties. The Anisotropic curvature refinement must be unchecked!

Simulation setup

To be able to view and save field data, include a field monitor;

- Under '*Simulation*' click '*Field Monitor*'.
- In the pop-up window select the E-Field monitor and choose a frequency.
- Click '*OK*', the monitor should be visible in the Navigation Tree.

The simulation is now ready to run.

Exporting data

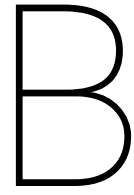
To calculate the participation ratio the simulated electric field is exported as an ASCII file. In order to separate data pertaining to different lossy layers the data for the field on the Pads, Substrate and Ground must be exported separately.

- In the Navigation Tree under '*Components*' hide all objects until only the Pads are visible.
- Again in the Navigation Tree open the '*2D/3D Results*' folder.
- Select the '*Abs*' component of the '*E-Field*'.
- Under '*Post Processing*' click '*Import/Export*' and click '*Plot Data (ASCII)*'.

Repeat these steps for the Substrate and Ground.

The last value needed from CST is the voltage over the Lumped element.

- In the Navigation Tree open '*1D Results*'.
- Open '*Lumped Elements*' and select '*Voltages*'.
- Select the element representing the Josephson Junction and extract the peak voltage at the resonance frequency from the graph.



Matlab procedure

A Matlab script is used to calculate the participation ratio of the lossy layers using the previously exported files from CST. The script will ask for the location of the files containing the data. To calculate the total energy in the system the script will ask for the capacitance and the voltage over the inductor. After the correct values are submitted the script will calculate and save the ratio.