1. Combinational Logic v.s. sequential logic

Memory : none/has

Determined by : current values of inputs/previous and current values of inputs

**Combinational logic**

No cyclic paths

Precedence: NOT > AND > OR (not do first if there is no parentheses)

Definitons:

**Complement**互補的: with a bar over it. (

**Literal**字面的: variable or its complement. (,

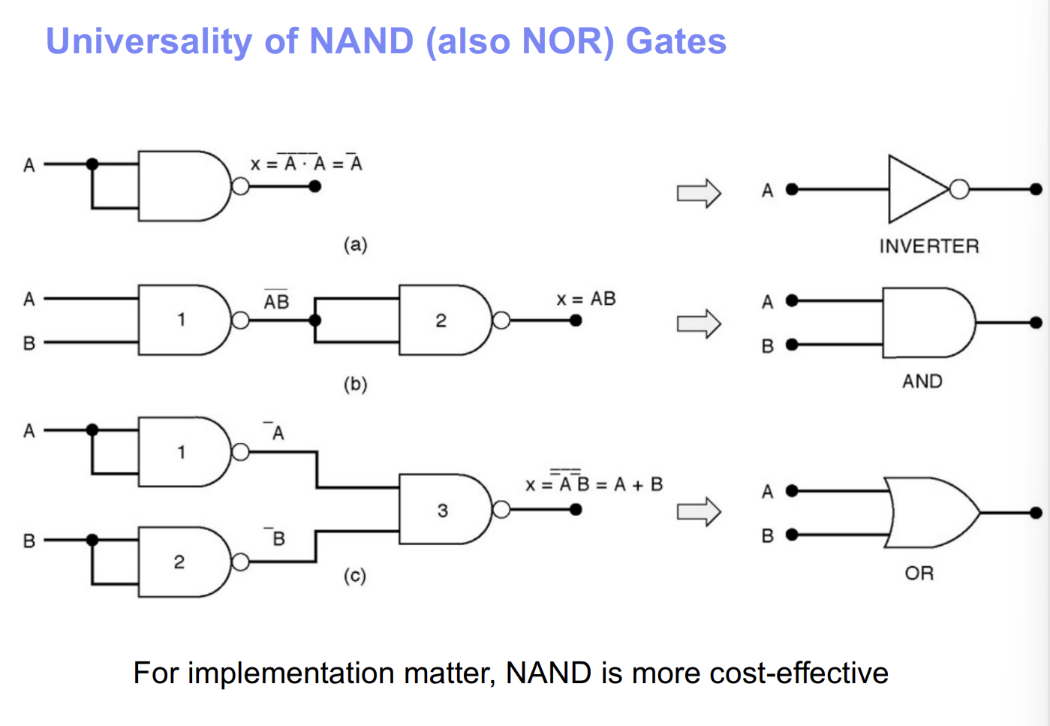
**Implicant**蘊含項: product of literals(not all) (

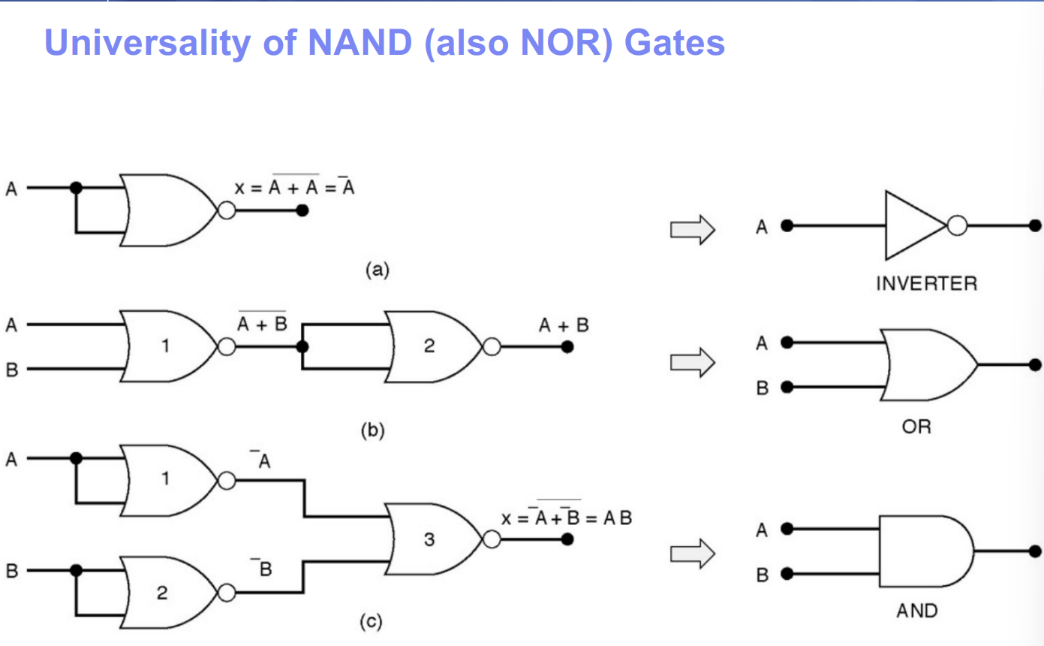
**Prime implicant**: implicant corresponding to the largest circle in a K-map

**Minterm(只有一項)**: product that includes all input Literals. (,

**Maxtem(有多項)**: sum that includes all input Literals. (

NAND and NOR could be used to compose every other gates.





Calculating tricks should be practiced on ppt……QAQ

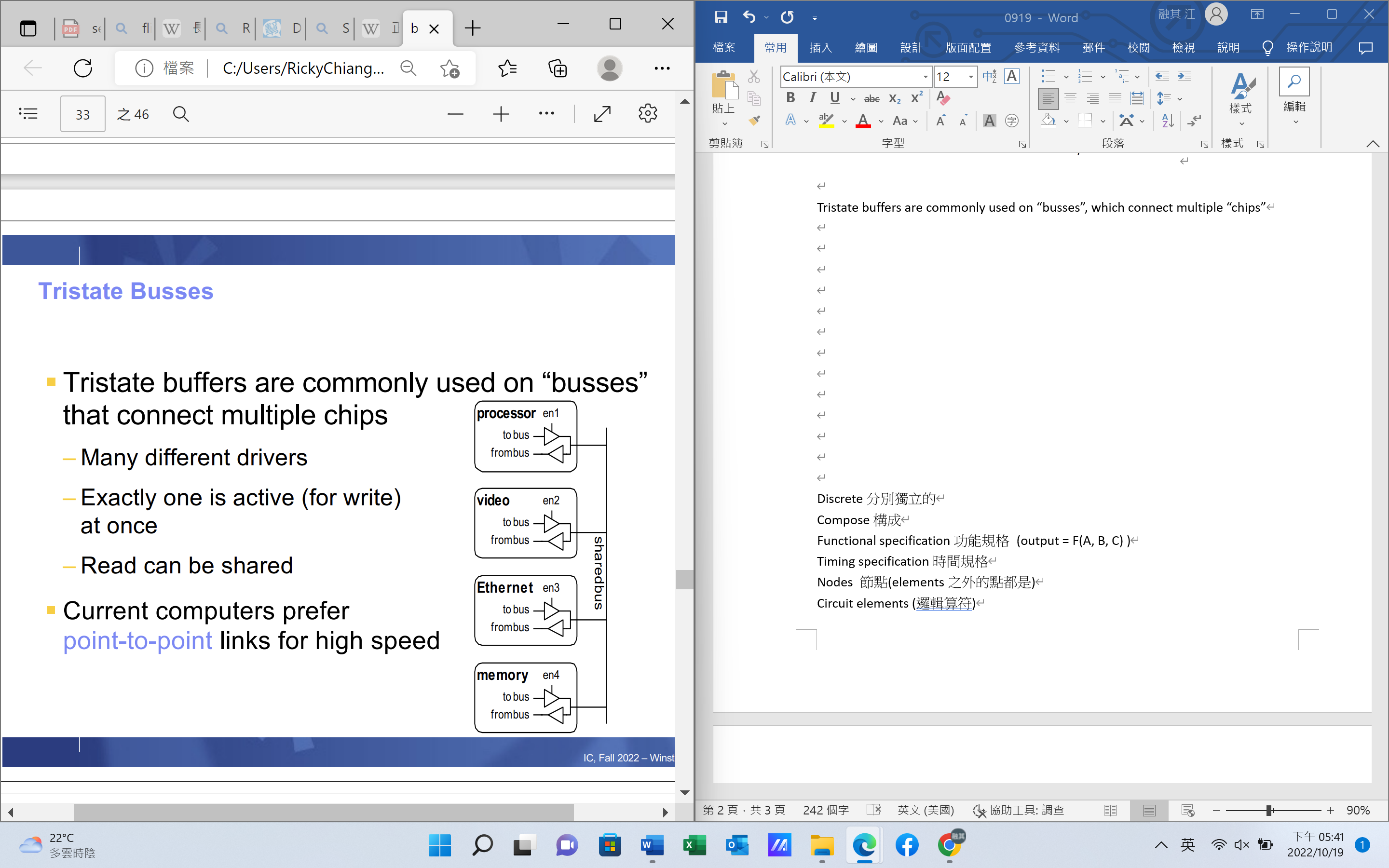
Like bubble pushing, theorem or something……

**From logic to gate**

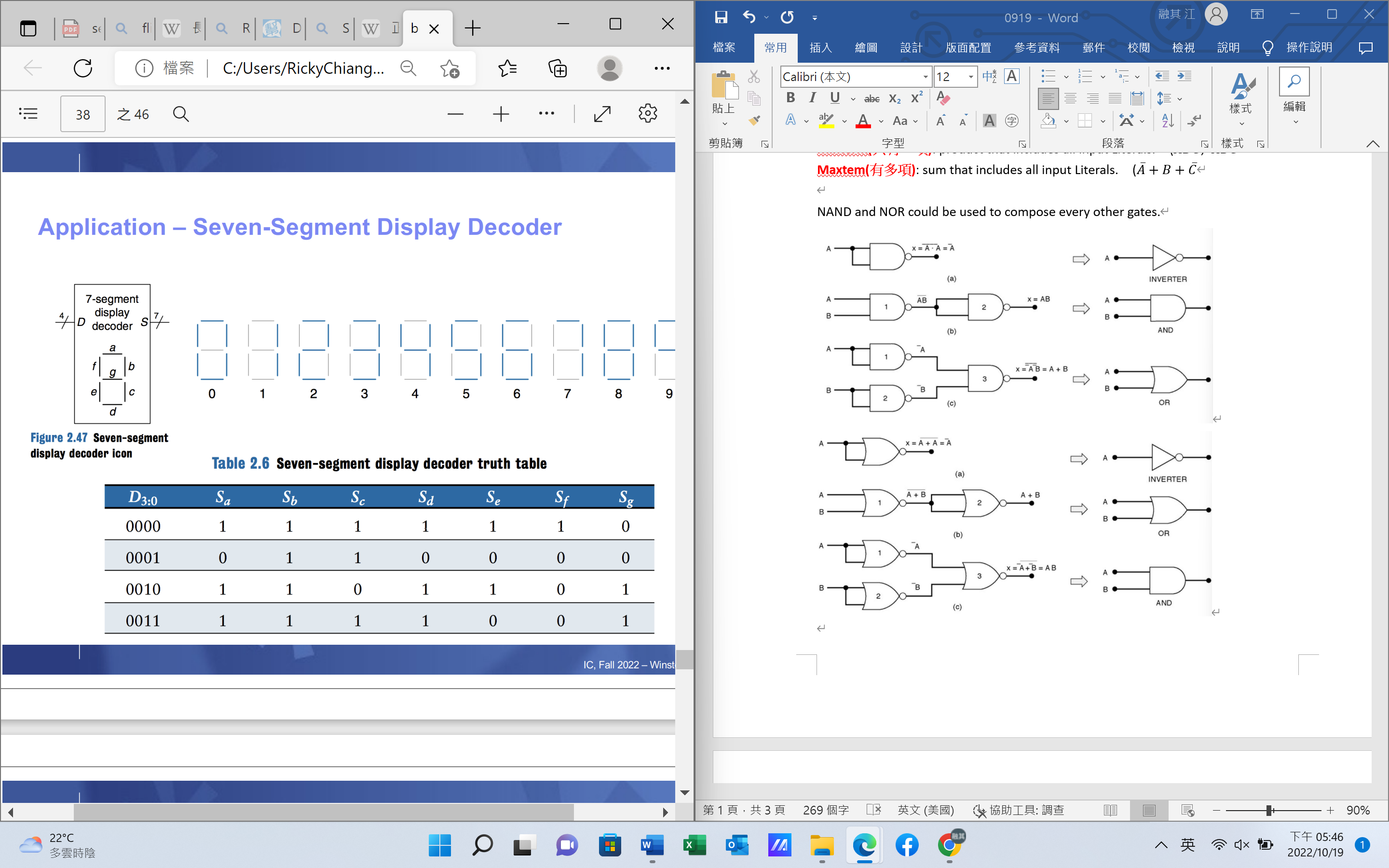


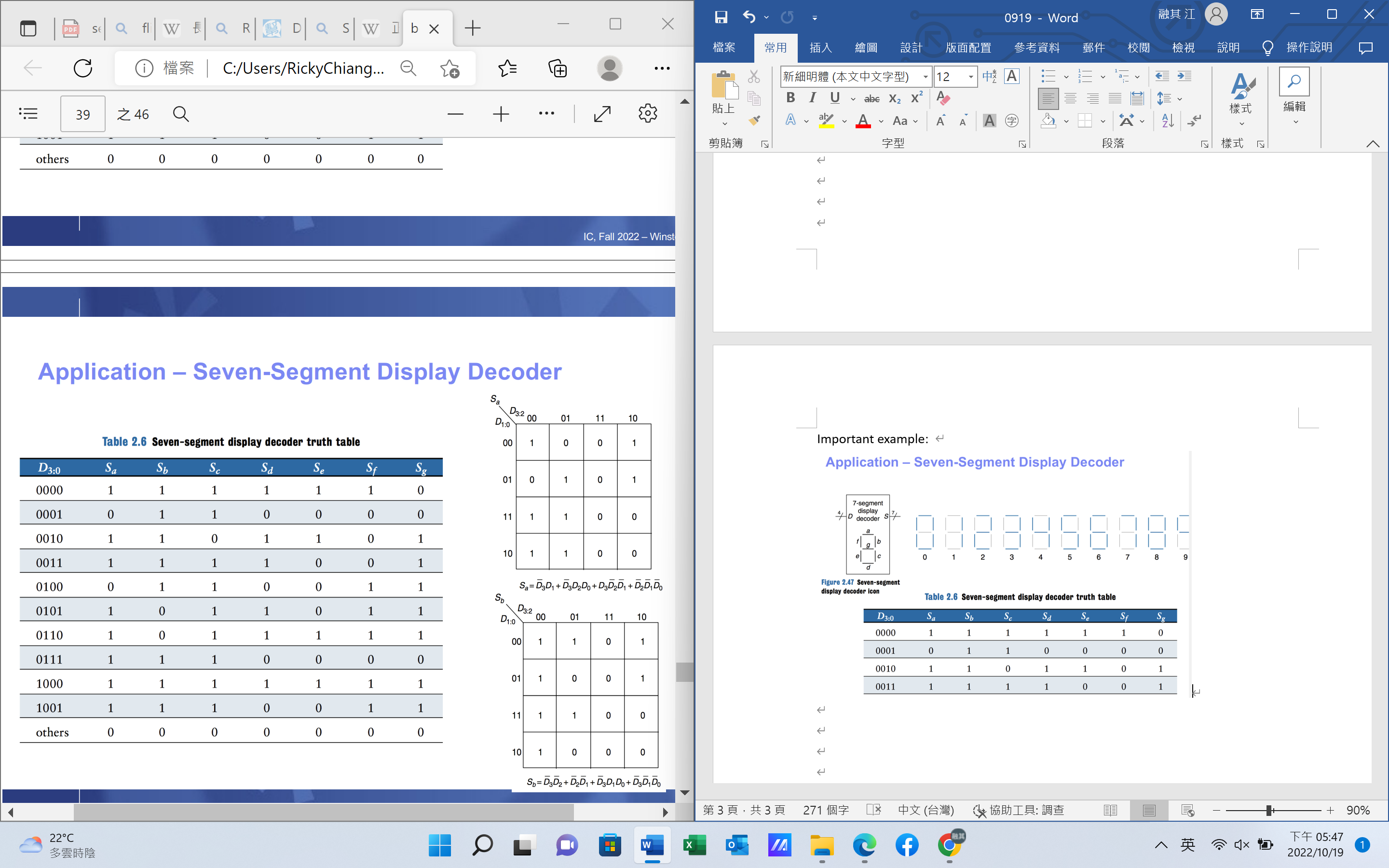
Using tristate buffers(or more) to obtain floating (except of 1, 0, floating is ‘ Z ’)

Tristate buffers are commonly used on “busses”, which connect multiple “chips”

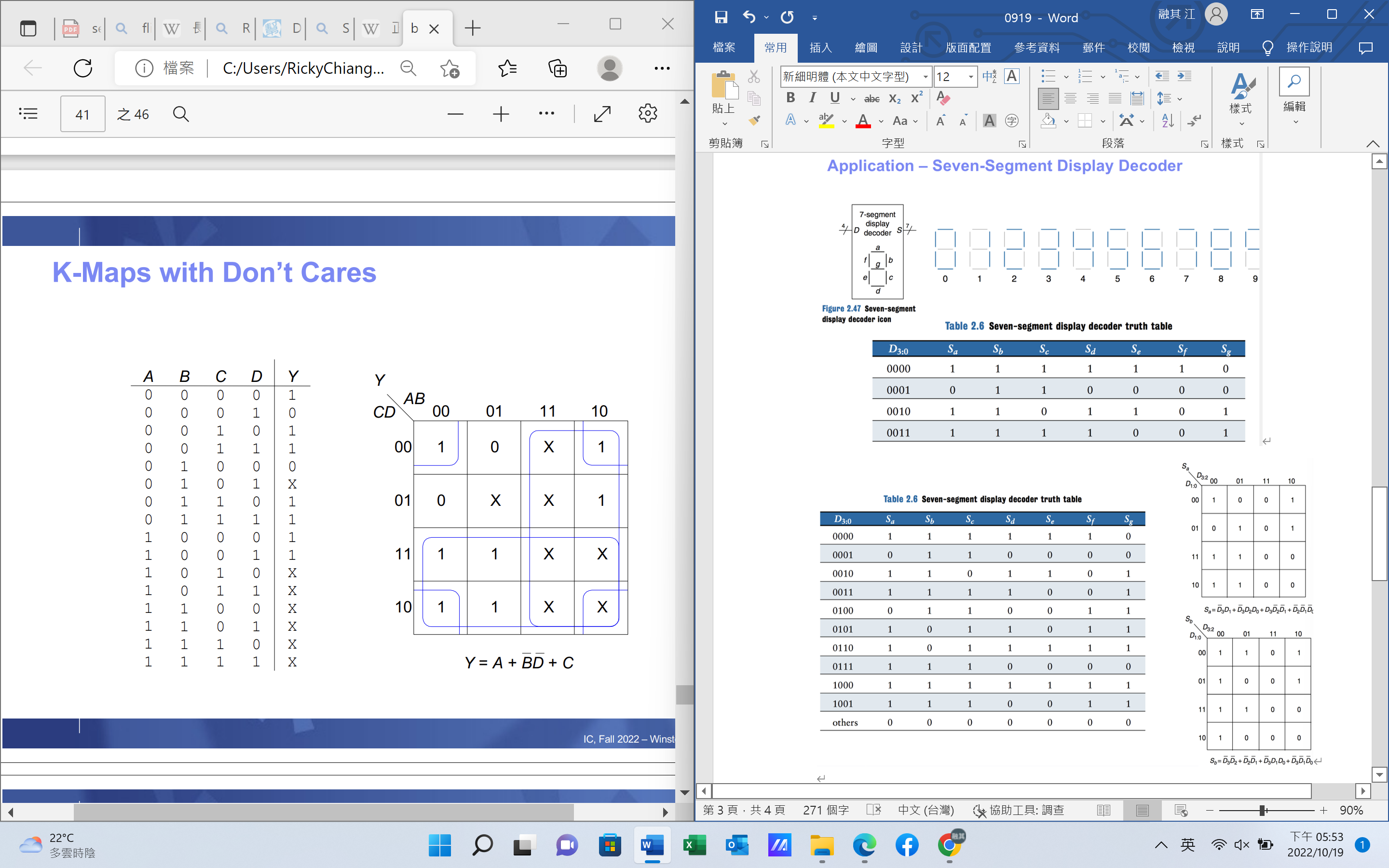


**Important example:**





Another example:

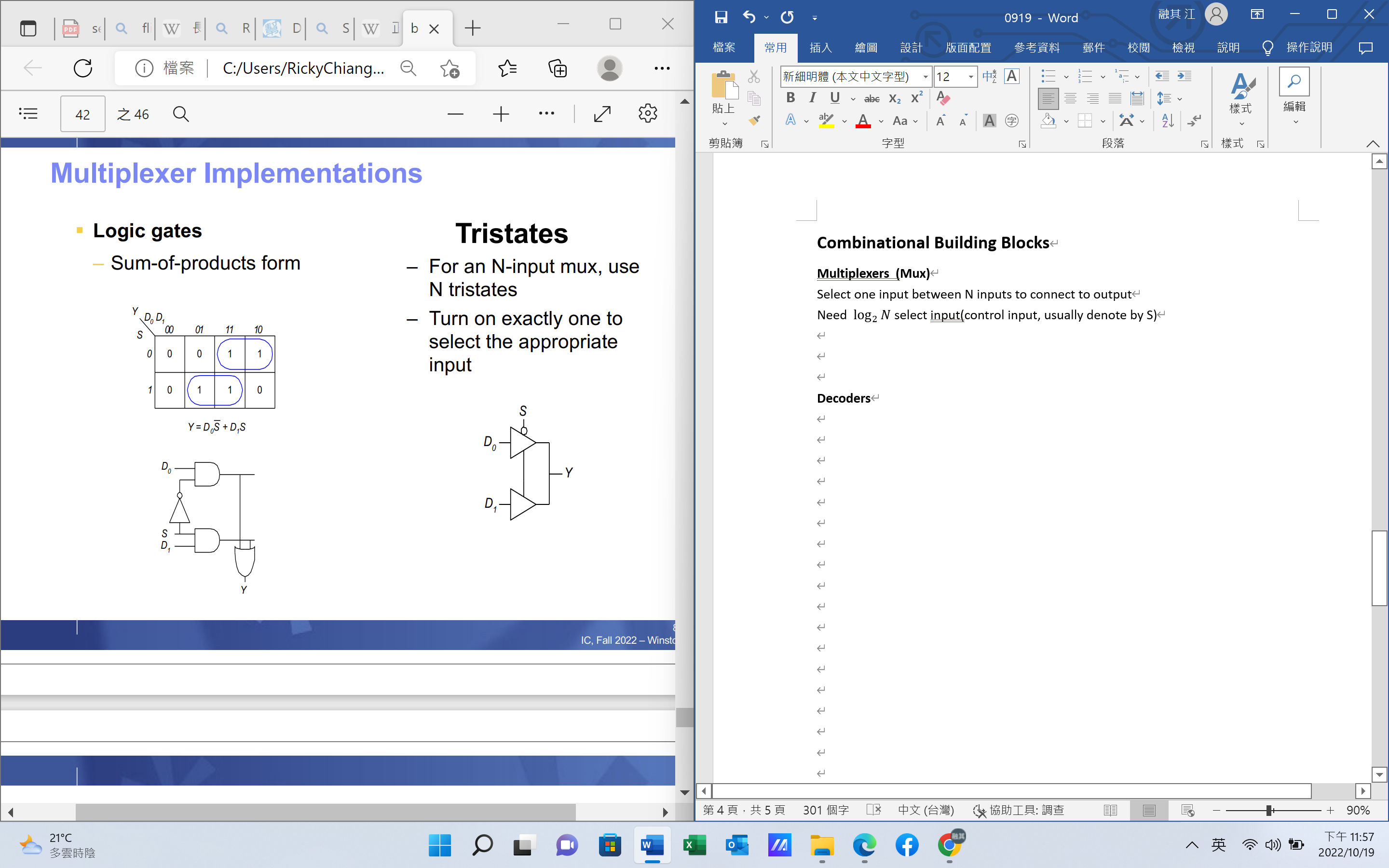


**Combinational Building Blocks**

**Multiplexers (Mux)**

Select one input between N inputs to connect to output

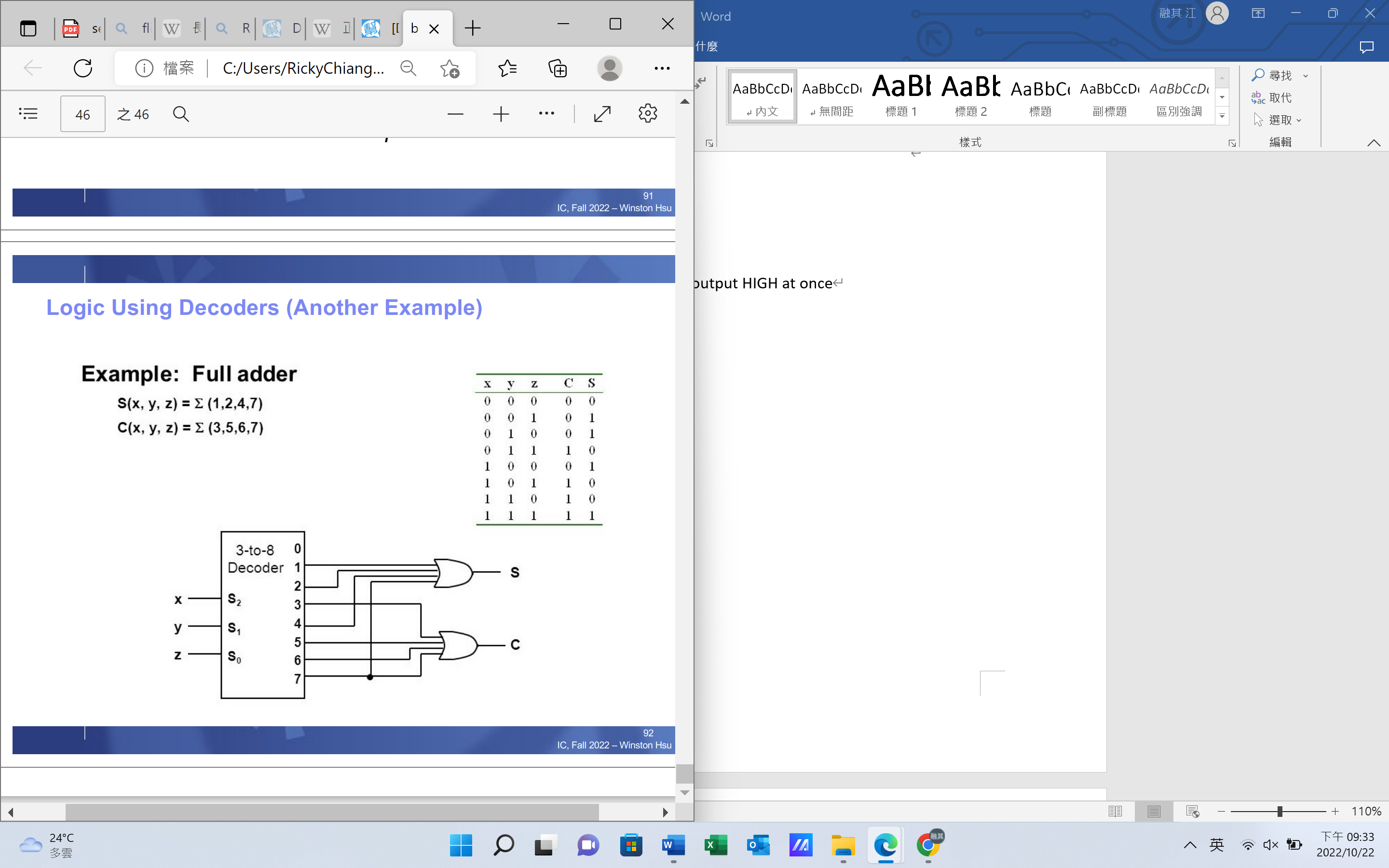
Need select input(control input, usually denote by S)



P.84 and below

**Decoders**

N inputs and outputs, but only One-hot output HIGH at once



x, y, z共為7時7的位置輸出1, 其他都是0

discrete分別獨立的

Compose構成

Functional specification功能規格 (output = F(A, B, C) )

Timing specification時間規格

Nodes 節點(elements之外的點都是)

Circuit elements (邏輯算符)

Cyclic path循環路徑

In terms of就…來說

Diagram示意圖

Parentheses 括弧

Schematic rule 圖解 法

T junction T字形

Assert斷言

Correspond相對應

Contention衝突點

Tristate buffer三態緩衝器(三個接口)

Chip 片 晶片

Select 選取