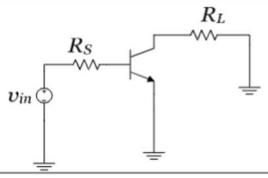
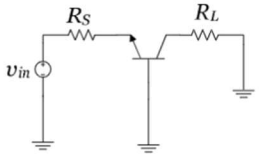
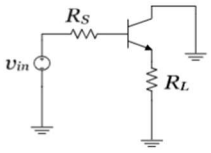
11. BJT Single Stage Transistors

	Common Emitter	Common Base	Common Collector
Circuit			
$A_v = \frac{v_o}{v_{in}}$	$-g_m(R_L \parallel r_o)\frac{r_\pi}{R_S + r_\pi}$	$\frac{+g_m(R_L \parallel r_o)}{1+g_m R_S}$	$\frac{g_m R_L}{1+g_m R_L}\cdot\frac{R_{in}}{R_{in}+R_S} \approx 1$
R_{in} (to the right of R_S)	r_π	$1/g_m$	$r_\pi(1+g_m R_L)$
R_{out} (to the left of R_L)	r_o	$r_o(1+g_m R_S)$	$\frac{\alpha}{g_m}+\frac{R_S}{\beta+1}$
Allowed input signal range	$0.2V_T$	$0.2V_T(1+g_m R_S)$	$0.2V_T(1+g_m R_L)$

c. (5) What calculations did you use to determine the required component values?

The Gain Formula:

$$A_v = \frac{g_m R_L}{1 + g_m R_L} \cdot \frac{R_{\text{in}}}{R_t + R_{\text{in}}}$$

Since we are using the common collector topology, we can assume that:

$$\frac{R_{\text{in}}}{R_t + R_{\text{in}}} \approx 1 \text{ ,for } R_{\text{in}} \gg R_t)$$

Knowing this we can solve for the minimum requirement for gm:

$$\frac{g_m R_L}{1 + g_m R_L} \cdot 1 \geq 0.9$$

$$g_m \geq 90\,\text{mS}$$

Now we can calculate the component values alongside the constraints given for this project:

Given that the formula and values:

$$|v_{\text{in}}| = 0.2\,V_T\,(1 + g_m R_L) \geq 0.5$$

$$v_{\text{in}} = 0.5, \quad V_T = 25\,\text{mV}, \quad R_L = 100\,\Omega,$$

We can calculate the gm of the created circuit

$$0.2 \times 0.025 \times (1 + g_m \times 0.1\,\text{k}\Omega) \geq 0.5$$

$$g_m \geq 990\,\text{mS}$$

0.99 satisfies the minimum requirement of 90mS which proves this circuit is valid in terms of the transconductance

$$R_{\text{in}} = R_t \parallel [r_\pi(1 + g_m R_L)],$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{990mS} = 101\,\Omega,$$

We can solve for Rin given the values for the resistors from the project instruction and the calculated value of gm

$$g_m R_L = (990\,mS)(100\,\Omega) = 99{,}000, \quad R_t = 100\,\Omega.$$

$$A_v = \frac{g_m R_L}{1 + g_m R_L} \times \frac{R_{\text{in}}}{R_t + R_{\text{in}}} \geq 0.9, \quad R_{\text{in}} \geq 900\,\Omega \approx 0.9\,\text{k}\Omega.$$

With Rin we can now solve for the minimum resistance needed for the circuit to function without any voltage disruptions or issues

$$R_{\text{in}} = R_{eq} \parallel \left[101\,\Omega\left(1 + (0.99)(100\,\Omega)\right)\right],$$

$$R_{eq} \geq 988\,\Omega$$

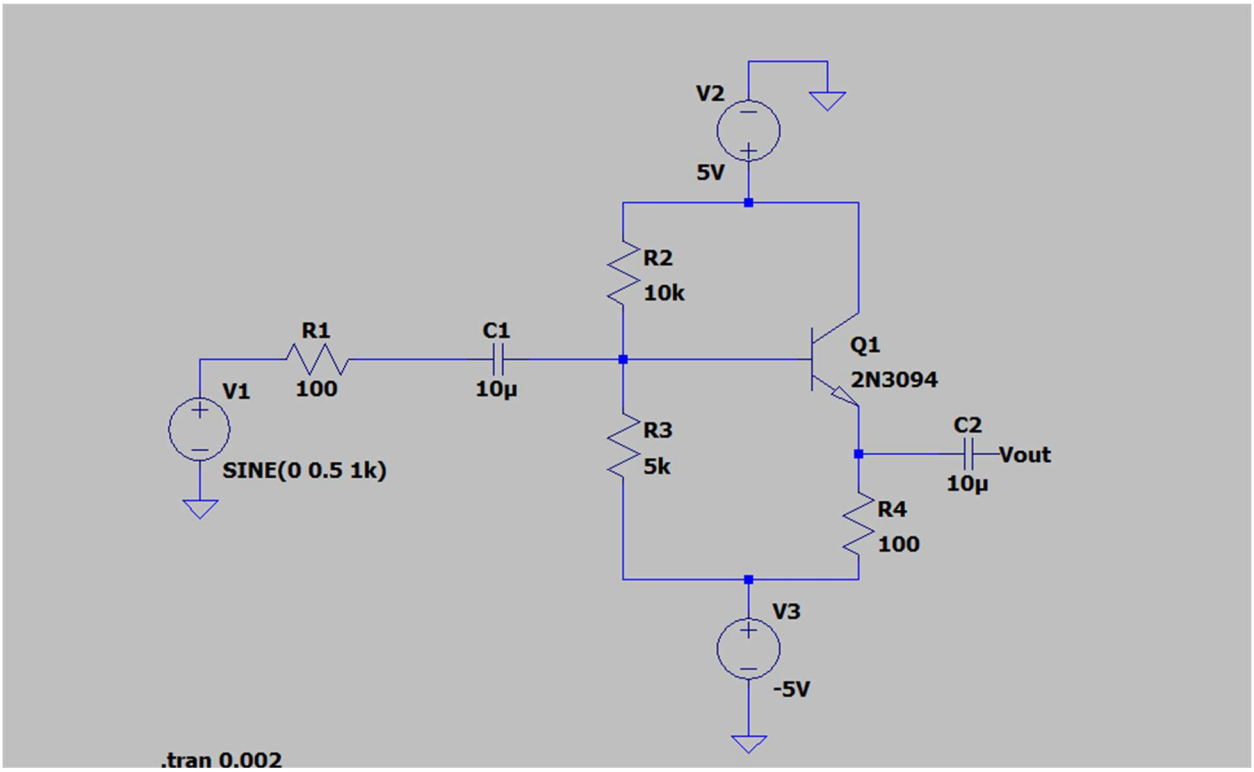
For our gain requirements, we need two resistors in parallel to yield an equivalent resistance greater than 988 Ω. Using 10 kΩ and 5k resistors easily meets this condition and also helps keep the gain as close to unity as possible.

$$R_{\text{eq}} = 10\,\text{k}\Omega \,|\, 5\,\text{k}\Omega \approx 3.33\,\text{k}\Omega = 3330$$

$$R_{\text{in}} = 3330\,\Omega \,|\, [101\,\Omega(1 + 0.99 \times 100\,\Omega)] \approx 2.5\,\text{k}\Omega$$

$$A_v = \frac{(990)(100)}{1 + (990)(100)} \times \frac{3300}{100 + 3300} = \frac{99000}{99001} \times \frac{3300}{3400} \approx 0.97$$

a. (5) How did you model the transistor in the simulator you used?



c. (5) The overall gain determined from the simulations.

d. (5) Other performance parameters determined from the simulations.

$$V_{\text{in}} = 0.471\,V \quad V_{\text{out}} = -0.471\,V$$

$$V_{\text{in}} = 0.5\,V \quad V_{\text{out}} = -0.5\,V$$

$$A_v = \frac{0.471}{0.5} = 0.942$$

$$\text{Attenuation} = (1 - 0.942) \times 100\% = 5.8\%$$

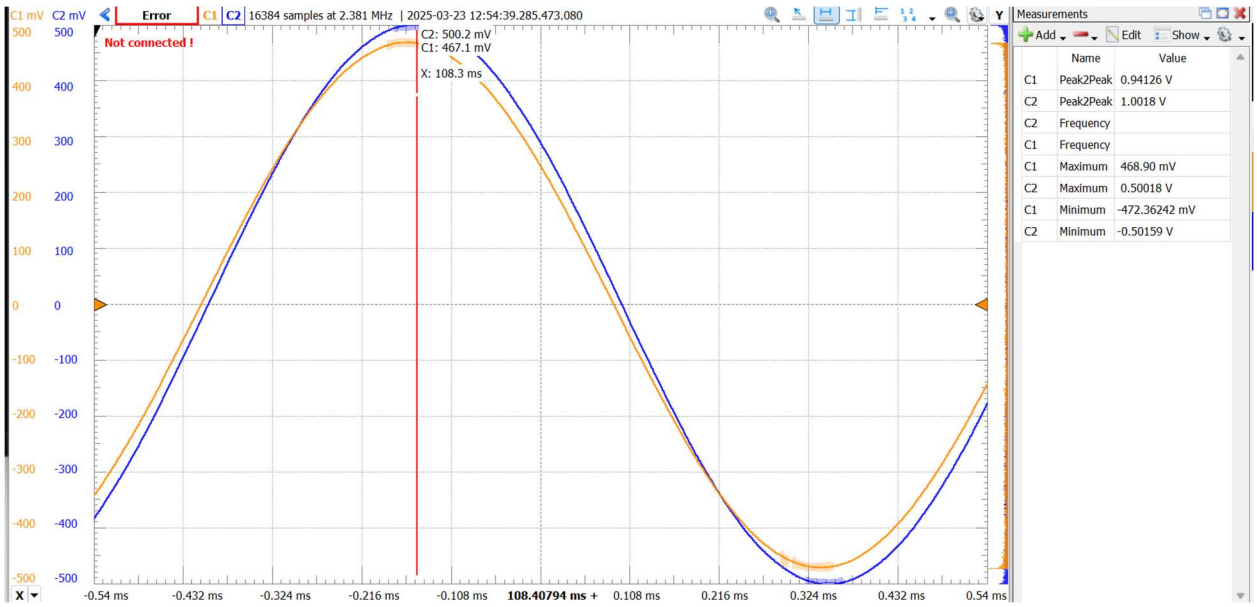
Here, from the measured input and output voltages, we calculated a gain of 0.924, corresponding to an attenuation of 5.8%. This result confirms that the amplifier meets the project requirement of keeping attenuation below 10%. In other words, the circuit maintains the output

signal sufficiently close to the input, indicating proper biasing and suitable component values. Consequently, this amplifier design successfully fulfills the specified constraints and operates as intended.

$$R_{\text{in}} = \frac{0.5\,\text{V}}{164.08\,\mu\text{A}} \approx 3047.3\Omega$$

4. (2 minutes) Show your physical circuit on camera. Point to the wires from input to output to show how the circuit is connected in a way corresponding to your schematic.

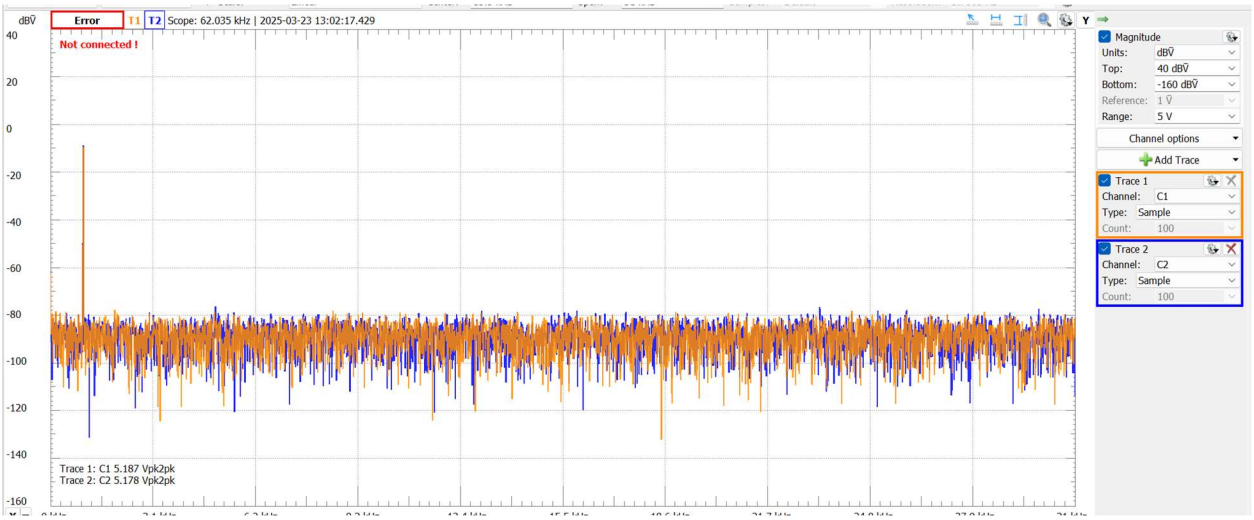
5. (5 minutes) Share your screen to show your waveforms measurements. Explain:

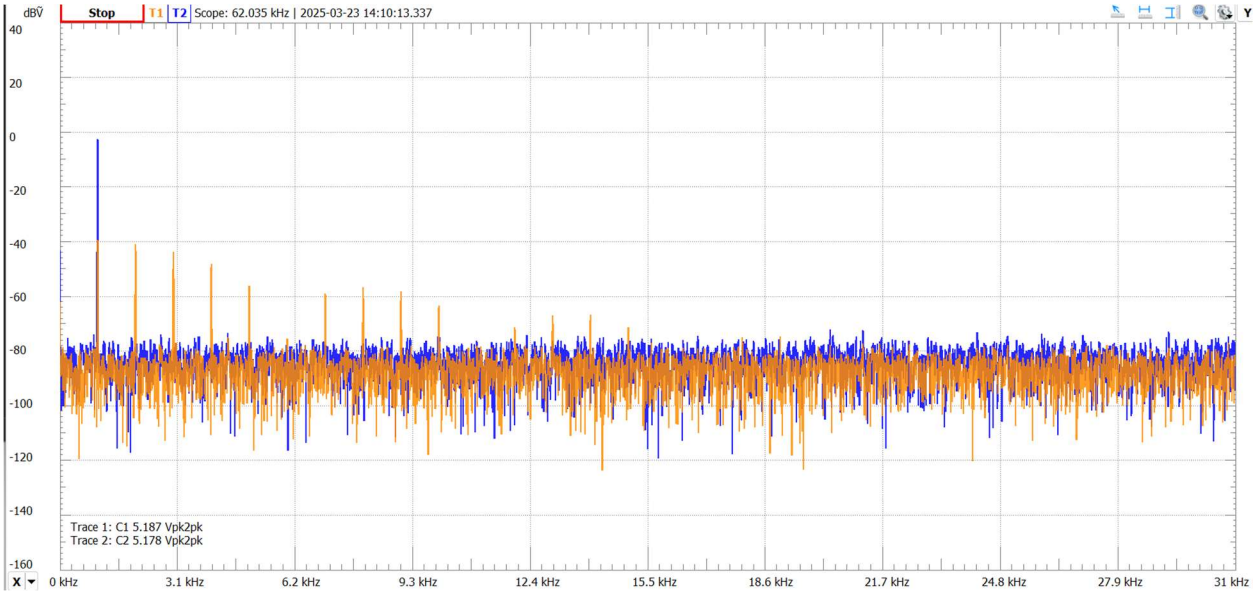


$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{467\,\text{mV}}{500\,\text{mV}} = 0.934$$

$$\text{Attenuation} = (1 - 0.934) \times 100\% = 6.6\%$$

c. (5) Demonstrate linearity at an input amplitude of 0.5V.





To verify the linearity of the amplifier circuit, we used the spectrum analyzer on the AD3 to compare the input and output signals. In the first graph, where the voltage range was set from 0.5V to -0.5V, the waveforms were nearly identical, which indicates a linear response. Furthermore, at the 1 kHz mark, there is a significant peak approaching -6 dB, corresponding to our 0.5V input. This consistency between the input and output spectra confirms the linear behavior of the circuit.

On the second graph, where the sinusoidal input range was increased to 1V to -1V, the amplifier's linearity noticeably deteriorates. The appearance of spikes at frequencies other than 1 kHz suggests that the amplifier is being driven beyond its optimal operating range. This breakdown

in linearity is likely due to design limitations and the non-linear behavior of certain circuit components when exposed to higher voltages. As a result, the increased input voltage causes distortion and the generation of unwanted harmonics, confirming that the amplifier is best suited for input voltages of 0.5V or less.