

# **PROJECT 4**

## **ELECENG 2EI4: Electronic Devices and Circuits I**

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Ricky Huang, huangr86, 400508848]**

## Circuit Schematic:

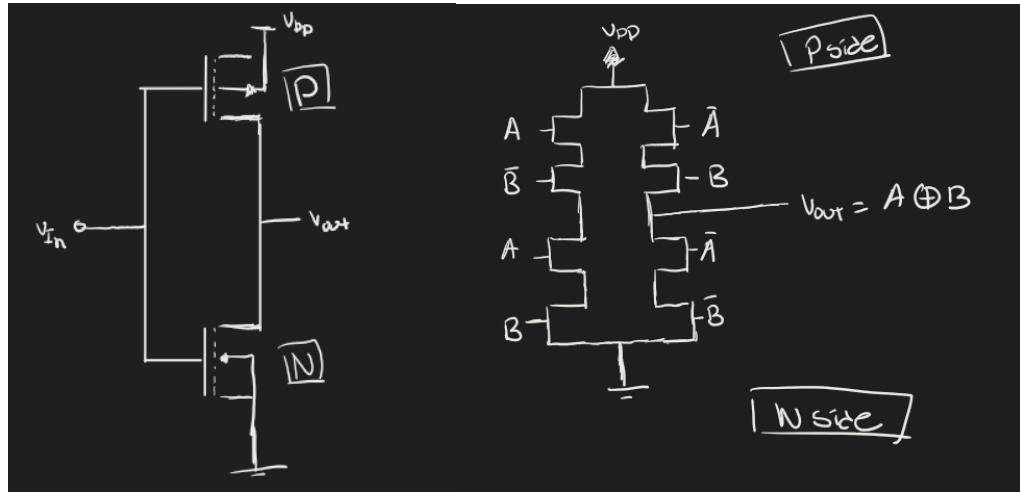


Figure 1: Circuit Schematics

## Ideal Sizing

The ideal sizing for the P-MOS and N-MOS mosfets of our XOR circuit allows for smooth electron flow and minimizes the time delay of the circuit. This ideal sizing requires symmetry between the pull-down network ( PDU ) and our pull up network ( PNU ), this is ensured that both networks have the same time delay.

As shown in Figure () we can see how we can calculate the difference in sizing between both transistors, as we know electron conduction in our N-MOS mosfets are faster than the hole conduction in our P-MOS mosfets, more specially by a factor of 2.5. This factor comes from the difference in conduction speeds between electrons and holes as shown in the calculations. With this we now know the ideal sizing ratio that the P-MOS and N-MOS must have for the circuit to exhibit minimal time delay is 2.5:1.

Additionally, in our CMOS design of an XOR gate, the conduction paths consist of multiple transistors in series. As a result, effective resistance is increased compared to having just a single transistor, which is used in the inverter circuit for our inputs. Since the propagation delay depends on both our effective resistance and load capacitance as seen in the calculations, we must compensate by widening the transistors that are in series paths. This act ensures that the combined resistance of the series transistors math the resistance from our input inverters, which leads to symmetric performance and timing across both circuits. If these variables aren't matched the delays between both circuits would be different and could lead to timing mismatching

$$k = \mu C_{\text{ox}} \frac{W}{L}$$

$$k_P = \mu_p C_{\text{ox}} \frac{W_p}{L_p} \quad k_N = \mu_n C_{\text{ox}} \frac{W_n}{L_n}$$

$$\mu_n C_{\text{ox}} \frac{W_n}{L} = \mu_p C_{\text{ox}} \frac{W_p}{L}$$

$$\mu_n W_n = \mu_p W_p$$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$$

Figure 2: Transistor Sizing Ratio

$$R_{\text{ref}} \propto \frac{L}{W_{\text{ref}}} \quad R_{\text{series}} = R_1 + R_2 = 2 R_{\text{new}}$$

$$2 R_{\text{new}} = R_{\text{ref}}$$

$$R_{\text{new}} \propto \frac{L}{W_{\text{new}}}$$

$$\frac{L}{W_{\text{new}}} = \frac{1}{2} \cdot \frac{L}{W_{\text{ref}}}$$

$$\frac{1}{W_{\text{new}}} = \frac{1}{2} \cdot \frac{1}{W_{\text{ref}}}$$

$$W_{\text{new}} = 2 W_{\text{ref}}$$

Figure 3: Transistor Series Sizing Ratio

Regrettably despite all the above calculations and explanations we cannot implement this ideal sizing to our specific hardware design, as this is because physical measurements such as width and length of a transistor are fixed when they are manufactured into the IC, meaning they cannot be altered after creation. Due to this we don't expect our circuit to achieve ideal time delay due to this limitation as cause to the IC manufacturer. However, if provided a P-MOS transistor which is perfectly fit for the sizing ratio of our circuit specially then the ideal timing delay is possible.

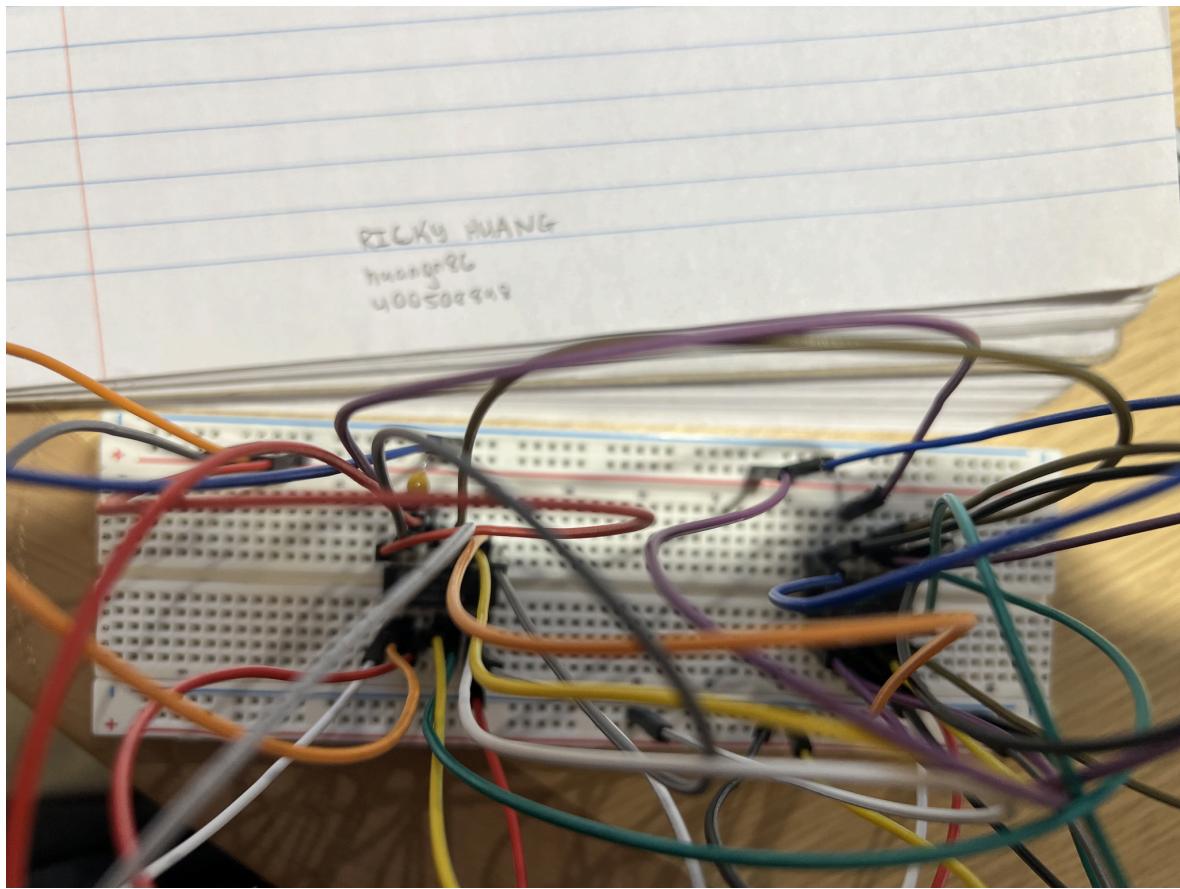


Figure 4: Circuit

## Functional Testing

Functionality testing was carried out on the CMOS XOR gate by using the digital I/O pins on the AD3 to showcase the circuit implementation of the XOR function. This step was essential as it confirmed that the inputs and outputs align with the expected logic operations of an XOR gate. For testing, the input voltages were set as square waves, with one having a period twice as long as the other, thereby allowing us to observe every possible scenario of the XOR logic. As seen in Figure (), the designed CMOS XOR gate performs as expected: when both inputs are logic low or high, the output is logic low, but when the inputs differ, the output becomes logic high.

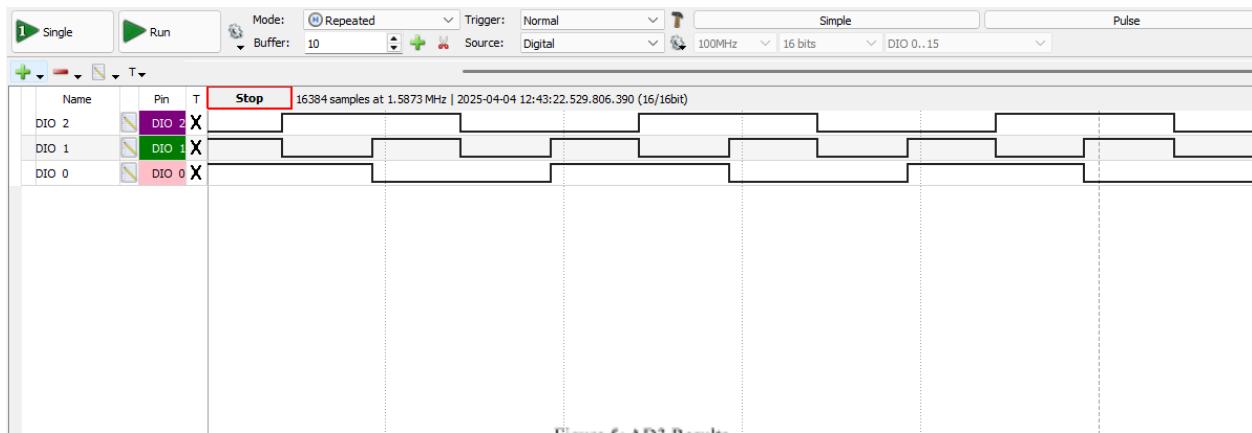


Figure 5: AD3 Results

## Static Level Testing

To perform static level testing we set one of the inputs to logic high, 5V in this case and the second input to a square wave that oscillates from 0V to 5V. This static was done for both inputs to see the variation that may occur when different inputs were used. As seen in Figure (), the  $V_H$  for when input A was set to logic high was measured to be at 5.05V and the  $V_L$  was measured to be 0V. When the inputs were reverse and B was set to be logic high, as seen in Figure() it can be observed that  $V_H$  was 5.238V and  $V_L$  was once again 0V. This variation in the  $V_H$  measurements can be attributed to component tolerances, slight supply voltage fluctuations, or increased internal resistance from one of the inputs. Despite these minor differences, the outputs for both inputs remain consistent, ensuring that our circuit is functioning as intended.

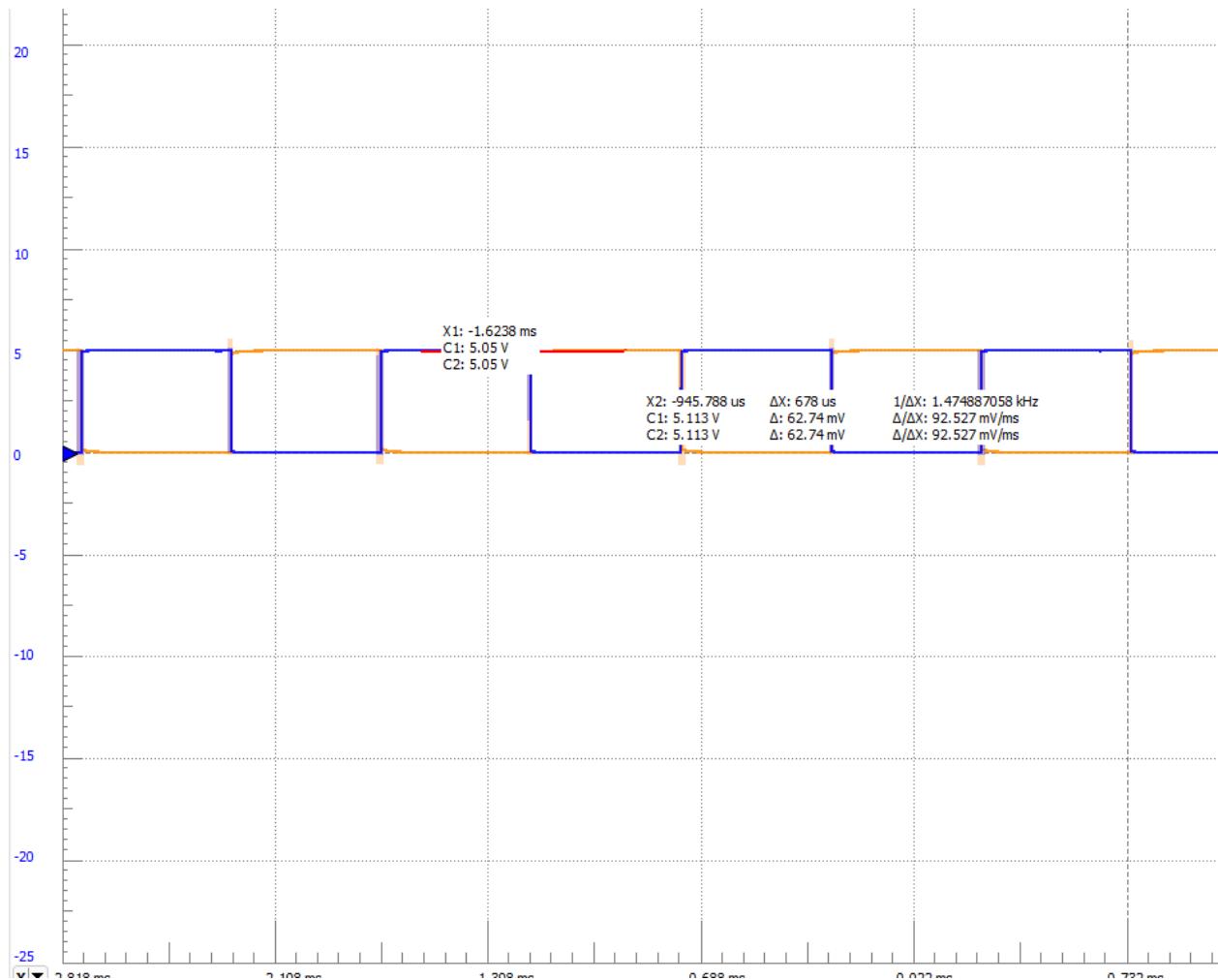


Figure 6: Static Testing Results

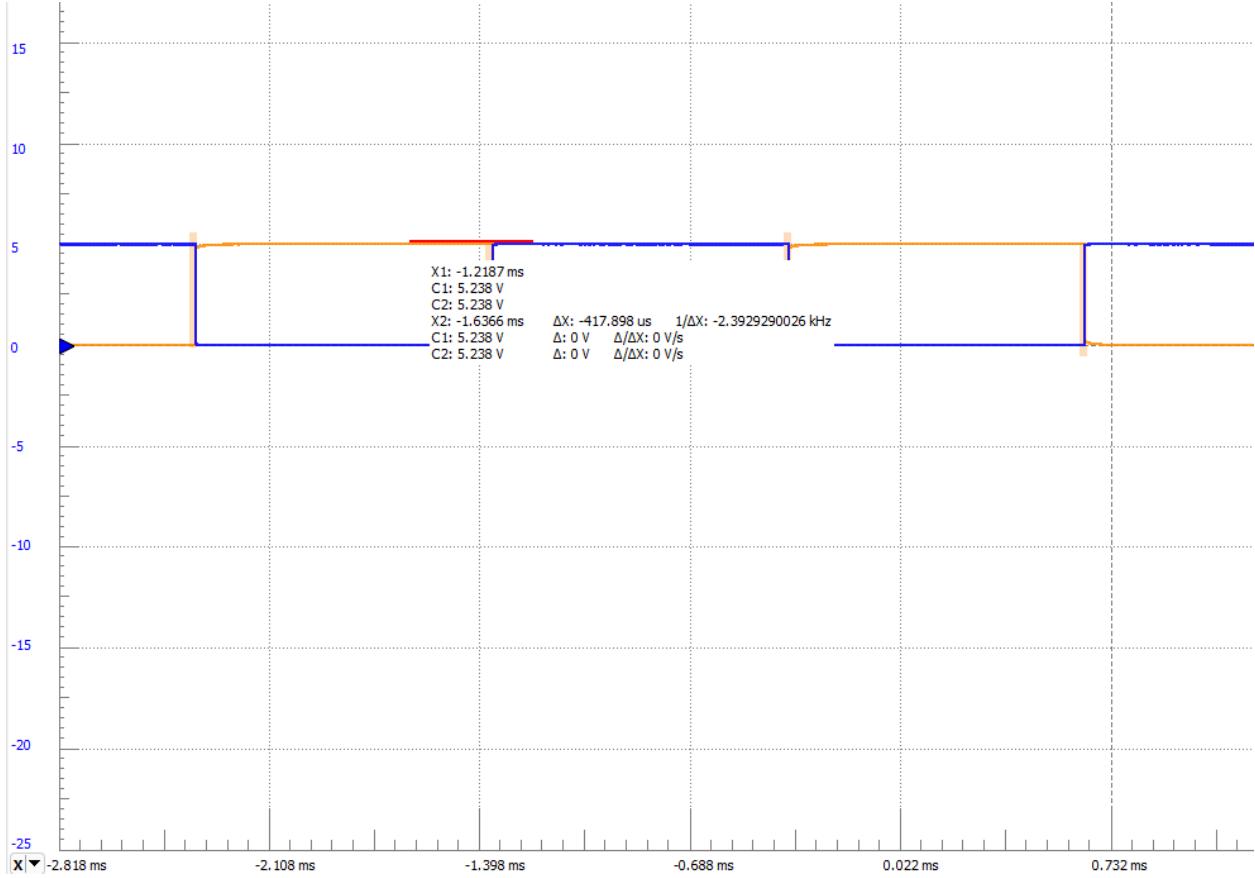


Figure 7: Static Testing Results Cont.

## Timing

The next test that was preformed was a test analysis of the XOR gate circuit. This allows insight into the transition delay of the circuit from when it transitions from high to low and vice versa. This was done by attached a 100nF capacitor to the output location and measuring the voltage there. Input A was set as high whilst input B was set to be a square wave oscillating from 0V to 5V. The results can be seen in the following figures as we can observe that our rise time was  $t_{rise} \approx 378 \mu s$  and the fall time was  $t_{fall} \approx 337 \mu s$ .

Furthermore, the high-low propagation delay was observed by measuring from 50% of the time taken from to input to go from high to low, it can be observed in Figure () that this value is  $\tau_{pHL} \approx 172 \mu s$ . The low-to-high propagation delay is measured similarly, except here we record the time at which the input signal reaches 50% of its transition from low to high, as illustrated in Figure (),  $\tau_{pLH} \approx 181 \mu s$ . Finally we can measure the overall propagation delay with the following calculation:

$$\tau_p = \frac{\tau_{pHL} + \tau_{pLH}}{2} = \frac{172 + 181}{2} = 176.5 \mu s$$

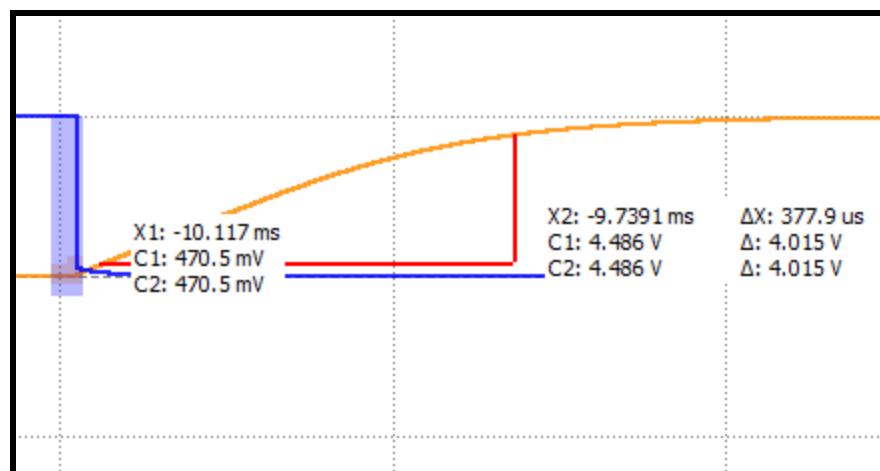


Figure 8: Timing Low-High

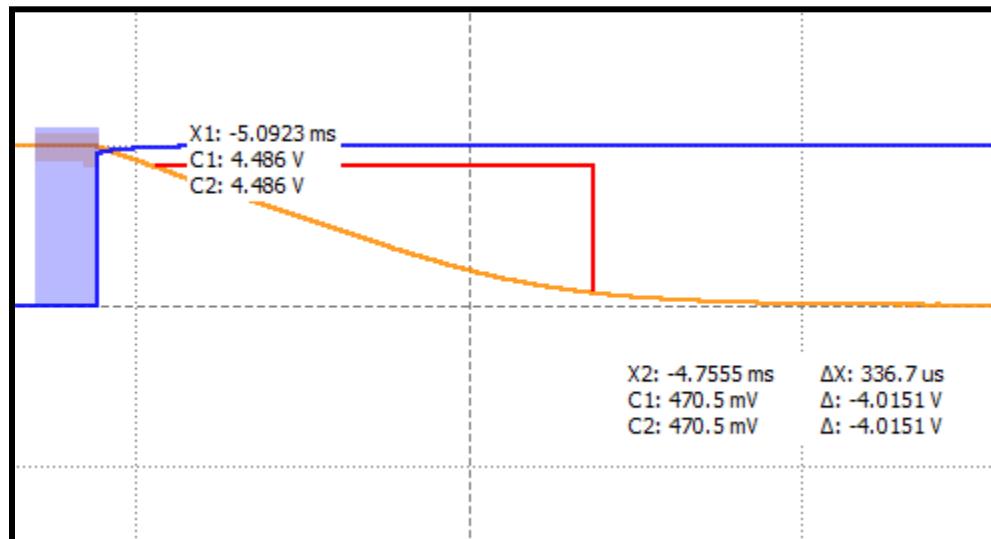


Figure 9: Timing High-Low

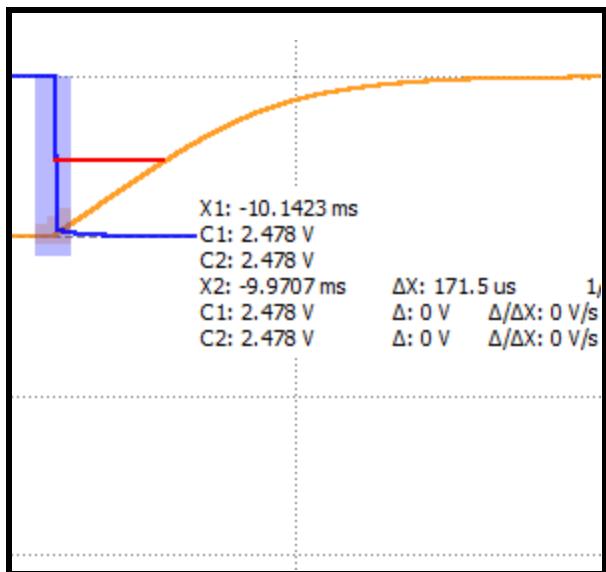


Figure 10: Timing Low-High Propagation

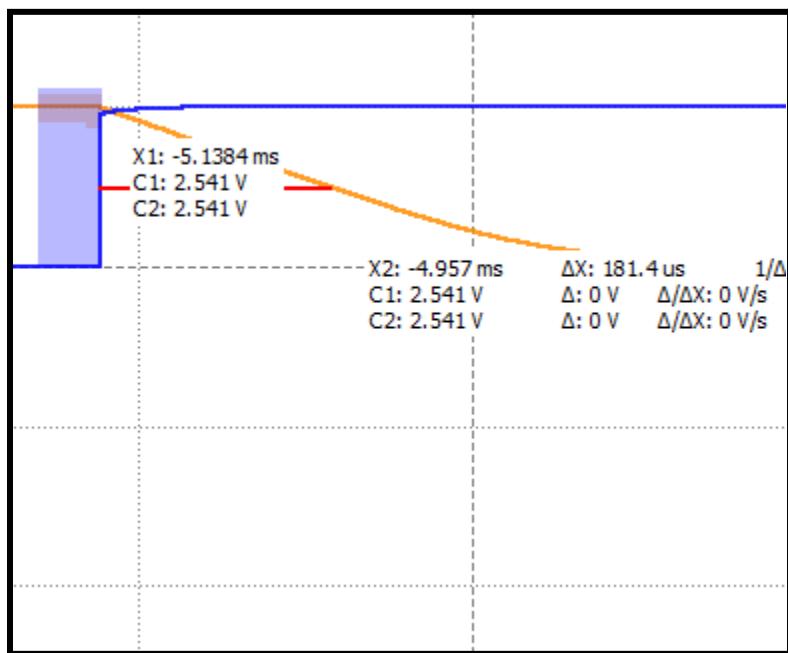


Figure 11: Timing High-Low Propagation

## References & Datasheets

- [1] McMaster University, “Home,” [Online]. Available:  
<https://avenue.cllmcmaster.ca/d2l/le/content/638927/Home>. [Accessed: Apr. 5, 2025].
- [2] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, *Microelectronic Circuits*, 8th ed. New York, NY, USA: Oxford Univ. Press, 2020.
- [3] “CD4007 datasheet,” Digi-Key Electronics. [Online]. Available:  
<https://mm.digikey.com/Volume0/opasdata/d220001/medias/docus/1133/CD4007.pdf>. [Accessed: Apr. 5, 2025].