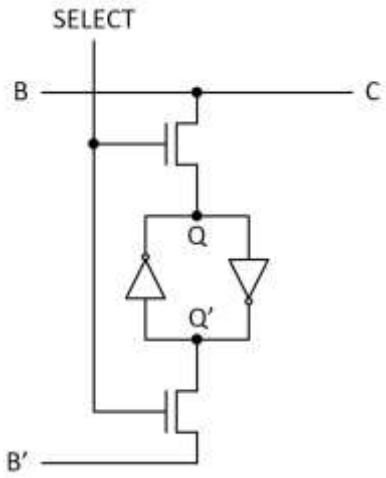
Your Name: _____ netid:_____ Group #:
Name: _____ netid:_____
Name: _____ netid:_____
Name: _____ netid:_____

ECE 120 Worksheet 10: Storage elements

In this discussion section, you will analyze the work of a static RAM cell. You will also implement the logic necessary to control the RAM cell in order to enable it to store data at a location specified by an address. And finally you will learn how to build memory systems by using smaller memory chips.

1. RAM cell

Shown below is a static RAM cell based on a dual-inverter loop. Analyze its work and fill in the table below.



a. What should we apply to Select, B and B' in order to hold a value Q?

Answer:

Select=0 B=don't care B'=don't care

b. What should we apply to Select, B and B' in order to read the value Q to C?

Answer:

Select=1 B=don't apply anything B'=don't apply anything

c. What should we apply to Select, B and B' in order to write a 0 to Q

Answer:

Select=1 B=0 B'=1

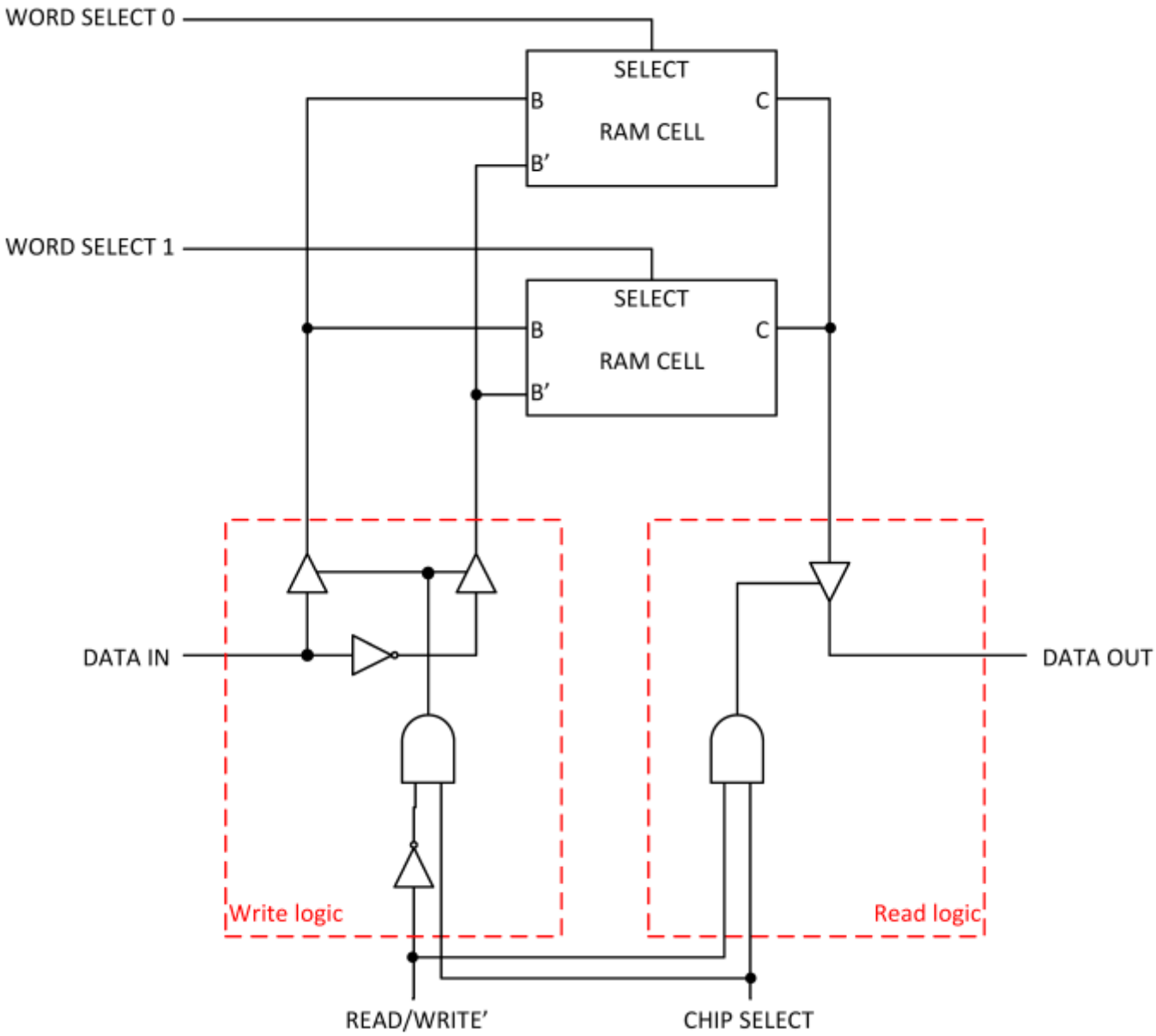
d. What should we apply to Select, B and B' in order to write a 1 to Q

Answer:

Select=1 B=1 B'=0

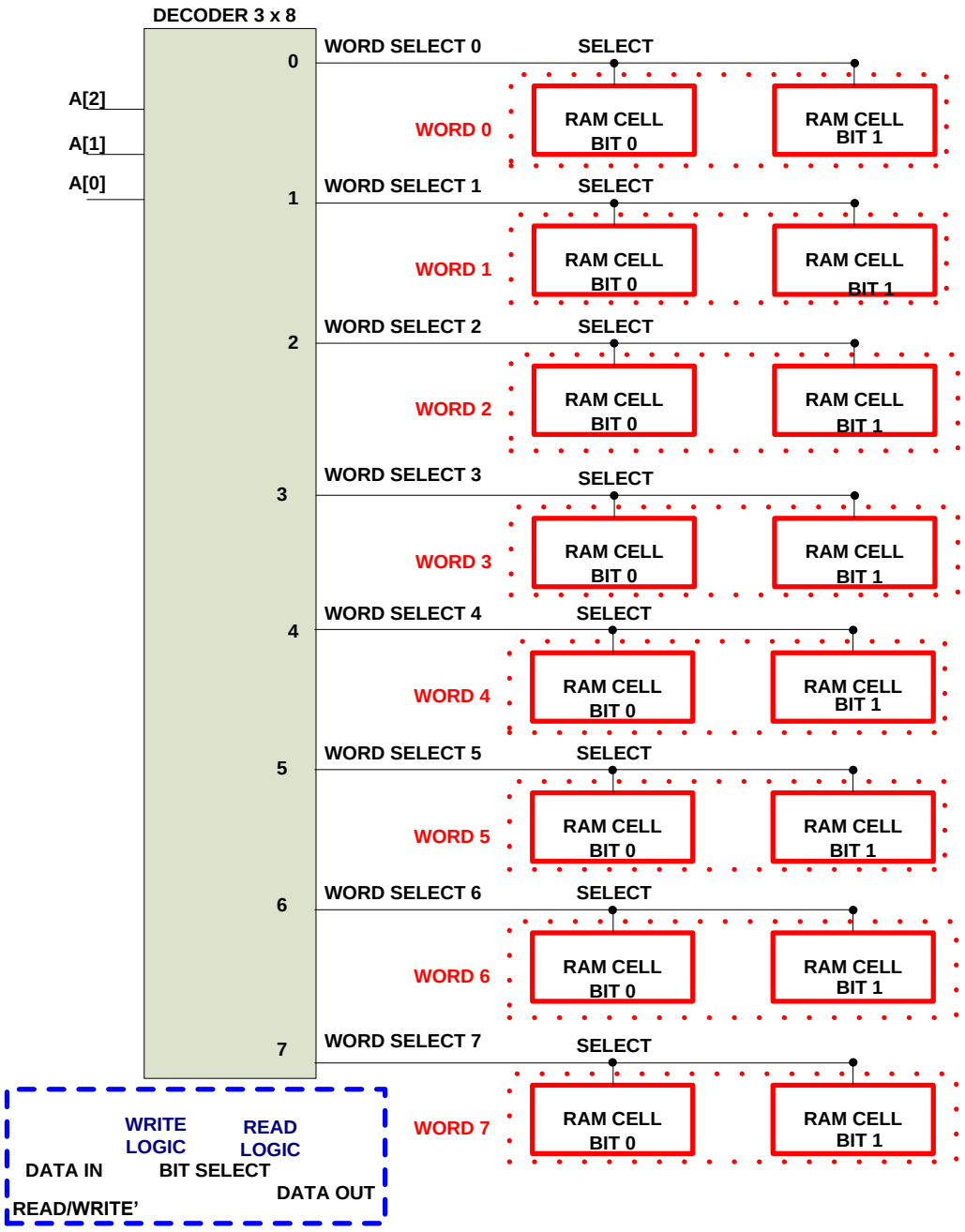
2. RAM bit slice

Shown below is a RAM bit slice. Its *write logic* circuit is missing and you need to implement it using gates and tri-state buffers. The circuit should enable writing the DATA IN value into a RAM cell whose SELECT signal is asserted when READ/WRITE' signal is set to 0 and the CHIP SELECT signal is set to 1.



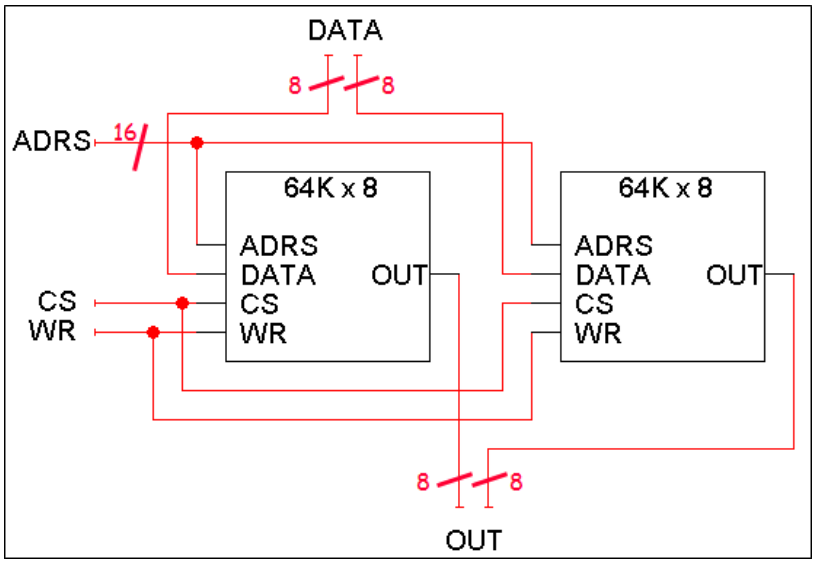
3. RAM

Shown below are two bit slices used to implement an 8x2 RAM. Add an appropriately sized decoder to enable asserting *word select* lines based on unique addresses A[2:0].



4. Larger RAM from smaller parts

Build a 64K x 16 RAM from two 64K x 8 chips.



Build a 256K x 8 RAM from 64K x 8 chips and 2:4 decoder. Assume that the outputs of the RAM chips are gated with the tri-state buffers.