ECE 120: Introduction to Computing **Spring 2019 ZJUI**

demo signup by 11:59:59 p.m. on Monday 8 April 2019

demos from 10 to 12 April 2019

Lab 3: Implementing Functions with TTL

Lab 3 is due during the week of April 8. You will use the same kit and wiring set-up that you developed in Lab 2, and will continue to work with the same partner. You will sign up (on Piazza) for a demo slot by Monday 8 April, and will demonstrate your implementation in an evening slot from Wednesday 10 April to Friday 12 April. We have electronics lab E-201 (the same lab that you used for ECE 110) reserved for the demos. You will continue to build with the same kit in Lab 4, which will follow in two weeks.

You need to demonstrate your circuit with your teammate present.

Please note that you must complete the logic design for the functions discussed in this lab in Homework 6 Problem 4 part (c), which is due in lecture on 4 April 2019 (a day earlier than usual because of the holiday on 5 April 2019).

Lab Procedure

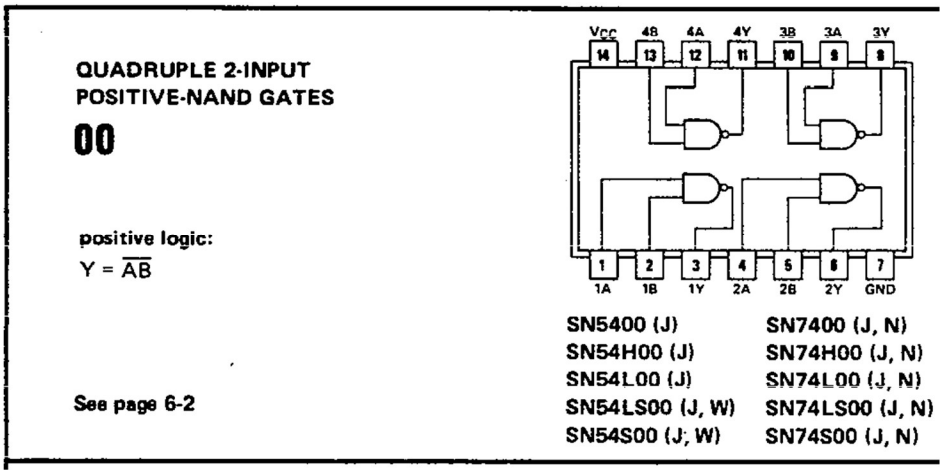
In this lab, you will implement the circuit that you designed in HW6P4(c) as a working prototype on your protoboard. The circuit must be implemented using NAND or NOR gates only, with as few inverters as possible. (Yes, you can use NOT gates as needed, but try to use as few as possible.) Your circuit must implement the specification at the top of page 103 of the class notes and generate two output signals, A and P.

1. Use the Lab 3 Worksheet to draw your truth table and the layout of your TTL DIPs before implementing them on the protoboard.
    a. Your TTL DIPs, LEDs, and DIP switches should all be across a channel separating two blocks on the breadboard, just as you did in Lab 2.
    b. Try to layout your design for minimal clutter. This will not only help you debug if problems arise, but it will also make it easier to grade.
    c. Label each TTL DIP with a letter (e.g., A, B).
    d. Label each used pin on your TTL DIPs with the pin number (1,2,...14). This will help when you go to wire the actual circuit.
    e. Only labeling is required, but showing some wiring may be useful for you when assembling the circuit. In fact, you do not need to show entire wiring, just signal labeling may be sufficient.
2. Using a copy of your circuit diagram from HW6P4(c), label each input and output with a DIP letter and pin number as a schematic for how you will connect the chips on your protoboard.
    a. The TTL chipset you received allows you to use only NOT, 2-input NAND, 2-input NOR, 3-input NAND, 3-input NOR, and 4-input NAND gates. Make sure you can implement your circuit with just those gates.
    b. Use the datasheets below to choose which TTL DIPs you will use and to determine how you will select which pins to use.

3. Implement, test, and debug your circuit on the protoboard by using your TTL DIPs, switches, and LEDs.
    a. You will need to use at last 3 switches and 2 LEDs to demonstrate the functionality of your circuit. We recommend using more LEDs to help you debug.
    b. During your testing and demonstration, bring your worksheet and use the switches to send all possible combinations of inputs into your circuit. Keep track of whether the LEDs show the behavior specified on page 103 of the notes. (Note that if you implemented HW4P6(d) correctly based on part (c), and implemented your protoboard circuit the same way, the implementation will be correct.)

TTL DIP Data

Use the datasheets below to find out which TTL DIP to use for the different types of gates (2-input NAND, 2-input NOR, 3-input NAND, etc.) and to determine the pin assignments for your schematic. The title in the top left of each datasheet tells you what types of gates are in the DIP. The schematic on the top right of each datasheet shows you how the inputs and outputs of the various gates are connected to the pins of the TTL DIP. The text on the bottom right tells you which labels on your TTL DIPs to look for. The different serial numbers represent slightly different implementations of the same basic design. Notice that there are many ways to implement even simple 2-input NAND gates. If you need extra NAND chips, ask a TA during office hours to provide them to you.



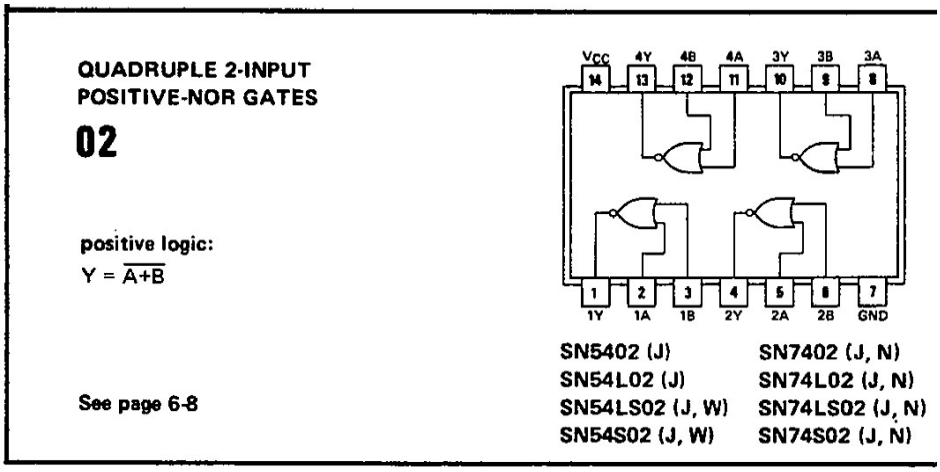
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

00

positive logic:
$Y = \overline{AB}$

See page 6-2

SN5400 (J) SN7400 (J, N)
SN54H00 (J) SN74H00 (J, N)
SN54L00 (J) SN74L00 (J, N)
SN54LS00 (J, W) SN74LS00 (J, N)
SN54S00 (J, W) SN74S00 (J, N)



QUADRUPLE 2-INPUT
POSITIVE-NOR GATES

02

positive logic:
$Y = \overline{A+B}$

See page 6-8

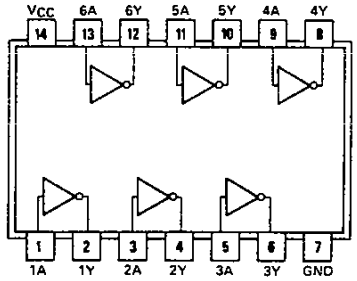
SN5402 (J) SN7402 (J, N)
SN54L02 (J) SN74L02 (J, N)
SN54LS02 (J, W) SN74LS02 (J, N)
SN54S02 (J, W) SN74S02 (J, N)

HEX INVERTERS

04

positive logic:
$Y = \overline{A}$

See page 6-2



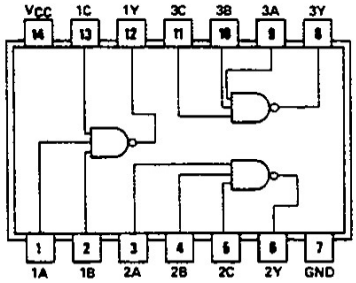
SN5404 (J)	SN7404 (J, N)
SN54H04 (J)	SN74H04 (J, N)
SN54L04 (J)	SN74L04 (J, N)
SN54LS04 (J, W)	SN74LS04 (J, N)
SN54S04 (J, W)	SN74S04 (J, N)

TRIPLE 3-INPUT POSITIVE-NAND GATES

10

positive logic:
$Y = \overline{ABC}$

See page 6-2



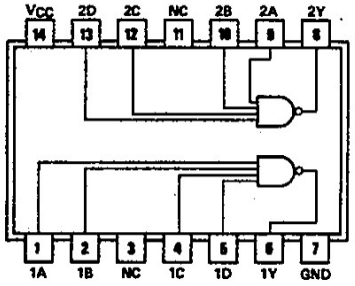
SN5410 (J)	SN7410 (J, N)
SN54H10 (J)	SN74H10 (J, N)
SN54L10 (J)	SN74L10 (J, N)
SN54LS10 (J, W)	SN74LS10 (J, N)
SN54S10 (J, W)	SN74S10 (J, N)

DUAL 4-INPUT POSITIVE-NAND GATES

20

positive logic:
$Y = \overline{ABCD}$

See page 6-2



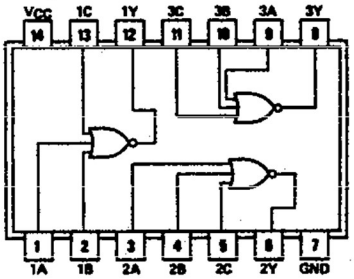
SN5420 (J)	SN7420 (J, N)
SN54H20 (J)	SN74H20 (J, N)
SN54L20 (J)	SN74L20 (J, N)
SN54LS20 (J, W)	SN74LS20 (J, N)
SN54S20 (J, W)	SN74S20 (J, N)

TRIPLE 3-INPUT POSITIVE-NOR GATES

27

positive logic:
$Y = \overline{A+B+C}$

See page 6-8



SN5427 (J, W) SN7427 (J, N)
SN54LS27 (J, W) SN74LS27 (J, N)

What to Bring to the Demonstration

- The copy of your HW6P4(c) circuit diagram labeled with pin and chip assignments. If you realize that your HW6 design is not practical to implement, redraw it and tell the instructor what the difference is between your HW6 design and the protoboard implementation.
- Completed lab worksheet.
- Demonstrate your working circuit to the instructor by showing that your circuit creates the correct outputs for all input combinations.

Do not disassemble your protoboard circuit; you will need it in Lab 4!