Your Name: _____ netid:_____ Group #:
Name: _____ netid:_____
Name: _____ netid:_____
Name: _____ netid:_____

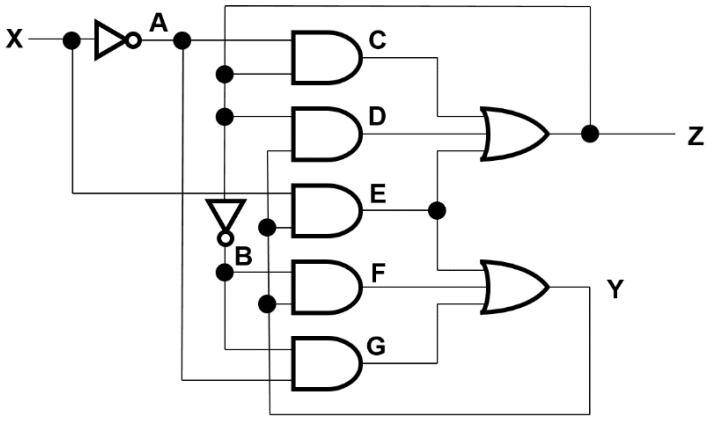
ECE 120 Worksheet 7: Storage elements

Before you come to discussion, please read Lecture Notes Sections 2.6 and 2.7.

In this discussion you will analyze an asynchronous sequential feedback circuit (like a latch) to understand its operation. Designing such devices is beyond the scope of our class, but seeing a few asynchronous circuits will help you to understand and appreciate the complexity that has been abstracted away for you when you do clocked synchronous designs in our class.

1. An Asynchronous Clock Divider

The circuit below is an asynchronous sequential feedback circuit with one input and one output. Your task is to analyze the circuit and to understand how it is intended to operate and how variations in gate timing can make it fail.



output	expression
A	X’
B	Z’
C	AZ
D	YZ
E	XY
F	BY
G	AB
Y	E+F+G
Z	C+D+E

1. Begin by filling in the table to the right of the circuit to indicate the value of each gate output **in terms of its inputs**. The first two have been done for you.
2. Now substitute the expressions for **A**, **B**, **E**, **F**, and **G** into the expression for **Y** to obtain an expression for the next state Y^+ in terms of **X**, **Y**, and **Z**. Also substitute the expressions for **A**, **C**, **D**, and **E** into the expression for **Z** to obtain an expression for the next state Z^+ in terms of **X**, **Y**, and **Z**.

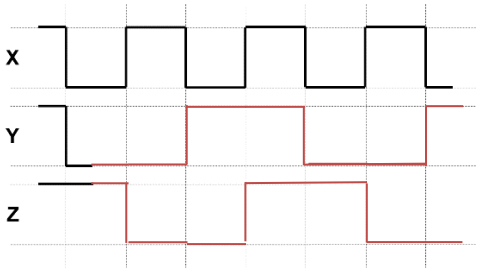
$Y^+ =$ E + F + G = XY + BY + AB = XY + Z’Y + X’Z’

$Z^+ =$ C + D + E = AZ + YZ + XY = X’Z + YZ + XY

3. Using the expressions that you found in **Part 2**, calculate the next state for each combination of input **X** and internal state variables **Y** and **Z**. Those states that do not change (until input **X** changes) are said to be **stable states**. Indicate the stable states in the table below.

X	Y	Z	Y^+	Z^+	Stable? (yes or no)
0	0	0	1	0	No
0	0	1	0	1	Yes
0	1	0	1	0	Yes
0	1	1	0	1	No
1	0	0	0	0	Yes
1	0	1	0	0	No
1	1	0	1	1	No
1	1	1	1	1	Yes

4. Fill in the timing diagram below to indicate how the internal variable **Y** and output **Z** change in response to changes in input **X** when the input takes the form of a square wave (as shown).



5. Explain why one might call this circuit a clock divider.

The output Z is half the clock frequency (or double the clock period).

6. When we discussed timing heuristics, we suggested that you count "gate delays" from input to output. Assuming that every gate in our circuit takes the same amount of time to change its output, use your answers to **Part 1** to fill in the table below by recalculating each variable value from the current output values one gate delay earlier (using a column one to the left as variable values). Shading in the part already done for you indicates values that have not changed. In the part you fill in, **circle values that have changed from the previous column**. Note that the last column should not contain any changes (the circuit should be stable again after three gate delays).

		Time in gate delays				
	stable	**0**	**1**	**2**	**3**	**4**
X	1	0	0	0	0	0
A	0	0	**1**	1	1	1
B	0	0	0	0	0	0
C	0	0	0	**1**	1	1
D	1	1	1	1	**0**	0
E	1	1	**0**	0	0	0
F	0	0	0	0	0	0
G	0	0	0	0	0	0
Y	1	1	1	**0**	0	0
Z	1	1	1	1	1	1

7. Based on the table in **Part 6**, explain the role of the gate with output labeled **D**.

Without this gate, the Z output would drop to 0 for one gate delay and produce a static-1 hazard.

(for fun) What might happen if the gate that produces output **C** is an unusually slow gate?

Similar to part 6, the output Z would drop to 0 and cause the internal state to change to YZ=00 instead of the desired 01.