CPE301 – SPRING 2019

Design Assignment 1A

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Primary Github address: https://github.com/mendos1/subnission\_da/tree/master/DesignAssignments

Directory: DA1A

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

The only component used for this lab is the Atmel Studio 7.

1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

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.org 0x0000

ldi r16, 0x08 ; Decrementing counter control

clr r18 ; Product Low Bytes

clr r19 ; Product Mid Bytes

clr r20 ; Product High Bytes

ldi r21, 0x00 ; Always Zero

ldi r22, 0xFF ; Plier

ldi r23, 0x00 ; Virtual High Bytes for Cand

ldi r24, 0xFF ; Cand Low Bytes

ldi r25, 0xFF ; Cand Mid Bytes

BitCheck:

mov r17, r22 ; Bit Checking Register

andi r17, 0b00000001 ; Logical AND Bit Check Set Up

brne AddCandStage ; 1 Is Detected As First Bit

breq ShiftStage ; 0 Is Detected As First Bit

ShiftStage:

lsl r23 ; Logical Shift Left Of Virtual Bytes

lsl r25 ; Logical Shift Left Of High Bytes of Cand

adc r23, r21 ; Add Carry Bit Of Previouse Step To Virtual Bytes Of Cand

lsl r24 ; Logical Shift Left Of Low Bytes Of Cand

adc r25, r21 ; Add Carry Bit of Previouse Step To High Bytes

lsr r22 ; Logical Shift Right Of Plier

dec r16 ; Decrement Bit/Shift Counter

brne BitCheck ; If Not Zero Branch To Label BitCheck

breq Done ; If Zero Branch To Label Done

AddCandStage:

add r18, r24 ; Add Low Bytes Of Product And Cand respectively

adc r19, r21 ; Add Carry Bit To Mid Reg Of Product

adc r20, r21 ; Add Propagated Bit To High Bytes of Product

add r19, r25 ; Add Mid/High Bytes of Product And Cand Respectively

adc r20, r21 ; Add Carry Bit to Higher

add r20, r23 ; Add High Byte of Product with Virtual Byte of Cand

rjmp ShiftStage

Done:

BREAK

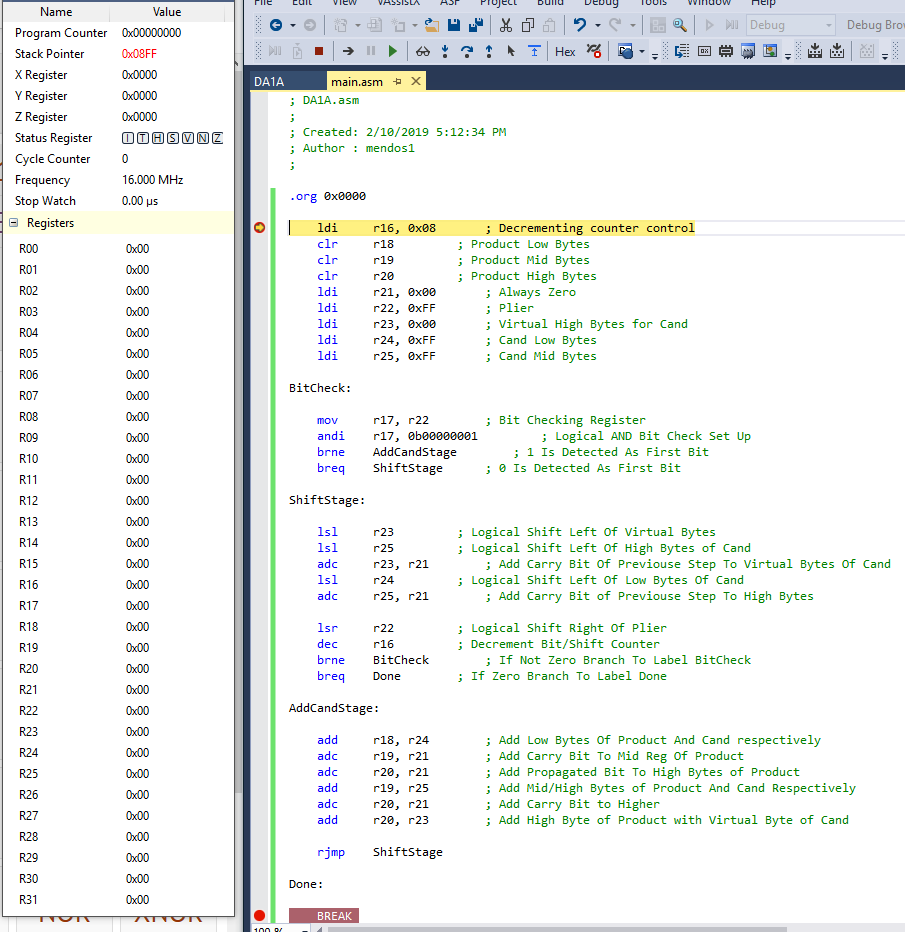
1. **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**

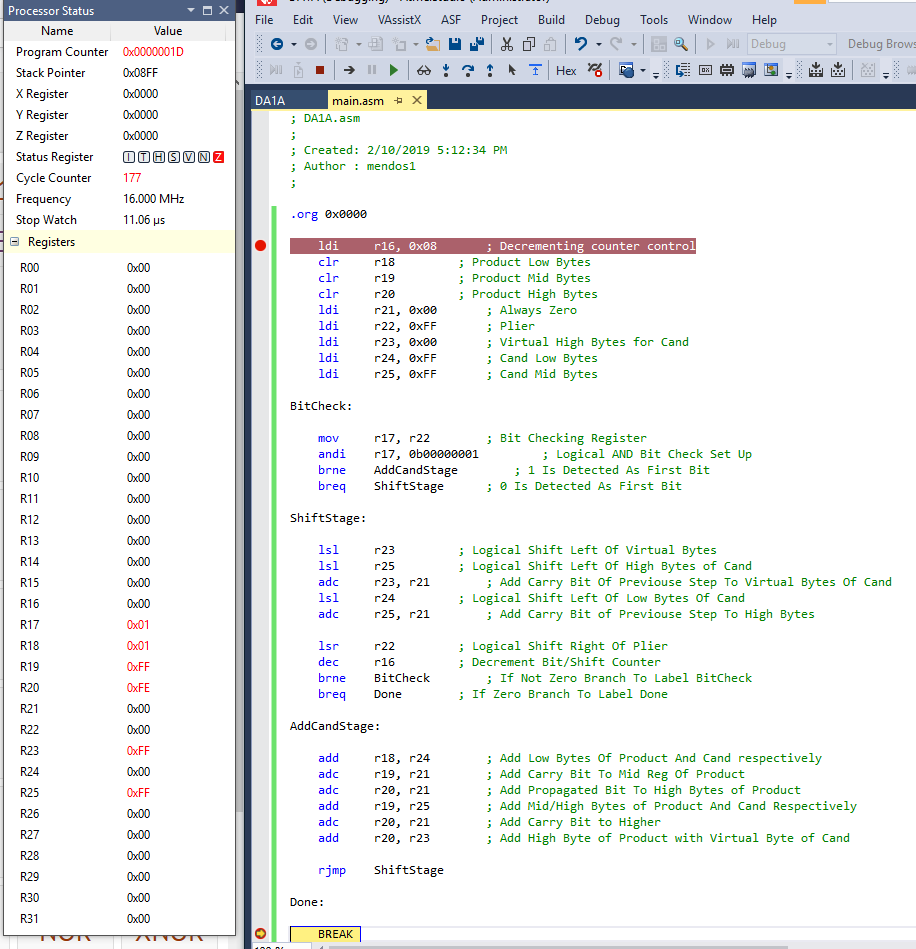
Insert only the modified sections here

1. **SCHEMATICS**

None for this lab

1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**





1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**

none

1. **VIDEO LINKS OF EACH DEMO**

none

1. **GITHUB LINK OF THIS DA**

<https://github.com/mendos1/subnission_da/tree/master/DesignAssignments/DA1A>

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

NAME OF THE STUDENT