CSCI 212: Computer Organization & Assembly Language

Palomar College

Chapter 2: x86 Processor Architecture

Based upon the book: Assembly Language for x86 Processors, 7th Edition

Some slides were prepared by the book author, Kip Irvine.

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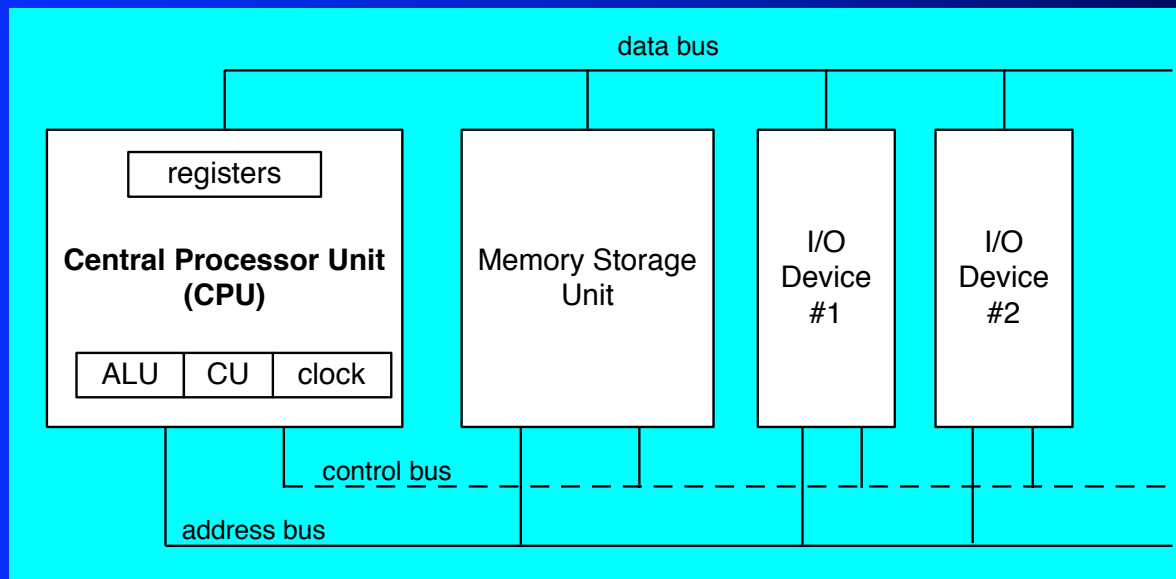
Chapter Overview

- General Concepts
- IA-32 Processor Architecture
- IA-32 Memory Management
- 64-bit Processors
- Components of an IA-32 Microcomputer
- Input-Output System

General Concepts

- Basic microcomputer design
- Instruction execution cycle
- Reading from memory
- How programs run

Basic Microcomputer Design

- clock synchronizes CPU operations
- control unit (CU) coordinates sequence of execution steps
- ALU performs arithmetic and bitwise processing

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Clock

- synchronizes all CPU and BUS operations
- machine (clock) cycle measures time of a single operation
- clock is used to trigger events
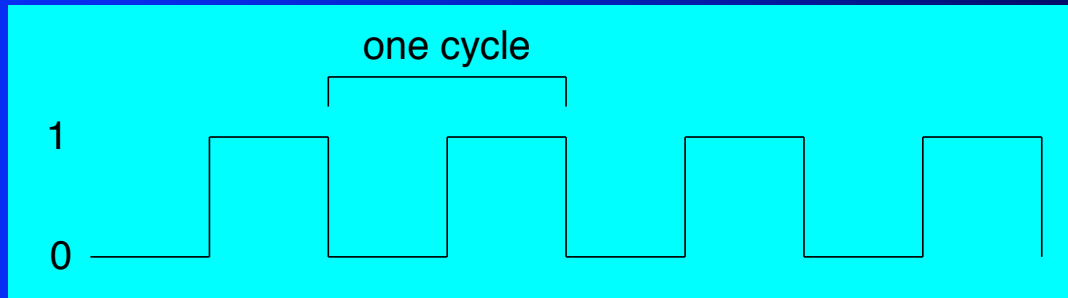
one cycle

1

0

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What's Next

- General Concepts
- **IA-32 Processor Architecture**
- IA-32 Memory Management
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Instruction Execution Cycle

- Fetch
- Decode
- Fetch operands
- Execute
- Store output

Figure 2–2   Simplified Pentium CPU Block Diagram.

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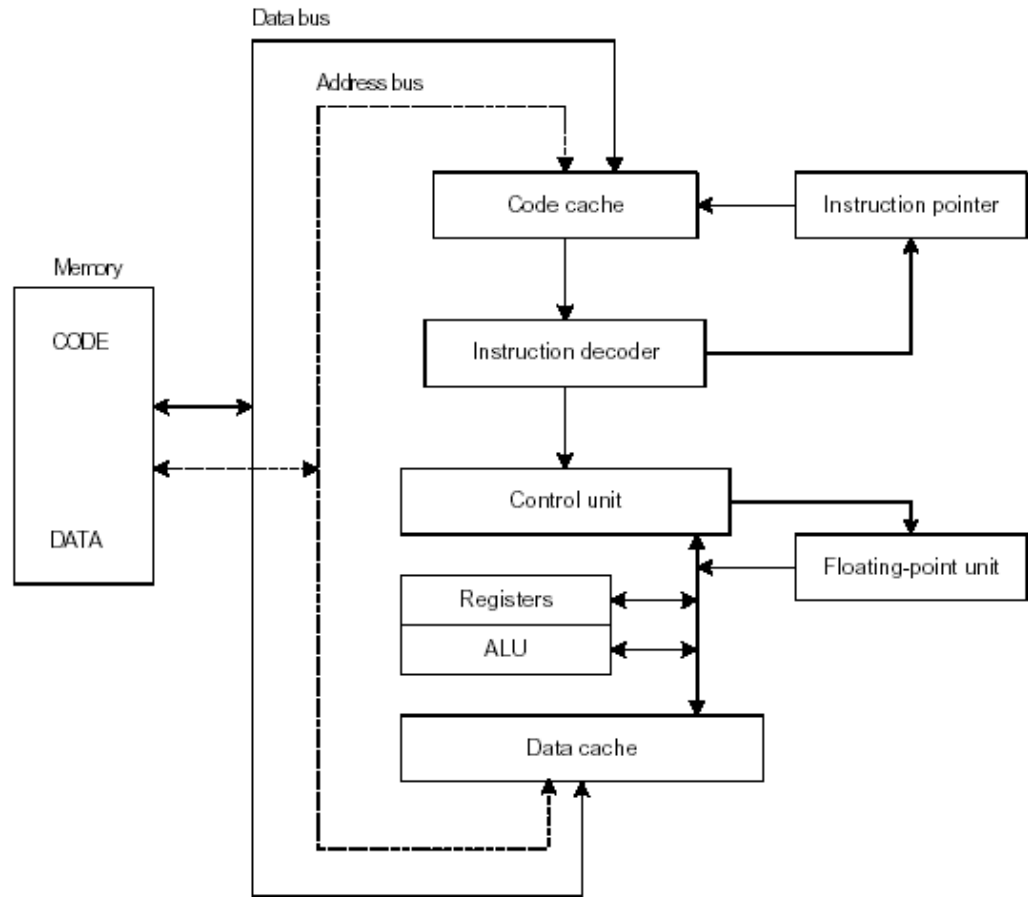
Cache Memory

- High-speed expensive static RAM both inside and outside the CPU.
    - Level-1 cache: inside the CPU
    - Level-2 cache: outside the CPU
- Cache hit: when data to be read is already in cache memory
- Cache miss: when data to be read is not in cache memory.

How a Program Runs

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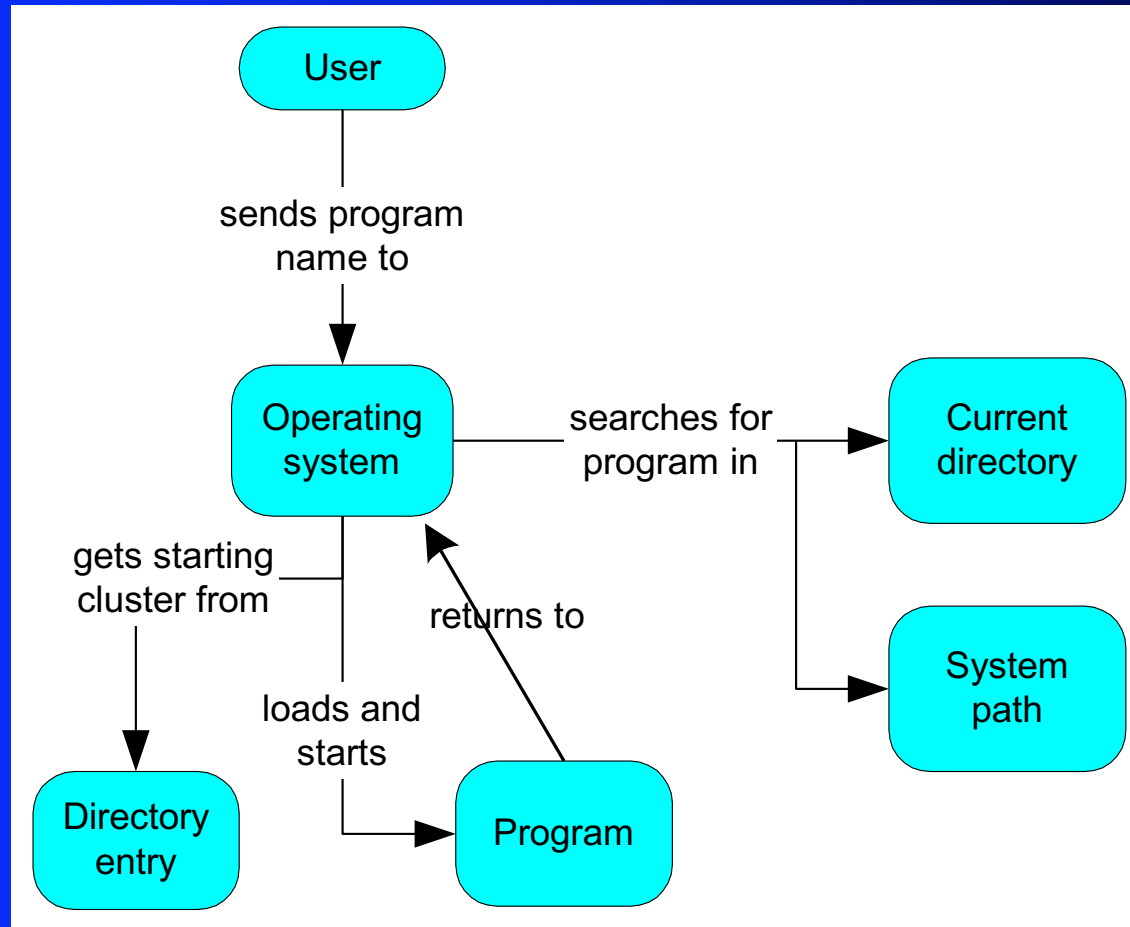
IA-32 Processor Architecture

- Modes of operation
- Basic execution environment
- Floating-point unit
- Intel Microprocessor history

Modes of Operation

- Protected mode
  - native mode (Windows, Linux)
- Real-address mode
  - native MS-DOS
- System management mode
  - power management, system security, diagnostics

- Virtual-8086 mode
  - hybrid of Protected
  - each program has its own 8086 computer

Basic Execution Environment

- Addressable memory
- General-purpose registers
- Index and base registers
- Specialized register uses
- Status flags
- Floating-point, MMX, XMM registers

Addressable Memory

- Protected mode
  - 4 GB
  - 32-bit address
- Real-address and Virtual-8086 modes
  - 1 MB space
  - 20-bit address

General-Purpose Registers

Named storage locations inside the CPU, optimized for speed.

32-bit General-Purpose Registers
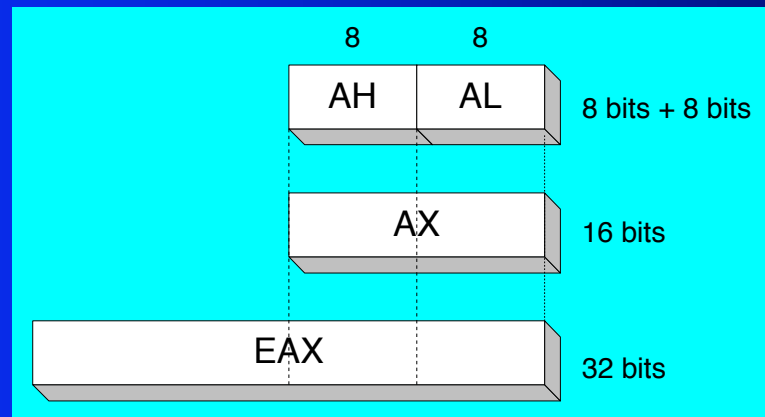
EAX
EBX
ECX
EDX

EBP
ESP
ESI
EDI

EFLAGS

EIP

16-bit Segment Registers

CS	ES
SS	FS
DS	GS

Accessing Parts of Registers

- Use 8-bit name, 16-bit name, or 32-bit name
- Applies to EAX, EBX, ECX, and EDX

32-bit	16-bit	8-bit (high)	8-bit (low)
EAX	AX	AH	AL
EBX	BX	BH	BL
ECX	CX	CH	CL
EDX	DX	DH	DL

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Index and Base Registers

- Some registers have only a 16-bit name for their lower half:

32-bit	16-bit
ESI	SI
EDI	DI
EBP	BP
ESP	SP

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Some Specialized Register Uses (1 of 2)

- General-Purpose
    - EAX – accumulator
    - ECX – loop counter
    - ESP – stack pointer
    - ESI, EDI – index registers
    - EBP – extended frame pointer (stack)
- Segment
    - CS – code segment
    - DS – data segment
    - SS – stack segment
    - ES, FS, GS - additional segments

# Some Specialized Register Uses

- EIP – instruction pointer
- EFLAGS
  - status and control flags
  - each flag is a single binary bit

Status Flags

- Carry
  - unsigned arithmetic out of range
- Overflow
  - signed arithmetic out of range
- Sign
  - result is negative
- Zero
  - result is zero
- Auxiliary Carry
  - carry from bit 3 to bit 4
- Parity
  - sum of 1 bits is an even number

Floating-Point, MMX, XMM Registers

- Eight 80-bit floating-point data registers

  - ST(0), ST(1), . . . , ST(7)

  - arranged in a stack

  - used for all floating-point arithmetic

- Eight 64-bit MMX registers

- Eight 128-bit XMM registers for single-instruction multiple-data (SIMD) operations
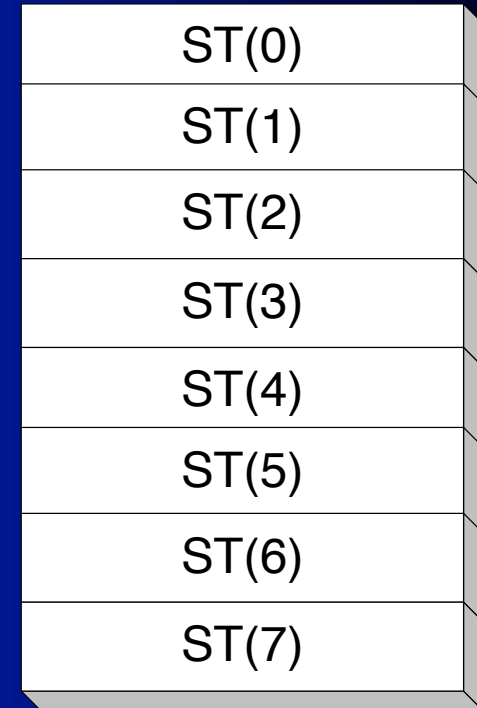
| ST(0) |
| ST(1) |
| ST(2) |
| ST(3) |
| ST(4) |
| ST(5) |
| ST(6) |
| ST(7) |

What's Next

- General Concepts
- IA-32 Processor Architecture
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- **64-Bit Processors**
- Components of an IA-32 Microcomputer
- Input-Output System

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64-Bit Processors

- 64-Bit Operation Modes
  - Compatibility mode – can run existing 16-bit and 32-bit applications (Windows supports only 32-bit apps in this mode)
  - 64-bit mode
- Basic Execution Environment
  - addresses can be 64 bits (48 bits, in practice)
  - 16 64-bit general purpose registers
  - 64-bit instruction pointer named RIP

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64-Bit General Purpose Registers

- 32-bit general purpose registers:
  - EAX, EBX, ECX, EDX, EDI, ESI, EBP, ESP, R8D, R9D, R10D, R11D, R12D, R13D, R14D, R15D
- 64-bit general purpose registers:
  - RAX, RBX, RCX, RDX, RDI, RSI, RBP, RSP, R8, R9, R10, R11, R12, R13, R14, R15

What's Next

- General Concepts
- IA-32 Processor Architecture
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- 64-Bit Processors
- **Components of an IA-32 Microcomputer**
- Input-Output System

Components of an IA-32 Microcomputer

- Motherboard
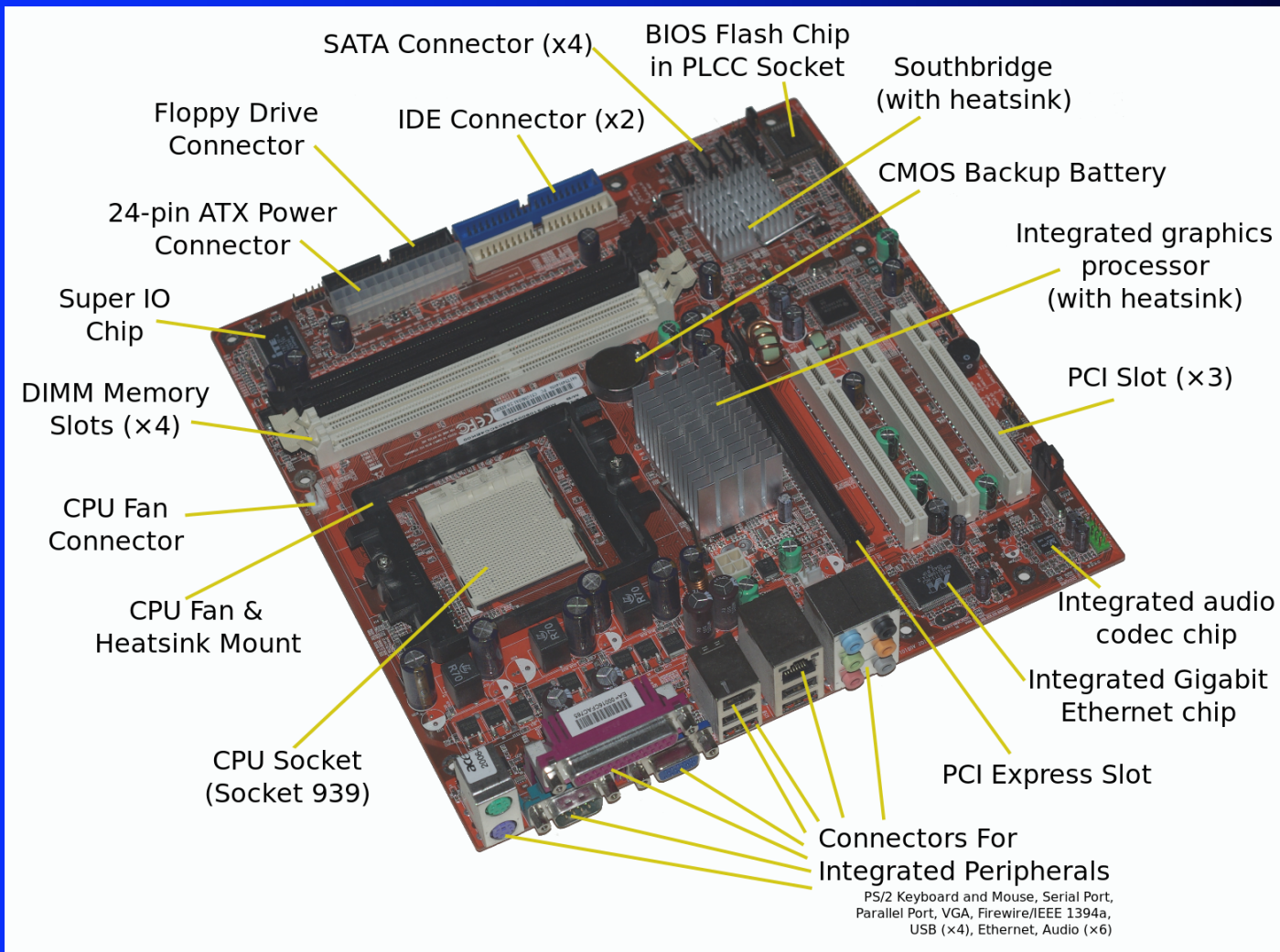- Video output
- Memory
- Input-output ports

Motherboard

- CPU socket
- External cache memory slots
- Main memory slots
- BIOS chips
- Sound synthesizer chip (optional)
- Video controller chip (optional)
- IDE, parallel, serial, USB, video, keyboard, joystick, network, and mouse connectors
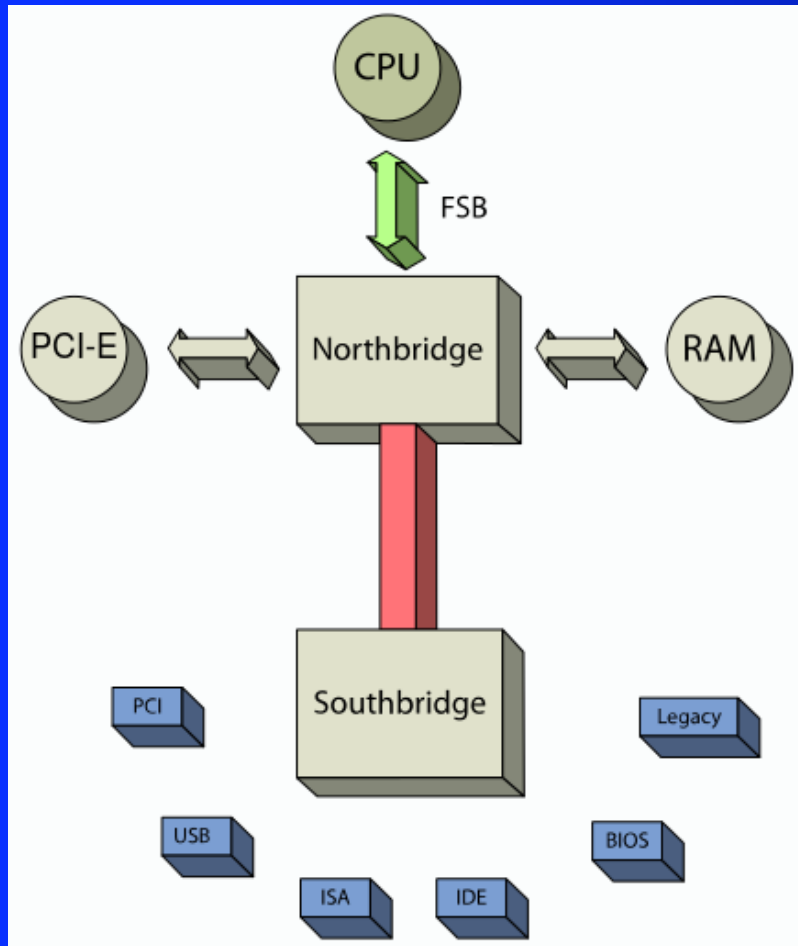- PCI bus connectors (expansion cards)

Motherboards at Local Retailer

Motherboard

SATA Connector (x4)

BIOS Flash Chip in PLCC Socket

Southbridge (with heatsink)

Floppy Drive Connector

IDE Connector (x2)

CMOS Backup Battery

24-pin ATX Power Connector

Integrated graphics processor (with heatsink)

Super IO Chip

PCI Slot (×3)

DIMM Memory Slots (×4)

CPU Fan Connector

CPU Fan & Heatsink Mount

Integrated audio codec chip

Integrated Gigabit Ethernet chip

CPU Socket (Socket 939)

PCI Express Slot

Connectors For Integrated Peripherals
PS/2 Keyboard and Mouse, Serial Port, Parallel Port, VGA, Firewire/IEEE 1394a, USB (×4), Ethernet, Audio (×6)

Chipset Schematic

- The **southbridge** is one of the two chips in the core logic chipset on a PC motherboard, the other being the northbridge.
- The southbridge typically implements the slower capabilities of the motherboard in a northbridge/southbridge computer architecture.

Video Output

- Video controller
  - on motherboard, or on expansion card
  - AGP (<u>accelerated graphics port technology</u>)*
  - PCIE 3.0
- Video memory (VRAM)
- Video CRT Display
  - uses raster scanning
  - horizontal retrace
  - vertical retrace
- Direct digital LCD monitors
  - no raster scanning required

* This link may change over time.

Video Controller Example

- Video controller
  - PCIE 3.0
  - 2048 MB GDDR5 Memory
  - 81.9GT/s Texture Fill Rate
  - 112.16GB/s Memory Bandwidth

Memory

- ROM
  - read-only memory
- EPROM
  - erasable programmable read-only memory
- Dynamic RAM (DRAM)
  - inexpensive; must be refreshed constantly
- Static RAM (SRAM)
  - expensive; used for cache memory; no refresh required

Input-Output Ports

- USB 2.0 (universal serial bus)
  - intelligent high-speed connection to devices
  - up to 480 megabits/second
  - USB hub connects multiple devices
  - *enumeration*: computer queries devices
  - supports *hot* connections
- USB 3.0
  - up to 5 gigabits/second

Input-Output Ports (cont)

- Serial
    - RS-232 serial port
    - one bit at a time
    - uses long cables and modems
    - 16550 UART (universal asynchronous receiver transmitter)
    - programmable in assembly language

Device Interfaces

- ATA host adapters
  - intelligent drive electronics (hard drive, CDROM)
- SATA (Serial ATA)
  - inexpensive, fast, bidirectional
- FireWire
  - high speed (800 MB/sec), many devices at once
- Bluetooth
  - small amounts of data, short distances, low power usage
- Wi-Fi (wireless Ethernet)
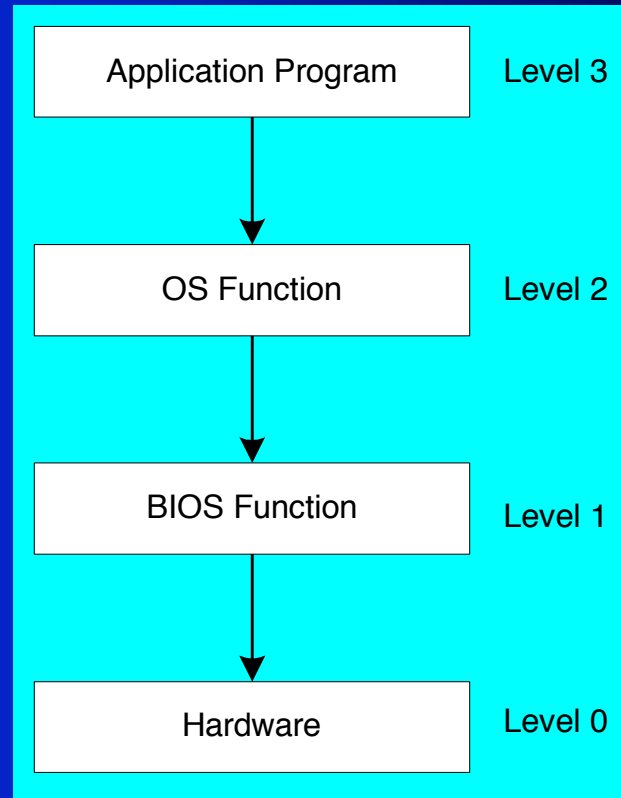 - IEEE 802.11 standard, faster than Bluetooth

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Levels of Input-Output

- Level 3: High-level language function
  - examples: C++, Java
  - portable, convenient, not always the fastest
- Level 2: Operating system
  - Application Programming Interface (API)
  - extended capabilities, lots of details to master
- Level 1: BIOS
  - drivers that communicate directly with devices
 - OS security may prevent application-level code from working at this level

Displaying a String of Characters

When a HLL program displays a string of characters, the following steps take place:

Application Program	Level 3
↓	
OS Function	Level 2
↓	
BIOS Function	Level 1
↓	
Hardware	Level 0

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Programming levels

Assembly language programs can perform input-output at each of the following levels:
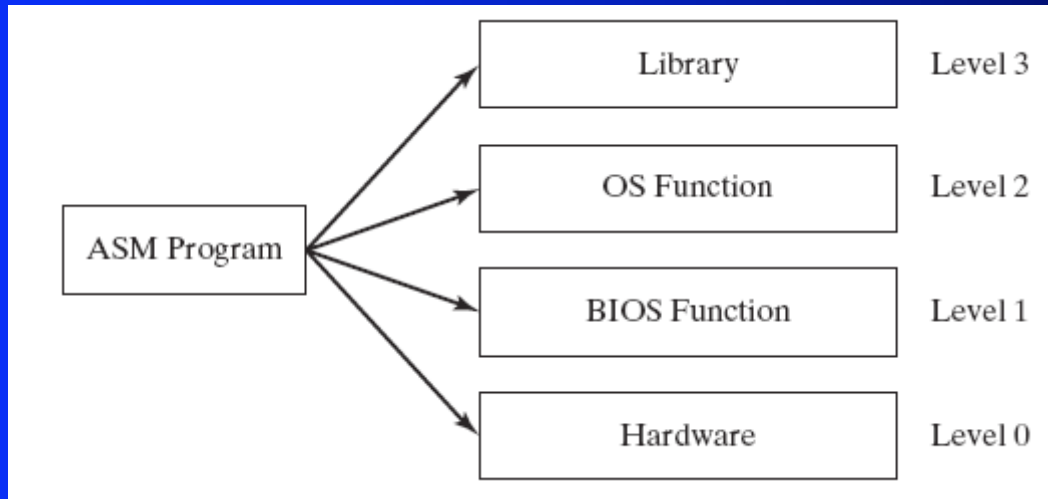
Summary

- Central Processing Unit (CPU)
- Arithmetic Logic Unit (ALU)
- Instruction execution cycle
- Multitasking
- Floating Point Unit (FPU)
- Complex Instruction Set
- Real mode and Protected mode
- Motherboard components
- Memory types
- Input/Output and access levels

Assignments/Quiz

- Read Chapters 3 by next week
- Review material covered in Chapters 1 & 2
- Lab assignments must be completed by the beginning of class next week.
- Quiz at the beginning of class next week on the material covered in Chapters 1 & 2 (Blackboard)
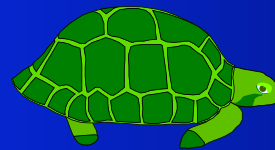
42 69 6E 61 72 79

What does this say?