Lab4 - Parking Meter

Introduction and Requirement

In this lab, similar to project3, the goal is to design a fintie state machine (FSM) in Verilog HDL that matches the specified behavior. We need to figure out what states should we have and how the machine transitions from one state to another. The significance of this lab is to learn how to apply FSM design to the real problems in life. For this assignment, we are required to design a parking meter, which simulates coins being added and displays the appropriate time remaining.

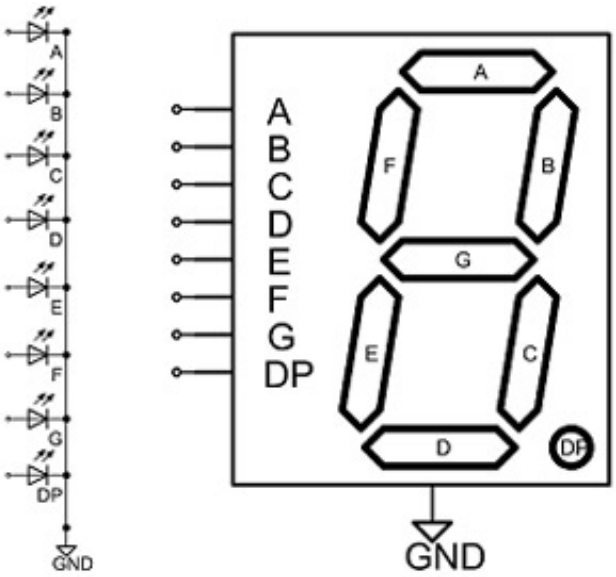
Inputs & Outputs

The inputs to the system have been listed in the table below:

Inputs	Function
add1	Add 60 seconds
add2	Add 120 seconds
add3	Add 180 seconds
add4	Add 300 seconds
rst1	Reset time to 16 seconds
rst2	Reset time to 150 seconds
clk	Frequency of 100 Hz
rst	Resets to the initial state

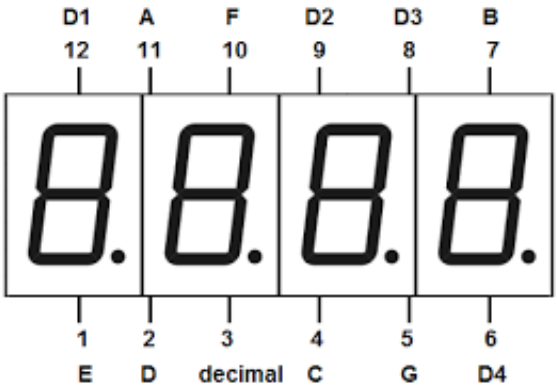
The output is modeled as 4 seven segment LED displays which display the time remaining before the meter expires inn seconds.

> A **seven**-**segment display** is a form of electronic **display** device for **displaying** decimal numerals that is an alternative to the more complex dot matrix **displays**. **Seven**-**segment displays** are widely used in digital clocks, electronic meters, basic calculators, and other electronic devices that **display** numerical information. —From Wiki



In this lab, each of the segments could be divided into one bit signals `a1` , `a2` , `a3` , `a4` by the adnodes, the design need to output these signal properly.

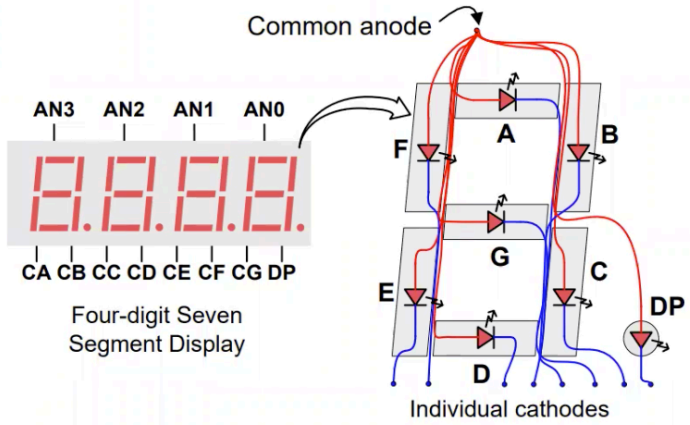
In this lab, we need to implement a 4-digit seven segment display as below:

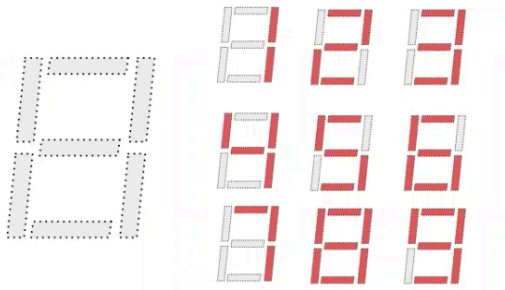


The output ports (`var1` , `var2` , `var3` , `var4`) are 4-bit vectors that represent the actual digit in binary coded decimal corresponding to each of the segments.

And the output module need to consists of a 7-bit vector `leg_seg` , which displays the actual value fed to the 4 segments corresponding to the digits being displayed. The order of the mapping is from CA to CG with CA (as below image) being the MSB. The actual bits (from LSB to MSB) of `leg_seg` is actually map to A-F as below image. (0-> bright, 1-> dark)

Screen shot from Lecture in week 9:





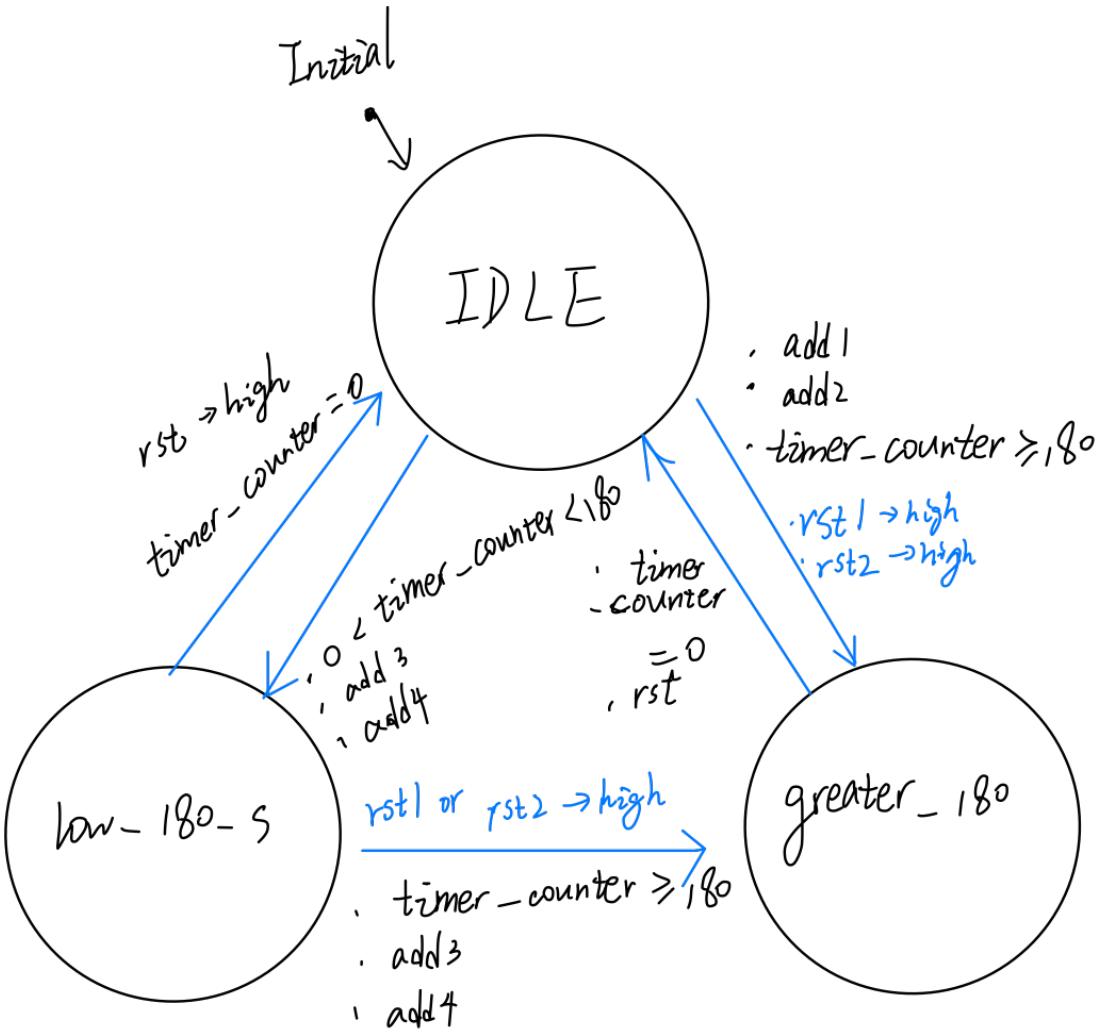
An un-illuminated seven-segment display, and nine illumination patterns corresponding to decimal digits

A scanning display controller circuit can be used to show a four-digit number on this display. This circuit drives the anode signals and corresponding cathode patterns of each digit in a repeating, continuous succession, at an update rate that is faster than the human eye can detect. Each digit is illuminated just one-quarter of the time, but because the eye cannot perceive the darkening of a digit before it is illuminated again, the digit appears

Design Description (FSM diagram)

Before start writing the code, the first step is to draw the FSM diagram to help us to organize the idea to design the module. Basically, I am following the instructioons in the spec. The `IDLE` state is the initial state in the machine, all the other state will return to `IDLE` when the input `reset` =1, and all item counters and outputs are set to 0 in `IDLE` state.

State Diagram:



Details and explanations for the states in the diagram as below:

Note that if `rst1` input goes high, the display get reset to 16 secs (timer_counter => 16) and start counting down 1 at 1 Hz. `rst2` is similar, but it is reset to 150 secs. The state will move to `greater_180` when these two inputs are high.

1. **IDLE** (Initial State) [2'b00]
    - Timer couter = 0
    - Flash 0000 with period 1 sec. i.e., Display flashed at 1Hz.
    - Duty cycle 50% with period 1 sec (i.e., on for 0.5 sec and off for 0.5 sec)
2. **low_180_s** [2'b01] : state when less than 180 seconds are remaining.
    - Timer counter < 180 secs
    - Display flash with a period of 2 secs and 50% duty cycle (i.e. on for 1 sec and off for 1 sec.)
    - The timer counter counts down 1 at 1 Hz. (decrement by 1 at 1 sec)
    - Blink out odd values, only show up even values.
3. **greater_180** [2'b10]
    - When `rst1` or `rst2` goes high, transist to this state from others.
    - Timer counter ≥ 180 secs
    - The timer counter counts down 1 at 1 Hz. (decrement by 1 at 1 sec)

- Max value for timer_counter is 9999. Any attempt to increment beyond 9999, should result in the counter latching to 9999 and counting down there.

According these three states and the timer counter, the different cases of making change on the value of the remaing time are hold.

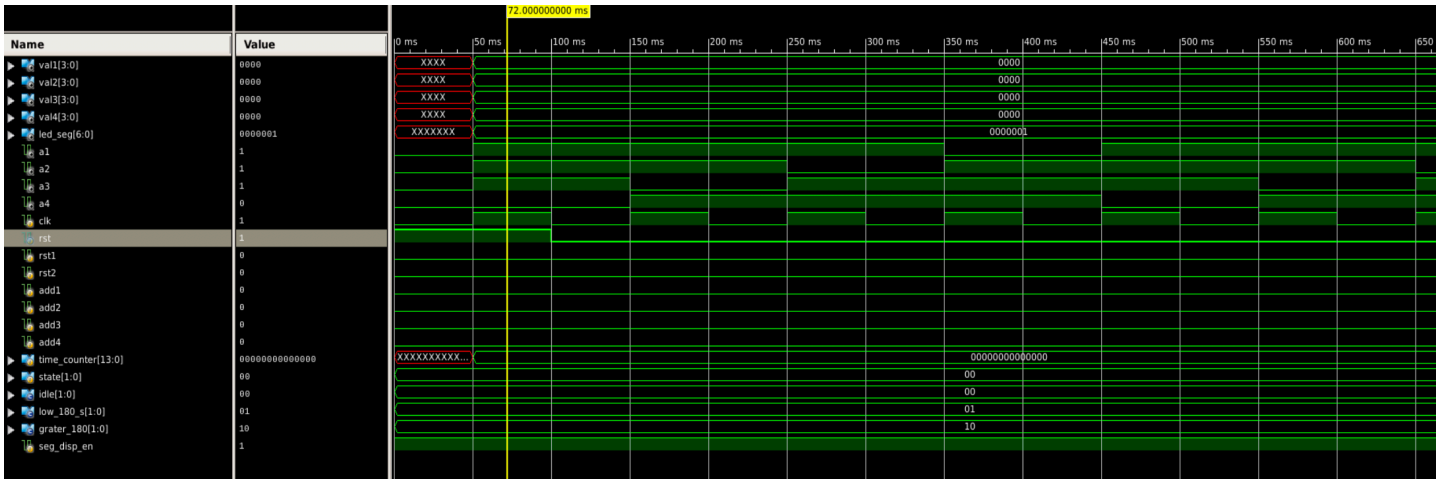
For the coding, I didn't use the given example template, I only use one always block. I put the updates of the current_state, next_state, and output values, all the logic operation in this block.

Simulation Documentation

To test the correctness of my code, check if the state transit properly, I created the test bench file and some test cases inside. The below screenshot of the waveforms are basically showing if the variables hold the correct values when they are in the specific states, and the relation between states. And in the specific condition (e.g., edge case 9999 secs), whether the program outputs properly or not. And I assigned an 1-bit signal variable `seg_disp_en` which represent the nixie tube is on/off, it helps me to check if the display flash at the required frequency.

1. **INITIAL STATE**

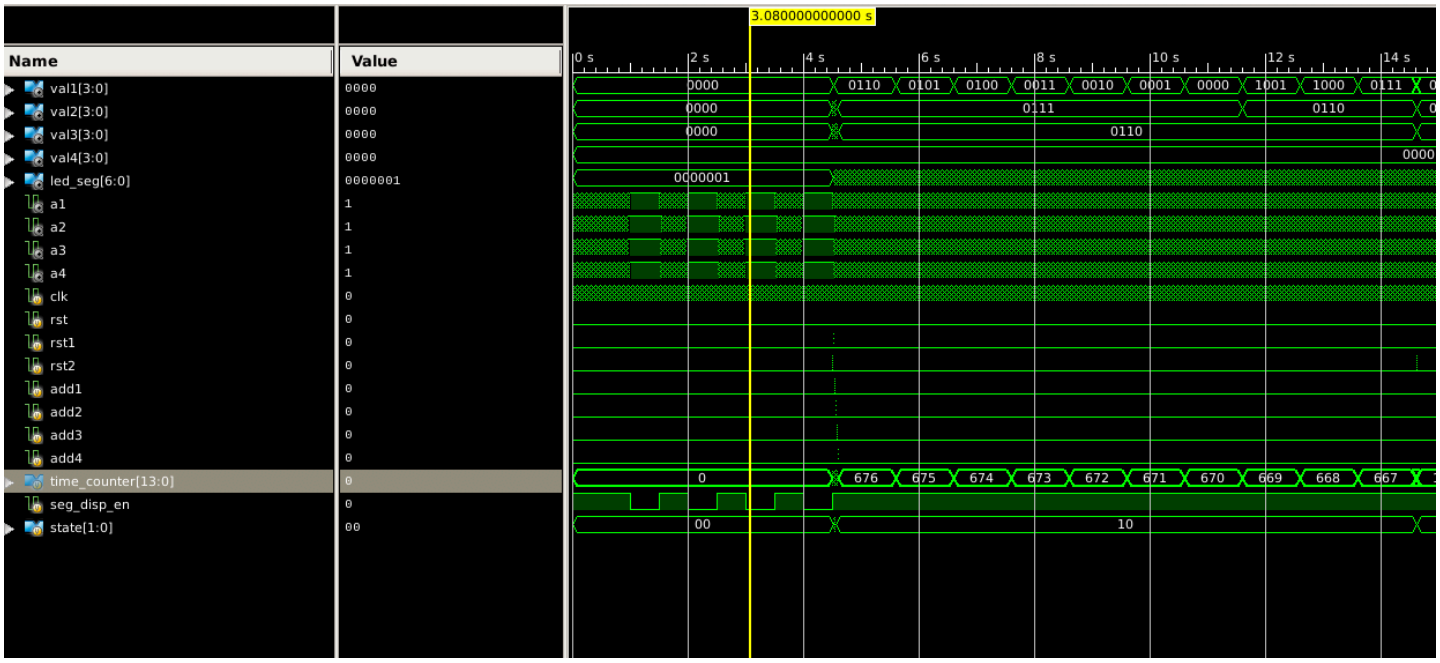
First, check the initial state, IDLE. Through the waveform below, when `rst` goes high, we can see that outputs from `val1` to `val4` all holds the value 0 when the state is in IDLE [2b'00]. And the remaining time is 0 (timer_counter = 0).



Then check if the display flash with period 1 sec and duty cycle 50%.

According to below waveform, nixel tube signal `seg_disp_en` is low (dark) for 0.5 sec and high (bright) for 0.5 sec. The result is as expected.

And the image also indicates that the value of `var1` to `val4` change when the state moves to another state from IDLE, and the value of `timer_counter` is also changed. This is also as expected.



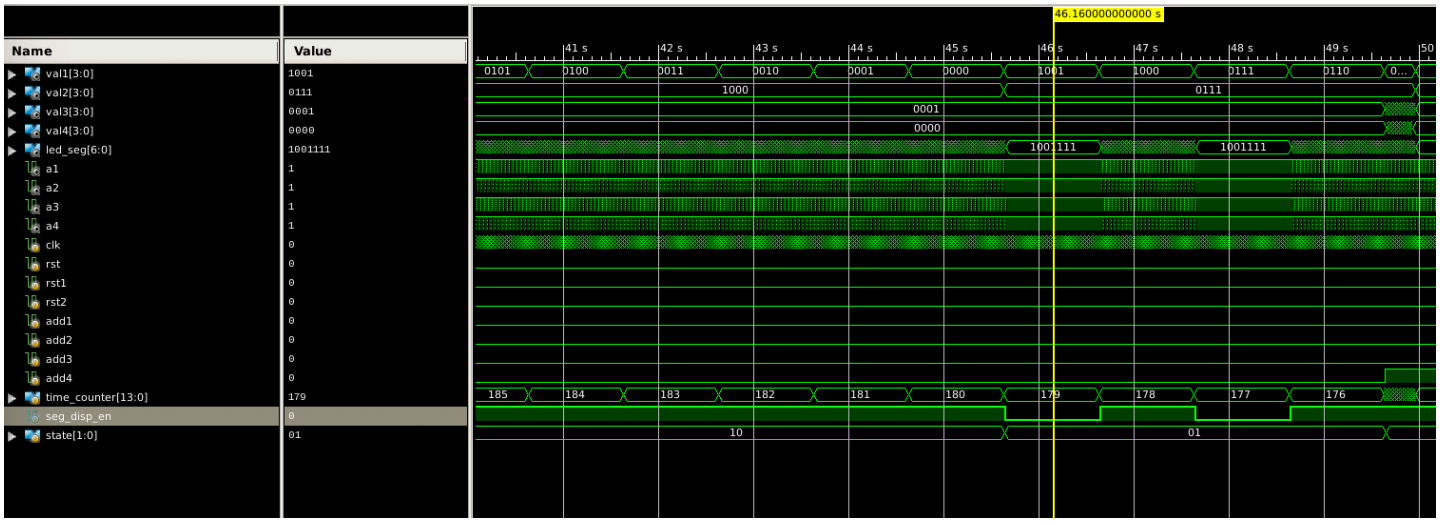
2. **Display even values but blank out odd values when timer < 180 sec**

The test case is to check the given required implementation in the spec. i.e., the logic in `low_180_s` state.

According the above image, when the `timer_counter` reachs 180 and start couting down, the state moves from `greater_180` [2b'10] to `low_180_s` [2b'01]. When the timer is at 179 and 177, all the one bit signals `a1` , `a2` , `a3` , `a4` are set to 1 (means dark), and the signal `seg_disp_en` which represents nixie tube goes low means it is dark.

When the `timer_counter` is at 180, 178 or 176, the signals `a1` , `a2` , `a3` , `a4` works as usual. And the the signal `seg_disp_en` which represents nixie tube goes high means it is bright.

The result is as expected.

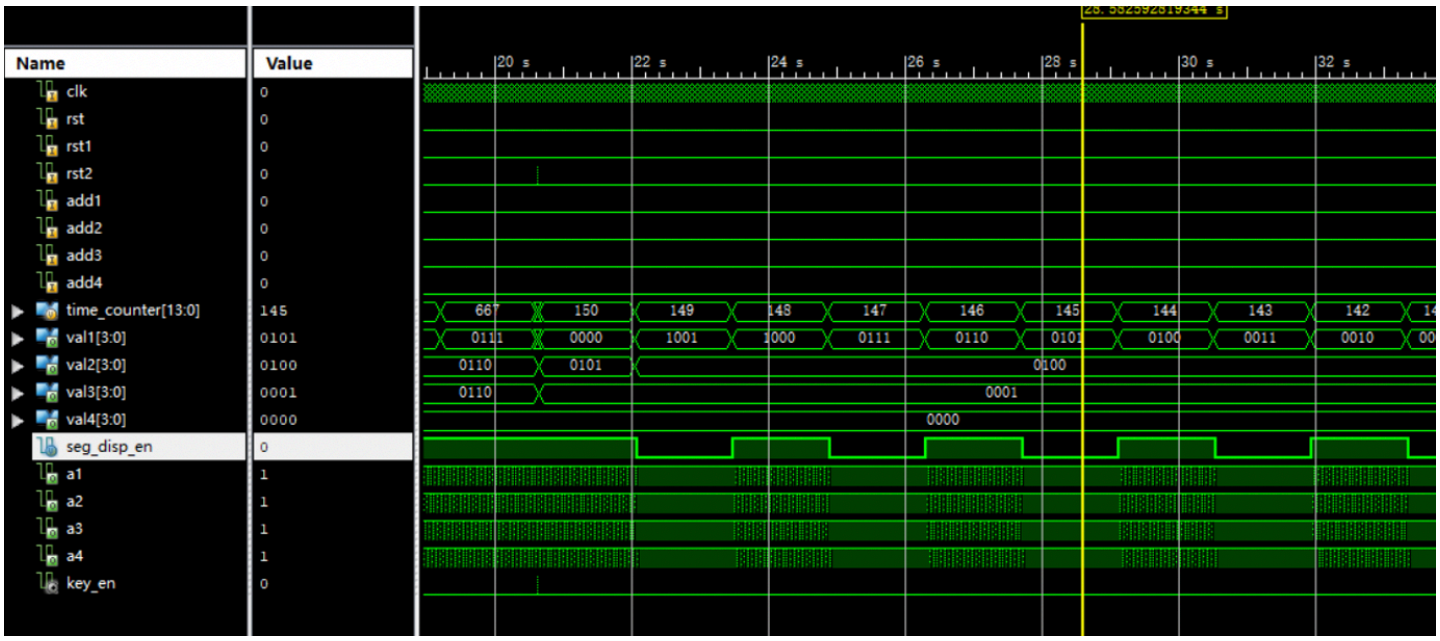


3. **Flash at 0.5 Hz when timer < 180 sec**

This test case is to test if the display would flash with a period of 2 secs and 50% duty cycle. (on for 1 sec and off for 1 sec).

As below image shown, when `rst2` goes high, the `timer_counter` is reset to 150 secs, which is smaller than 180. The the nixel tube signal `seg_disp_en` goes high (bright) for 1 sec, then it goes (dark) for 1 sec, and then goes high for 1 sec again and so on.

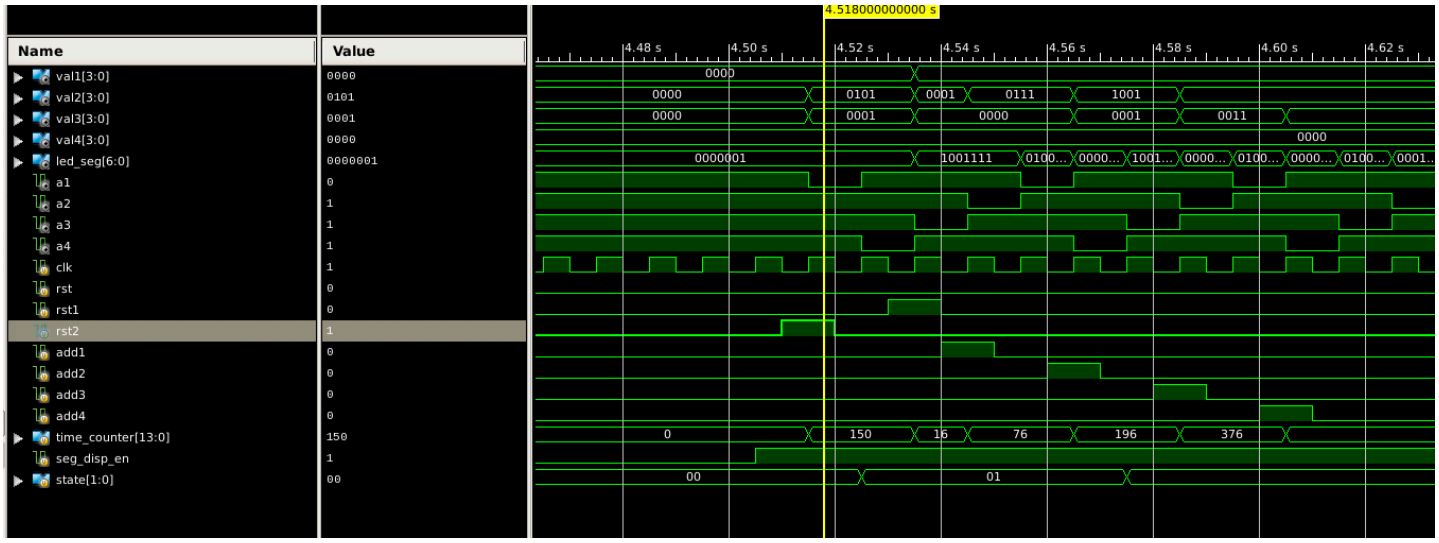
The result is as expected.



4. **`rst1` and `rst2` goes high**

This testcase is to check if the remaining time reset properly when rst1 and rst2 goes high and if the state moves the correspond state.

First check rst2. According the waveforms, when `rst2` goes high, the value `timer_counter` is reset to [8b'10010110] = 150, an the state is moved from `IDLE` to `low_180_s` as the reamining time changed, which is correct.



Then check `rst1` . According the below waveforms, when `rst1` goes high, the value `timer_counter` is reset to [5b'10000] = 16. And `timer_counter` start count down at 1hz.

The result is as expected.

5. **Test buttons of add**

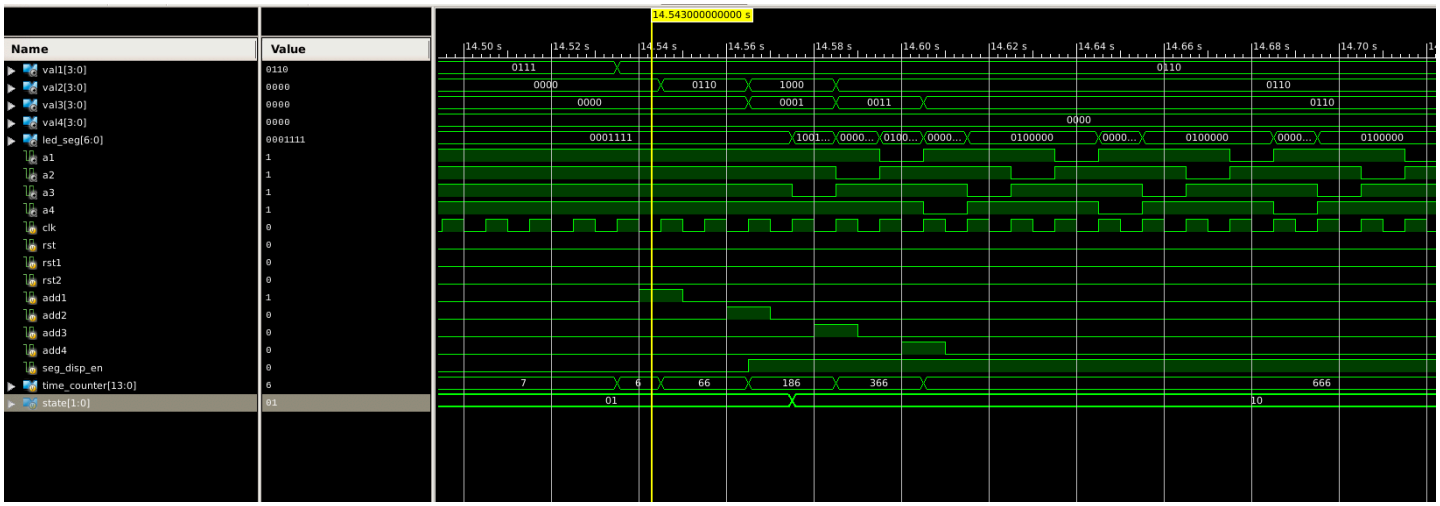
The initial value of the timer is 16, the test case is to test if the value of the timer could add the time correctly when press the different add button.

According to the below image, we could see when the timer value is 6,

- First, `add1` goes high, the timer adds 60 secs, the value is changed to 66.
- Then `add2` goes high, the timer adds 120 secs, the value is changed to 186.
- Then `add3` goes high, the timer adds 180 secs, the value is changed to 36.
- Then `add4` goes high, the timer adds 300 secs, the value is changed to 666.

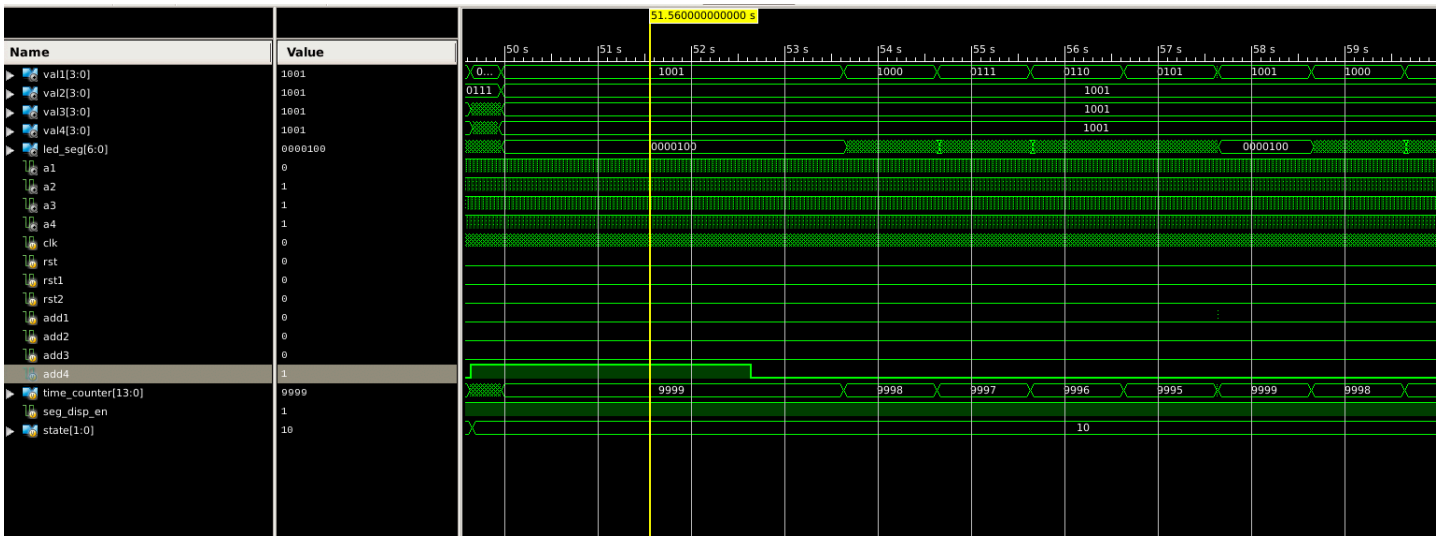
The display adds to the corresponding time when add button is pressed, and then starts counting down.

The result is as expected, the add buttons work.



6. **Max Value 9999**

The purpose of this test is to ensure that the amount of time remaining, stored in time_counter, cannot exceed 14'd9999, and any attempts to increase it beyond that value will result in it latching to 14'd9999. This was achieved by keeping `add4` high for a long period, thus ensuring that the time remaining reached 14'd9999, and then attempt to add more time in the timer.

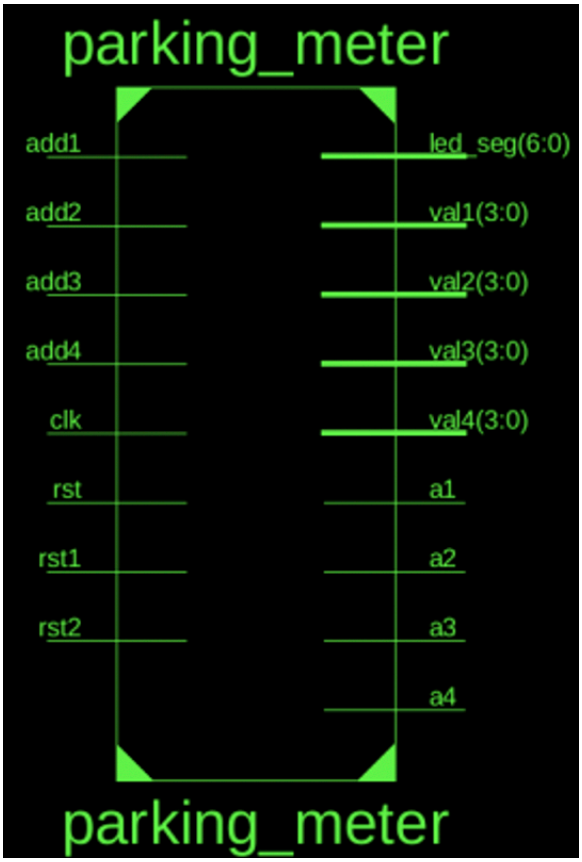


According to the above waveform, when the value of the timer has reached 9999, even if the `add4` is still high, the value of timer is latching to 9999. Then when `add4` reset to 0, the timer count down from 9999.

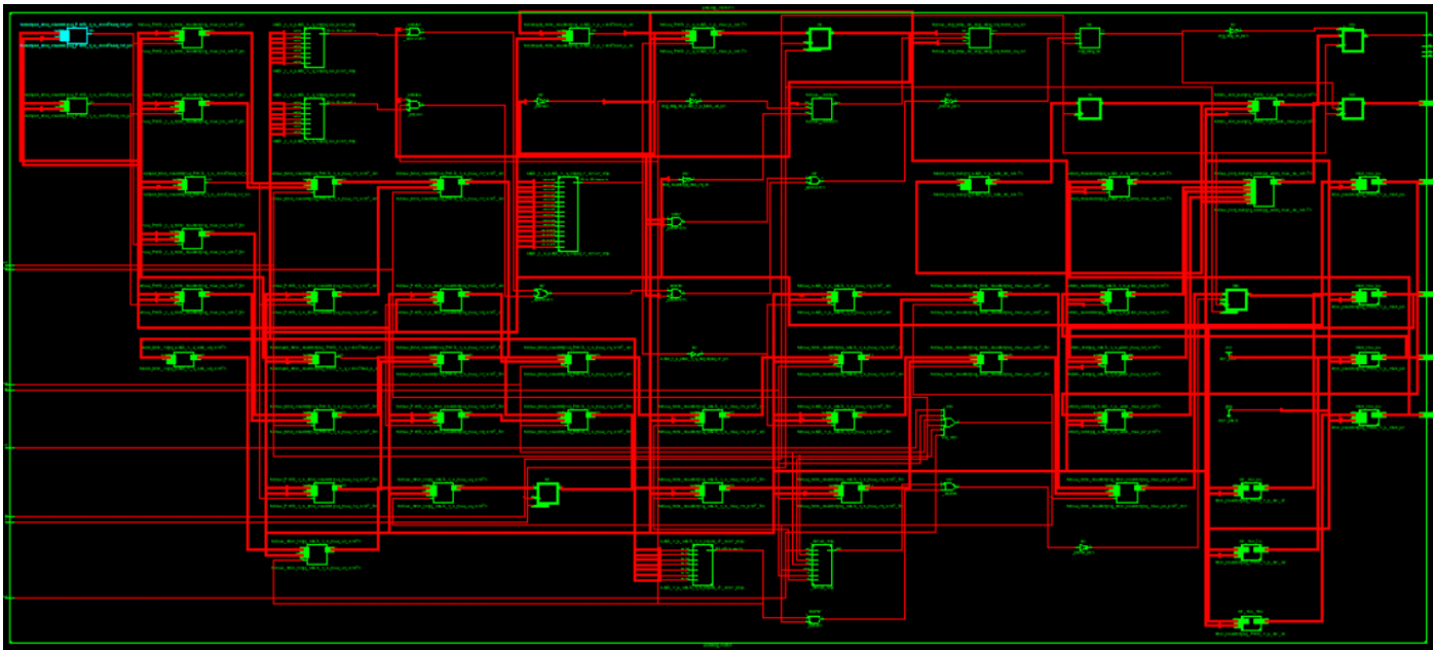
The result is as expected.

Schematics

The below image is the RTL generated from ISE. It indicate the I/O design of the module I designed.



Through the image, we know the I/O of the module `parking_meter` in my design is match with the input and output module required in this lab.



Briefly, we could see some vertically long rectangles with inputs, which represent the blocks taking in all bits of important large registers (e.g. `timer_counter`). This is important control block to control other different functions of the mudule.

Design Summary

Design Summary Report

parking_meter Project Status (06/06/2021 - 14:15:42)			
Project File:	Project4.xise	**Parser Errors:**	No Errors
Module Name:	parking_meter	**Implementation State:**	Placed and Routed
Target Device:	xc6slx16-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	7 Warnings (0 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	63	18,224	1%	
Number used as Flip Flops	63			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	667	9,112	7%	
Number used as logic	663	9,112	7%	
Number using O6 output only	622			
Number using O5 output only	1			
Number using O5 and O6	40			
Number used as ROM	0			

Implementation (Map) Report

```
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'parking_meter'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o parking_meter_map.ncd parking_meter.ngd
parking_meter.pcf
Target Device  : xc6slx16
Target Package : csg324
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun Jun  6 14:15:09 2021

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                    63 out of  18,224    1%
```

```
    Number used as Flip Flops:                63
    Number used as Latches:                    0
    Number used as Latch-thrus:                0
    Number used as AND/OR logics:              0
  Number of Slice LUTs:                      667 out of   9,112    7%
    Number used as logic:                    663 out of   9,112    7%
      Number using O6 output only:           622
      Number using O5 output only:             1
      Number using O5 and O6:                 40
      Number used as ROM:                      0
    Number used as Memory:                     0 out of   2,176    0%
    Number used exclusively as route-thrus:    4
      Number with same-slice register load:    3
      Number with same-slice carry load:       1
      Number with other load:                  0

Slice Logic Distribution:
  Number of occupied Slices:                 222 out of   2,278    9%
  Number of MUXCYs used:                      76 out of   4,556    1%
  Number of LUT Flip Flop pairs used:        678
    Number with an unused Flip Flop:         623 out of     678   91%
    Number with an unused LUT:                11 out of     678    1%
    Number of fully used LUT-FF pairs:        44 out of     678    6%
    Number of unique control sets:             5
    Number of slice register sites lost
      to control set restrictions:            17 out of  18,224    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                      35 out of     232   15%

Specific Feature Utilization:
  Number of RAMB16BWERs:                       0 out of      32    0%
  Number of RAMB8BWERs:                        0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:               0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:           0 out of      32    0%
  Number of BUFG/BUFGMUXs:                     1 out of      16    6%
    Number used as BUFGs:                      1
    Number used as BUFGMUX:                    0
  Number of DCM/DCM_CLKGENs:                   0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                 0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:       0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:                 0 out of     248    0%
```

```
    Number of BSCANs:                         0 out of       4    0%
    Number of BUFHs:                          0 out of     128    0%
    Number of BUFPLLs:                        0 out of       8    0%
    Number of BUFPLL_MCBs:                    0 out of       4    0%
    Number of DSP48A1s:                       0 out of      32    0%
    Number of ICAPs:                          0 out of       1    0%
    Number of MCBs:                           0 out of       2    0%
    Number of PCILOGICSEs:                    0 out of       2    0%
    Number of PLL_ADVs:                       0 out of       2    0%
    Number of PMVs:                           0 out of       1    0%
    Number of STARTUPs:                       0 out of       1    0%
    Number of SUSPEND_SYNCs:                  0 out of       1    0%

  Average Fanout of Non-Clock Nets:                5.06

  Peak Memory Usage:  771 MB
  Total REAL time to MAP completion:  15 secs
  Total CPU time to MAP completion:   14 secs

  Table of Contents
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  Section 2 - Warnings
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  Section 8 - Guide Report
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  Section 10 - Timing Report
  Section 11 - Configuration String Information
  Section 12 - Control Set Information
  Section 13 - Utilization by Hierarchy

  Section 1 - Errors
  ------------------

  Section 2 - Warnings
  --------------------

  Section 3 - Informational
  -------------------------
  INFO:MapLib:562 - No environment variables are currently set.
  INFO:LIT:244 - All of the single ended outputs in this design are using slew
     rate limited output drivers. The delay on speed critical single ended outputs
     can be dramatically reduced by designating them as fast outputs.
  INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
```

```
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
---------------------------------
   2 block(s) optimized away

Section 5 - Removed Logic
-------------------------

Optimized Block(s):
TYPE    BLOCK
GND     XST_GND
VCC     XST_VCC

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties
--------------------------

+-----------------------------------------------------------------------------------------------
-------------------------------------------------------------+
| IOB Name                           | Type             | Direction | IO Standard          |
Diff  | Drive    | Slew | Reg (s)      | Resistor | IOB      |
|                                    |                  |           |                      |
Term  | Strength | Rate |              |          | Delay    |
+-----------------------------------------------------------------------------------------------
-------------------------------------------------------------+
| a1                                 | IOB              | OUTPUT    | LVCMOS25             |
      | 12       | SLOW |              |          |          |
| a2                                 | IOB              | OUTPUT    | LVCMOS25             |
      | 12       | SLOW |              |          |          |
| a3                                 | IOB              | OUTPUT    | LVCMOS25             |
      | 12       | SLOW |              |          |          |
| a4                                 | IOB              | OUTPUT    | LVCMOS25             |
      | 12       | SLOW |              |          |          |
| add1                               | IOB              | INPUT     | LVCMOS25             |
      |          |      |              |          |          |
| add2                               | IOB              | INPUT     | LVCMOS25             |
      |          |      |              |          |          |
| add3                               | IOB              | INPUT     | LVCMOS25             |
      |          |      |              |          |          |
```

```
154 | add4                                | IOB              | INPUT     | LVCMOS25             |
          |          |      |              |          |          |
155 | clk                                 | IOB              | INPUT     | LVCMOS25             |
          |          |      |              |          |          |
156 | led_seg<0>                          | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
157 | led_seg<1>                          | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
158 | led_seg<2>                          | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
159 | led_seg<3>                          | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
160 | led_seg<4>                          | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
161 | led_seg<5>                          | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
162 | led_seg<6>                          | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
163 | rst                                 | IOB              | INPUT     | LVCMOS25             |
          |          |      |              |          |          |
164 | rst1                                | IOB              | INPUT     | LVCMOS25             |
          |          |      |              |          |          |
165 | rst2                                | IOB              | INPUT     | LVCMOS25             |
          |          |      |              |          |          |
166 | val1<0>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
167 | val1<1>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
168 | val1<2>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
169 | val1<3>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
170 | val2<0>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
171 | val2<1>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
172 | val2<2>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
173 | val2<3>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
174 | val3<0>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
175 | val3<1>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
176 | val3<2>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
177 | val3<3>                             | IOB              | OUTPUT    | LVCMOS25             |
          | 12       | SLOW |              |          |          |
```

```
| val4<0>                          | IOB              | OUTPUT    | LVCMOS25            |
      | 12       | SLOW |              |          |          |
| val4<1>                          | IOB              | OUTPUT    | LVCMOS25            |
      | 12       | SLOW |              |          |          |
| val4<2>                          | IOB              | OUTPUT    | LVCMOS25            |
      | 12       | SLOW |              |          |          |
| val4<3>                          | IOB              | OUTPUT    | LVCMOS25            |
      | 12       | SLOW |              |          |          |
+-------------------------------------------------------------------------------------------
-------------------------------------------------------------+

Section 7 - RPMs
----------------

Section 8 - Guide Report
------------------------
Guide not run on this design.

Section 9 - Area Group and Partition Summary
--------------------------------------------

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

Area Group Information
----------------------

  No area groups were found in this design.

----------------------

Section 10 - Timing Report
--------------------------
A logic-level (pre-route) timing report can be generated by using Xilinx static
timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the
mapped NCD and PCF files. Please note that this timing report will be generated
using estimated delay information. For accurate numbers, please generate a
timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing
Analyzer Reference Manual; for more information about TRCE, consult the Xilinx
Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details
```

```
---------------------------------------
Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information
------------------------------------
Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy
-------------------------------------
Use the "-detail" map option to print out the Utilization by Hierarchy section.

```

Synthese Report

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Reading design: parking_meter.prj

TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
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       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
```

```
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "parking_meter.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "parking_meter"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : parking_meter
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
```

```
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/ise/152A/Project4/parking_meter.v" into library work
Parsing module <parking_meter>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <parking_meter>.
WARNING:HDLCompiler:413 - "/home/ise/152A/Project4/parking_meter.v" Line 89: Result of 15-bit expression is truncated to fit in 14-bit target.
WARNING:HDLCompiler:413 - "/home/ise/152A/Project4/parking_meter.v" Line 96: Result of 15-bit expression is truncated to fit in 14-bit target.
WARNING:HDLCompiler:413 - "/home/ise/152A/Project4/parking_meter.v" Line 103: Result of 15-bit expression is truncated to fit in 14-bit target.
WARNING:HDLCompiler:413 - "/home/ise/152A/Project4/parking_meter.v" Line 110: Result of 15-bit expression is truncated to fit in 14-bit target.
WARNING:HDLCompiler:413 - "/home/ise/152A/Project4/parking_meter.v" Line 121: Result of 32-bit expression is truncated to fit in 14-bit target.
WARNING:HDLCompiler:413 - "/home/ise/152A/Project4/parking_meter.v" Line 126: Result of 8-bit expression is truncated to fit in 7-bit target.
```

```
WARNING:HDLCompiler:413 - "/home/ise/152A/Project4/parking_meter.v" Line 178: Result of 3-bit expression is truncated to fit in 2-bit target.

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <parking_meter>.
    Related source file is "/home/ise/152A/Project4/parking_meter.v".
        idle = 2'b00
        low_180_s = 2'b01
        grater_180 = 2'b10
    Found 14-bit register for signal <time_counter>.
    Found 7-bit register for signal <time_1s>.
    Found 1-bit register for signal <seg_disp_en>.
    Found 2-bit register for signal <sen_num>.
    Found 4-bit register for signal <an>.
    Found 7-bit register for signal <led_seg>.
    Found 2-bit register for signal <state>.
    Found 14-bit adder for signal <time_counter[13]_GND_1_o_add_9_OUT> created at line 89.
    Found 14-bit adder for signal <time_counter[13]_GND_1_o_add_12_OUT> created at line 96.
    Found 14-bit adder for signal <time_counter[13]_GND_1_o_add_15_OUT> created at line 103.
    Found 14-bit adder for signal <time_counter[13]_GND_1_o_add_18_OUT> created at line 110.
    Found 7-bit adder for signal <time_1s[6]_GND_1_o_add_30_OUT> created at line 126.
    Found 2-bit adder for signal <sen_num[1]_GND_1_o_add_58_OUT> created at line 178.
    Found 14-bit subtractor for signal <GND_1_o_GND_1_o_sub_29_OUT<13:0>> created at line 121.
    Found 16x7-bit Read Only RAM for signal <thousands[3]_GND_1_o_wide_mux_59_OUT>
    Found 16x7-bit Read Only RAM for signal <hundreds[3]_GND_1_o_wide_mux_60_OUT>
    Found 16x7-bit Read Only RAM for signal <tens[3]_GND_1_o_wide_mux_61_OUT>
    Found 16x7-bit Read Only RAM for signal <ones[3]_GND_1_o_wide_mux_62_OUT>
    Found 4x4-bit Read Only RAM for signal <sen_num[1]_PWR_1_o_wide_mux_63_OUT>
    Found 7-bit 4-to-1 multiplexer for signal <sen_num[1]_ones[3]_wide_mux_64_OUT> created at line 181.
    Found 14-bit comparator greater for signal <time_counter[13]_GND_1_o_LessThan_3_o> created at line 64
    Found 14-bit comparator lessequal for signal <n0011> created at line 88
    Found 14-bit comparator lessequal for signal <n0015> created at line 95
    Found 14-bit comparator lessequal for signal <n0019> created at line 102
    Found 14-bit comparator lessequal for signal <n0023> created at line 109
    Summary:
  inferred   5 RAM(s).
  inferred   3 Adder/Subtractor(s).
  inferred  37 D-type flip-flop(s).
  inferred   5 Comparator(s).
  inferred  28 Multiplexer(s).
Unit <parking_meter> synthesized.

```

```
Synthesizing Unit <mod_14u_4u>.
    Related source file is "".
    Found 18-bit adder for signal <n0565> created at line 0.
    Found 18-bit adder for signal <GND_2_o_b[3]_add_1_OUT> created at line 0.
    Found 17-bit adder for signal <n0569> created at line 0.
    Found 17-bit adder for signal <GND_2_o_b[3]_add_3_OUT> created at line 0.
    Found 16-bit adder for signal <n0573> created at line 0.
    Found 16-bit adder for signal <GND_2_o_b[3]_add_5_OUT> created at line 0.
    Found 15-bit adder for signal <n0577> created at line 0.
    Found 15-bit adder for signal <GND_2_o_b[3]_add_7_OUT> created at line 0.
    Found 14-bit adder for signal <n0581> created at line 0.
    Found 14-bit adder for signal <a[13]_b[3]_add_9_OUT> created at line 0.
    Found 14-bit adder for signal <n0585> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_11_OUT> created at line 0.
    Found 14-bit adder for signal <n0589> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_13_OUT> created at line 0.
    Found 14-bit adder for signal <n0593> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_15_OUT> created at line 0.
    Found 14-bit adder for signal <n0597> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_17_OUT> created at line 0.
    Found 14-bit adder for signal <n0601> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_19_OUT> created at line 0.
    Found 14-bit adder for signal <n0605> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_21_OUT> created at line 0.
    Found 14-bit adder for signal <n0609> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_23_OUT> created at line 0.
    Found 14-bit adder for signal <n0613> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_25_OUT> created at line 0.
    Found 14-bit adder for signal <n0617> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_27_OUT> created at line 0.
    Found 14-bit adder for signal <n0621> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_2_o_add_29_OUT> created at line 0.
    Found 18-bit comparator lessequal for signal <BUS_0001> created at line 0
    Found 17-bit comparator lessequal for signal <BUS_0002> created at line 0
    Found 16-bit comparator lessequal for signal <BUS_0003> created at line 0
    Found 15-bit comparator lessequal for signal <BUS_0004> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0005> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0006> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0007> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0008> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0009> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0010> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0011> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0012> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0013> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0014> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0015> created at line 0
    Summary:
```

```
    inferred  30 Adder/Subtractor(s).
    inferred  15 Comparator(s).
    inferred 197 Multiplexer(s).
Unit <mod_14u_4u> synthesized.

Synthesizing Unit <div_14u_4u>.
    Related source file is "".
    Found 18-bit adder for signal <GND_3_o_b[3]_add_1_OUT> created at line 0.
    Found 17-bit adder for signal <GND_3_o_b[3]_add_3_OUT> created at line 0.
    Found 16-bit adder for signal <GND_3_o_b[3]_add_5_OUT> created at line 0.
    Found 15-bit adder for signal <GND_3_o_b[3]_add_7_OUT> created at line 0.
    Found 14-bit adder for signal <a[13]_b[3]_add_9_OUT> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_11_OUT> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_13_OUT> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_15_OUT> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_17_OUT> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_19_OUT> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_21_OUT> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_23_OUT[13:0]> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_25_OUT[13:0]> created at line 0.
    Found 14-bit adder for signal <a[13]_GND_3_o_add_27_OUT[13:0]> created at line 0.
    Found 18-bit comparator lessequal for signal <BUS_0001> created at line 0
    Found 17-bit comparator lessequal for signal <BUS_0002> created at line 0
    Found 16-bit comparator lessequal for signal <BUS_0003> created at line 0
    Found 15-bit comparator lessequal for signal <BUS_0004> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0005> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0006> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0007> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0008> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0009> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0010> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0011> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0012> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0013> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0014> created at line 0
    Found 14-bit comparator lessequal for signal <BUS_0015> created at line 0
    Summary:
  inferred  14 Adder/Subtractor(s).
  inferred  15 Comparator(s).
  inferred 157 Multiplexer(s).
Unit <div_14u_4u> synthesized.

Synthesizing Unit <div_14u_7u>.
    Related source file is "".
    Found 21-bit adder for signal <GND_4_o_b[6]_add_1_OUT> created at line 0.
    Found 20-bit adder for signal <GND_4_o_b[6]_add_3_OUT> created at line 0.
    Found 19-bit adder for signal <GND_4_o_b[6]_add_5_OUT> created at line 0.
    Found 18-bit adder for signal <GND_4_o_b[6]_add_7_OUT> created at line 0.
```

```
265       Found 17-bit adder for signal <GND_4_o_b[6]_add_9_OUT> created at line 0.
266       Found 16-bit adder for signal <GND_4_o_b[6]_add_11_OUT> created at line 0.
267       Found 15-bit adder for signal <GND_4_o_b[6]_add_13_OUT> created at line 0.
268       Found 14-bit adder for signal <a[13]_b[6]_add_15_OUT> created at line 0.
269       Found 14-bit adder for signal <a[13]_GND_4_o_add_17_OUT> created at line 0.
270       Found 14-bit adder for signal <a[13]_GND_4_o_add_19_OUT> created at line 0.
271       Found 14-bit adder for signal <a[13]_GND_4_o_add_21_OUT> created at line 0.
272       Found 14-bit adder for signal <a[13]_GND_4_o_add_23_OUT[13:0]> created at line 0.
273       Found 14-bit adder for signal <a[13]_GND_4_o_add_25_OUT[13:0]> created at line 0.
274       Found 14-bit adder for signal <a[13]_GND_4_o_add_27_OUT[13:0]> created at line 0.
275       Found 21-bit comparator lessequal for signal <BUS_0001> created at line 0
276       Found 20-bit comparator lessequal for signal <BUS_0002> created at line 0
277       Found 19-bit comparator lessequal for signal <BUS_0003> created at line 0
278       Found 18-bit comparator lessequal for signal <BUS_0004> created at line 0
279       Found 17-bit comparator lessequal for signal <BUS_0005> created at line 0
280       Found 16-bit comparator lessequal for signal <BUS_0006> created at line 0
281       Found 15-bit comparator lessequal for signal <BUS_0007> created at line 0
282       Found 14-bit comparator lessequal for signal <BUS_0008> created at line 0
283       Found 14-bit comparator lessequal for signal <BUS_0009> created at line 0
284       Found 14-bit comparator lessequal for signal <BUS_0010> created at line 0
285       Found 14-bit comparator lessequal for signal <BUS_0011> created at line 0
286       Found 14-bit comparator lessequal for signal <BUS_0012> created at line 0
287       Found 14-bit comparator lessequal for signal <BUS_0013> created at line 0
288       Found 14-bit comparator lessequal for signal <BUS_0014> created at line 0
289       Found 14-bit comparator lessequal for signal <BUS_0015> created at line 0
290       Summary:
291     inferred  14 Adder/Subtractor(s).
292     inferred  15 Comparator(s).
293     inferred 157 Multiplexer(s).
294   Unit <div_14u_7u> synthesized.
295
296   Synthesizing Unit <div_14u_10u>.
297       Related source file is "".
298       Found 24-bit adder for signal <GND_5_o_b[9]_add_1_OUT> created at line 0.
299       Found 23-bit adder for signal <GND_5_o_b[9]_add_3_OUT> created at line 0.
300       Found 22-bit adder for signal <GND_5_o_b[9]_add_5_OUT> created at line 0.
301       Found 21-bit adder for signal <GND_5_o_b[9]_add_7_OUT> created at line 0.
302       Found 20-bit adder for signal <GND_5_o_b[9]_add_9_OUT> created at line 0.
303       Found 19-bit adder for signal <GND_5_o_b[9]_add_11_OUT> created at line 0.
304       Found 18-bit adder for signal <GND_5_o_b[9]_add_13_OUT> created at line 0.
305       Found 17-bit adder for signal <GND_5_o_b[9]_add_15_OUT> created at line 0.
306       Found 16-bit adder for signal <GND_5_o_b[9]_add_17_OUT> created at line 0.
307       Found 15-bit adder for signal <GND_5_o_b[9]_add_19_OUT> created at line 0.
308       Found 14-bit adder for signal <a[13]_b[9]_add_21_OUT> created at line 0.
309       Found 14-bit adder for signal <a[13]_GND_5_o_add_23_OUT[13:0]> created at line 0.
310       Found 14-bit adder for signal <a[13]_GND_5_o_add_25_OUT[13:0]> created at line 0.
311       Found 14-bit adder for signal <a[13]_GND_5_o_add_27_OUT[13:0]> created at line 0.
312       Found 24-bit comparator lessequal for signal <BUS_0001> created at line 0
```

```
313       Found 23-bit comparator lessequal for signal <BUS_0002> created at line 0
314       Found 22-bit comparator lessequal for signal <BUS_0003> created at line 0
315       Found 21-bit comparator lessequal for signal <BUS_0004> created at line 0
316       Found 20-bit comparator lessequal for signal <BUS_0005> created at line 0
317       Found 19-bit comparator lessequal for signal <BUS_0006> created at line 0
318       Found 18-bit comparator lessequal for signal <BUS_0007> created at line 0
319       Found 17-bit comparator lessequal for signal <BUS_0008> created at line 0
320       Found 16-bit comparator lessequal for signal <BUS_0009> created at line 0
321       Found 15-bit comparator lessequal for signal <BUS_0010> created at line 0
322       Found 14-bit comparator lessequal for signal <BUS_0011> created at line 0
323       Found 14-bit comparator lessequal for signal <BUS_0012> created at line 0
324       Found 14-bit comparator lessequal for signal <BUS_0013> created at line 0
325       Found 14-bit comparator lessequal for signal <BUS_0014> created at line 0
326       Found 14-bit comparator lessequal for signal <BUS_0015> created at line 0
327       Summary:
328     inferred  14 Adder/Subtractor(s).
329     inferred  15 Comparator(s).
330     inferred 157 Multiplexer(s).
331   Unit <div_14u_10u> synthesized.
332
333   =========================================================================
334   HDL Synthesis Report
335
336   Macro Statistics
337   # RAMs                                                : 5
338    16x7-bit single-port Read Only RAM                  : 4
339    4x4-bit single-port Read Only RAM                   : 1
340   # Adders/Subtractors                                  : 165
341    14-bit adder                                        : 109
342    14-bit addsub                                       : 1
343    15-bit adder                                        : 11
344    16-bit adder                                        : 11
345    17-bit adder                                        : 11
346    18-bit adder                                        : 11
347    19-bit adder                                        : 2
348    2-bit adder                                         : 1
349    20-bit adder                                        : 2
350    21-bit adder                                        : 2
351    22-bit adder                                        : 1
352    23-bit adder                                        : 1
353    24-bit adder                                        : 1
354    7-bit adder                                         : 1
355   # Registers                                           : 7
356    1-bit register                                      : 1
357    14-bit register                                     : 1
358    2-bit register                                      : 2
359    4-bit register                                      : 1
360    7-bit register                                      : 2
```

```
# Comparators                                          : 110
 14-bit comparator greater                             : 1
 14-bit comparator lessequal                           : 72
 15-bit comparator lessequal                           : 7
 16-bit comparator lessequal                           : 7
 17-bit comparator lessequal                           : 7
 18-bit comparator lessequal                           : 7
 19-bit comparator lessequal                           : 2
 20-bit comparator lessequal                           : 2
 21-bit comparator lessequal                           : 2
 22-bit comparator lessequal                           : 1
 23-bit comparator lessequal                           : 1
 24-bit comparator lessequal                           : 1
# Multiplexers                                         : 1287
 1-bit 2-to-1 multiplexer                              : 1248
 14-bit 2-to-1 multiplexer                             : 31
 2-bit 2-to-1 multiplexer                              : 1
 4-bit 2-to-1 multiplexer                              : 4
 7-bit 2-to-1 multiplexer                              : 2
 7-bit 4-to-1 multiplexer                              : 1

=========================================================================
INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic
operations in this design can share the same physical resources for reduced device
utilization. For improved clock frequency you may try to disable resource sharing.

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


Synthesizing (advanced) Unit <parking_meter>.
The following registers are absorbed into counter <sen_num>: 1 register on signal <sen_num>.
INFO:Xst:3231 - The small RAM <Mram_sen_num[1]_PWR_1_o_wide_mux_63_OUT> will be implemented
on LUTs in order to maximize performance and save block RAM resources. If you want to force
its implementation on block, use option/constraint ram_style.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 4-word x 4-bit                      |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <sen_num>       |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    -----------------------------------------------------------------------
```

```
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_ones[3]_GND_1_o_wide_mux_62_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 16-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <val1>          |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_tens[3]_GND_1_o_wide_mux_61_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 16-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <val2>          |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_hundreds[3]_GND_1_o_wide_mux_60_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 16-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <val3>          |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    -----------------------------------------------------------------------
```

```
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_thousands[3]_GND_1_o_wide_mux_59_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 16-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <val4>          |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    -----------------------------------------------------------------------
Unit <parking_meter> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 5
 16x7-bit single-port distributed Read Only RAM        : 4
 4x4-bit single-port distributed Read Only RAM         : 1
# Adders/Subtractors                                   : 104
 14-bit adder                                          : 42
 14-bit adder carry in                                 : 56
 14-bit addsub                                         : 1
 4-bit adder carry in                                  : 4
 7-bit adder                                           : 1
# Counters                                             : 1
 2-bit up counter                                      : 1
# Registers                                            : 35
 Flip-Flops                                            : 35
# Comparators                                          : 110
 14-bit comparator greater                             : 1
 14-bit comparator lessequal                           : 72
 15-bit comparator lessequal                           : 7
 16-bit comparator lessequal                           : 7
 17-bit comparator lessequal                           : 7
 18-bit comparator lessequal                           : 7
 19-bit comparator lessequal                           : 2
 20-bit comparator lessequal                           : 2
 21-bit comparator lessequal                           : 2
 22-bit comparator lessequal                           : 1
 23-bit comparator lessequal                           : 1
 24-bit comparator lessequal                           : 1
```

```
# Multiplexers                                        : 1287
 1-bit 2-to-1 multiplexer                             : 1248
 14-bit 2-to-1 multiplexer                            : 31
 2-bit 2-to-1 multiplexer                             : 1
 4-bit 2-to-1 multiplexer                             : 4
 7-bit 2-to-1 multiplexer                             : 2
 7-bit 4-to-1 multiplexer                             : 1

=========================================================================

=========================================================================
*                        Low Level Synthesis                            *
=========================================================================

Optimizing unit <parking_meter> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block parking_meter, actual ratio is 6.
FlipFlop time_counter_10 has been replicated 4 time(s)
FlipFlop time_counter_11 has been replicated 3 time(s)
FlipFlop time_counter_12 has been replicated 3 time(s)
FlipFlop time_counter_13 has been replicated 3 time(s)
FlipFlop time_counter_6 has been replicated 2 time(s)
FlipFlop time_counter_7 has been replicated 2 time(s)
FlipFlop time_counter_8 has been replicated 5 time(s)
FlipFlop time_counter_9 has been replicated 4 time(s)

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 63
 Flip-Flops                                          : 63

=========================================================================

=========================================================================
*                          Partition Report                             *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

```

```
------------------------------

=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : parking_meter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 842
#      GND                         : 1
#      INV                         : 2
#      LUT1                        : 1
#      LUT2                        : 20
#      LUT3                        : 35
#      LUT4                        : 42
#      LUT5                        : 162
#      LUT6                        : 413
#      MUXCY                       : 68
#      MUXF7                       : 23
#      VCC                         : 1
#      XORCY                       : 74
# FlipFlops/Latches                : 63
#      FD                          : 6
#      FDE                         : 8
#      FDR                         : 9
#      FDRE                        : 40
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 34
#      IBUF                        : 7
#      OBUF                        : 27

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:             63  out of  18224     0%
 Number of Slice LUTs:                 675  out of   9112     7%
    Number used as Logic:              675  out of   9112     7%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    708
   Number with an unused Flip Flop:     645  out of    708    91%
```

```
    Number with an unused LUT:             33  out of    708     4%
    Number of fully used LUT-FF pairs:     30  out of    708     4%
    Number of unique control sets:          5

IO Utilization:
 Number of IOs:                            35
 Number of bonded IOBs:                    35  out of    232    15%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                  1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=================================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 63    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 17.318ns (Maximum Frequency: 57.745MHz)
   Minimum input arrival time before clock: 6.654ns
   Maximum output required time after clock: 17.876ns
   Maximum combinational path delay: No path found
```

```
Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 17.318ns (frequency: 57.745MHz)
  Total number of paths / destination ports: 275345894 / 111
-------------------------------------------------------------------------
Delay:               17.318ns (Levels of Logic = 16)
  Source:            time_counter_13_1 (FF)
  Destination:       led_seg_3 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: time_counter_13_1 to led_seg_3
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q            10   0.447   1.104  time_counter_13_1 (time_counter_13_1)
     LUT5:I1->O            2   0.203   0.845
 time_counter[13]_PWR_1_o_div_47/Madd_a[13]_GND_3_o_add_15_OUT_lut<10>1
(time_counter[13]_PWR_1_o_div_47/Madd_a[13]_GND_3_o_add_15_OUT_lut<10>)
     LUT6:I3->O           11   0.205   0.987
 time_counter[13]_PWR_1_o_div_47/Mmux_a[0]_a[13]_MUX_479_o1211_SW1 (N301)
     LUT6:I4->O            1   0.203   0.580  time_counter[13]_PWR_1_o_div_47_OUT<5>1_SW4
(N326)
     LUT6:I5->O           10   0.205   0.961
 time_counter[13]_PWR_1_o_div_47/Mmux_a[0]_a[13]_MUX_493_o1141
(time_counter[13]_PWR_1_o_div_47/Mmux_a[0]_a[13]_MUX_493_o114)
     LUT6:I4->O            5   0.203   1.059  time_counter[13]_PWR_1_o_div_47_OUT<4>1_1
(time_counter[13]_PWR_1_o_div_47_OUT<4>1)
     LUT6:I1->O           18   0.203   1.050
 time_counter[13]_PWR_1_o_mod_48/BUS_0012_INV_196_o11
(time_counter[13]_PWR_1_o_mod_48/BUS_0012_INV_196_o)
     LUT6:I5->O           15   0.205   0.982
 time_counter[13]_PWR_1_o_mod_48/Madd_a[13]_GND_2_o_add_25_OUT_Madd_cy<4>11
(time_counter[13]_PWR_1_o_mod_48/Madd_a[13]_GND_2_o_add_25_OUT_Madd_cy<4>)
     LUT6:I5->O           11   0.205   0.883
 time_counter[13]_PWR_1_o_mod_48/BUS_0013_INV_211_o1
(time_counter[13]_PWR_1_o_mod_48/BUS_0013_INV_211_o)
     LUT3:I2->O            2   0.205   0.721
 time_counter[13]_PWR_1_o_mod_48/Mmux_a[9]_a[13]_MUX_292_o11
(time_counter[13]_PWR_1_o_mod_48/a[9]_a[13]_MUX_292_o)
     LUT6:I4->O            1   0.203   0.580
 time_counter[13]_PWR_1_o_mod_48/BUS_0014_INV_226_o13_SW1 (N684)
```

```
653         LUT6:I5->O            8   0.205   0.803
     time_counter[13]_PWR_1_o_mod_48/BUS_0014_INV_226_o13
    (time_counter[13]_PWR_1_o_mod_48/BUS_0014_INV_226_o)
654         LUT6:I5->O            1   0.205   0.580
     time_counter[13]_PWR_1_o_mod_48/Madd_a[13]_GND_2_o_add_29_OUT_Madd_Madd_cy<2>11
    (time_counter[13]_PWR_1_o_mod_48/Madd_a[13]_GND_2_o_add_29_OUT_Madd_Madd_cy<2>)
655         LUT6:I5->O           10   0.205   1.104  time_counter[13]_PWR_1_o_mod_48/Mmux_o41
    (val2_3_OBUF)
656         LUT5:I1->O            1   0.203   0.580
     Mmux_sen_num[1]_ones[3]_wide_mux_64_OUT41_SW2_SW0 (N559)
657         LUT6:I5->O            1   0.205   0.684  Mmux_sen_num[1]_ones[3]_wide_mux_64_OUT41_SW2
    (N484)
658         LUT6:I4->O            1   0.203   0.000  Mmux_sen_num[1]_ones[3]_wide_mux_64_OUT44
    (sen_num[1]_ones[3]_wide_mux_64_OUT<3>)
659         FDE:D                     0.102          led_seg_3
660        ----------------------------------------
661        Total                     17.318ns (3.815ns logic, 13.503ns route)
662                                        (22.0% logic, 78.0% route)
663
664   ==========================================================================
665   Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
666     Total number of paths / destination ports: 9836 / 136
667   --------------------------------------------------------------------------
668   Offset:              6.654ns (Levels of Logic = 10)
669     Source:            rst1 (PAD)
670     Destination:       time_counter_13 (FF)
671     Destination Clock: clk rising
672
673     Data Path: rst1 to time_counter_13
674                                   Gate     Net
675       Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
676       ----------------------------------------  ------------
677        IBUF:I->O            34   1.222   1.685  rst1_IBUF (rst1_IBUF)
678        LUT6:I0->O           34   0.203   1.665  key_en1 (key_en)
679        LUT5:I0->O            1   0.203   0.944
     Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_A261
    (Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_A<8>)
680         LUT6:I0->O            1   0.203   0.000
     Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_lut<8>
    (Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_lut<8>)
681         MUXCY:S->O            1   0.172   0.000
     Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<8>
    (Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<8>)
682         MUXCY:CI->O           1   0.019   0.000
     Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<9>
    (Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<9>)
```

```
683         MUXCY:CI->O           1   0.019   0.000
     Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<10>
    (Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<10>)
684         MUXCY:CI->O           1   0.019   0.000
     Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<11>
    (Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<11>)
685         MUXCY:CI->O           0   0.019   0.000
     Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<12>
    (Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_cy<12>)
686         XORCY:CI->O           4   0.180   0.000
     Mmux_time_counter[13]_time_counter[13]_mux_34_OUT_rs_xor<13>
    (time_counter[13]_time_counter[13]_mux_34_OUT<13>)
687         FDRE:D                    0.102          time_counter_13
688        ----------------------------------------
689        Total                      6.654ns (2.361ns logic, 4.293ns route)
690                                       (35.5% logic, 64.5% route)
691
692    ==========================================================================
693    Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
694      Total number of paths / destination ports: 34688527 / 27
695    --------------------------------------------------------------------------
696    Offset:              17.876ns (Levels of Logic = 14)
697      Source:            time_counter_13_1 (FF)
698      Destination:       val2<2> (PAD)
699      Source Clock:      clk rising
700
701      Data Path: time_counter_13_1 to val2<2>
702                                    Gate     Net
703        Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
704        ----------------------------------------  ------------
705         FDRE:C->Q            10   0.447   1.104  time_counter_13_1 (time_counter_13_1)
706         LUT5:I1->O            2   0.203   0.845
     time_counter[13]_PWR_1_o_div_47/Madd_a[13]_GND_3_o_add_15_OUT_lut<10>1
    (time_counter[13]_PWR_1_o_div_47/Madd_a[13]_GND_3_o_add_15_OUT_lut<10>)
707         LUT6:I3->O           11   0.205   0.987
     time_counter[13]_PWR_1_o_div_47/Mmux_a[0]_a[13]_MUX_479_o1211_SW1 (N301)
708         LUT6:I4->O            1   0.203   0.580  time_counter[13]_PWR_1_o_div_47_OUT<5>1_SW4
    (N326)
709         LUT6:I5->O           10   0.205   0.961
     time_counter[13]_PWR_1_o_div_47/Mmux_a[0]_a[13]_MUX_493_o1141
    (time_counter[13]_PWR_1_o_div_47/Mmux_a[0]_a[13]_MUX_493_o114)
710         LUT6:I4->O            5   0.203   1.059  time_counter[13]_PWR_1_o_div_47_OUT<4>1_1
    (time_counter[13]_PWR_1_o_div_47_OUT<4>1)
711         LUT6:I1->O           18   0.203   1.050
     time_counter[13]_PWR_1_o_mod_48/BUS_0012_INV_196_o11
    (time_counter[13]_PWR_1_o_mod_48/BUS_0012_INV_196_o)
```

```
     LUT6:I5->O           15   0.205   0.982
 time_counter[13]_PWR_1_o_mod_48/Madd_a[13]_GND_2_o_add_25_OUT_Madd_cy<4>11
(time_counter[13]_PWR_1_o_mod_48/Madd_a[13]_GND_2_o_add_25_OUT_Madd_cy<4>)
     LUT6:I5->O           11   0.205   0.883
 time_counter[13]_PWR_1_o_mod_48/BUS_0013_INV_211_o1
(time_counter[13]_PWR_1_o_mod_48/BUS_0013_INV_211_o)
     LUT3:I2->O            2   0.205   0.721
 time_counter[13]_PWR_1_o_mod_48/Mmux_a[9]_a[13]_MUX_292_o11
(time_counter[13]_PWR_1_o_mod_48/a[9]_a[13]_MUX_292_o)
     LUT6:I4->O            1   0.203   0.580
 time_counter[13]_PWR_1_o_mod_48/BUS_0014_INV_226_o13_SW1 (N684)
     LUT6:I5->O            8   0.205   0.803
 time_counter[13]_PWR_1_o_mod_48/BUS_0014_INV_226_o13
(time_counter[13]_PWR_1_o_mod_48/BUS_0014_INV_226_o)
     LUT6:I5->O            7   0.205   0.878
 time_counter[13]_PWR_1_o_mod_48/Madd_a[13]_GND_2_o_add_29_OUT_Madd_Madd_cy<2>11_SW0 (N282)
     LUT6:I4->O            7   0.203   0.773  time_counter[13]_PWR_1_o_mod_48/Mmux_o31
(val2_2_OBUF)
     OBUF:I->O                 2.571          val2_2_OBUF (val2<2>)
    ----------------------------------------
    Total                     17.876ns (5.671ns logic, 12.205ns route)
                                       (31.7% logic, 68.3% route)

==========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |   17.318|         |         |         |
---------------+---------+---------+---------+---------+

==========================================================================


Total REAL time to Xst completion: 21.00 secs
Total CPU time to Xst completion: 19.62 secs

-->


Total memory usage is 490712 kilobytes

Number of errors   :    0 (   0 filtered)
```

```
749   Number of warnings :    7 (   0 filtered)
750   Number of infos    :    6 (   0 filtered)
751
752
```

And from the design summary report, I could see the Macro Statistics section about the number of differnt logic gate in my design. And I can check how my program performs through the report.

Conclusion

The project is similar to project3 but the logic of the implementation is easier.

In this project, I designed and implemented the parking meter, Final State Machine according to the behavior in the project manuscript. To correctly implement this, I first draw the FSM diagram to help me to have the clear idea that what output should be in each state and how to transit to a different state.

No major difficulties meet as long as you attend the lecture and understand how the outputs represent the seven-segment display and how to check if the display at correct frequency.

References

- http://web.engr.oregonstate.edu/~traylor/ece474/beamer_lectures/modules.pdf
- https://www.electronics-tutorials.ws/blog/7-segment-display-tutorial.html