B. TECH.

(SEM-III) THEORY EXAMINATION 2019-20

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours *Total Marks: 100*

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Qno.	Question	Marks	CO
a.	Define the term Computer Architecture.	2	1
b.	Draw the basic functional units of a computer.	2	1
c.	Perform the 2's complement subtraction of smaller number (101011) from larger number (111001).	2	2
d.	What is the role of Multiplexer and Decoder?	2	2
e.	Write the differences between RISC and CISC.	2	3
f.	What are the types of microinstructions available?	2	3
g.	What is SRAM and DRAM?	2	4
h.	What is the difference between 2D and $2^{1/2}$ D memory organization?	2	4
i.	What is I/O control method?	2	5
j.	What is bus arbitration?	2	5

SECTION B

2. Attempt any *three* of the following:

Qno.	Question	Marks	CO
a.	Convert the following arithmetic expressions from infix to reverse polish notation: i. A*B+C*D+E*F ii. A*[B+C*CD+E]/F*(G+H)	5+5	1
b.	Design a 4-bit Carry-Look ahead Adder and explain its operation with an example.	10	2
c.	i. Draw the timing diagram for a instruction cycle and explain. ii. Give a note on subroutine.	5+5	3
d.	What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory.	10	4
e.	What is DMA? Describe how DMA is used to transfer data from peripherals.	10	5

SECTION C

3. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Describe in detail the different kinds of addressing modes with an example.	10	1
b.	Discuss stack Organization. Explain the following in details- (i) Register stack (ii) Memory stack	10	1

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4. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Represent the following decimal number in IEEE standard floating-point format in a single precision method (32-bit) representation method. i. $(65.175)_{10}$ ii. $(-307.1875)_{10}$	5+5	2
b.	Using Booth algorithm perform the multiplication on the following 6-bit unsigned integer 10110011 * 11010101	10	2

5. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	What is parallelism and pipelining in computer Architecture?	10	3
b.	Explain the organization of Microprogrammed control unit in detail.	10	3

6. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Discuss the different mapping techniques used in cache memories and their relative merits and demerits.	10	4
b.	RAM chip 4096 × 8 bits has two enable lines. How many pins are needed for the integrated circuits package? Draw a block diagram and label all input and outputs of the RAM. What is main feature of random-access memory?	5+5	4

7. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Write down the difference between isolated I/O and memory mapped I/O. Also discuss advantages and disadvantages of isolated I/O and memory mapped I/O.	10	5
b.	i. Discuss the design of a typical input or output interface. ii. What are interrupts? How are they handled?	10	5