Fall 2019

California State University of Northridge
Department of Electrical & Computer Engineering

Experiment 13
Design of a Multistage Amplifier

ECE 340L
December 04, 2019

Professor Soraya Roosta
Written by: Ridge Tejuco

Introduction:

The purpose of this experiment was to design and implement a multistage amplifier using the MOSFET 2n7000 and the BJT. The design must have at least 2 stages and follow the following specifications.

$A_v \geq |V_o/V_i| \geq 5$

$Z_i \geq$ 100 kΩ

Z_o = 650 Ω +/- 10%

V_o swing ≥ 2 V_{p-p}

R_L = 650 Ω

Vcc ≤ 20V

Low end cutoff frequency ≤ 40 Hz.

This experiment is used to test understanding of the theory of BJTs and MOSFETS discussed in lecture based on all the different amplifiers.

Equipment:

Type	Model
Oscilloscope	Agilent Technologies DSO1002A
Digital Multimeter	Tektronix CDM250
Function Generator	Agilent 3322OA
Power supply	Hewlett Packard E363OA

Parts used:

QTY	Component	Value	Type
1	Resistor	10 Ω	Carbon +/- 5%
1	Resistor	100 Ω	Carbon +/- 5%
1	Resistor	650 Ω	Carbon +/- 5%
1	Resistor	1 kΩ	Carbon +/- 5%
1	Resistor	100 kΩ	Carbon +/- 5%
1	Resistor	120 kΩ	Carbon +/- 5%
1	Resistor	150 kΩ	Carbon +/- 5%
1	Resistor	10 kΩ	Carbon +/- 5%
1	Resistor	470 kΩ	Carbon +/- 5%
3	Capacitor	10 µF	Polypropylene film +/- 5%
1	Capacitor	100 µF	Polypropylene film +/- 5%
1	Transistor	2N7000	MOSFET
1	Transistor	2N2222	BJT

Software:

Pspice

Microsoft Word

Microsoft Excel

Procedure & Results:

Testing the DC Bias

The circuit design in Figure 1 was constructed. Both stages were tested for DC biasing by supplying the V_{CC} and disabling the input signal. Voltages at the pins of the transistors were recorded. Table 1 and Table 2 shows the results for the common collector and common source respectively.

Figure 1. Multistage amplifier design

Table 1. Results of DC Biasing for common collector

	V_ce (V)	V_be (V)	V_e (V)	V_c (V)	I_c (mA)
calc	18.35	0.62	1.65	20	0.5
meas	18.47	0.6	1.51	19.95	0.458
% error	0.65%	3.23%	8.48%	0.25%	8.40%

Table 2. Results of DC Biasing for common source

	V_ds (V)	V_gs (V)	V_s (V)	V_d (V)	I_d (mA)
calc	17.14	2.19	2.55	19.69	0.5
meas	16.93	2.08	2.68	19.63	0.525
%error	1.23%	5.02%	5.10%	0.30%	5.00%

Q-point of the amplifier

The Q point of the common collector was calculated to be V_{CE} = 18.35 v and I_C = 0.5 mA, while the actually measured Q point was V_{CE} = 18.47 v and I_C = 0.458 mA.

The collector current is slightly off because a value of 270kΩ was used instead of 256kΩ resistor in the diagram. This however does not affect the rest of the operation of the amplifier.

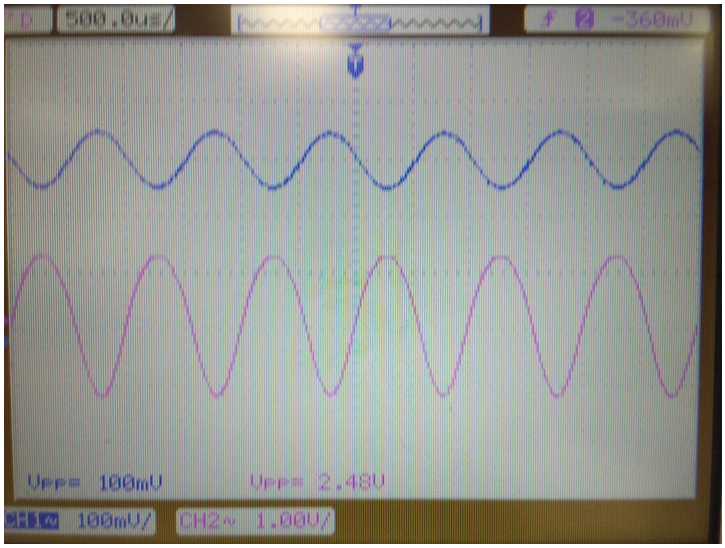
The Q common source was calculated to be V_{DS} = 17.14 v and I_D = 0.5 mA, while the actual measured value was V_{DS} = 16.93 v and I_D = 0.525 mA. These values are within the 5% of the calculated values and can be explained by differences found in nominal resistances chosen. Another aspect to consider is the operation of the transistors and how their operating voltages may differ from the design.

Voltage Gain of the input

A 100 mV $_{P\text{-}P}$ sine wave was input to the Amplifier. An oscilloscope was used to measure the input and output. This oscilloscope can be seen in Figure 2. Using these values the gain was calculated.

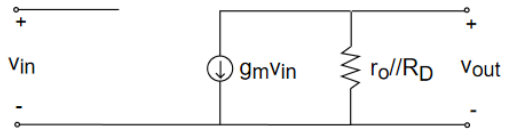
$$A_V = \frac{V_o}{V_i} = \frac{2.48\,V_{P-P}}{100\,mV_{P-P}} = 24.8$$

Figure 2. Oscilloscope showing gain.



Calculated Gain

The gain was calculated by analyzing the small signal parameters for the MOSFET.



R_S is excluded from the small signal circuit because a bypass capacitor is placed.
From the small signal circuit, the following equation is true.
$V_{out} = -g_m V_{in} (r_o \parallel R_D)$

$A_V = V_{out} / V_{in} = -g_m (r_o \parallel R_D) = -g_m R_D$ assuming $r_o >> R_D$

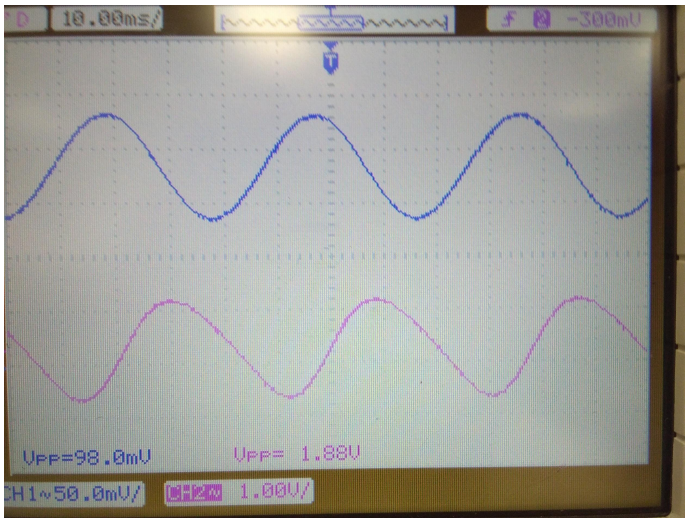
Cutoff frequency

The cutoff frequency was found by lowering the frequency of the input until the output voltage was 3dB less. The 3dB less voltage was calculated by the following equation.

$$(V)_{\text{-3 dB}} = \frac{V_o}{\sqrt{3}} = \frac{2.48\, V_{P-P}}{1.732} = 1.84\ V_{\text{P-P}}$$

The required output was found at a cutoff frequency of 22 Hz. Figure 3 shows the output.

Figure 3. Voltage output at 22 Hz

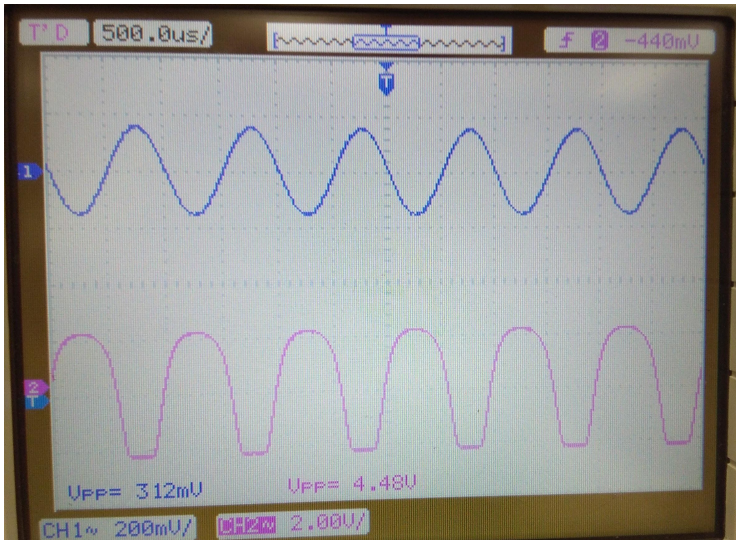


Distortion and Swing voltage

The input signal was returned to a 1 kHz sine wave. The input signal was increased until the voltage output showed distortion by hard clipping.

Hard clipping can be seen in the oscilloscope in Figure 4.

Figure 4. Hard Clipping



Input impedance

The input impedance was found by placing resistor values in series with the input to the amplifier. The output voltage was expected to drop by half when the series resistor is equal to the nominal input impedance. Table 3 shows a list of values for the series resistor and their resulting output voltages. Figure 5 shows the output viewed in the oscilloscope once the resistance value equal to the input impedance was found.

$V_1 = 2.6$ V $V_2 = 1.3$ V

Table 3. Series resistors at the input

R_s (kΩ)	V_o (V_pp)
120	1.36
130	1.34
140	1.3
142	1.24
145	1.26

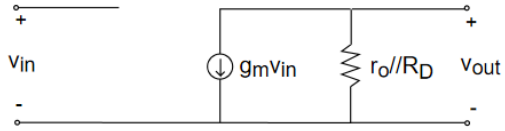
Figure 5. Output at resistance of 140 kΩ

The resulting input impedance meets the specification of

$Z_i > 100$ kΩ

Calculated Input impedance

The calculated input impedance was found by finding the Thevenin equivalent circuit seen at the input of the amplifier. The input to the gate is an open circuit. Therefore the thevenin circuit only includes R_1 and R_2.



$$Z_i = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{480k * 150\ k}{480\ k + 150k} = 114.3\ k\Omega$$

For the second stage, the input impedance to the BJT is the following

As can be seen, the calculated value of 114.3 kΩ is not close to the measured value of 140 kΩ seen in Table 3. The input impedance was successfully found using the half voltage method discussed in the lab.

Output impedance

The output impedance was found by placing series resistance across the load.

First, the V_1 was found by removing the load resistance and measuring across the open circuit. A resistance was placed until the voltage was ½ of V_1.

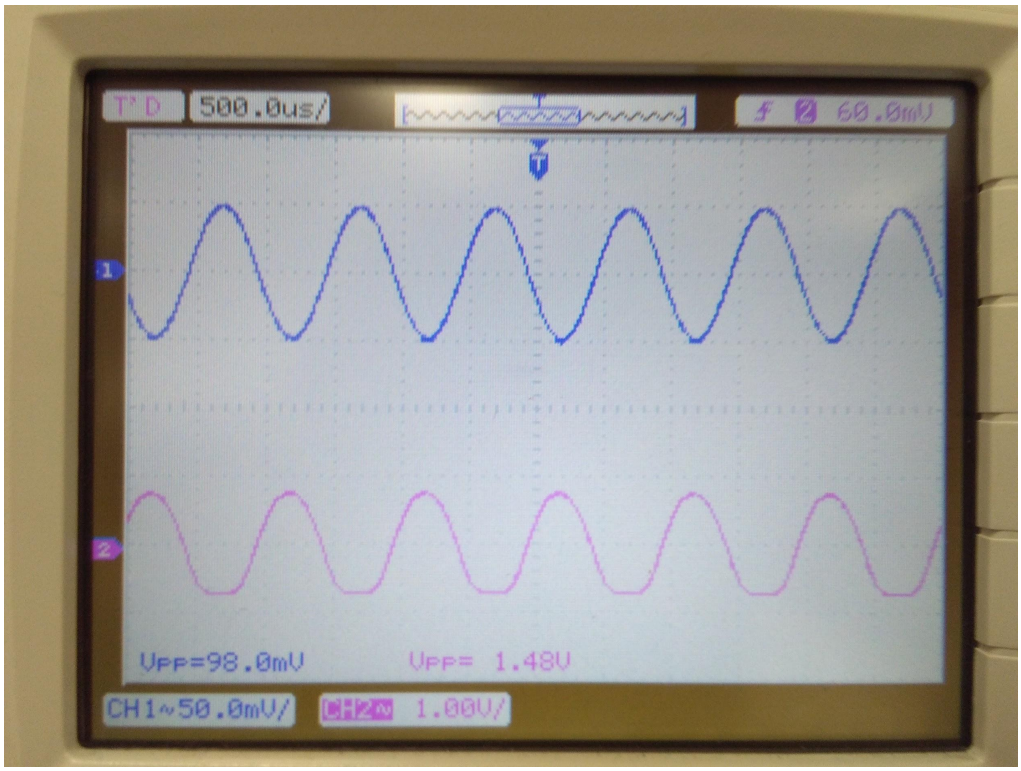
The resulting resistance found which resulted in ½ V_1 was 150 Ω in Table 3.

V_1 = 2.96 V. V_2 = 1.48 V.

Table 4. Series resistors at the output

R_s (Ω)	V_o (V_pp)
470	2.32
200	1.8
180	1.56
150	1.48

Figure 6. Output at load of 150 Ω



Current Gain

The current gain is calculated by the following.

$$I_{out} = \frac{V_o}{Z_o} = \frac{2.48\ V}{150\ \Omega} = 16.5\ \text{mA}$$

$$I_{in} = \frac{V_i}{Z_i} = \frac{100\ mV}{143k\ \Omega} = 0.69\ \mu\text{A}$$

$$A_I = \frac{I_{out}}{I_{in}} = \frac{16.5\ mA}{0.69\ \mu A} = 23.59\ \text{k}$$

Power Gain

The power gain was calculated by the following steps..

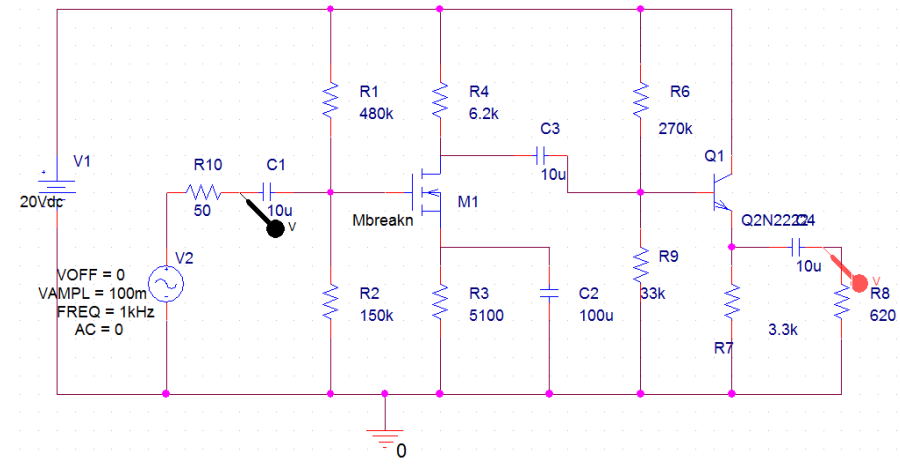
$$P_{in} = \frac{V_i^{\,2}}{Z_i} = \frac{0.01\ V^2}{143k\ \Omega} = 69\ \text{nW}$$

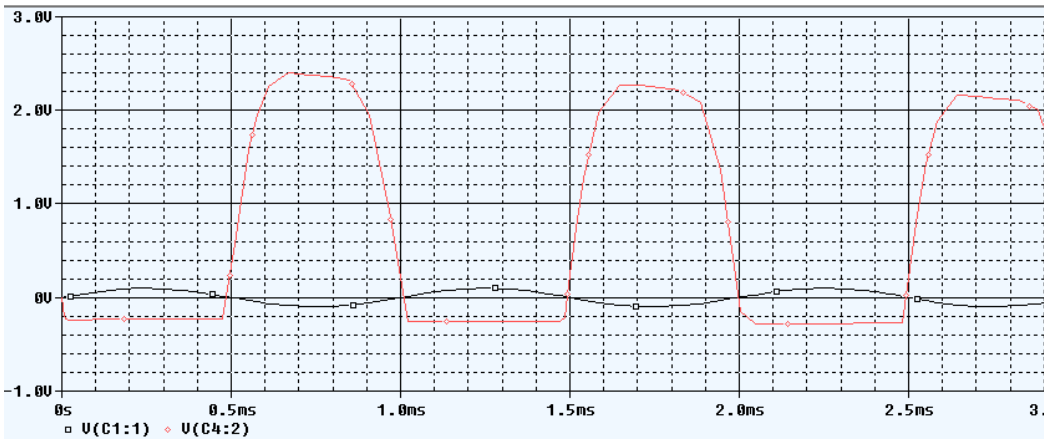
$$P_{out} = \frac{V_o^{\,2}}{Z_o} = \frac{6.15\ V^2}{150\ \Omega} = 41\ \text{mW}$$

$$A_P = \frac{41\ mW}{69\ nW} = 594202$$

Pspice of gain

The design was configured in Pspice. Figure 8. Shows the design.





A voltage of 2.5 V_{P-P} was displayed at the output with a 100 mV_{P-P} input.

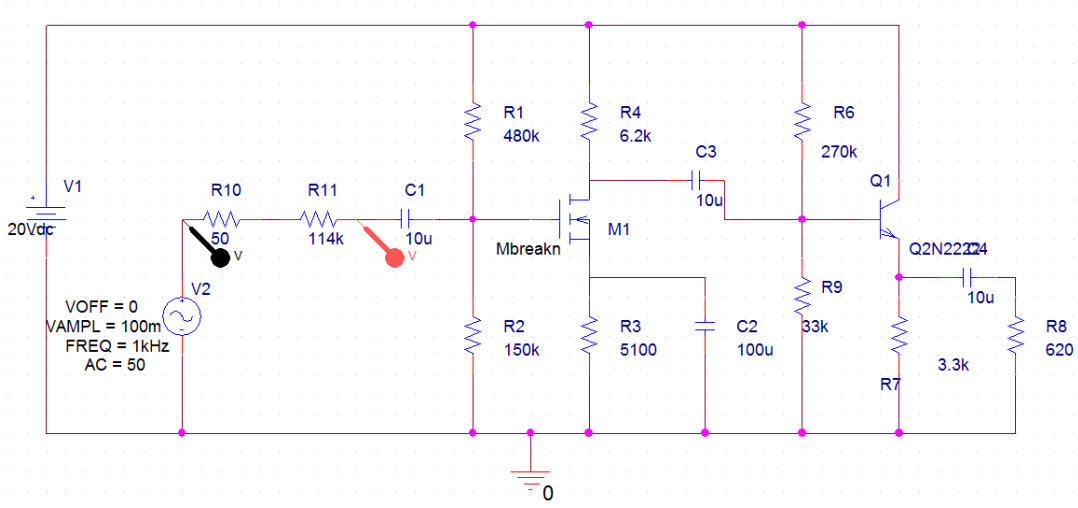
$A_V = 2.5$

This is significantly close to the results achieved in the Lab.

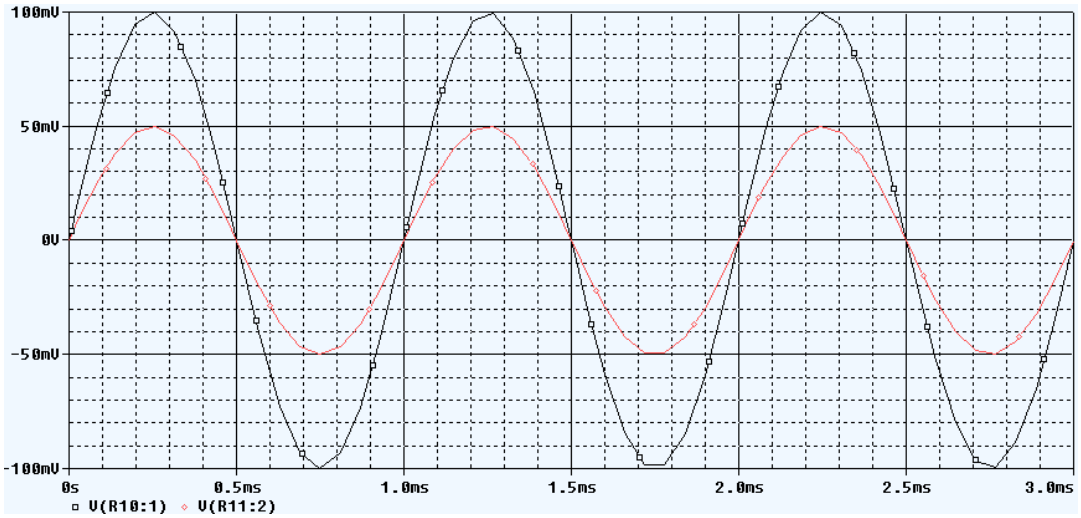
Pspice of input impedance

Similarly to the lab, the input impedance in Pspice was found by placing resistors in series at the input, however in Pspice the input voltage was dropped to half rather than the output voltage. The following Schematic 3 was constructed in Pspice and its results are shown below.

Schematic 3.



Pspice 3. ½ voltage of the input



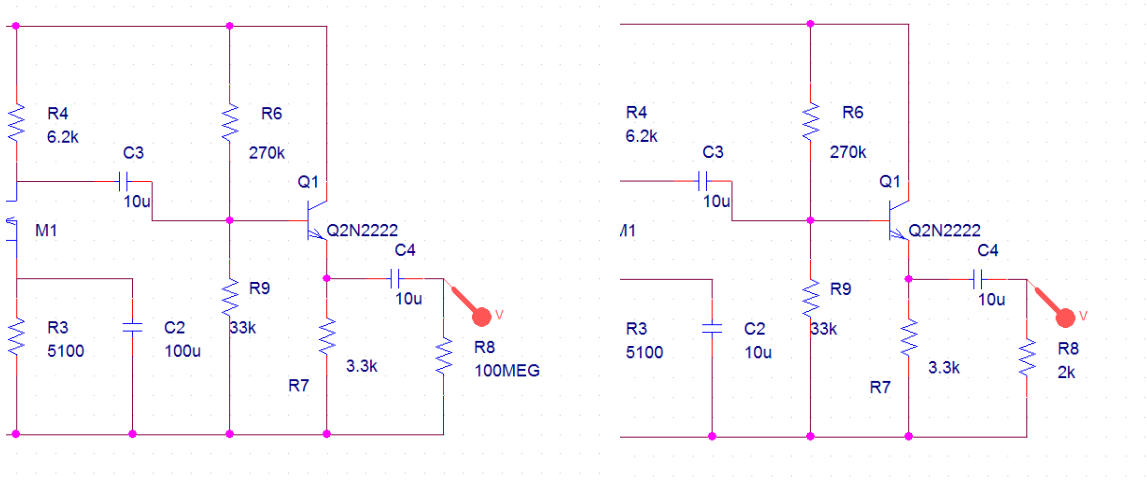
The simulated input impedance was 114 kΩ which is very close to the calculated input impedance of 114.3 kΩ.

Pspice of output impedance

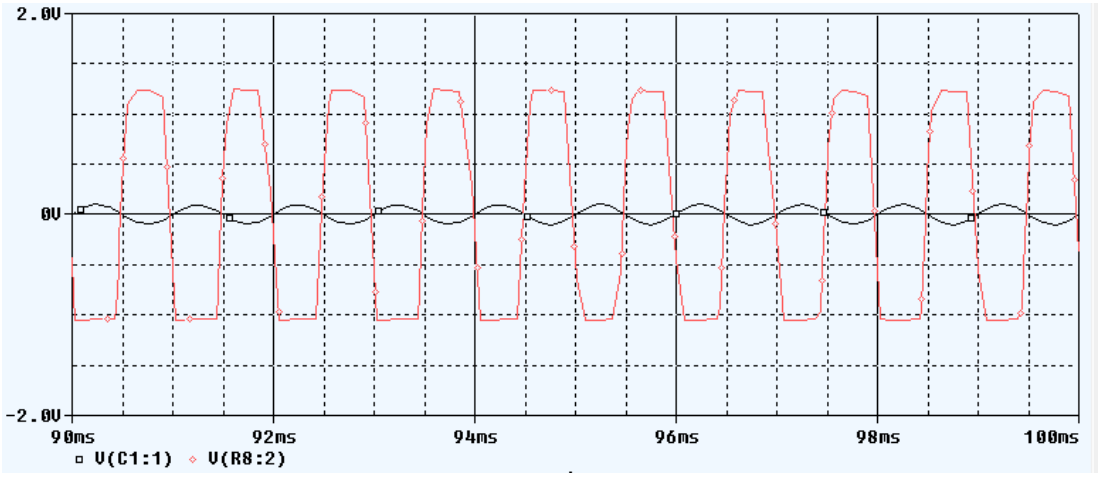
To simulate an open circuit across the load resistor was set to 100 MEG in the schematic.
The voltage across this 100 MEG is the V_1 in the impedance calculation.
Schematic 4 shows the V_1 on the left and the V_2 circuit on the right.
V_1 was measured to be 2.52 V.

Schematic 4

100 MEGΩ 2KΩ



Pspice 4. Output voltage at R_8 = 2kΩ.



The output impedance for this schematic was around 2k. This makes sense because the output impedance of this multistage amplifier is dependant on ($1/g_m$) which is different for every transistor.

Conclusion

Overall , the design was almost a success, but failed in one specification. The experiment was successful in meeting the following requirements.

$A_v \geq |V_o/V_i| \geq 5$

$Z_i \geq 100\ k\Omega$

V_o swing $\geq 2\ V_{p-p}$

$R_L = 650\ \Omega$

$Vcc \leq 20V$

The design failed to meet the output impedance specification.

$Z_o = 650\ \Omega$ +/- 10%

The design is a multistage amplifier consisting of a common source and then a common collector amplifier. The common source was used because its input impedance could easily be controlled with R_1 and R_2.. Upon review of the results, the output impedance could have been controlled by increasing the value of the R_D resistor.