

Fall 2018



California State University, Northridge
Department of Electrical & Computer Engineering

Experiment 11
Adder and Magnitude Comparator
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ECE 320L
Professor: Ramin Roosta

Author: Ridge Tejuco
Lab partner: Alexander Henriquez

Introduction:

The purpose of the experiment is to understand how to design, build, and analyze circuits with binary adders and magnitude comparators to use convert number systems. This experiment considers the conversion of binary input to BCD and excess-3 code.

Equipment used:

| <u>Type</u> | <u>Model</u> | <u>Serial No.</u> | <u>Calibration Date</u> |
|--------------------|-------------------|-------------------|-------------------------|
| Power Supply | Tektronix PWS2323 | MY48004846 | N/A |
| Digital Multimeter | Tektronix CDM250 | DM 250TWS2380 | N/A |

Parts Used:

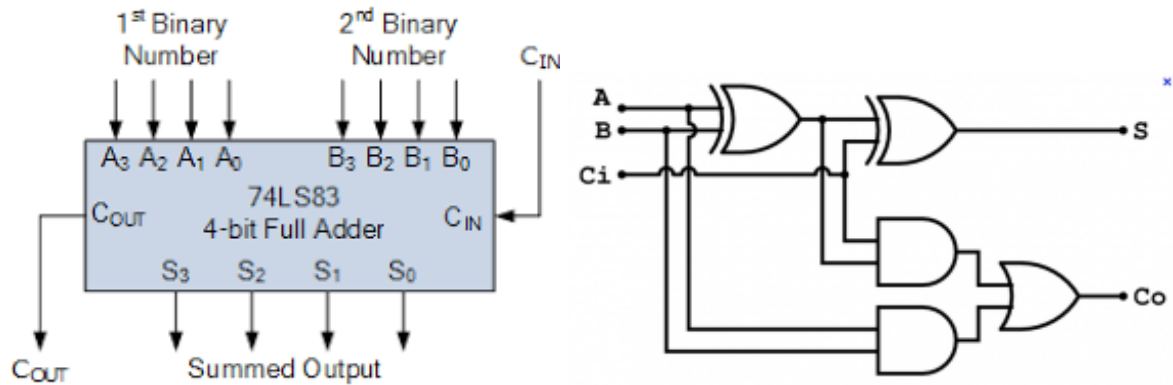
| <u>QTY</u> | <u>Component</u> | <u>Value</u> |
|------------|--------------------|--------------|
| 5 | Resistor | 330 Ω |
| 1 | 7404 Hex Inverter | N/A |
| 8 | Resistor | 1k Ω |
| 1 | 7483A binary adder | N/A |
| 1 | 7485 Comparator | N/A |
| 5 | LEDS | N/A |

Software Used:

1. Google Docs
2. Krita
3. Snipping Tool
4. Google Sheets

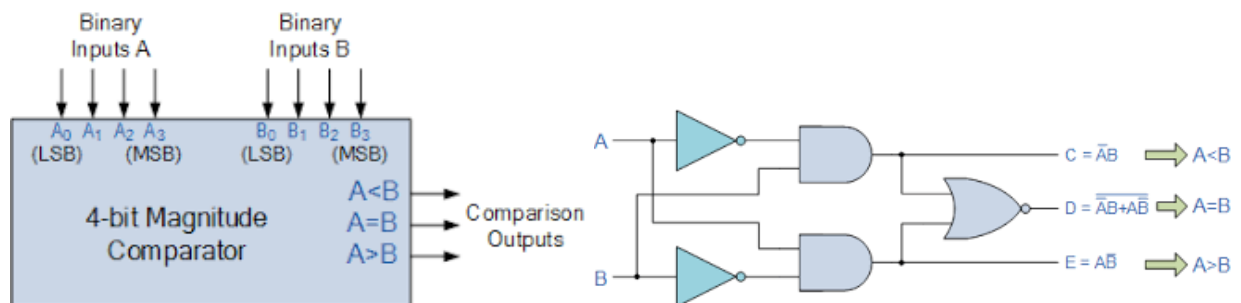
Theory:

7483a 4-bit binary adder



| Input | | | Output | |
|-------|---|-----|--------|-------|
| A | B | Cin | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

7485 magnitude comparator



The schematic for figure 11-2 was completed.

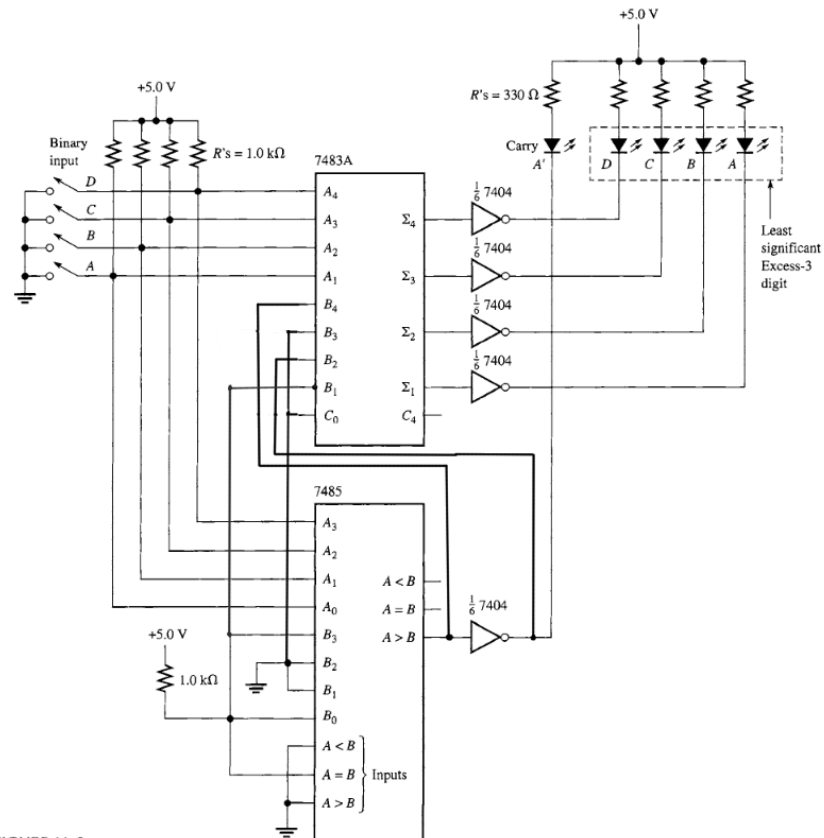
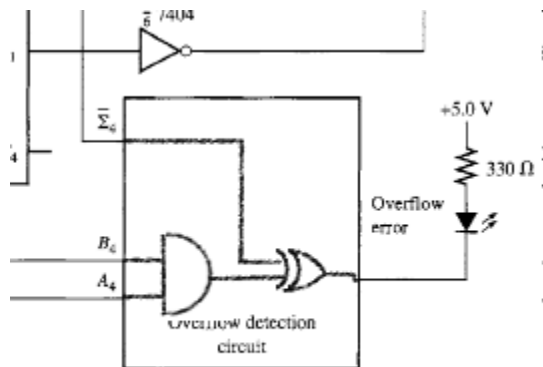


FIGURE 11-2
Binary to Excess-3 converter.

TABLE 11-4
Truth table for Figure 11-2.

A circuit for detecting overflow for a 4-bit signed binary adder was designed.



The truth table 11-5 for the the overflow error was completed.

| Sign Bits | | | Error |
|-----------|-------|------------|-------|
| A_4 | B_4 | Σ_4 | X |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

The Karnaugh map figure 11-5 was completed.

And the boolean expression for the overflow error was simplified using the Karnaugh map.

| $A_4 B_4$ | | Σ_4 | |
|-----------|---|------------|---|
| | | 0 | 1 |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |

$$X = A_4 B_4 \oplus \Sigma_4$$

Conclusions:

The experiment was a success as the design and construction of the the final circuit was a success. The truth tables results show the exact same outputs that are expected to be seen in theory. When constructing the circuit trouble was seen when displaying the carry, but was solved once all inputs had been checked and properly grounded. For further investigation, the carry for the signed bit was correctly designed, and its boolean expression was properly identified. The experiment was a success in understanding the use and application of binary adders and magnitude comparators.