CMOS D-LATCH DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

Ridge Tejuco and Jesus Adame

California State University, Northridge, College of Engineering and Computer Science, Electrical and Computer Engineering Department
Ridge.Tejuco.881@my.csun.edu, Jesus.Adame.846@my.csun.edu

ABSTRACT:

A D-latch was simulated in Pspice using CMOS inverters and CMOS transmission gates. The method of frequency division using D- latches was used to test the circuit for proper operation. The results show that frequency divisions of 2, 4, 8 and 16 were successfully simulated as the period of the output increased by a factor of 2 for each circuit.

KEYWORDS:

CMOS, NMOS, PMOS, Transmission gate, CMOS Inverter, D-latch, Frequency division, PSPICE

5.1 INTRODUCTION

The purpose of this lab is to construct a D-latch using CMOS inverters and transmission gates. To understand the construction and operation of the D-latch it's important to understand the operation of transmission gates and inverters which are the building blocks for constructing the circuit.

Looking closely at figure 5.1, the CMOS transmission uses pass transistor logic with an NMOS and PMOS transistor in parallel. The clock signal C and C' turn on both transistors and allow current from signal X to charge the load capacitance at the output Y completely to the voltage supplied by X. This operation allows the CMOS transmission gate to be used as a switch.

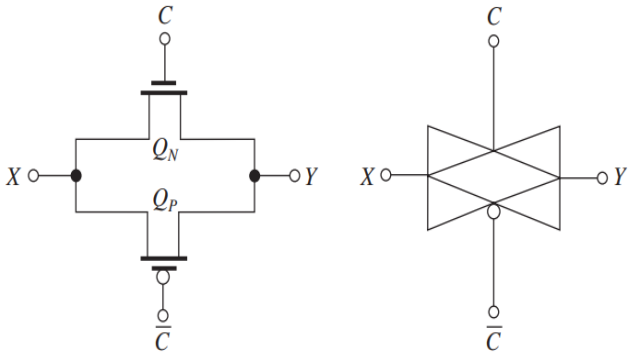

Fig. 5.1 The CMOS transmission gate and the corresponding gate symbol

Looking closely at figure 5.2, the CMOS transmission gate consists of a PMOS above a NMOS transistor. An input X turns on Q_N which allows output Y to discharge and a low input X turns on Q_P which allows the supply voltage to charge the output Y.

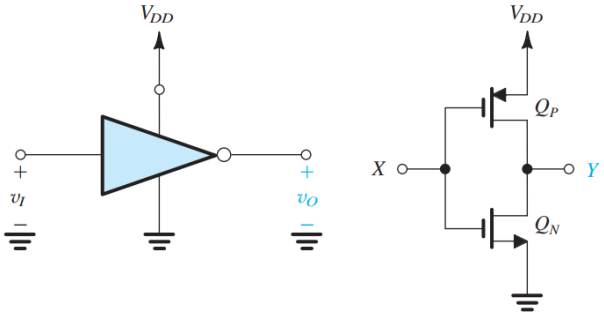

Fig. 5.2 The CMOS inverter and gate symbol.

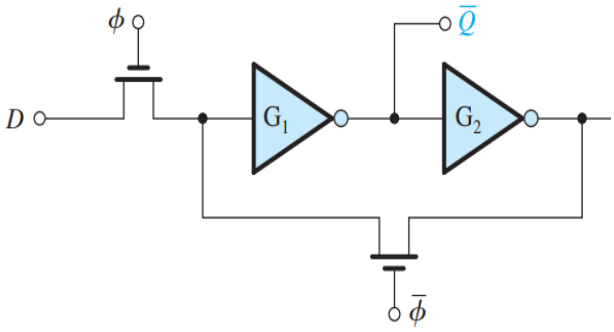

Fig. 5.3 D-flip flop circuit using NMOS transmission gate.

Figure 5.3 shows a D-flipflop circuit using NMOS transmission gates. The circuit used in this lab is similar, but an CMOS transmission gate is used instead. A positive clock signal ϕ turns on the top transmission gate allowing the input D to be set at output Q after two inverter delays. A negative clock signal ϕ closes the top transmission gate and opens the bottom one. This allows the output Q to feedback into the inverters and retain its data. Figure 5.4 shows the use of this D-flipflop as a frequency divider. The output Q' feeds back into input D and returns the Data at half the frequency of the input clock.

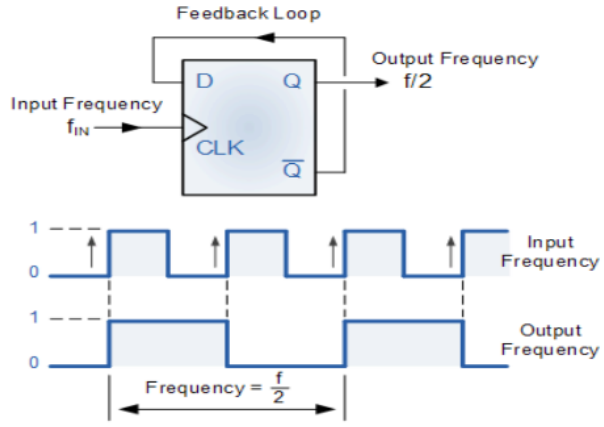

Fig. 5.4 Frequency division using D-flipflop

5.2 PROCEDURES, SIMULATION AND EXPERIMENTAL SET-UP

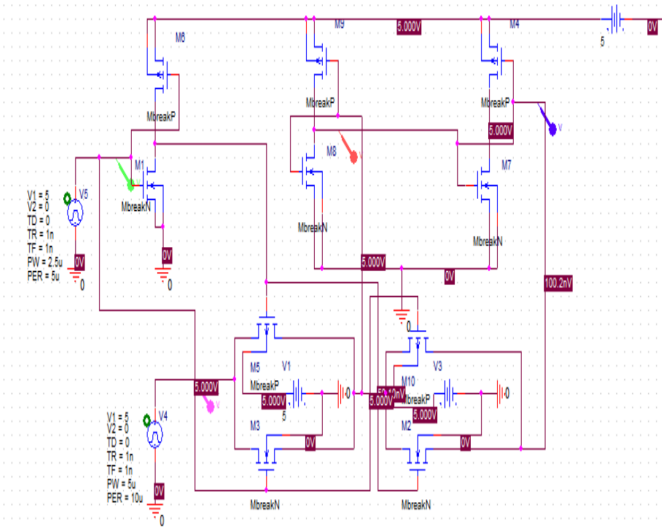

Fig. 5.5 Case 1: Division by 2 at 200kHz

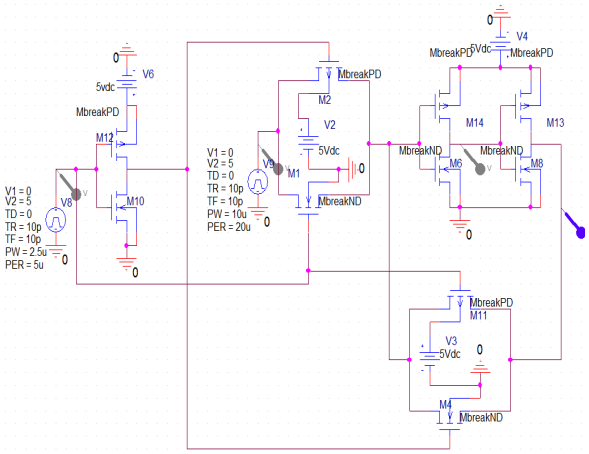

Fig. 5.6 Case 2: Division by 4

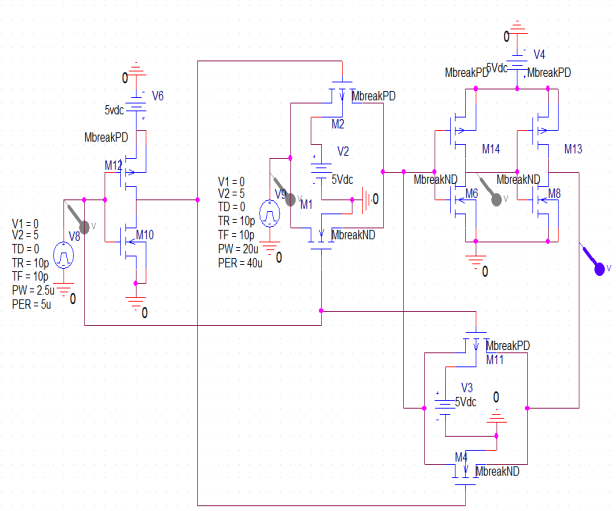

Fig. 5.7 Case 3: Division by 8

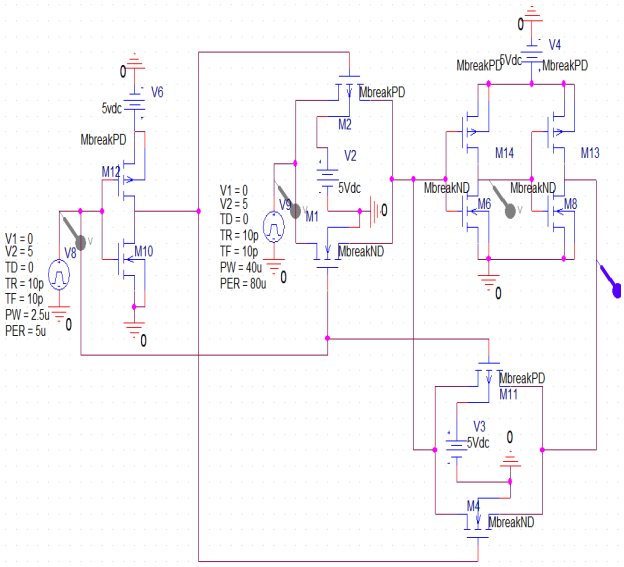

Fig. 5.8 Case 3: Division by 16

5.3 SIMULATION AND EXPERIMENTAL RESULTS

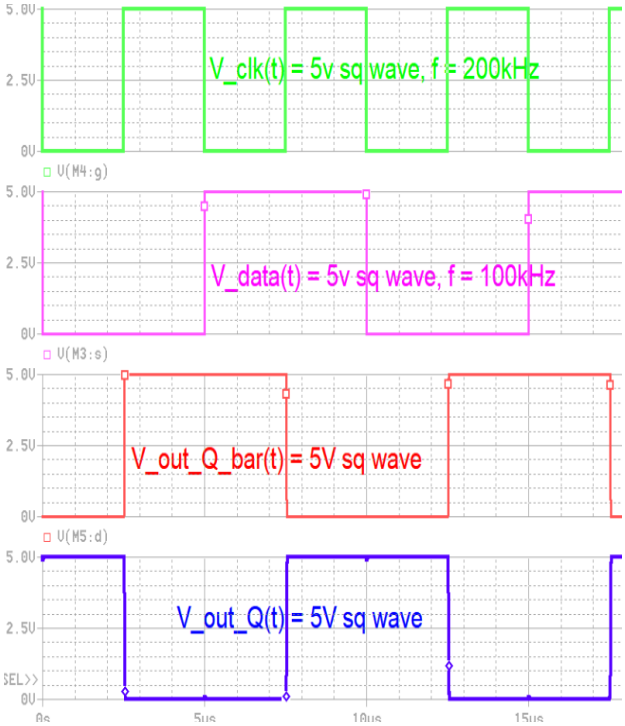

Fig. 5.9 Case 1: Division by 2

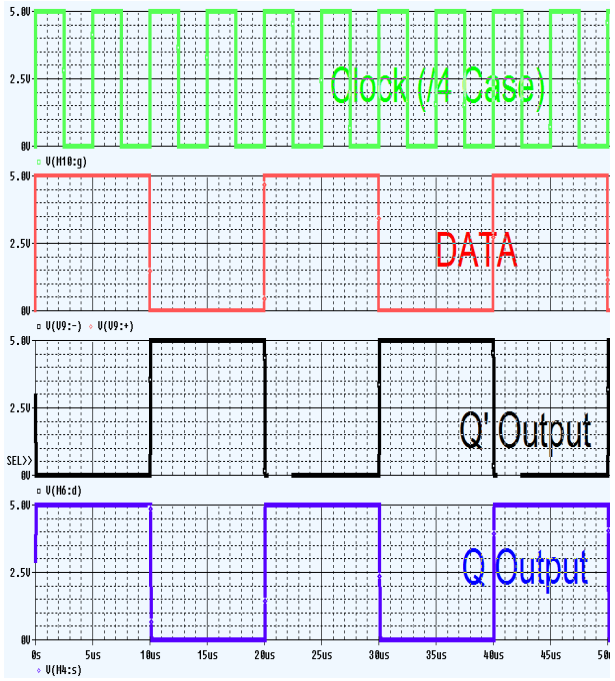

Fig. 5.10 Case 2: Division by 4

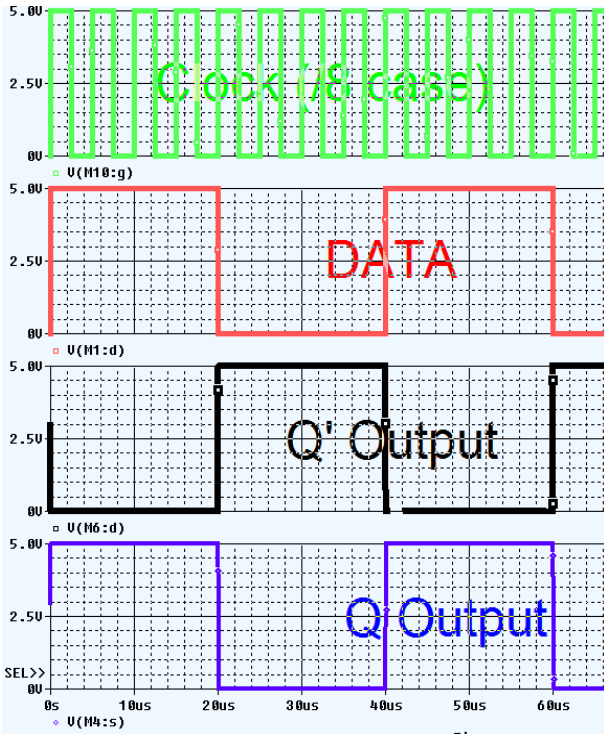

Fig. 5.11 Case 3: Division by 8

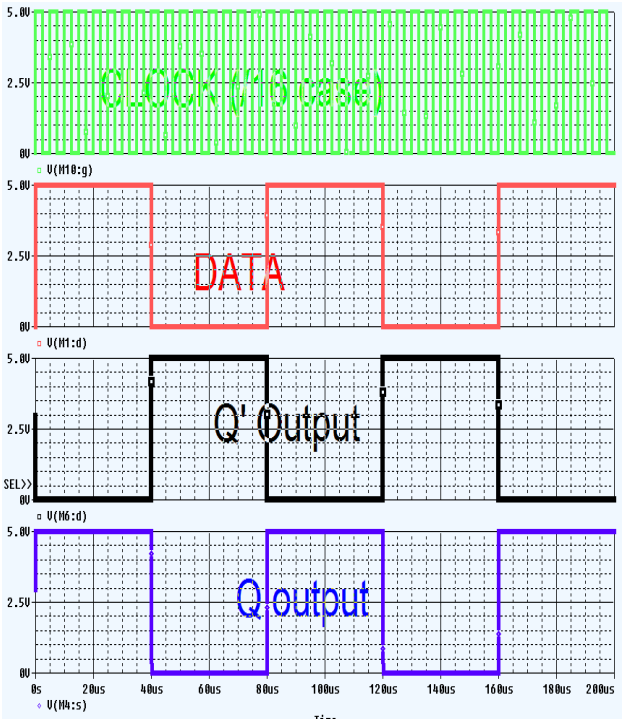

Fig. 5.12 Case 1: Division by 16

5.4. DISCUSSION AND CONCLUSION:

The setup for the frequency division using the D-latch is shown in figure 5.5. A pulse wave function at 200 kHz was used as input square wave of the D-latch. An inverter was constructed to produce the complement of the clock. A pulse wave was used as the data input at half the frequency. The D-latch was properly constructed in Pspice using 2 transmission gates and two inverters. Figure 5. 9 shows the results of the division by 2 case. The output shows the correct frequency that is half the input clock.

The setup was then changed to have a data input that was a quarter of the input frequency. This simulates the cascading of frequency dividers. This setup is shown in figure 5.6. The results in figure 5.10 show that the output period is 4 times longer than the input period.

Next, the setup was changed to have a data input that was an eighth of the frequency. The setup is seen in figure 5.7. The results in figure 5.11 show the frequency division of 8 in this case.

Lastly, the frequency division was simulated in figure 5.8. The results show that the frequency was divided by 16 and the period of the output is 16 times longer than the initial clock frequency.

REFERENCES

[1] A. S. Sedra and K. C. Smith, Microelectronic circuits. New York: Oxford University Press, 2015.

[2] ECE lab manual