CMOS RING OSCILLATION AND CLOCK GENERATION DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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ABSTRACT:

A 2-input NAND Gate was created using CMOS transistors. The methodology of transistor sizing was used to design and modify the series transistors of the Pull-down network in order to match its sizing with the Pull-up network. The 2-input NAND gate was tested in lab under 3 different case frequencies and simulated in PSPICE. The results show the correct logic output expected of the NAND gate given the input square waves.

KEYWORDS:

CMOS, NMOS, PMOS, Pull-up Network (PUN), Pull-down Network (PDN), & Two-Input CMOS NAND Gate, PSPICE

2.1 INTRODUCTION

The purpose of this lab is to use the design of CMOS inverters to create a 2-input NAND Gate. Looking closely at figure 2.1, the NAND gate consists of a Pull-up network containing the PMOS transistors in parallel. These parallel PMOS transistors ensure that if any of the inputs A or B are logic high, then the output Y will receive current from the supply voltage V_{DD}. The supply voltage will charge the load capacitance. The Pull-down network consists of 2 NMOS transistors in series. The series connection ensures that if both inputs A and B are logic high, then the output will be set to ground as the load capacitance is discharged. The aspect ratio of the NMOS transistors must be doubled in size to match the PMOS transistors. In the lab this can be done by adding a second set of NMOS transistors in parallel.

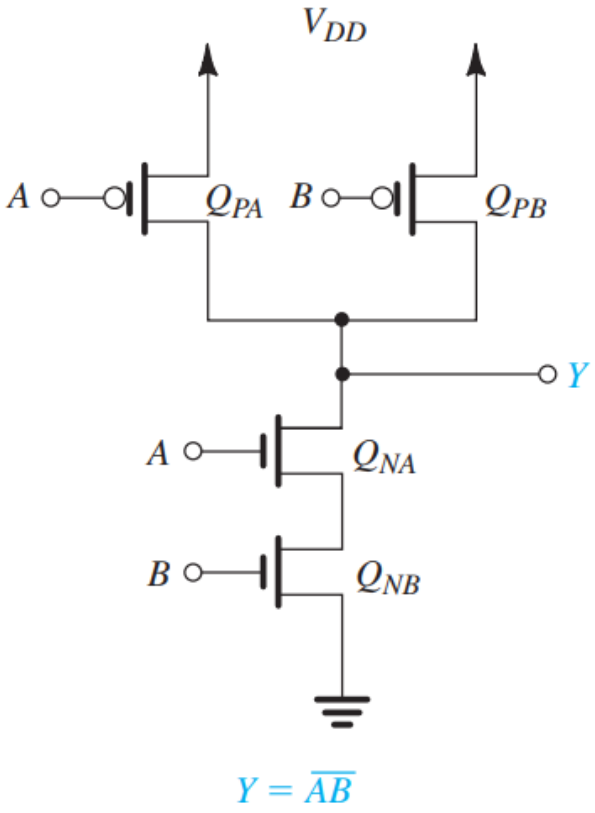


Fig. 2.1 Two-Input CMOS NAND Gate

Input	Input	Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 2.2 NAND Gate Truth Table

Figure 2.3 below shows the simple representation of a 2 input NAND gate when used in logic circuit design.

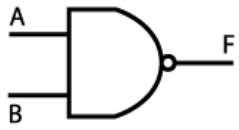


Fig. 2.3 Two-Input NAND Gate

2.2 PROCEDURES, SIMULATION AND EXPERIMENTAL SET-UP

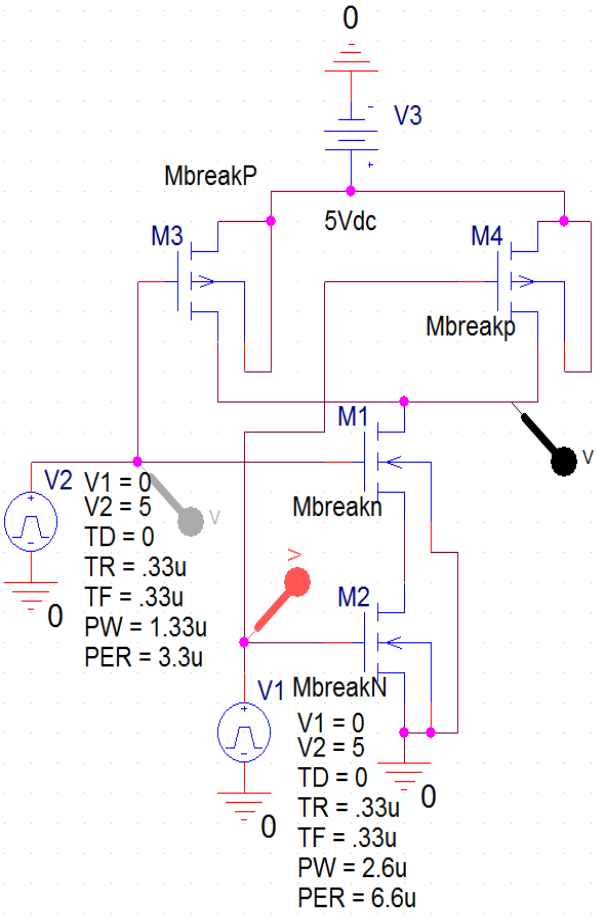


Fig. 2.4 Case 1: Two-Input NAND Gate at 300kHz

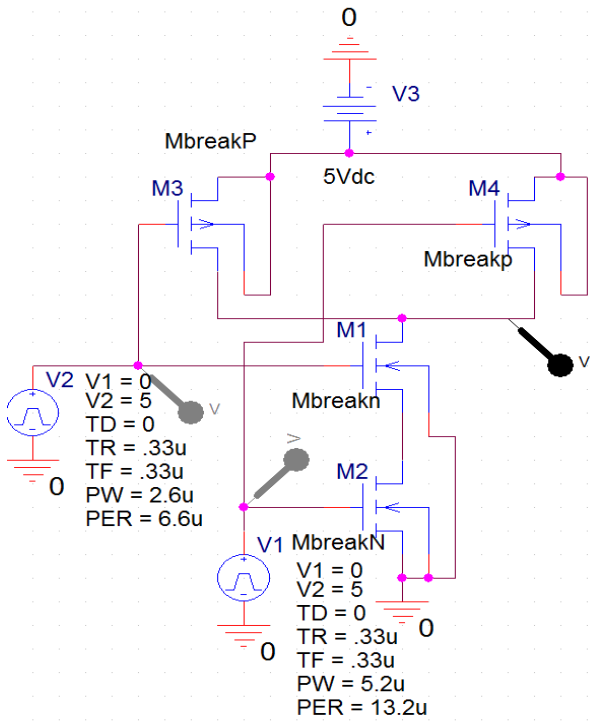


Fig. 2.5 Case 2: Two-Input NAND Gate at 600kHz

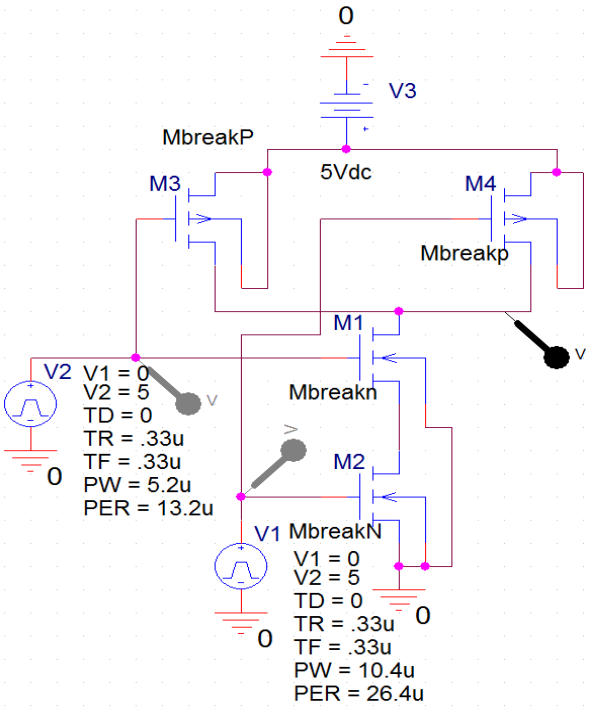


Fig. 2.6 Case 3: Two-Input NAND Gate at 1.2 MHz

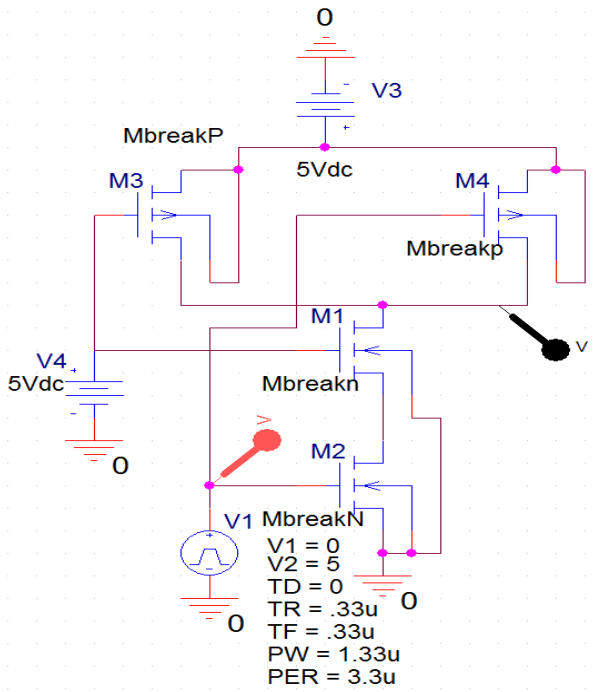


Fig. 2.7 NAND Gate Design for the VTC Curve

2.3 SIMULATION AND EXPERIMENTAL RESULTS

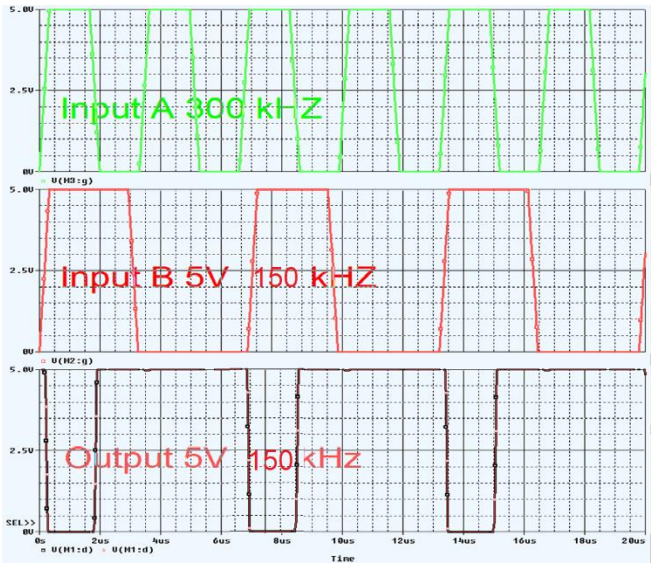


Fig. 2.8 Case 1: NAND Gate Simulation at 300kHz

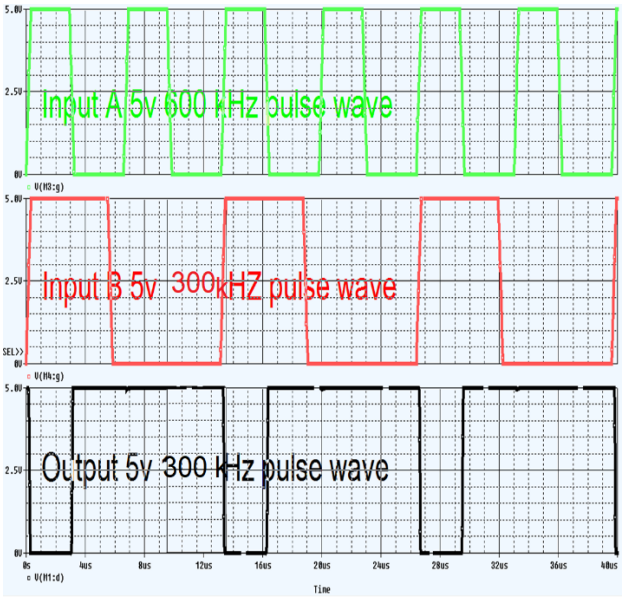


Fig. 2.9 Case 2: NAND Gate Simulation at 600kHz

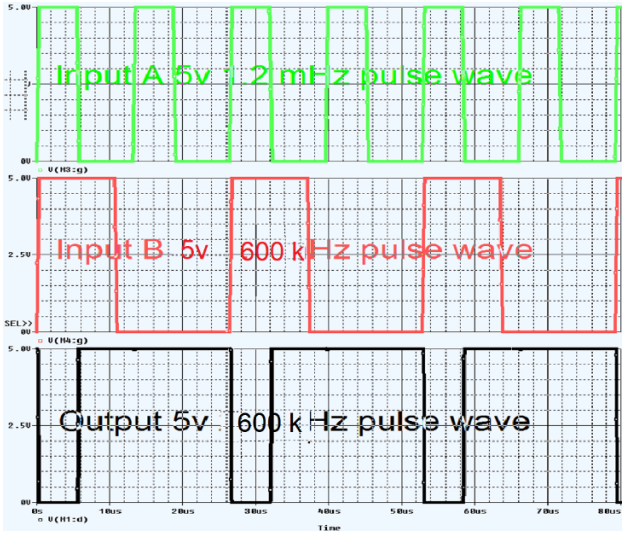
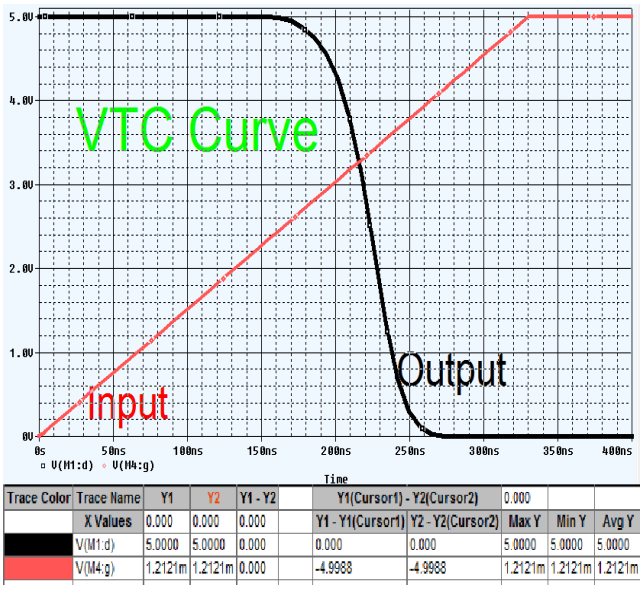


Fig. 2.10 Case 3: NAND Gate Simulation at 1.2MHz



Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	0.000		
	X Values	0.000	0.000	0.000	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(M1:d)	5.0000	5.0000	0.000	0.000	0.000	5.0000	5.0000	5.0000
	V(M4:g)	1.2121m	1.2121m	0.000	-4.9988	-4.9988	1.2121m	1.2121m	1.2121m

Fig 2.11 VTC Curve for the NAND Gate

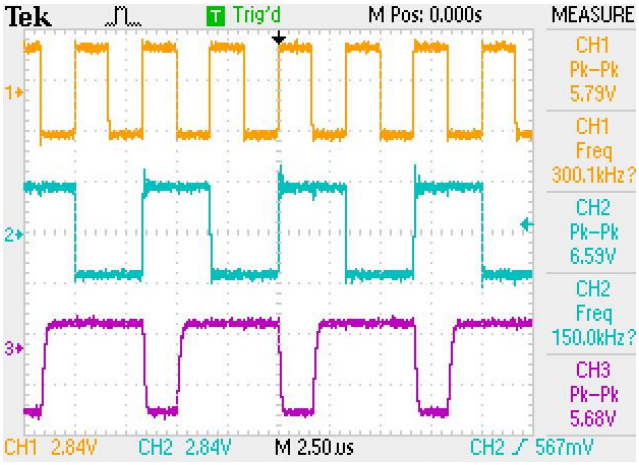


Fig. 2.12 Case 1: NAND Gate Experiment at 300kHz

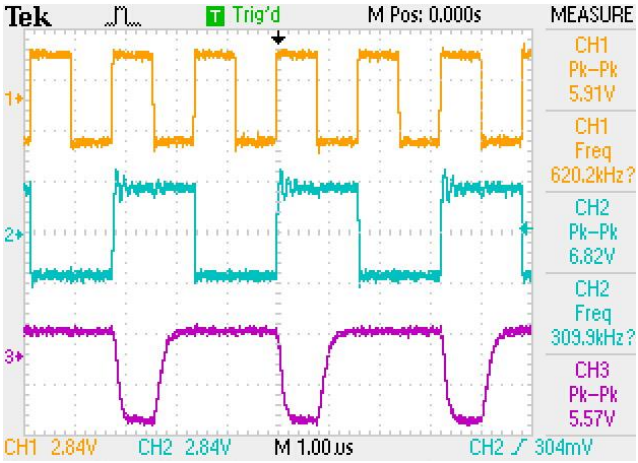


Fig. 2.13 Case 2: NAND Gate Experiment at 600kHz

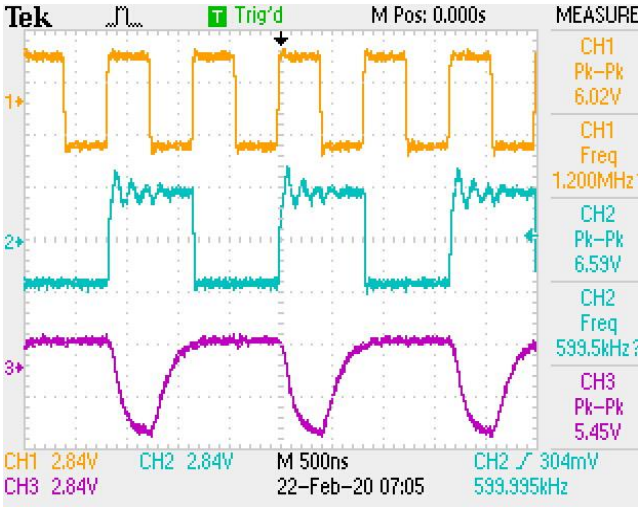


Fig. 2.14 Case 3: NAND Gate Experiment at 1.2MHz

2.4. DISCUSSION AND CONCLUSION:

The setup for the 2 input NAND gate at 300 kHz is shown in figure 2.4. A pulse wave function at 300 kHz was used as input A of the NAND gate. A frequency divider was used to out half the frequency of the previous signal to input B. Looking closely at figure 2.8, the simulation shows the correct output of the NAND gate where the output is only 0v when both inputs A and B are high at 5v. Comparing figure 2.8 to figure 2.12, the experimental results closely match that of the simulation results. The experimental results show poor values of voltage and noise in the signal. This is due to poor quality of our input oscilloscope probes.

The setup was then changed to have a 2 input NAND gate for an input pulse wave of 600 kHz and 1.2 MHz shown in figure 2.5 and figure 2.6. The simulation of 600 kHz is shown in figure 2.9 which agrees with the experimental results in figure 2.13.

Similarly, the simulation results of the 1.2 MHz pulse wave input in figure 2.10 agrees with the experimental results of the NAND gate with input 1.2 MHz pulse wave in figure 2.14.

Lastly, the vtc curve was generated by the setup in figure 2.7. The first input was set to a constant 5v DC. The second input was given a 5v 300 kHz pulse wave. The rise time of the first period was recorded as the vtc curve. The vtc curve is shown in figure 2.11.

In conclusion, the results agree with the function table of a 2-input NAND gate. The method of transistor sizing was correctly used to size the aspect ratios of the NMOS transistors both in the lab and in simulation. The results for all 3 frequency cases show the correct outputs. The purpose of creating a 2-input NAND gate with CMOS transistors was successful.

REFERENCES

[1] A. S. Sedra and K. C. Smith, Microelectronic circuits. New York: Oxford University Press, 2015.

[2] ECE lab manual

[3]