Digital to Analog Converter

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***Abstract*- In this lab, a combination of an op amp, NMOS transistors, and resistors were used to create a digital to analog converter circuit. The digital to analog converter will be 3-bit and will use the R-2R ladder design. The advantage of using this design is that some resistor values are twice the amount as other resistors, making our calculations simpler. This circuit must have a least significant bit of 1 V which means that the output voltage will increase by 1 V when the binary input increases by 1. The output voltage must start at 0 V and increase until 7 V is reached. In order to achieve this requirement, the resistor and reference voltage values must be calculated. Since there are no switches provided in class, NMOS transistors will be used as switches. Once the requirements were achieved, a pulse wave was inserted to the input to achieve a staircase like plot.**

I. INTRODUCTION

The purpose of this lab is to design a digital to analog converter circuit. DAC circuits convert digital signals into analog form which is a more naturally occurring type of signal. The basic circuit of the DAC uses an op amp, series and parallel resistors, and single pole double throw switches. The circuit in this lab is used to convert a 3-bit digital signal into a voltage value. The least significant bit voltage change must be 1 V for each binary change. Pulse waves will be used to simulate the different binary inputs which will start from "000" and end at "111". The final output voltage value must be 7 V. The R-2R circuit design will be used due to the small amount of resistors and switches used. The resistance ratio is 2, making the calculations easier. The lab also covers the use of R-2R ladders which reduce the amount of resistance values.

II. CIRCUIT THEORY

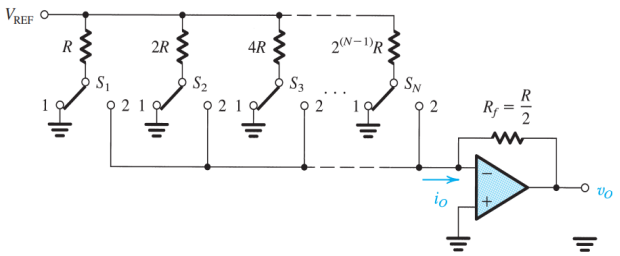

Fig. 1 A binary weighted D/A converter

A basic DAC circuit is shown in Fig. 1. Looking closely, the switch S_1 is controlled by the most significant bit, b_1. The current provided when b_1 is logic high is shown in (1). Each subsequent resistor provides a current

decreased by a factor of 2. Because the switches of the circuit are connected to virtual ground when they are closed, the current provided by each resistor remains constant.

$$i_o = V_{REF}/R \qquad (1)$$

The total current must pass through the resistor R_F as no current can go through the input terminals of the op amp. Therefore, the output voltage is calculated by (2).

$$v_o = 0v - i_o\left(\frac{R}{2}\right) \qquad (2)$$

The least significant bit has the highest resistance in the ladder. This is a necessary design to ensure that the weight of each bit is considered. The disadvantage of this circuit is that higher resolution circuits require increasingly larger resistors by a factor of 2^N where N is the number of bits.

The issue of increasingly large resistances is solved using R-2R ladders shown in Fig. 2. This circuit only requires the use of 2 resistance values . Looking closely at the circuit, for each node in the ladder, the total resistance seen to the right of each node is equal to 2R. Thus the following (3) is true.

$$I_1 = 2I_2 = 4I_3 = \cdots = 2^{N-1}I_N \qquad (3)$$

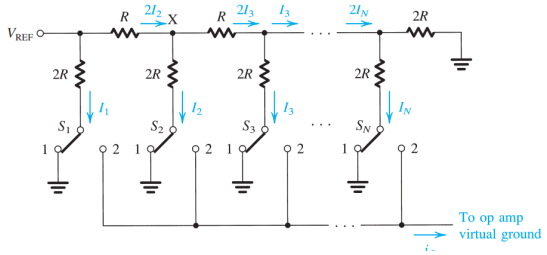

Fig. 2 An R-2R ladder

Thus, the total output current is also binary weighted. The output voltage can be calculated by (4).

$$V_o = \frac{R_f}{R}\sum_{i=0}^{N}\frac{b_i}{2^i} \qquad (4)$$

III. SIMULATION AND EXPERIMENTAL RESULTS

A digital to analog converter was built to be able to convert binary bits into a voltage value. The goal is to

have the least significant bit value equal to 1 V. This circuit can be seen in Fig. 3. The values that were calculated are R_6= R_7= 100 kΩ, R_2= 160kΩ, R_5= R_8= R_9= R_{10}= 200 kΩ, and V_{ref}= 5 V.

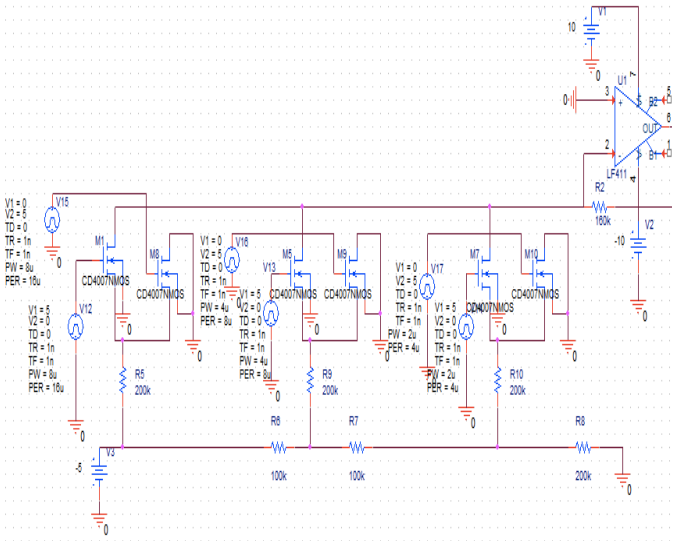

Fig. 3. A digital to analog converter circuit.

Voltage pulse waves were used to create the different binary values. When an input's value is 5 V, the binary value is considered high or '1'. If the input's value is 0 V, the binary value is considered low or '0'. The inputs used can be seen in Fig. 4., which shows the transition from 000 to 111. The binary value increases every 2 µs.

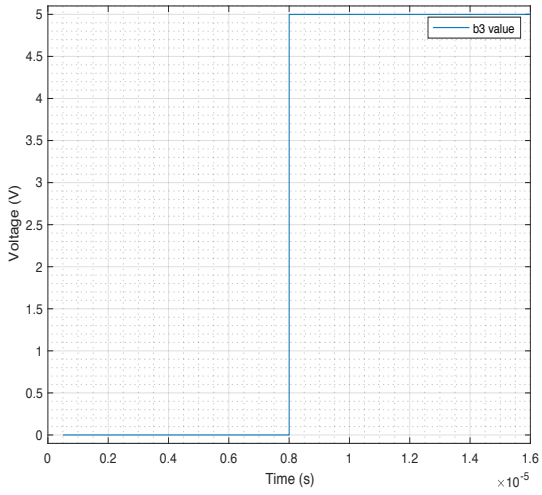

Fig. 4a. B_3 voltage input for the digital to analog converter.

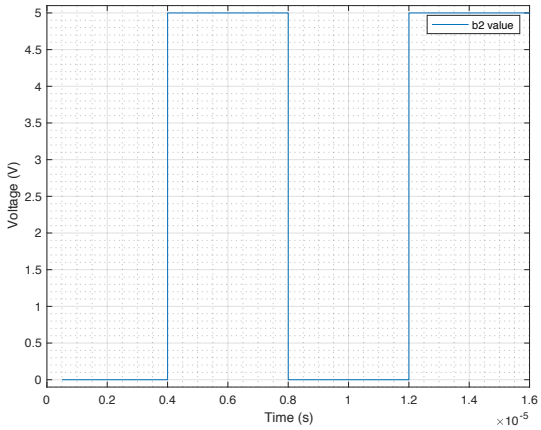

Fig. 4b. B_2 voltage input for the digital to analog converter.

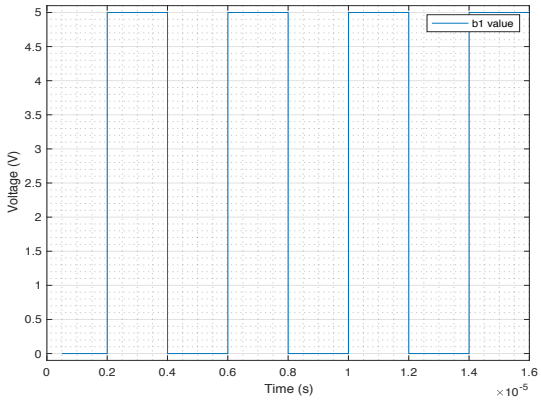

Fig. 4c. B_1 voltage input for the digital to analog converter.

The voltage output can be seen in Fig. 5. The voltage can be seen to change by 1 V every time the binary value increases by 1. The binary value of 000 can be seen to be 0 V and the binary value of 111 can be seen to be 7 V. The output voltage value increases every 2 µs, which is the same amount of time the binary value increases.

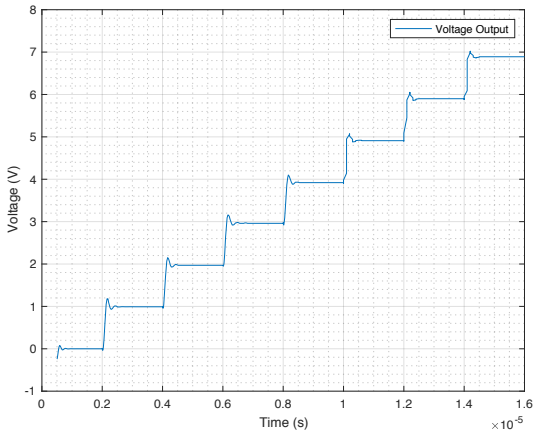

Fig. 5. Voltage output values of the digital to analog converter.

IV. DISCUSSION AND CONCLUSION

A digital to analog converter circuit was designed to have a least significant bit value of 1 V. This was designed by using specific resistor values. Voltage pulse waves were used to simulate the different binary values. A maximum value of 7 V was achieved but then lowers to 6.9 V. This is known as a unipolar glitch and occurs when one voltage switches to another. This occurs in digital to analog converters. One way to get rid of the glitch energy is to build a deglitching filter to lower the glitch energy.

The binary values change every 2 μs, which causes the output voltages to increase by 1 V every 2 μs. This transition was previously less than 1 μs. This caused a problem, as the voltage values didn't look like a staircase but more of a triangle. The time was changed to 2 μs and the problem was fixed.

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