CMOS RING OSCILLATION AND CLOCK GENERATION DESIGN, SIMULATION AS WELL AS ANALYSIS

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Abstract:

In this experiment, we will be exploring the effect of connecting inverters in series and having the last inverter act as a feedback. There will be four test cases for this experiment, 3, 5, 7, 9 ring oscillation. We will observe how the frequency is affected by the number of inverters and capacitors.

Keywords:

NMOS, PMOS, Inverter, Ring Oscillator, frequency, capacitor.

3.1 INTRODUCTION

We know that an inverter or a not gate outputs the opposite of the input; a logic '1' input results to a logic '0' output. When we put these inverters in series, we create a ring oscillator, however it is required to be in an odd-number series connection. In this lab we do a 3,5,7, and 9 ring oscillators. Figure 3.1 illustrates the circuit.
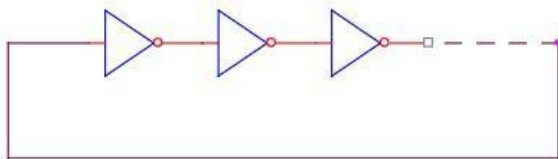

Fig. 3.1 Ring Oscillator Circuit

Since we have to construct various CMOS and PMOS in series we used the schematic in Figure 3.2 as reference. Again we had to connect 3,5,7, and 9 ring oscillators.
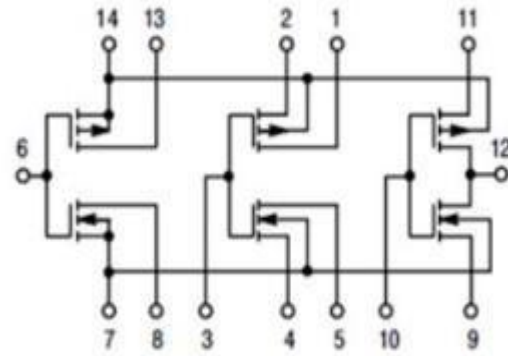

Fig. 3.2 CD4007 Pin Layout

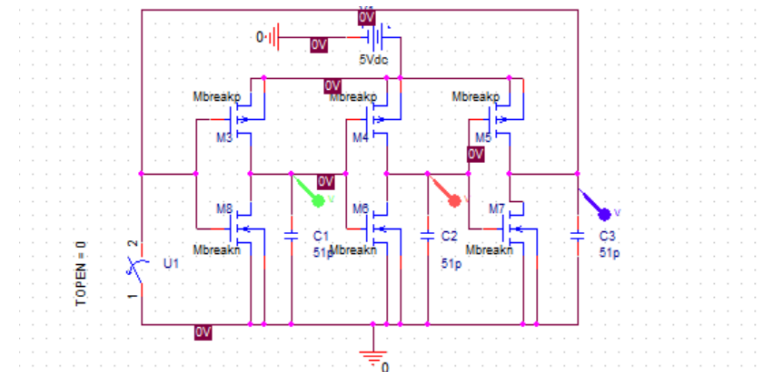## 3.2 PROCEDURES, SIMULATION AND EXPERIMENTAL SET-UP
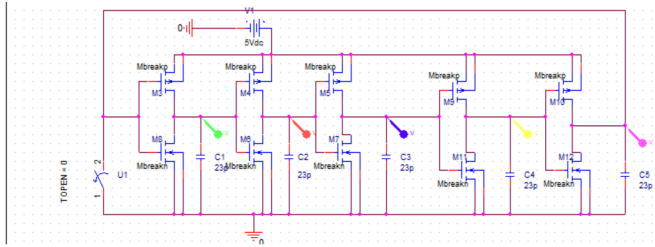

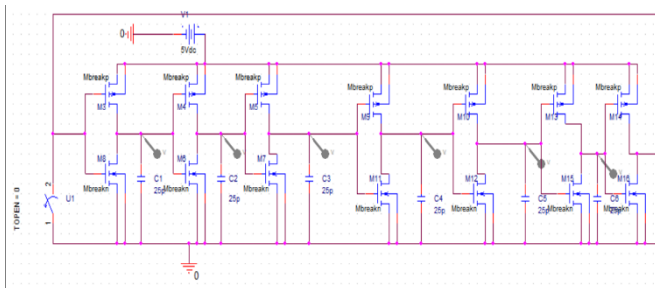Fig. 3.3 Case 1: 3 Ring Oscillator

Fig. 3.4 Case 2: 5 Ring Oscillator

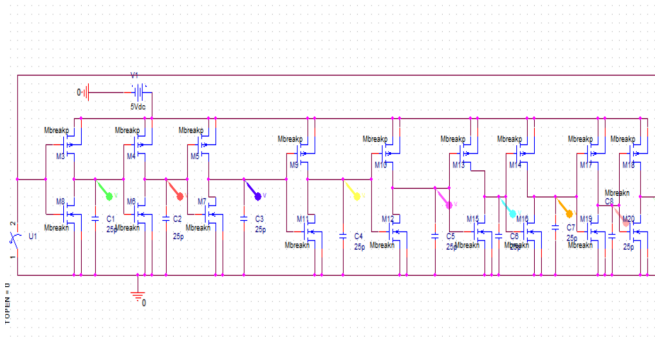Fig. 3.5 Case 3: 7 Ring Oscillator

Fig. 3.6 Case 4: 9 Ring Oscillator
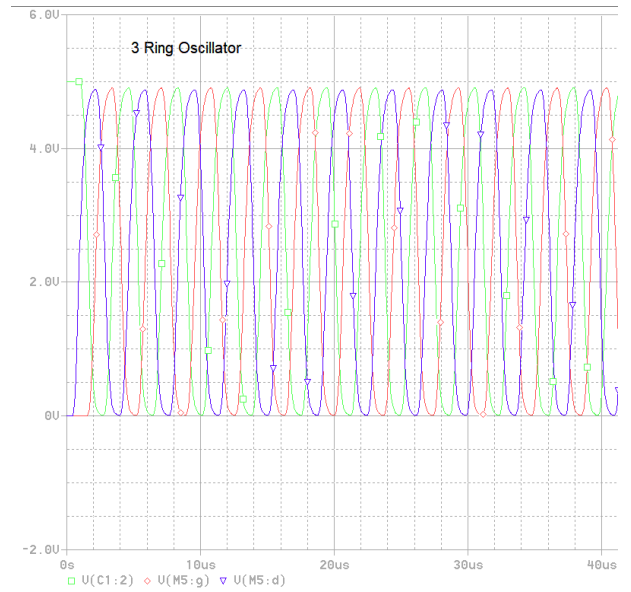
1.3 SIMULATION AND EXPERIMENTAL RESULTS

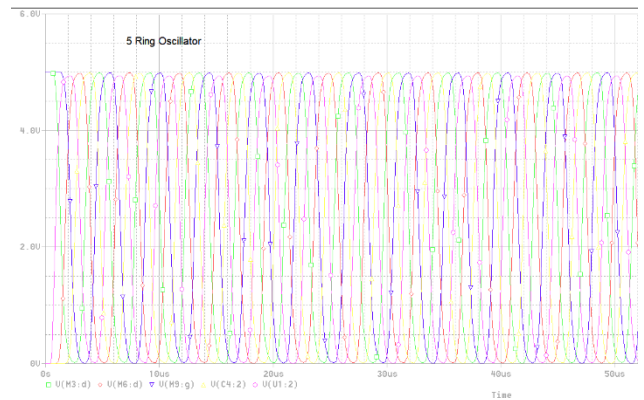Fig. 3.7 Case 1: 3 Ring Oscillator

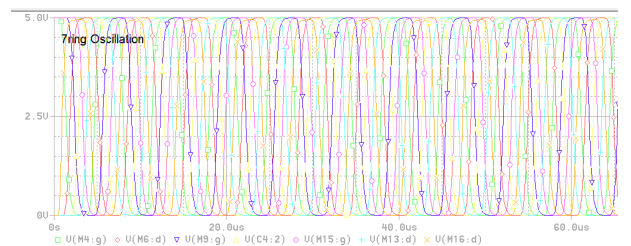Fig. 3.8 Case 2: 5 Ring Oscillator
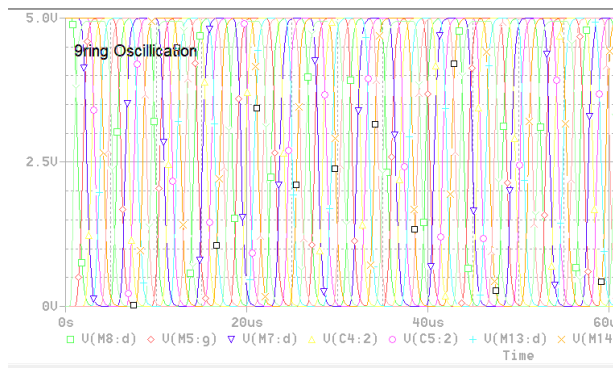

Fig. 3.9 Case 3: 7 Ring Oscillator

Fig. 3.10 Case 4: 9 Ring Oscillator

1.4. DISCUSSION AND CONCLUSION:

All in all, the third lab utilized a ring oscillator and demonstrated the affects it has on the frequency when inverters are in series. We used a total of 4 cases that is, 3,5,7, and 9 ring respectively. As the number of inverters increased we saw a different number of waveforms as results of the inverters.

REFERENCES

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[2]
    https://www.electronics-tutorial.net/Digital
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