Sample and Hold Circuits

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***Abstract*- In this lab, a combination of op amps, an NMOS transistor and a capacitor were used to create a sample and hold circuit. The sample and hold circuit that was built must sample the input signal for 10 µs and hold the instantaneous voltage level for 5 µs. The input signal will be a sinusoidal wave with a frequency of 10 kHz. In order to achieve this requirement, the capacitor value must be changed accordingly. This circuit must be built with the components found in class. This means that the switch must be built using an NMOS transistor. Each op amp will be used to create an amplifier with a unity gain of one. This means that the op amps will be used as a buffer. Once the requirements are achieved, different parameters will be measured. The parameters that will be measured will be the maximum and minimum input signal levels, supply voltage gain, and the limits of frequency of operation.**

I. INTRODUCTION

The purpose of this lab is to design a sample and hold circuit in order to track and hold an analog input. A clock is used to sample the input at a rate of 10 µs and hold the voltage level for 5 µs. The most common use of Sample and Hold circuits is its inclusion in an ADC because they provide stable and constant values of an input voltage. An unstable input during an analog to digital conversion could result in error. This lab also covers the operating performance of the sample and hold circuit. Different parameters will be measured with the circuit built for the given requirements.

II. CIRCUIT THEORY

The sample and hold circuit uses pass transistor logic. Looking closely at Fig. 1., the NMOS transistor is used as a switch controlled at node C.

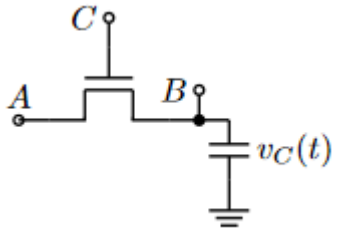

Fig.1 NMOS Switch charging a capacitor

When node C is logic high, the NMOS is turned allowing the input voltage at node A to charge the capacitor at node B. Fig.2 shows an input at node A and its corresponding output when the switch is closed. Because the capacitor charge and the voltage at node B increases, the NMOS transistor eventually enters the cutoff region upon increasing reaching $V_{GS} - V_t$. This means that the track voltage of the Sample and Hold circuit will have an offset and not track perfectly.

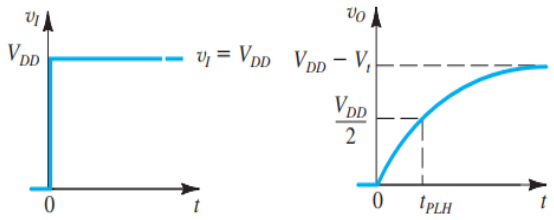

Fig. 2. Charging of the capacitor in PTL

After the capacitor is charged and the voltage at node C is set to logic low, the NMOS transistor is cutoff and the charges of the capacitor have nowhere to go. This results in the holding of the voltage regardless of the input at node A. This flat line effect can be seen in Fig.3 of the output voltage.

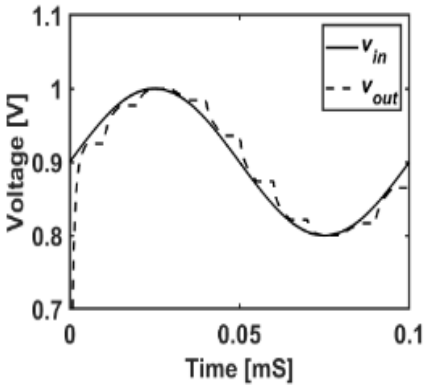

Fig. 3. Hold effect of cutoff NMOS

When the clock voltage at the gate returns to logic high, two case can happen. In the first case, the voltage at node A is higher than node B in which the capacitor will gain more charges and the voltage at node B will follow the increase in the voltage of A. The second case is when the voltage at node A has dropped and so the capacitor will discharge and the voltage at node B will follow the drop.

Another key element in sample and hold circuits is the unity gain buffers. Fig. 4 shows the use of the unity gain buffers at the input and output of the circuit. The unity gain buffers supply the circuit with high input and output impedance that reduce the leakage current that occurs from the capacitor. This will prevent the capacitor from prematurely discharging.

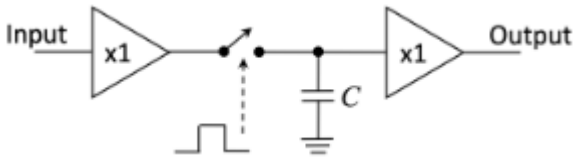

Fig. 4 . Unity gain buffers in Sample and Hold circuit

III. SIMULATION AND EXPERIMENTAL RESULTS

A sample and hold circuit was built to be able to sample an input for 10 µs and hold the value for 5 µs. This circuit is shown in Fig. 5. The values that were calculated is C = 1 nF and the values for the clock is period = 10 µs, pulse width = 5 µs, time fall = 0.1 ns, time rise = 0.1 ns, time delay = 0, V_1 = 0 V, and V_2 = 5 V.

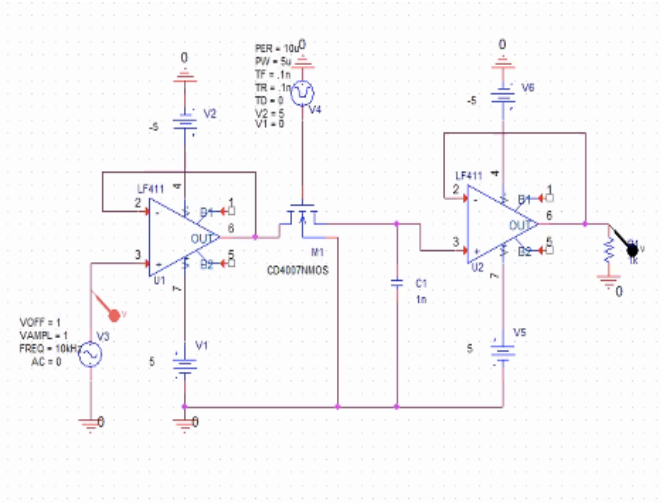

Fig. 5. A sample and hold circuit.

The results for the sample and hold circuit can be seen in Fig. 6.

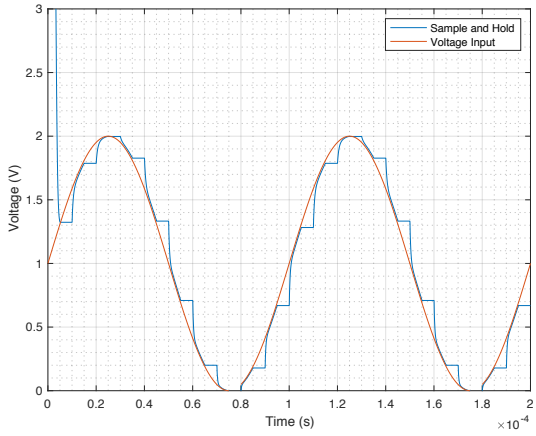

Fig. 6. Sample and hold results

The parameters for the sample and hold circuit were tested. The lowest input for the supply voltage was 2.5 V as seen in Fig. 7. The sample and hold part does not reach the input voltage.

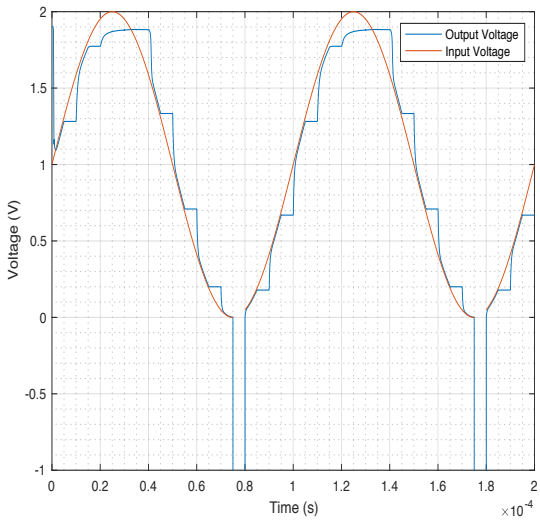

Fig. 7. 2.5 V Supply Voltage

The frequency parameters in which the sample and hold circuit worked were tested. The maximum frequency can be seen in Fig. 8. and the minimum frequency can be seen in Fig. 9. The sample and hold cannot keep up with the input voltage due to the high frequency. The sample and hold doesn't hold accurate values for the low frequency.

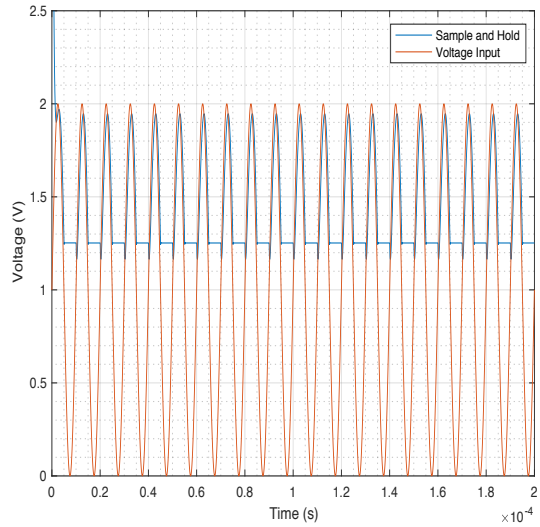

Fig. 8. 100 kHz input frequency.

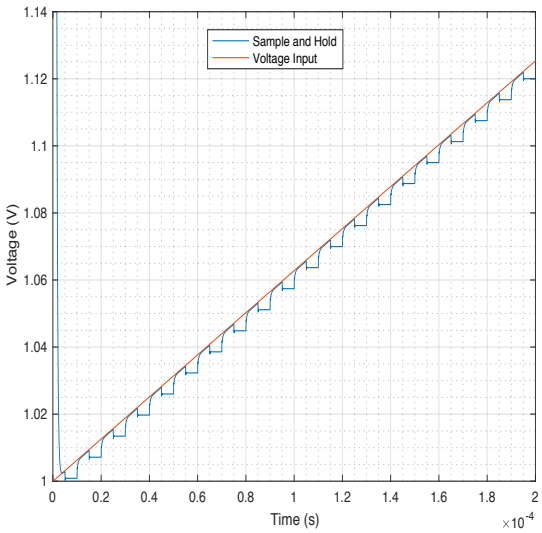

Fig. 9. 100 Hz input frequency.

The maximum voltage input that the sample and hold circuit can handle is 4 V as seen in Fig. 10. The sample and hold samples the wrong value once the voltage hits -3 V.

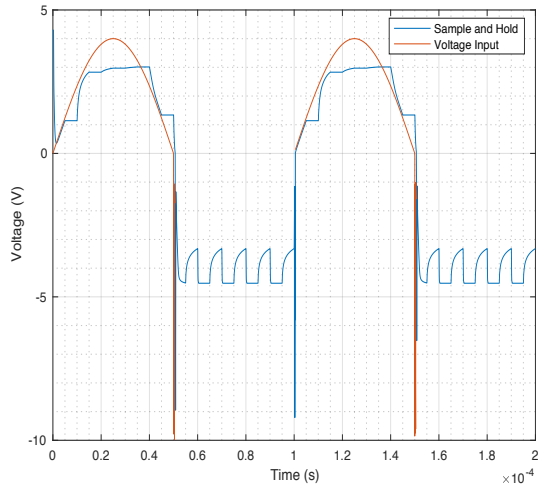

Fig. 10. Maximum input voltage

IV. DISCUSSION AND CONCLUSION

The voltage offset for the input must have a value of 1. This is because the sample and hold cannot get values below -0.45 V. This has something to do with the NMOS threshold voltage. To fix this, a PMOS transistor can be attached to the NMOS transistor to form a transmission gate. This is the reason why the maximum input voltage is 4 V. The maximum frequency that the input voltage can be is 100 kHz because the sample and hold cannot keep up with it and start sampling wrong values. The minimum frequency is 100 Hz because the sample and hold circuit holds the wrong value. Lowering the input supply voltage to the minimum 2.5 V causes the sample and hold circuit to not be able to reach the peak of the input voltage. The simulation allowed the maximum input voltage to have a big value but the data sheet for the LF411 op amp shows the maximum is 37 V. The simulation allowed the value to be in the hundreds and thousands but that will be bad in real life.

ACKNOWLEDGMENTS

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Ridge- 50% Lab, Introduction and Circuit Theory, Simulation and Results

REFERENCES

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