Fall 2019

California State University, Northridge

Department of Electrical and Computer Engineering

ECE 526L

Experiment # 2
Structural Modeling of a JK Flip-Flop

Sept. 19, 2019

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I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

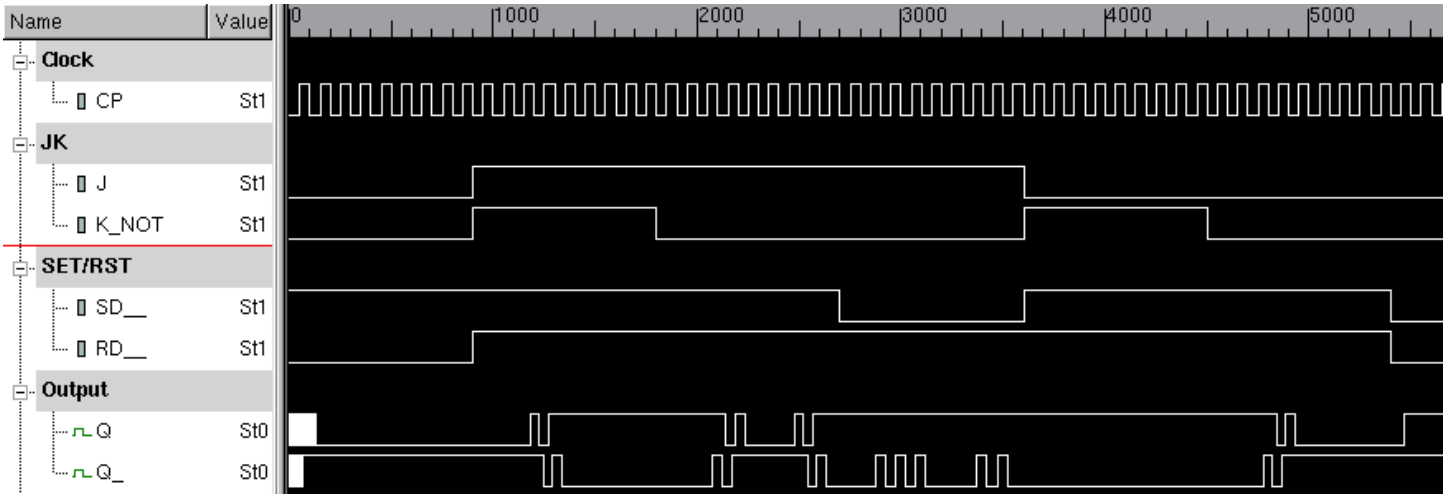
Name (printed) _____

Name (signed) _____

Date _____

Analysis

Figure 1. JK_FF Waveform at 50% Duty cycle

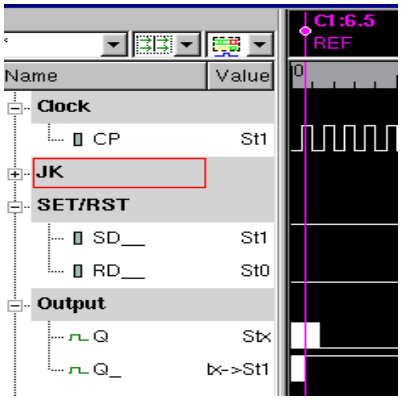


The first input that is checked is RD_NOT = 0 and SD_NOT = 1 which is an asynchronous RST. Looking closely at figure 2, The output Q_ is given after 6.5 ns, which makes sense because RD_NOT feeds a value of 0 right into Q_'s NAND Gate, therefore Q_ is logic high regardless of the other inputs. This NAND gate has 3 inputs and is a primary output, which overall has a total delay of $\mathbf{T_{NAND4}}$ = 6.5 ns.

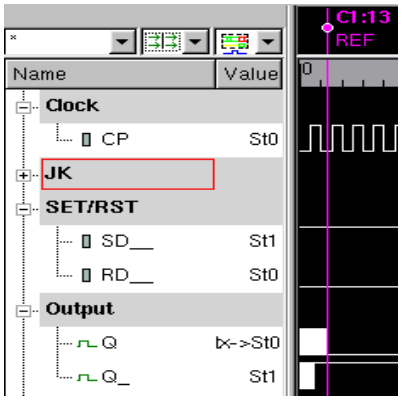
For output Q of RST, because SD_NOT = 1, the NAND4 needs to wait for Q_ and N2. NAND2 also has an input of 0 from CP, therefore no other gates need to be checked. NAND2 has a gate delay of 5.5 ns, which is less that Q_'s NAND5 of 6.5 ns, therefore Output Q has a delay of $\mathbf{T_{NAND4} + T_{NAND5}}$ = 13ns.

Figure 2. RST output delays

6.5ns



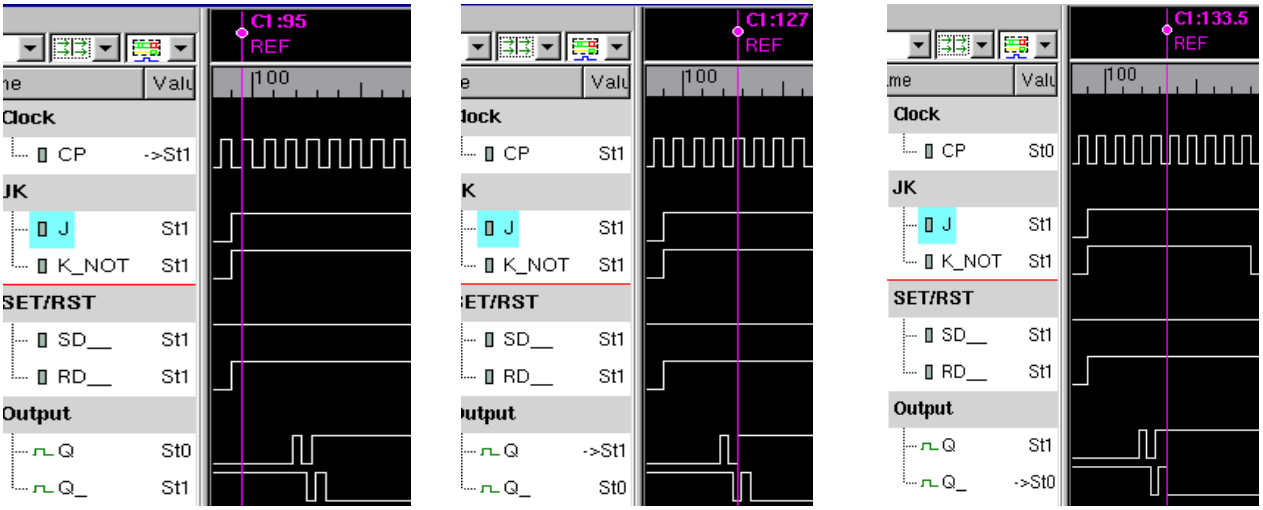
13ns



The second input checked is J = 1, K_NOT = 1, SD_NOT = 1 and RD_NOT = 1, which is a Load 1 where Q = 1 is expected. This function is synchronous, so it starts at the next clock pulse. Looking closely at the outputs of figure 3, the feed back between Q and Q_NOT cause the outputs to bounce back and forth between 0's and 1's. The Output completely stabilizes to the expected response after about 38.5 ns.

Figure 3.1 Load 1 start time and output delays

Start: 95ns 127ns 133.5ns

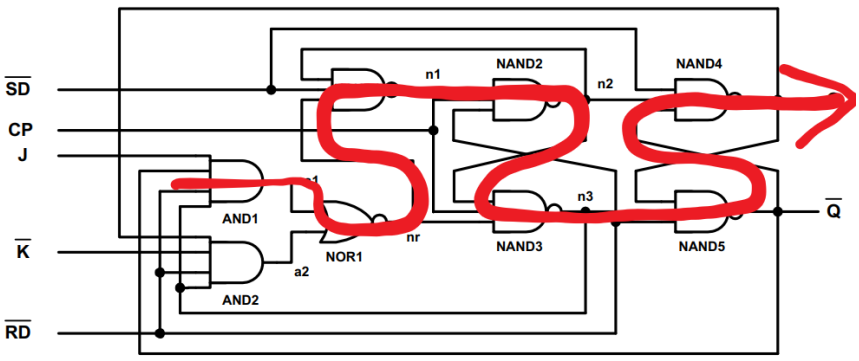


One way to determine response time is to analyze the longest path from an input to an output. Looking at Figure 4, the longest path from A1 to Q is seen. The total sum of these delays is 35.5 ns.

$$F = \frac{1}{T} = \frac{1}{35.5\,ns} = 28571\,MHz$$

Figure 4. Propagation delay for the longest path

Gate/Wire	Delay (ns)	Fanout (ns)
AND1/ a1	3.5	1
NOR1/ nr	1.5	2
NAND1/ n1	2.5	1
NAND2/ n2	2.5	3
NAND3/ n3	2.5	3
NAND5/Q_n	2.5	4
NAND4/Q	2.5	4
Total JK_FF	35.5 ns	

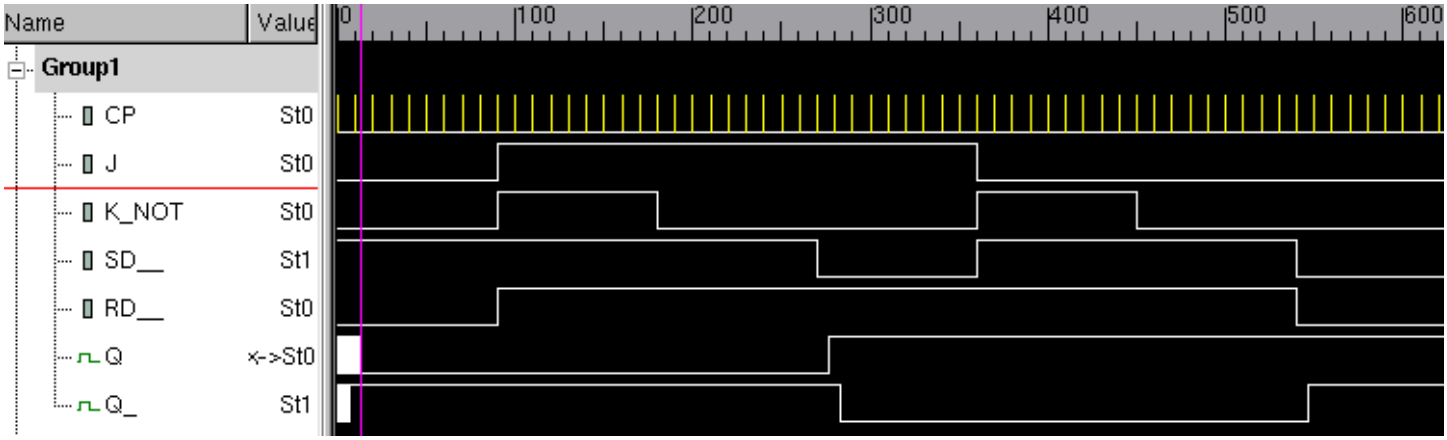


The most common and largest time delay found in the simulation is a total delay of 38.5 ns. The operating frequency of the circuit can be calculated as the following.

$$F = \frac{1}{T} = \frac{1}{38.5\,ns} = 25.96\,MHz$$

The simulation is a much more accurate representation of the Flip flop's operating frequency because it takes into account the previous inputs impact as previous conditions and as feedback. These conditions control can both shorten and lengthen the time it takes to read the correct output.

Figure 5. JK_FF Waveform @ 10% duty cycle



The clock pulse was set to a duty cycle of 10%. Looking closer at Figure 5, some of the outputs are not correct at all in the waveform. For example, where J = 1; K_NOT = 1; SD__ = 1; RD__ = 1;. A value of Q = 1 is expected,However, the value is held even over multiple clock cycles. Another thing that is missing is the bouncing of values between Q and Q_. This may be occurring because there is not enough delay to allow for propagation of the outputs. The higher duty cycle is needed because the positive level of the clock allows for propagation between Q and Q_. If a higher delay is needed to get the correct results, then the Operating Frequency must decrease as the duty cycle is decreased.

```
/*=========================================================
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JK_FF.v
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=========================================================*/
// Reference of 1 ns, accuracy of .1 ns;
`timescale 1 ns / 100 ps
//Define delays of inputs and fanouts
`define TIME_DELAY_1 1.5
`define TIME_DELAY_2 2.5
`define TIME_DELAY_3 3.5
`define FANOUT1 1.0
`define FANOUT2 2.0
`define FANOUT3 3.0
`define PRIMARY 4.0
module JK_FF(Q_,Q,J,K_NOT,CP,RD__,SD__);
    //outputs inputs
    output Q_,Q;
    input J,K_NOT,CP,RD__,SD__;
    //signal type & declare fanout delays
    wire #`PRIMARY Q_,Q;                          //Primary Output = 4 ns
    wire J,K_NOT,CP,RD__,SD__;
    //variables   & fanout delays
    wire #`FANOUT1 N1,A1,A2;                      //FANOUT1 = 1 ns
    wire #`FANOUT2 NR;                            //FANOUT2 = 2 ns
    wire #`FANOUT3 N2, N3;                        //FANOUT3 = 3 ns
    //netlist
    // 4 inputs gate delay = 3.5 ns
    and #`TIME_DELAY_3 (A1,N3,RD__,Q_,J);
    and #`TIME_DELAY_3 (A2,Q,K_NOT,RD__,N3);
    // 2 inputs delay = 1.5ns
    nor #`TIME_DELAY_1 (NR,A1,A2);
    nand #`TIME_DELAY_1 (N1,N2,NR);
    // 3 inputs delay = 2.5ns;
    nand #`TIME_DELAY_2 (N2,N1,CP,RD__);
    nand #`TIME_DELAY_2 (N3,N2,CP,NR);
    nand #`TIME_DELAY_2 (Q,SD__,N2,Q_);
    nand #`TIME_DELAY_2 (Q_,RD__,Q,N3);
endmodule
```

```
/*=========================================================
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TB_JK_FF.v
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`timescale 1 ns/ 100 ps;
`define DELAY #45

// Defines logging functions
`define CHECK_OUTPUT #45 $strobe("   OUTPUT: Q = %b, Q_ = %b,
@TIME:%0d",Q,Q_,$time)
//Delay of CHECK_OUTPUT allows for propogation
`define WRITE_INPUT $write("    INPUT: J = %b, K_NOT = %b, ",J,K_NOT)
`define DISPLAY_INPUT $display("     INPUT: J = %b, K_NOT = %b",J,K_NOT)
`define DISPLAY_TIME $display("TIME:%0d",$time);

//Defines test input functions
`define HOLD  J = 1'b0; K_NOT = 1'b1; SD__ = 1'b1; RD__ = 1'b1;
`define TOGGLE J = 1'b1; K_NOT = 1'b0; SD__ =1'b1; RD__ = 1'b1;
`define RST  SD__ =1'b1; RD__ = 1'b0;
`define LOAD0  J = 1'b0; K_NOT = 1'b0; SD__ = 1'b1; RD__ = 1'b1;
`define LOAD1  J = 1'b1; K_NOT = 1'b1; SD__ = 1'b1; RD__ = 1'b1;
`define SET   SD__ = 1'b0; RD__ = 1'b1;
`define INDETERMINATE SD__ = 1'b0; RD__ = 1'b0;

//Test bench module
module TB_JK_FF();
    //inputs
    reg CP,SD__,RD__,J,K_NOT;
    //outputs
    wire Q_, Q;
    //instantiate the JK_FF;
    JK_FF UUT(Q_,Q,J,K_NOT,CP,RD__,SD__);
  //Create the clock
    always begin
      #5.0 CP = !CP;
    end
//Start Inputs and Logging
//=========================================================
  initial
     $monitorb("     SET/RST: SD__ = %b , RD_ = %b",SD__, RD__);
```

```
    initial begin
     $vcdpluson;
      //initialize RST and CLK
      CP = 0;J = 0;K_NOT = 0; `RST
     `DISPLAY_TIME;
     `WRITE_INPUT;
     `CHECK_OUTPUT;
     //=================
     //test LOAD1
     `DELAY  `LOAD1
     `DISPLAY_TIME;
     `WRITE_INPUT;
     `CHECK_OUTPUT;
     //=================
     //test TOGGLE
     `DELAY  `TOGGLE // JK = 10, Q = Q_ = 0
     `DISPLAY_TIME;
     `DISPLAY_INPUT;// no need to check RD or SD
     `CHECK_OUTPUT;
     //=================
     //test SET
     `DELAY `SET     // SD = 1,  Q = 1
     `DISPLAY_TIME;
     `CHECK_OUTPUT;
     //=================
     //test HOLD
     `DELAY  `HOLD  // JK = 01, Q = Q = 0
     `DISPLAY_TIME;
     `WRITE_INPUT;
     `CHECK_OUTPUT;
     //=================
     //test LOAD0
     `DELAY  `LOAD0 // JK = 00, Q = 0
     `DISPLAY_TIME;
     `DISPLAY_INPUT;
     `CHECK_OUTPUT;
     //=================
     //test SET and RST at the same time.
     `DELAY `INDETERMINATE// SD = 1, RD = 1, Q = UNKNOWN
     `DISPLAY_TIME;
     `CHECK_OUTPUT;
     `DELAY $finish;
    end
endmodule
```

```
/*=========================================================
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lab2.log
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=========================================================*/
Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information.
Compiler version N-2017.12-SP2-2_Full64; Runtime version
N-2017.12-SP2-2_Full64;  Sep 19 09:27 2019
VCD+ Writer N-2017.12-SP2-2_Full64 Copyright (c) 1991-2017 by Synopsys Inc.
TIME:0
     INPUT: J = 0, K_NOT = 0,        SET/RST: SD__ = 1 , RD_ = 0
     OUTPUT: Q = 0, Q_ = 1, @TIME:45
TIME:90
     INPUT: J = 1, K_NOT = 1,        SET/RST: SD__ = 1 , RD_ = 1
     OUTPUT: Q = 1, Q_ = 0, @TIME:135
TIME:180
     INPUT: J = 1, K_NOT = 0
     OUTPUT: Q = 0, Q_ = 1, @TIME:225
TIME:270
     SET/RST: SD__ = 0 , RD_ = 1
     OUTPUT: Q = 1, Q_ = 0, @TIME:315
TIME:360
     INPUT: J = 0, K_NOT = 1,        SET/RST: SD__ = 1 , RD_ = 1
     OUTPUT: Q = 1, Q_ = 0, @TIME:405
TIME:450
     INPUT: J = 0, K_NOT = 0
     OUTPUT: Q = 0, Q_ = 1, @TIME:495
TIME:540
     SET/RST: SD__ = 0 , RD_ = 0
     OUTPUT: Q = 1, Q_ = 1, @TIME:585
$finish called from file "TB_JK_FF.v", line 85.
$finish at simulation time                6300
          V C S   S i m u l a t i o n   R e p o r t
Time: 630000 ps
CPU Time:       0.280 seconds;       Data structure size:   0.0Mb
Thu Sep 19 09:27:50 2019
```