

Fall 2019



California State University, Northridge

Department of Electrical and Computer Engineering

ECE 526L

Experiment # 5  
Scalable Multiplexer

October 17, 2019

Authors: Ridge Tejuco  
Professor: Ronald Mehler Ph.D

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

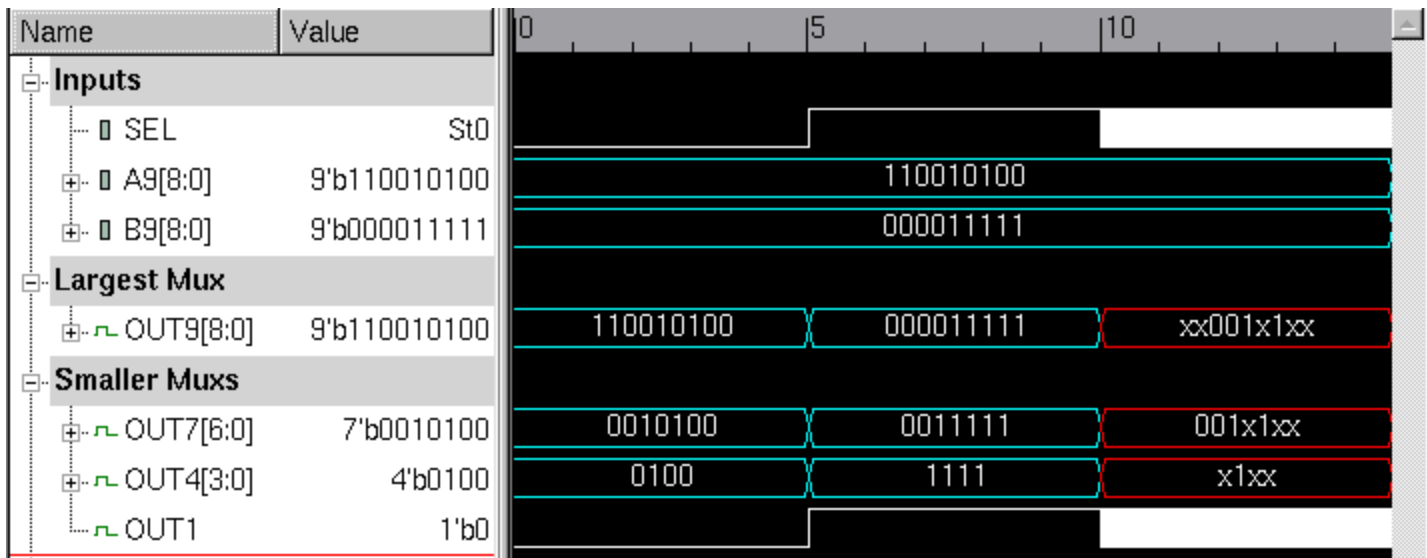
Name (printed) \_\_\_\_\_

Name (signed) \_\_\_\_\_

Date \_\_\_\_\_

## Analysis

Figure 1. Test bench waveform of the Scalable Multiplexer

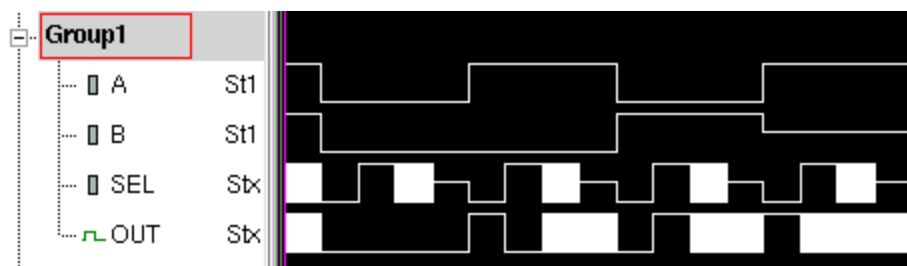


In Figure 1, the Largest Mux shows the output gets A9 when SEL = 0. The Largest Mux also shows the output gets B9 when SEL = 1.

When SEL = 1'bz, the output of the Largest Mux shows the values where A9 = B9, specifically at bits 2,4,5 and 6. When A does not equal B, the value of the output is unknown.

The smaller multiplexers of Figure 1 demonstrate the scalability of the design. For example, in the first 5 ns, OUT7 holds the least 7 bits of input A9, OUT4 holds the least 4 bits of A9, and OUT1 holds the least significant bit of A9.

Figure 2. Test bench waveform of Experiment # 1's multiplexer.



Looking at Figure 2, Experiment 1's waveform has similar output values. When both values of A and B are the same, it does not matter when SEL is high impedance or an unknown value, the output will take the value. This works exactly the same as experiment 5's multiplexer, even when checking high impedance.

```

/*=====
CSUN - ECE 526L
Ridge Tejuco
Oct 03 2019
=====
scale_mux.sv
GOALS
- Rescalable mux
- defaults to 1 bit [x]
- evaluates sel = 1'bx if bits a and b are the same [x]
=====*/
`timescale 1ns/1ns
module SCALE_MUX(A,B,SEL,OUT);
    parameter SIZE = 1;
    input wire [SIZE - 1:0] A,B;
    input wire SEL;
    output reg [SIZE - 1:0] OUT ;
    integer INDEX;
    always @(SEL,A,B) begin
        if(SEL == 1'b0)
            OUT <= A;
        else if (SEL == 1'b1)
            OUT <= B;
        else begin
            // If (A_index == B_index) then OUT_index = B_index
            for(INDEX = 0; INDEX < SIZE; INDEX++) begin
                if(A[INDEX] == B[INDEX])
                    OUT[INDEX] <= B[INDEX];
                else
                    OUT[INDEX] <= 1'bx;
            end
        end
    end
end
endmodule

```

```

/*=====
CSUN - ECE 526
Ridge Tejuco
Oct 03, 2019
=====
TB_SCALE_MUX.sv
GOALS
- Test 4 scalable mux
- test 4,9,7,1 (ID: 107497401)
=====*/
`timescale 1ns/1ns
module TB_SCALE_MUX ();
    parameter DELAY = 5;
    reg SEL;
    reg [8:0] A9,B9;
    wire [8:0] OUT9;
    wire [6:0] OUT7;
    wire [3:0] OUT4;
    wire OUT1;

    SCALE_MUX UUT1(A9[0],B9[0],SEL,OUT1);

    SCALE_MUX #(4) UUT4(A9[3:0],B9[3:0],SEL,OUT4);

    SCALE_MUX UUT7(A9[6:0],B9[6:0],SEL,OUT7);
    defparam UUT7.SIZE = 7;

    SCALE_MUX #(.SIZE(9)) UUT9(A9,B9,SEL,OUT9);

    initial begin
        $vcdpluson;
        SEL = 1'b0;
        A9 = 9'b110010100; B9 = 9'b000011111;
        #DELAY SEL = 1'b1;
        #DELAY SEL = 1'bx;
        #DELAY $finish;
    end
endmodule

```