

Fall 2019



California State University of Northridge
Department of Electrical & Computer Engineering

Experiment 10
Design of Common Source Amplifiers

ECE 340L
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Introduction:

The purpose of this experiment is to implement and verify the design of a common source amplifier under the following specifications.

$$A_v \geq |V_o/V_i| \geq 70$$

$$Z_i \geq 100 \text{ k}\Omega$$

$$Z_o \leq 20 \text{ k}\Omega$$

$$V_o \geq 6V_{p-p}$$

$$V_{cc} \leq 20V$$

This experiment will verify the theory behind MOSFETs discussed in lecture as well as cover the differences with the BJT.

Equipment:

Type	Model
Oscilloscope	Agilent Technologies DSO1002A
Digital Multimeter	Tektronix CDM250
Function Generator	Agilent 3322OA
Power supply	Hewlett Packard E3630A

Parts used:

QTY	Component	Value	Type
1	Resistor	2 k Ω	Carbon +/- 5%
1	Resistor	1 k Ω	Carbon +/- 5%
1	Resistor	100 k Ω	Carbon +/- 5%
1	Resistor	150 k Ω	Carbon +/- 5%
1	Resistor	480 k Ω	Carbon +/- 5%
1	Resistor	5.1 k Ω	Carbon +/- 5%
1	Resistor	20 k Ω	Carbon +/- 5%
2	Capacitor	10 μ F	Polypropylene film +/- 5%
1	Capacitor	100 μ F	Polypropylene film +/- 5%
1	Transistor	2N7000	MOSFET

Software:

Pspice
Microsoft Word
Microsoft Excel

Procedure & Results:

The circuit in Figure 1 was constructed to measure the g_m of the device. A V_G was incremented until the I_D current was inside equal to 0.5mA. The g_m was found using the following equation.

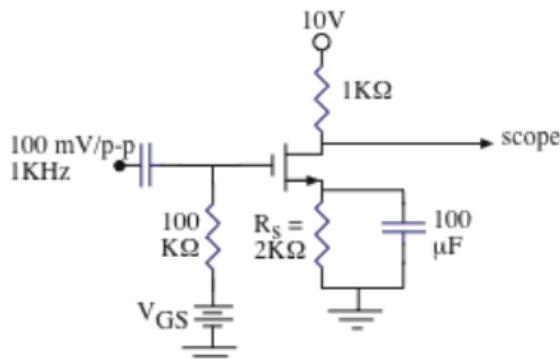
$$g_m = 0.01 * V_o$$

V_o was recorded for currents of 1,2, and 3 mA in Table 1.

g_m was graphed against I_D in Graph 1.

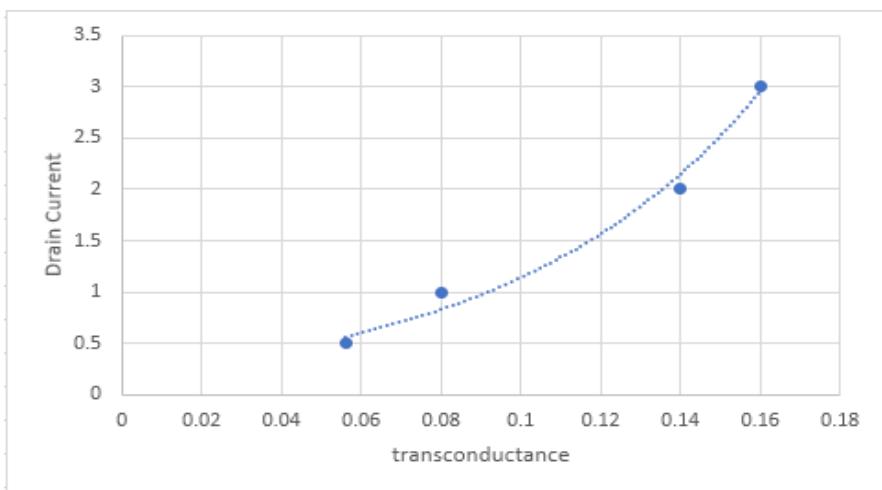
Figure 1.

Table 1.



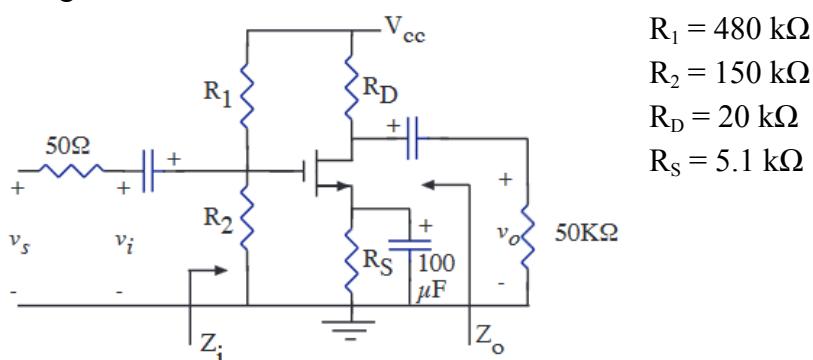
V_o	g_m	I_D
5.6	0.056	0.5
8	0.08	1
14	0.14	2
16	0.16	3

Graph 1.



The circuit in Figure 2 was constructed with the following resistance values.

Figure 2.



The circuit was first tested under a DC voltage. V_{GS} , V_{DS} , and V_{RD} were recorded in Table 2.

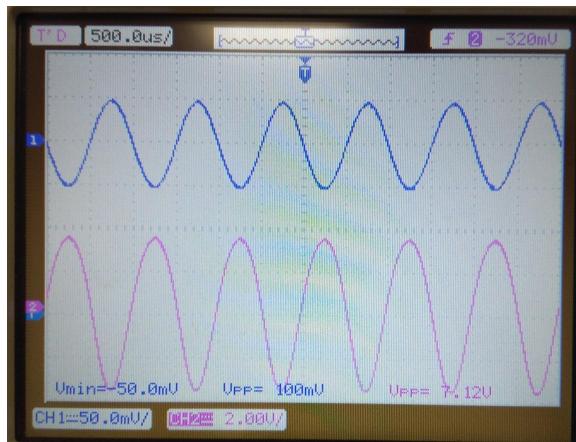
Table 2.

	V_{DS}	V_{RD}	V_D	V_{GS}	I_D
calc	7	10	10	2.19	0.5
meas	6.75	10.87	9.48	2.1	0.54
% error	3.6%	8.7%	5.2%	4.1%	8.0%

The calculated Q point was $V_{DS} = 7\text{V}$ and $I_D = 0.5 \text{ mA}$. The measured values for the bias of the transistor are significantly close to the calculated. However, the % error for current and voltage across the drain resistor are slightly high. This is probably due to the nominal value of the resistance being higher than expected.

The input and output voltages were measured and shown in Oscilloscope 1 and used to calculate the voltage gain. The measured gain meets the required specification of $A_v \geq |V_o/V_i| \geq 70$.

Oscilloscope 1.

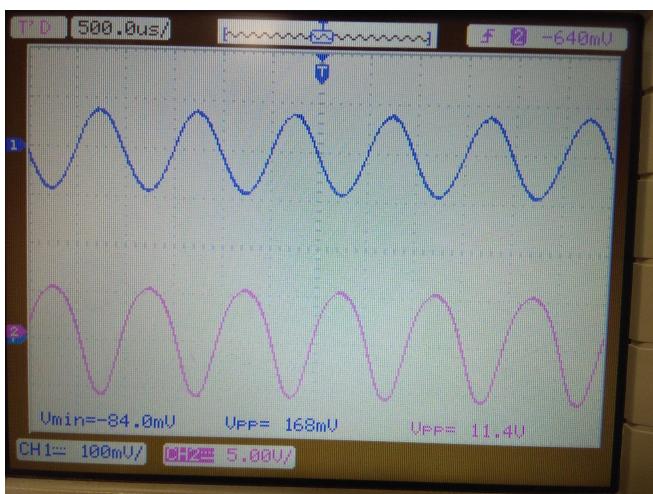


$$A_v = \frac{7.12 \text{ V}}{100 \text{ mV}} = 71.2$$

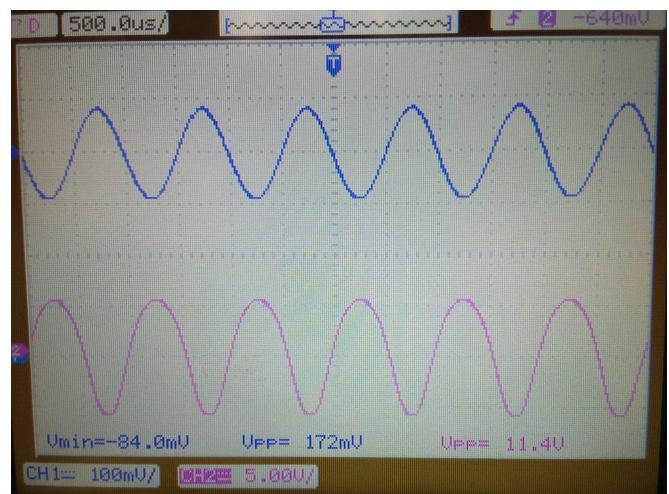
The input signal was then increased to determine the point of distortion. These points are shown below in Oscilloscope 2. Distortion starts to occur at an input of 168 - 172 mV and an Output of 11.4 V where the negative values of output voltage are clipped.

Oscilloscope 2.

a.) Before distortion



b.) After distortion



The input impedance of the design was found by inputting a series resistor value between the input and the amplifier. Until the value was dropped to $\frac{1}{2}$ of the initial output voltage. The following equation was used.

$$Z_i = \frac{R_s V_2}{V_1 - V_2} = \frac{R_s V_2}{2V_2 - V_2} = \frac{R_s V_2}{V_2} = R_s$$

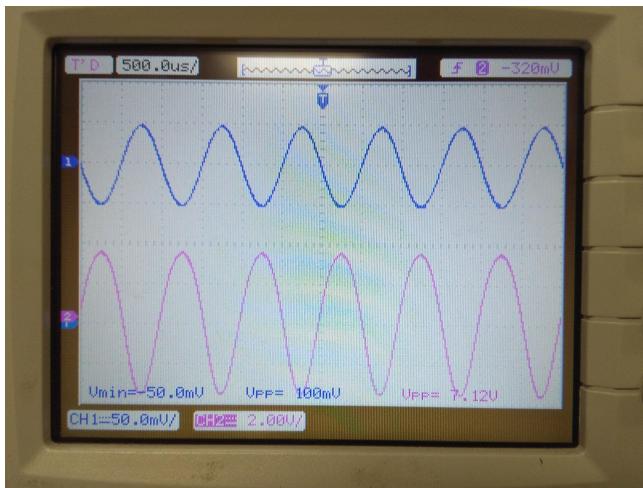
Oscilloscope 3 displays the results. The half output voltage occurred at a value of about $120\text{k}\Omega$. In the design, the calculated input impedance was found by the following.

$$R_{\pi} = \infty$$

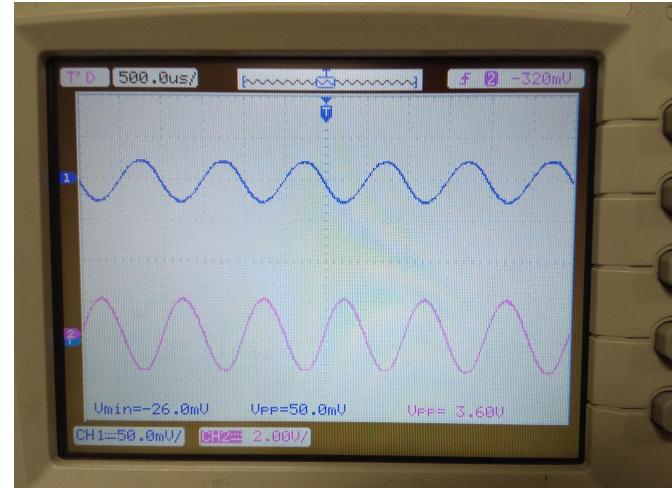
$$Z_i = R_1 || R_2 || R_{\pi} = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{480k * 150k}{480k + 150k} = 114\text{k}\Omega$$

Oscilloscope 3.

a.) initial output voltage



b.) half output voltage



A similar procedure was done for output impedance. The $50\text{k}\Omega$ resistor was removed from the load and the output voltage was measured to be about $9.4\text{V}_{\text{P-P}}$. A resistor was placed at the load until the output voltage dropped to exactly $\frac{1}{2}$ the initial voltage. $\frac{1}{2}$ Output voltage occurred at about $14.7\text{k}\Omega$. The results were shown in Oscilloscope 4.

$$Z_o = \frac{R_L(V_1 - V_2)}{V_2} = \frac{R_L(2V_2 - V_2)}{V_2} = \frac{R_s V_2}{V_2} = R_s$$

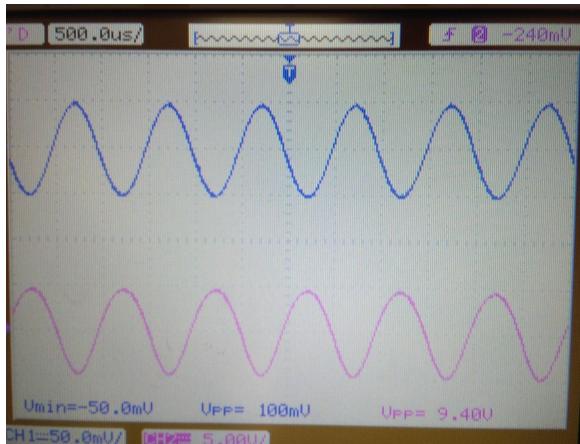
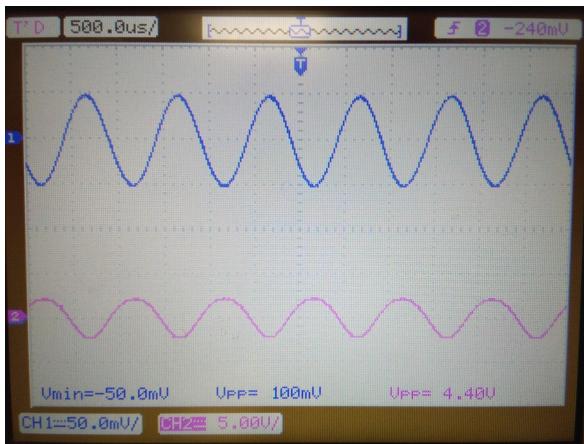
The output impedance of the design was calculated by the following.

$$Z_o = R_D || R_L = \frac{R_D R_L}{R_D + R_L} = \frac{20k * R_L}{20k + R_L} = 14.3\text{k}\Omega$$

The input impedance gets closer to $20k\Omega$ as R_L increases and has a minimum of 0.

Oscilloscope 4.

a.) initial output voltage

b.) $\frac{1}{2}$ output voltage

The $50\text{k}\Omega$ resistor was reconnected back into the circuit and the function generator set back to a $50 \text{ mV}_{\text{P-P}}$ sine wave at 1kHz frequency. The frequency was dropped until the voltage was about 3 dB less , approximately to power of $-\frac{1}{2}$, than initially.

For measuring voltage, the dB equation is the following.

$$(N)_{\text{dB}} = 20 \log_{10}(V/V_o)$$

In order to increase a value by 3dB , it is divided by the square root of 2.

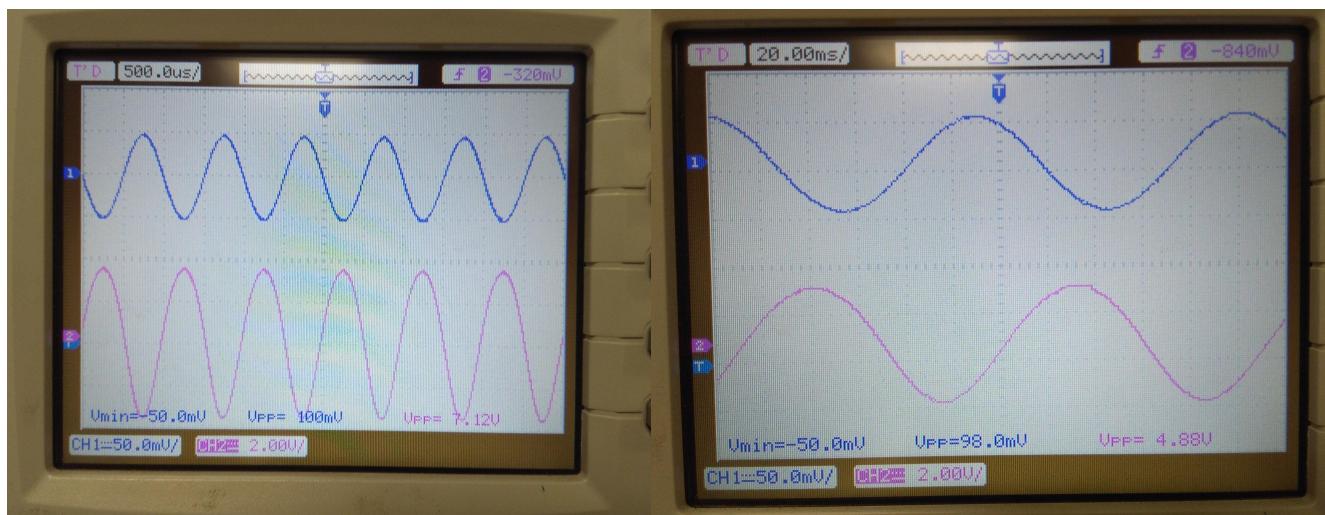
$$V_o = 7.12 \text{ V} / \sqrt{2} = 5 \text{ V}$$

Due to inconsistency of constantly changing values, the closest voltage measured was 4.88 v at 9 Hz .

The results were displayed in Oscilloscope 5.

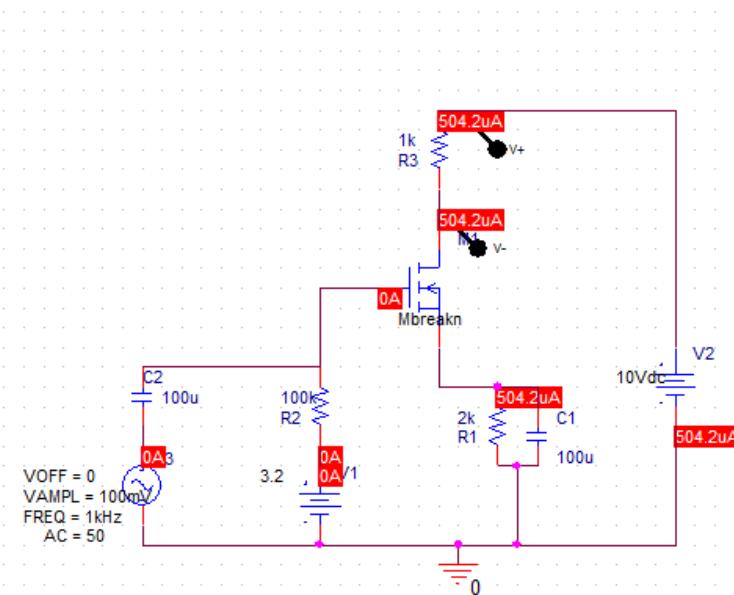
a.) 1 kHz

b.) 9 Hz



The first circuit was constructed and simulated in Pspice 1.

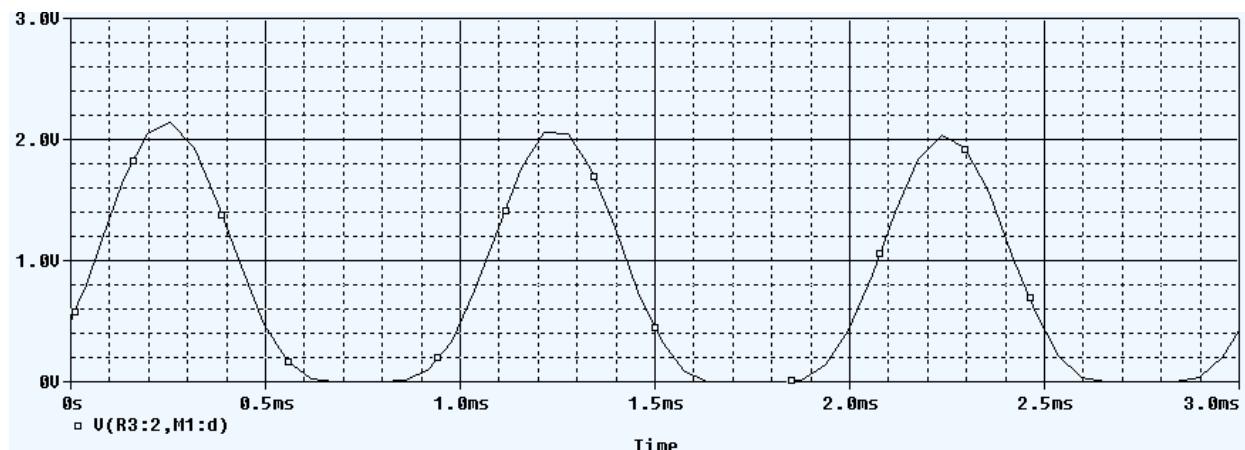
Pspice 1.



The voltage was measured across the 1k resistor.

An I_D of 500 mA was found at $V_{GS} = 3.2$ v and the V_{RD} was measured in Simulation 1.

Simulation 1.



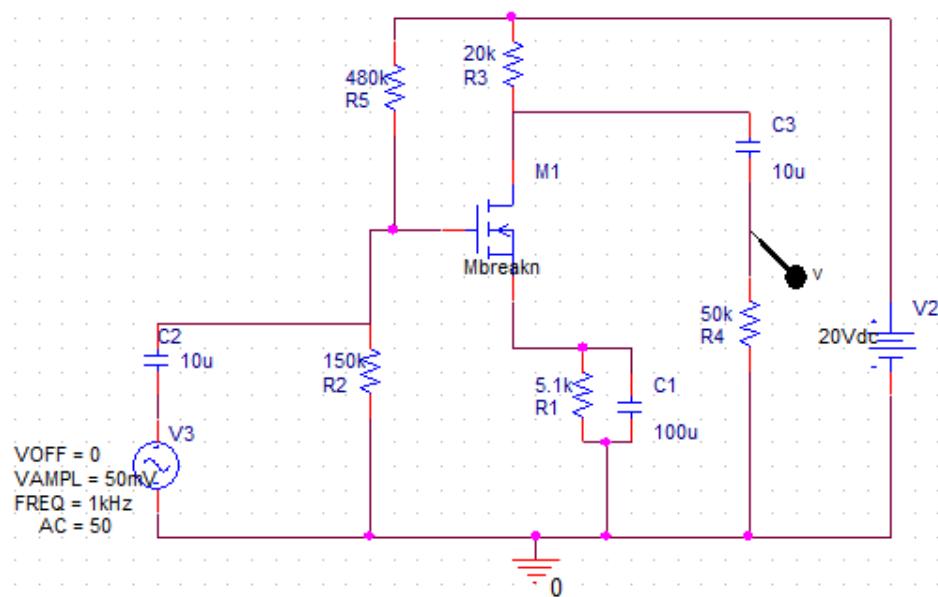
The simulation was repeated for 1, 2 , and 3 mA and the results were displayed in Table 3.

Table 3.

V_{gs} (V)	I_D (mA)	V_o (V)	gm (S)
3.2	0.5	2.1	0.021
4.3	1	3.1	0.031
6.3	2	4.6	0.046
8.3	3	3.2	0.032
9	3.3	0.7	0.007

The second circuit was simulated in Pspice 2. The output was displayed in Simulation 2.

Pspice 2.



Simulation 2.

