CMOS Transistor Characterization and Inverter Design

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***Abstract*—The CD4007 chips contains three NMOS transistors and three PMOS transistors. The i-v characteristics were measured on a NMOS and PMOS transistor for different V_{GS} values. These were measured through PSPICE and on the CD4007 chip that was provided to compare results. A CMOS inverter was designed on PSPICE and on the CD4007 chip. Sweeping the input voltage and observing the output voltage simulated the voltage transfer characteristic. A 5 V_{pp} input ramp wave was applied and the results were recorded. A 5 V_{pp} input square wave was applied. The high to low and low to high propagation delays were measured by zooming into the waveforms. The high to low propagation delay was 76 ns and the low to high propagation delay was 100 ns. The propagation delay was measured and calculated to be about 88ns. The maximum propagation delay is 100ns when the input voltage is 5V, which satisfies the CD4007 datasheet.**

***Index Terms*---CMOS Inverter, NMOS, PMOS, VTC, I-V characteristics, Propagation delay**

I. INTRODUCTION

Every CMOS transistor has i_D vs v_{DS} plot that look similar. This plot usually has different values of v_{GS} and is called the i-v characteristics. This plot shows the region that the transistor is at during a given voltage and current. The plots look similar between a NMOS and PMOS transistor.

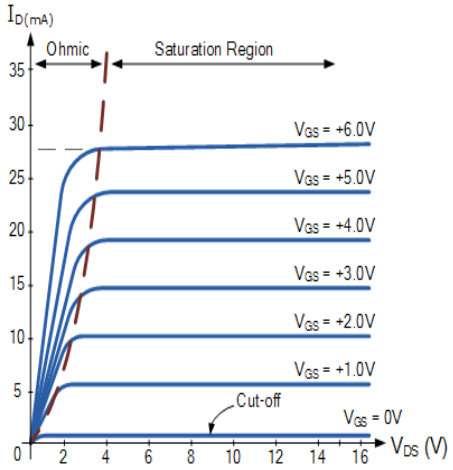

Fig. 1. The ideal i-v characteristic graph for a CMOS circuit.

A PMOS and NMOS transistor can be put in the same circuit to create a CMOS inverter. An inverter takes in a higher voltage value and gives back a voltage value closer to zero. If a low voltage value is inputted, a high voltage value will be given. In Boolean, an input of '1' will give an output of '0' and an input of '0' will give an output of '1'.

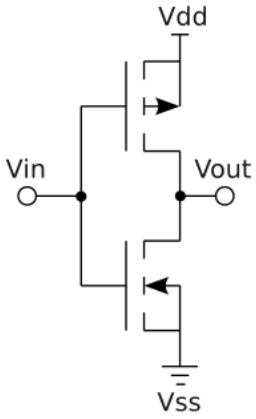

Fig. 2. A CMOS inverter circuit containing a PMOS and NMOS transistor.

The voltage transfer characteristic plot of a CMOS inverter shows that as the input voltage gets higher, the output voltage gets lower.

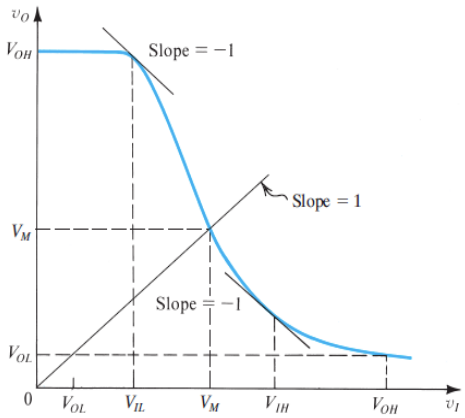

Fig. 3. The voltage transfer characteristic plot of a CMOS inverter.

Using the input and output voltage waveforms, the propagation delay can be calculated.

II. CIRCUIT THEORY, OPERATION, AND DESIGN METHODOLOGY

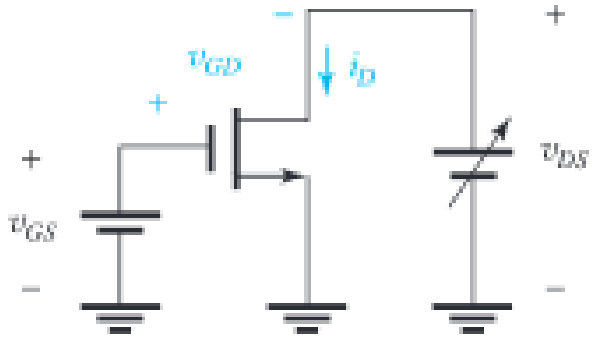

Fig. 4. NMOS circuit with a constant gate voltage and variable input voltage.

The NMOS circuit in Fig. 4 was constructed in the lab and in PSpice. NMOS transistors have three regions of operation which are the Cutoff, Saturation, and Triode region. The following (1), (2) and (3) show those regions of operation respectively for the NMOS.

$$V_{GS} < V_{TN} \qquad Cutoff \qquad (1)$$
$$V_{GS} > V_{TN}\,,\ V_{DS} > V_{GS} - V_{TN} \qquad Saturation \qquad (2)$$
$$V_{GS} > V_{TN}\,,\ V_{DS} < V_{GS} - V_{TN} \qquad Triode \qquad (3)$$

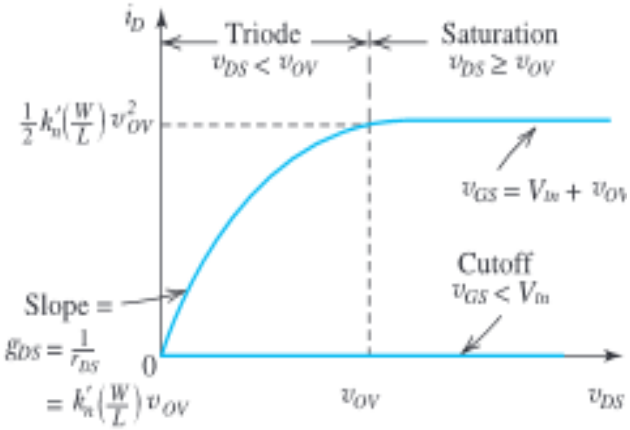

Fig. 5. NMOS I-V characteristic of a single gate voltage and variable drain voltage.

By applying a constant gate voltage and a variable drain voltage, the drain current can be measured to obtain the I-V characteristics of the NMOS transistor. This method is used within in the experiment to obtain the I-V characteristics of many different gate voltages. The bottom of the graph shows that current in the Cutoff region is at zero. The Saturation region shows a constant amount of current, while triode shows a decreasing slope while increasing in voltage. The following (4) and (5) can be used to model current of an NMOS in their respective region of operations.

$$I_D = \frac{1}{2}K_n'\left(\frac{W}{L}\right)_n (V_{GS} - V_{TN})^2 \qquad Saturation \qquad (4)$$
$$I_D = K_n'\left(\frac{W}{L}\right)_n \left[(V_{GS} - V_{TN})V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad Triode \qquad (5)$$

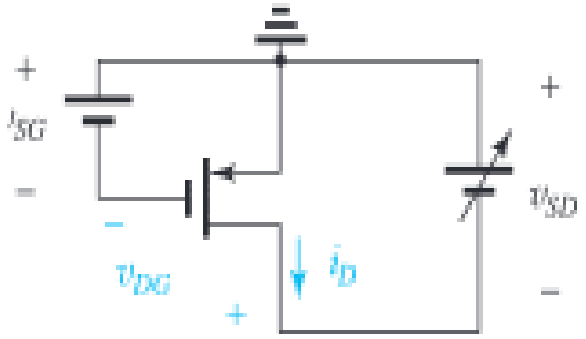

Fig. 6. PMOS circuit with a constant gate voltage and sweeping drain voltage.

The PMOS shown in Fig. 6 was used in the experiment to obtain the I-V characteristics of the PMOS in the lab and in Pspice. In PMOS, the source has the highest potential and applying a low gate voltage turns the PMOS transistor on. The following (6), (7) and (8) show the regions of operation for the PMOS.

$$V_{SG} < |V_{TP}| \qquad Cutoff \qquad (6)$$
$$V_{SG} > |V_{TP}|\,,\ V_{SD} > V_{SG} - |V_{TP}| \qquad Saturation \qquad (7)$$
$$V_{SG} > |V_{TP}|\,,\ V_{DS} < V_{GS} - |V_{TP}| \qquad Triode \qquad (8)$$

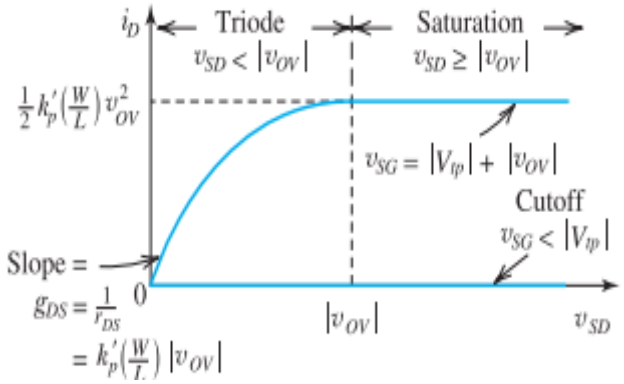

Fig. 7. PMOS I-V characteristic of a singular gate voltage and variable drain voltage

Using a current meter, the I-V characteristic of the PMOS transistor was recorded. The gate voltage was held at values from 0 V to 10 V by increments of 2 V, while the drain voltage was scanned for each gate voltage.

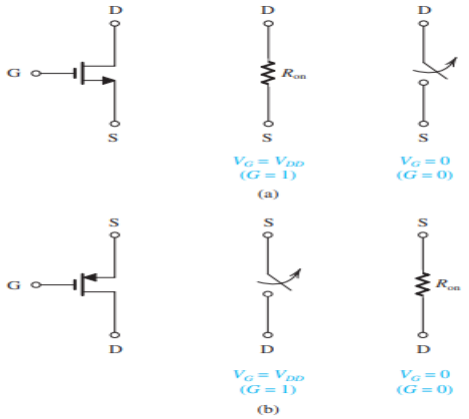

Fig. 8. Operation of NMOS and PMOS transistors within a CMOS circuits.

The NMOS and PMOS transistors in the triode region can be modeled as a switch when logic level voltages are applied to their gates. The NMOS is considered open when a logic low level voltage is applied to the gate. When a logic high level voltage is placed at the gate, then the voltage will allow current to pass from the drain to source and will behave as a resistor. The PMOS has the opposite operation, where a logic low level voltage at the gate will close the switch, allow current to pass from source to drain. Using these simple rules for PMOS and NMOS, a CMOS inverter was constructed.

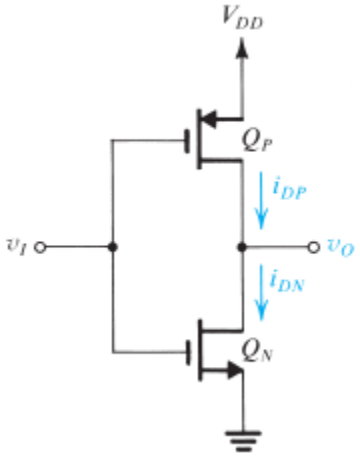

Fig. 9. Design of a CMOS inverter made of a PMOS on top and NMOS on the bottom.

The CMOS inverter can be simply analyzed by applying logic high and low voltages at the input and then determining which MOS transistors are on during those inputs. When a low logic level or ground is applied to the input the NMOS is turned off because V_{GS} is less than V_{TN} and is in the cutoff region. At the same time the low logic level turns the PMOS on because V_{SG} is greater than $|V_{TP}|$. There is no current traveling through the transistors or very little which pulls the output to V_{DD}. When a logic high is applied to the input the NMOS is turned on and the output is brought closer to ground.

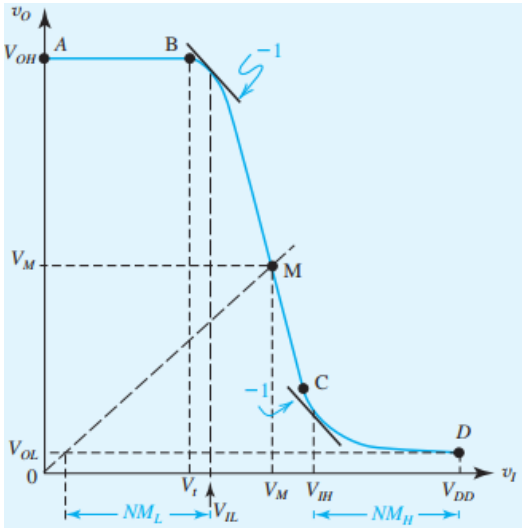

Fig. 10. Inverter VTC curve with lines showing the definitions of noise margins and marginal outputs.

The Voltage Transfer Characteristic details the specifications of the CMOS inverter. In the lab, the voltage transfer Characteristic was obtained by applying a ramp wave input to the inverter, the response was the VTC curve. Looking closely the definitions for each value can be identified. V_{OH} is the highest output possible for logic level high. V_{OL} is the smallest output for logic level low. V_{IH} and V_{IL} are the points defined when the slope of the gain is -1 V/V. V_M is the point in which the input voltage is equal to the output voltage. Ideally this is $V_{DD}/2$ which provides a good point for better noise margins. Noise margins determine the range of voltages for logic low and high levels. Higher noise margins means better noise immunity. The following (9) and (10) define the noise margins.

$$NM_H = V_{OH} - V_{IH} \quad (9)$$

$$NM_L = V_{IL} - V_{OL} \quad (10)$$

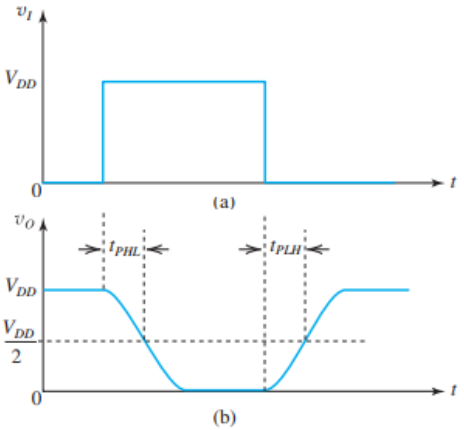

Fig. 11. Inverter input (a) and the corresponding output shown with a delay.

V_M also plays a role in determining the average propagation delay of the inverter. Looking closely at Fig. 11, the propagation delay is determined by measuring the time between the halfway point of the input transition and the halfway point of the output transition. The total propagation is the average of the two transitions from high to low and low to high. (11) shows the total propagation delay.

$$t_p = \frac{(t_{pHL}+t_{pLH})}{2} \quad (11)$$

The total propagation delay was obtained in the lab by inputting a pulse wave and recording the resulting output.

III. SIMULATION AND EXPERIMENTAL RESULTS

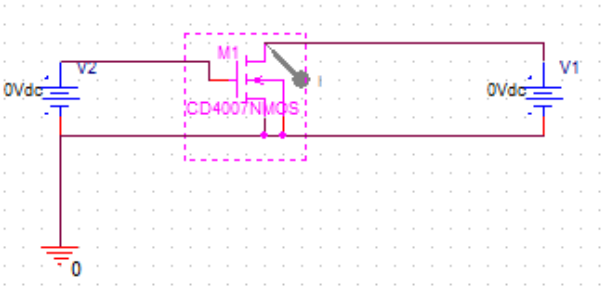

Fig. 12. A NMOS circuit with a DC sweep on the drain voltage

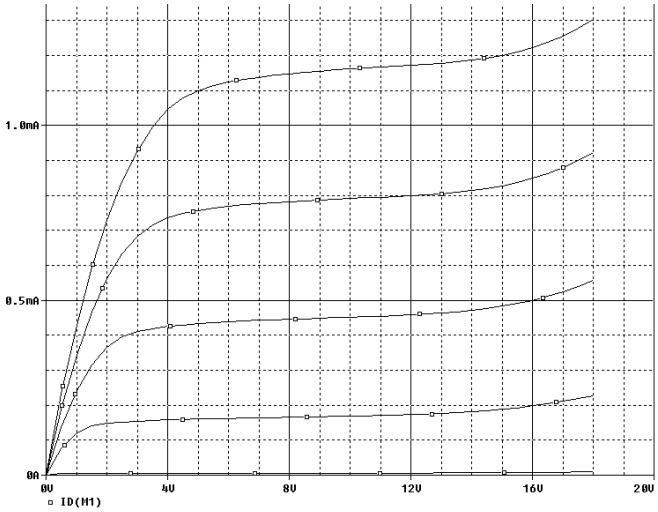

Fig. 13 Pspice simulation of the I-V Characteristic for the NMOS circuit.

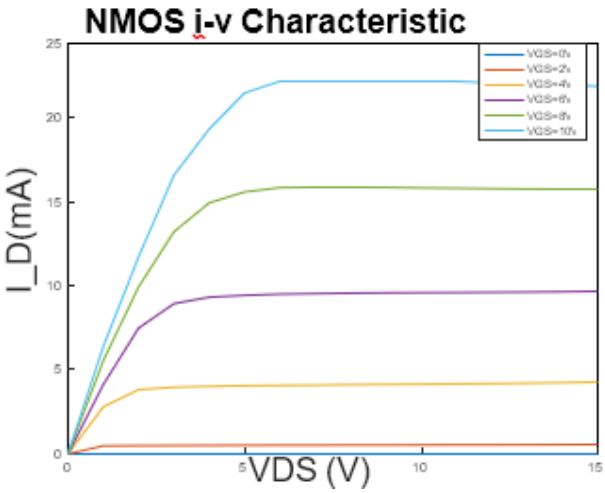

Fig. 14. NMOS i-v characteristic for CD4007UBE in lab

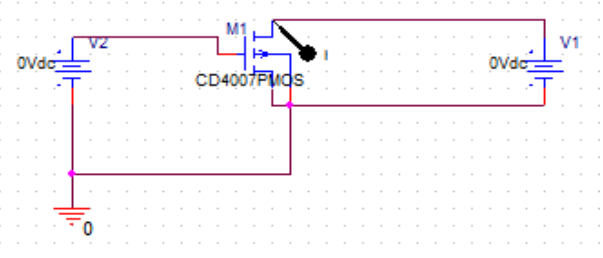

Fig. 15. A PMOS circuit with a DC sweep

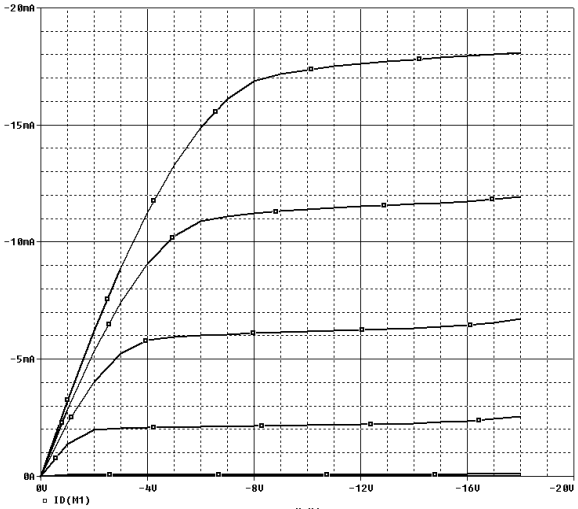

Fig. 16. Pspice simulation of the I-V characteristic of the PMOS circuit.

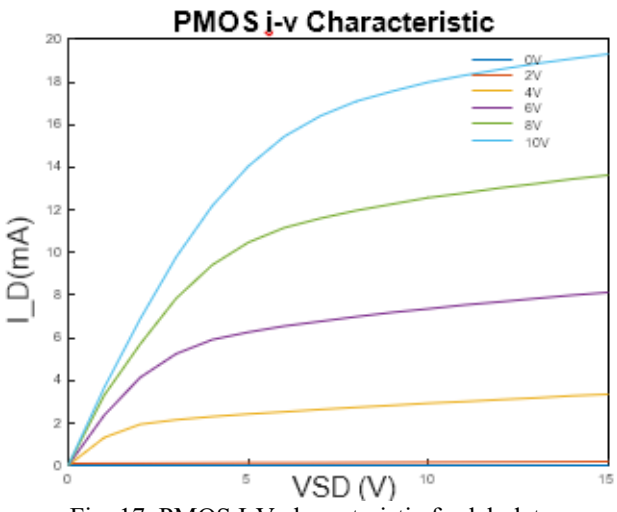

Fig. 17. PMOS I-V characteristic for lab data

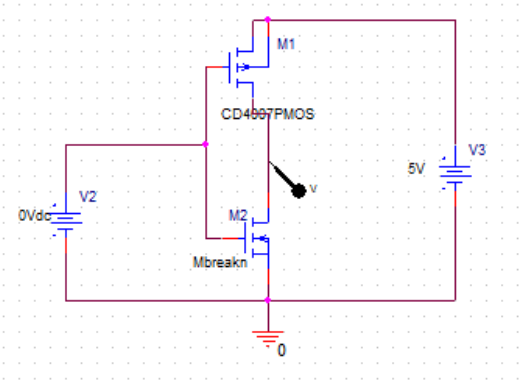

Fig. 18. Circuit design for the CMOS inverter

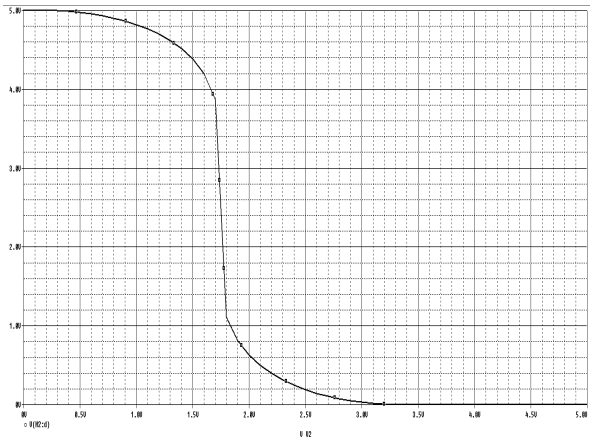

Fig. 19. Pspice simulation for the VTC curve of the CMOS inverter

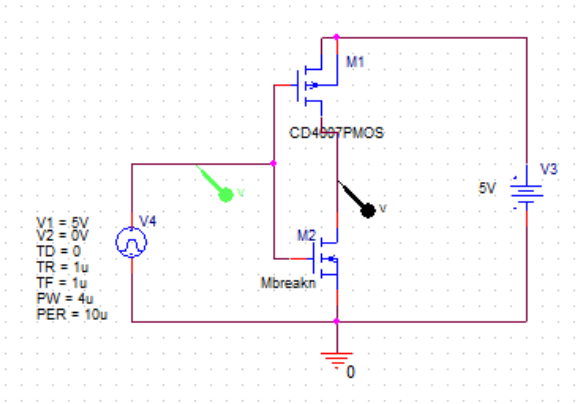

Fig. 20. CMOS inverter with a pulse wave at the input

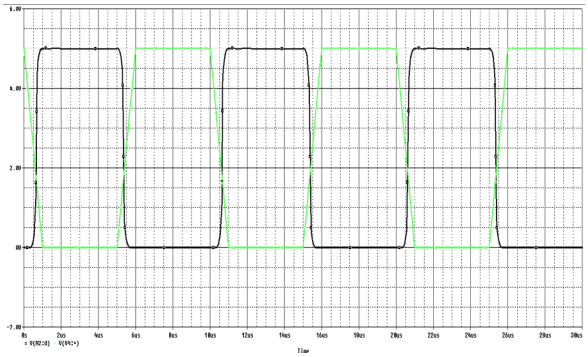

Fig. 21. Pulse wave with response wave in response.

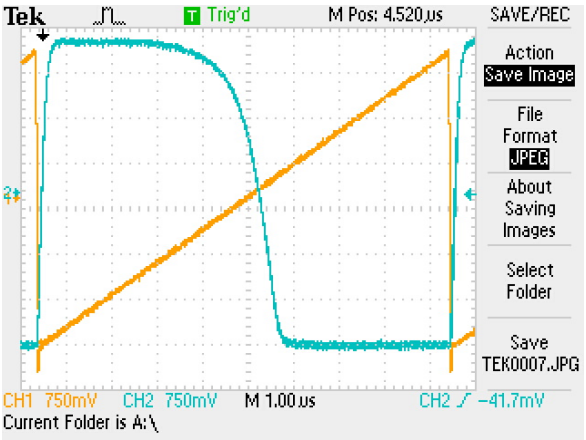

Fig 22. Oscilloscope showing VTC curve response of the CMOS inverter

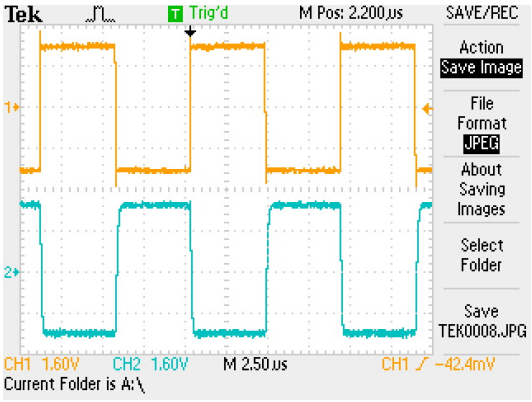

Fig. 23. Oscilloscope showing inverted response from Input to CMOS inverter.

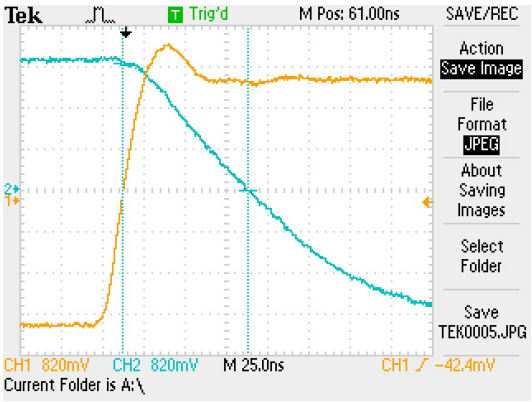

Fig. 24. Oscilloscope showing the propagation delay from high to low transition

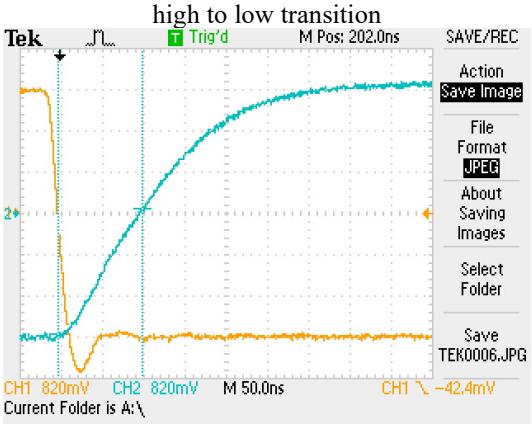

Fig. 25. Oscilloscope showing the propagation delay from low to high transition.

IV. DISCUSSION AND CONCLUSION

The NMOS and PMOS circuit was simulated on PSPICE to give the i-v characteristic plot. This circuit was recreated using the CD4007 chip to get the i-v characteristic plot, which is similar to the PSPICE plot. A CMOS inverter was created using PSPICE and the CD4007 to get the voltage transfer characteristic plot. Using the input and output voltage waveforms, the high to low and low to high propagation delay. These can be used to get the overall propagation delay. The high to low propagation delay received was 76ns and the low to high propagation delay was 100ns. The propagation delay calculated was 88ns. There are differences that were obtained between the PSPICE simulation and using the CD4007 chip. These differences can be due to the chip that was used or any other equipment. Every chip is a little different which can create a difference in results. The probes that were used

ACKNOWLEDGEMENT

The overall work was split 50-50. Ridge Tejuco worked on the Pspice simulations, the lab construction and data collection. Ridge also wrote the Section II of the lab report. Oscar Tejeda worked on lab construction data collection. Oscar wrote the Abstract, Introduction, Results Conclusion.

REFERENCES

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[2] ECE 443L Lab Manual, Northridge, CA: CSUN, 2020