4X4 NOR ROM ARRAY DESIGN, SIMULATION AND EXPERIMENTAL TEST AS WELL AS ANALYSIS

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ABSTRACT:

ROM is a commonly used form of memory in order to provide instructions and programming for many hardware devices and appliances. This lab covers the design, implementation, and analysis of a 4x4 NOR ROM Array. The 4x4 ROM array was successfully implemented in Pspice and the ideal output wave forms were generated.

KEYWORDS:

CMOS, NMOS, PMOS, Pull-up Network (PUN), Pull-down Network (PDN), ROM, NOR PSPICE

7.1 INTRODUCTION

The purpose of this lab is to design a 4x4 ROM Array. A NOR ROM array consists of an array of NMOS transistors in series with PMOS transistors. Fig 7.1 shows the general design of the 4x4 NOR ROM Array. Looking closely, the design also includes the use of a bit line and word line. The word line is used to access any specific row of bits. The bit line is used to read the outputs of the specific word. The PMOS device on each bit line provides the signal with a full voltage supply swing. When a row is selected the NMOS device on the word line is turned on allowing the current of the bit line to exit through the NMOS device. This pulls down the voltage at the bit line to almost 0.2 V when properly sized. If there is no NMOS device selected, the bit line will remain high at a voltage of 4.8 v.

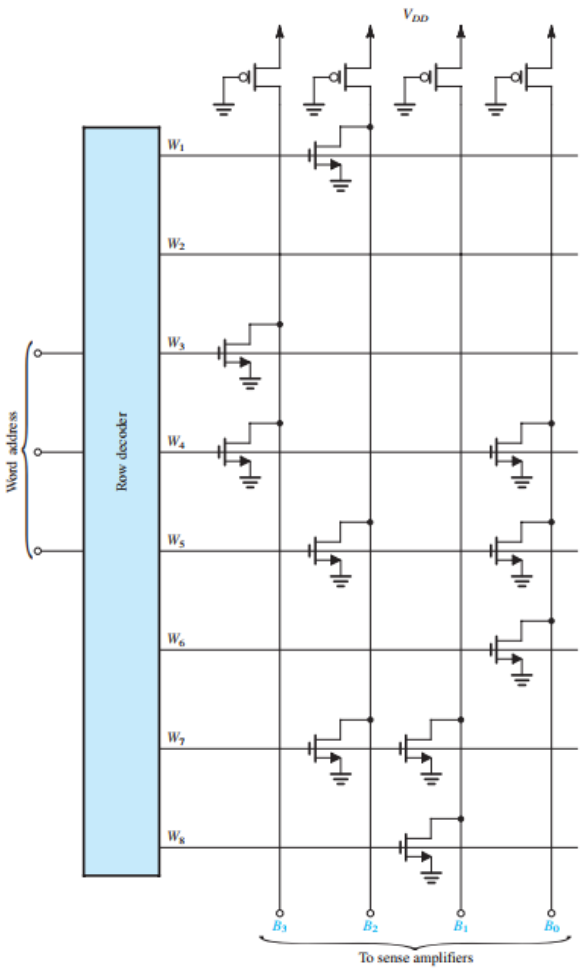

Fig. 7.1 A General ROM Array with a row decoder.

7.2 PROCEDURES, SIMULATION AND EXPERIMENTAL SET-UP

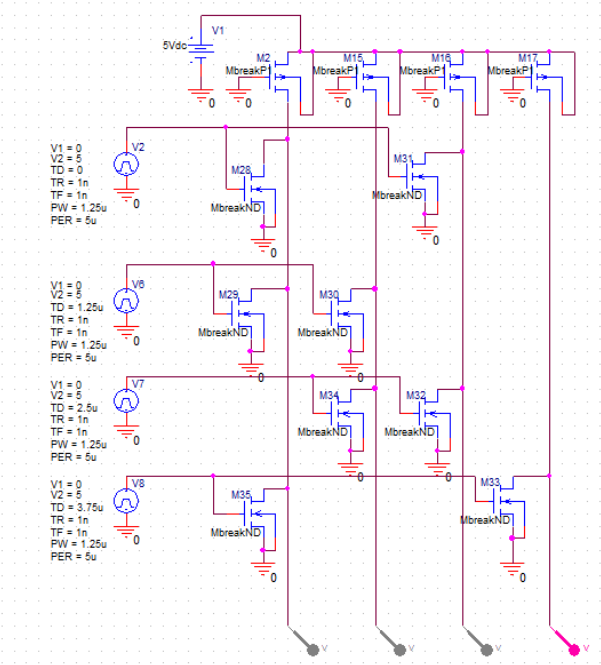

Fig. 7.2 Case 1: : 4x4 NOR ROM Array at 200kHz

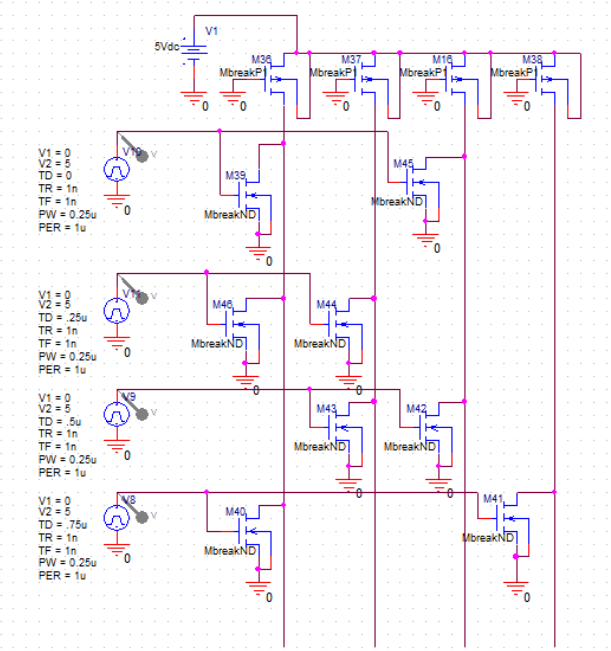

Fig. 7.4 Case 4: 4x4 NOR ROM Array at 1.2MHz

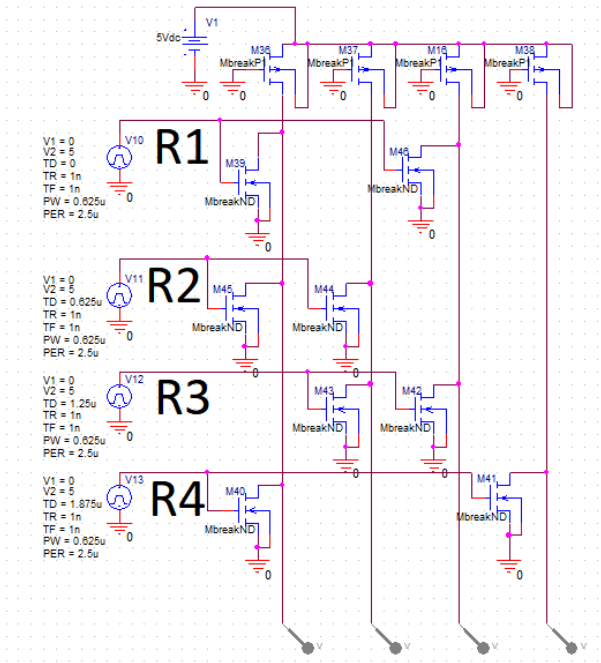

Fig. 7.3 Case 2: 4x4 NOR ROM Array at 400kHz

7.3 SIMULATION AND EXPERIMENTAL RESULTS

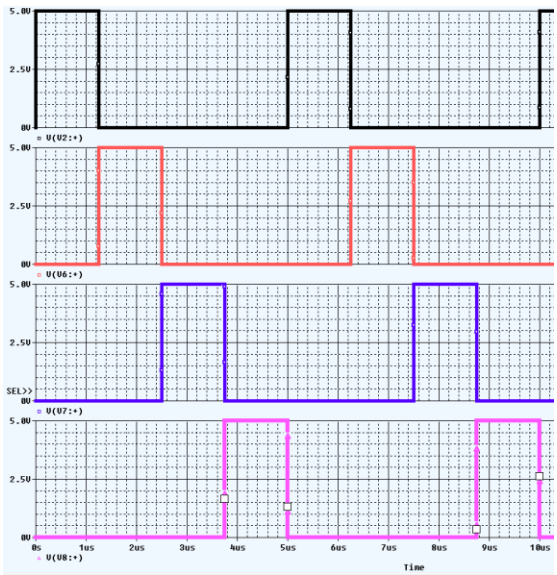

Fig. 7.5 Case 1: Input word line at 200 kHz

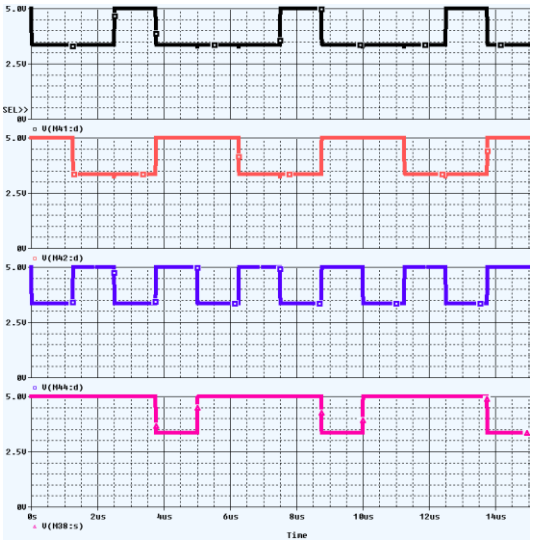

Fig. 7.6 Case 1: : 4x4 NOR ROM with normal sizing results at 200kHz

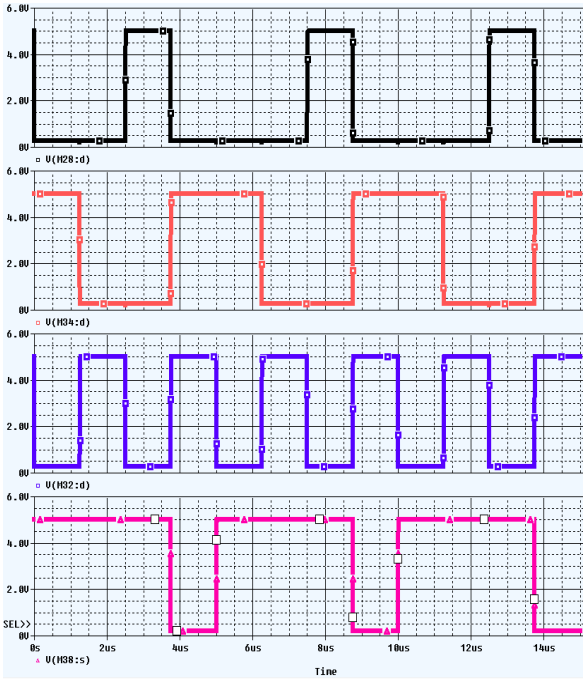

Fig. 7.7 Case 1: 4x4 NOR ROM with 13 times sizing results at 200kHz

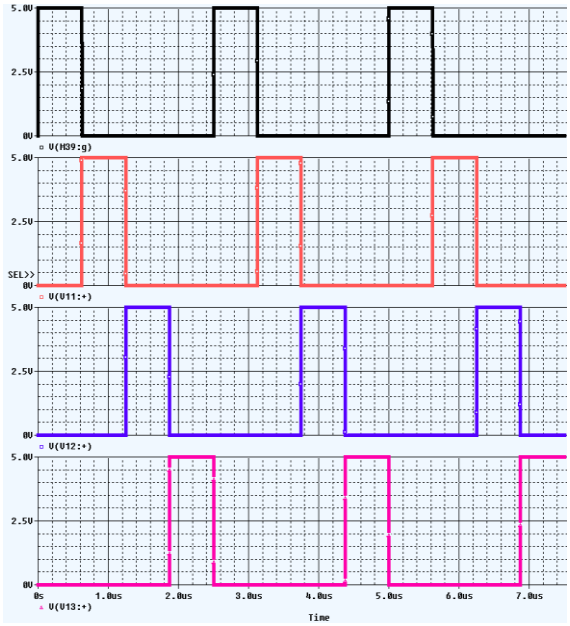

Fig. 7.8 Case 2: Input word line at 400 kHz

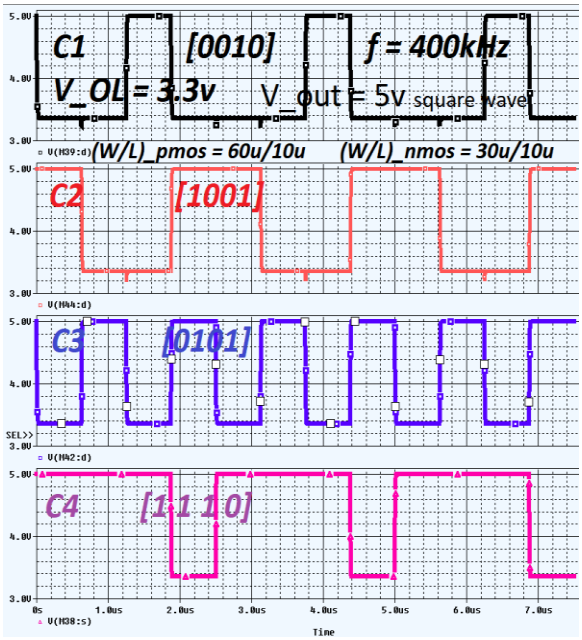

Fig. 7.9 Case 2: 4x4 NOR ROM with normal sizing results at 400kHz

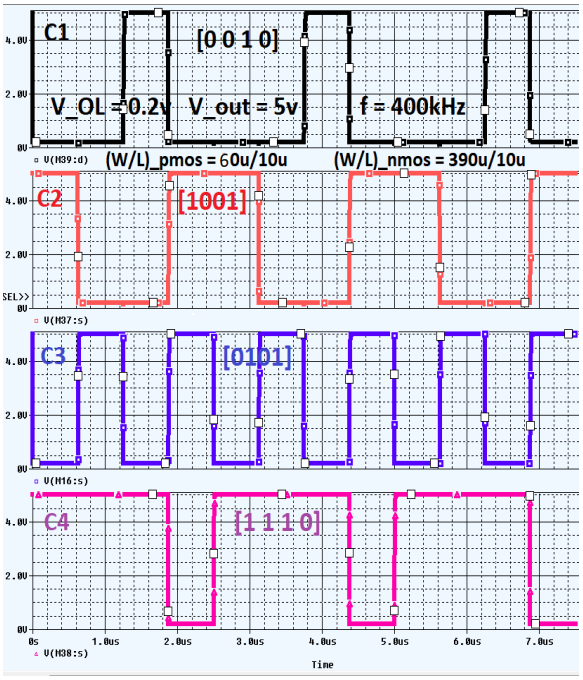

Fig. 7.10 Case 2: 4x4 NOR ROM with 13 times sizing results at 400kHz

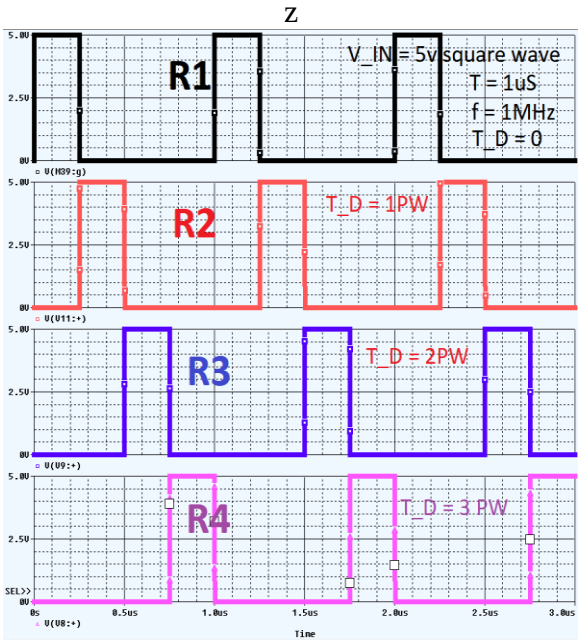

Fig. 7.11 Case 4: Input word line at 1 MHz

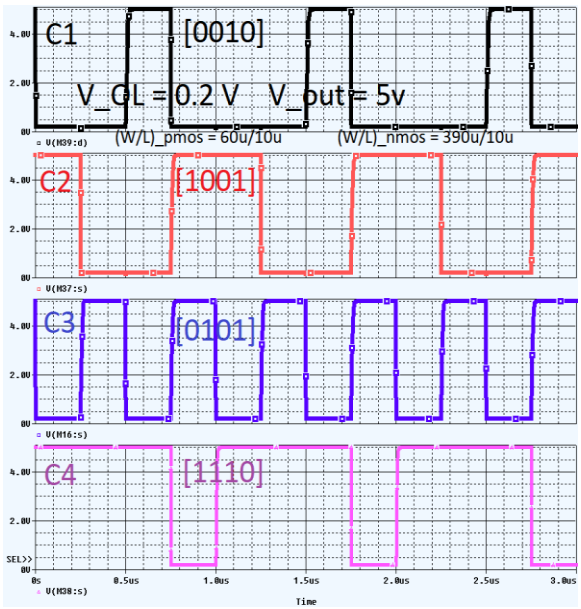

Fig. 7.12 Case 4: 4x4 NOR ROM with normal sizing results at 1 MHz

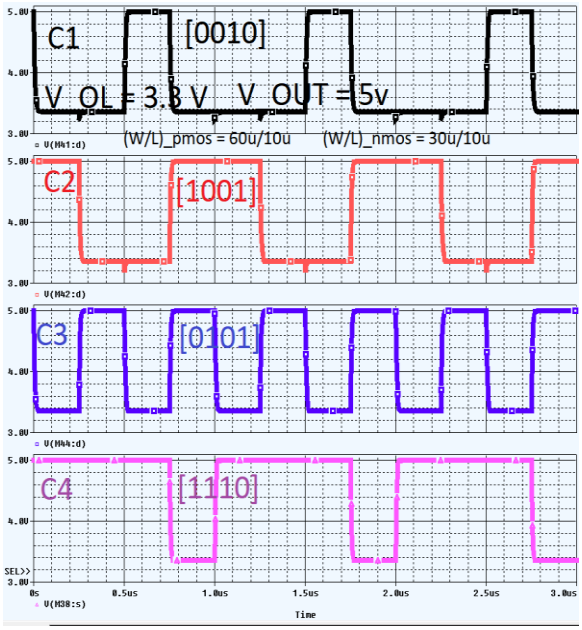

Fig. 7.13 Case 4: 4x4 NOR ROM with 13 times sizing results at 1MHz

7.4 . DISCUSSION AND CONCLUSION:

Overall, the results of the simulation were ideal. Each output wave form follows the truth table seen in Fig. 7.14. In each case, the occurrence of a NMOS transistor resulted in a logic 0 at 0.2v and the absence of one resulted in a logic high at 4.8 v.

R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0

Fig. 7.14. Truth table for the 4x4 NOR ROM Array.

The sizing of the transistors was considered. In the normal sizing case, all cases of different frequencies produced waveforms with an output low voltage of 3.3v which is low enough to be considered a logic ‘0’. In order to achieve this voltage, the transistors were sized 13 times to 390 micrometers in width. As you can see in Fig. 7.13, 7. 10, and 7.7 the output waveforms have a low output voltage of 0.2 v.

REFERENCES

[1] A. S. Sedra and K. C. Smith, Microelectronic circuits. New York: Oxford University Press, 2015.

[2] ECE lab manual

[3] CD4007 WikiAnalog.com