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Dr B R Ambedkar National Institute of Technology, Jalandhar

B Tech 4th Semester (Computer Science and Engineering)

CSPC–208, Computer Organization and Organization

End-Semester Examination, May-2024

Duration: 03 Hours Max. Marks: 50 Date: 22-May 2024

Marks Distribution & Mapping of Questions with Course Outcomes (COs)								
Question Number	1(a,b)	2(a,b)	3(a,b)	4(a,b)	5(a,b)	6	7(a, b)	8
Max. Marks	(3,2)	(3,2)	(2,3)	(2,3)	(3,2)	5	(5,5)	10
CO No.	2,2	1,1	4,1	2,2	3,1	2	3,2	1
*Cognitive Level	AP, AP	E,AN	U, AP	E, E	U, U	U	U, U	C
**Section/Chapter/Unit	7,5	7,1	4,2	6,6	8,8	7	8,6	4,5,8,9

*Remember (R), Understand (U), Apply (Ap), Analyse (An), Evaluate (E), and Create (C)
**The space can be left blank if sections and chapters are not defined for the present syllabus.
*Table 1 Exhibits a list of words for various cognitive levels.

Note:

- Attempt all the questions.
- Assume Suitable data if Necessary

1. **(a)** A virtual memory system has an address space of 8K words, a memory space of 4K words, and page and block sizes of 1K words. The following page reference changes occur during a given time interval. (Only page changes are listed. If the same page is referenced again, it is not listed twice.)

   1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6

   Determine the four-page frames that are resident in main memory after each page reference change, if the replacement algorithm used is **(i)** FIFO, **(ii)** LRU **(3)**

   (b) A computer has 32-bit instructions and 12-bit addresses. There are 250 two-address instructions. How many one-address instructions can be formulated? **(2)**

2. (a) A CPU has a 32-bit memory address and a 256 KB cache memory. The cache is organized as a 4-way set associative cache with a cache block size of 16 bytes. **(3)**

   i). What is the number of sets in the cache?

   ii). What is the size (in bits) of the tag field per cache block?

   iii). What is the number and size of comparators required for tag matching?

(b) A 7-bit Hamming code is received as 1110101. Is there any error? If yes, locate the position of the error bit. (Parity checks are created by odd parity). **(2)**

3. **(a)** Consider you have to gift a new laptop to your sister on her birthday who is studying in the first year of Computer Science and Engineering. You are required to finalize the specifications of the laptop you wish to gift. Write the detailed specifications of the laptop. **(2)**

   (b). An 8-bit register R has the following value: 11001010, find the value of R after performing the following shifts: **(3)**

   i. Logical shift left
   ii. Logical shift right
   iii. Circular shift left
   iv. Circular shift right
   v. Arithmetic shift left
   vi. Arithmetic shift right

4. **(a)** A five-stage pipeline has stage delays of 150,120,150,160 and 140 nanoseconds. The registers that are used between the Pipeline stages have a delay of 5 nanoseconds each. The total time to execute 100 independent instructions on this Pipeline, assuming there are no Pipeline stalls, is_____ nanoseconds. **(2)**

   (b) We have 2 designs D1 and D2 for a synchronous pipeline processor. D1 has 5 stage Pipeline with execution times of 3 ns, 2 ns, 4 ns, 2 ns, and 3 ns. While the design D2 has 8 Pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions? **(3)**

5. **(a)** Draw a diagram of a Bus system in which it uses 3 State buffers and a decoder instead of the multiplexers. **(3)**

   (b) Explain how the Computer Buses can be used to communicate with memory and I/O. Also, draw the block diagram for CPU-IOP communication. **(2)**

6. Discuss the Memory Hierarchy in computer systems with regard to Speed, Size, and Cost. **(5)**

7. **(a)** Explain the concept of Bus architecture and its different types. **(5)**

(b) Explain the concept of Pipeline and how conflict resolution is carried out and list Pipeline Hazards. **(5)**

8. Write short notes on the following. **(10)**
   - **a)** RISC vs CISC
   - **b)** Interrupts
   - **c)** SIMD vs MIMD
   - **d)** DMA

PTO