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Dr B R Ambedkar National Institute of Technology, Jalandhar

B Tech 4th Semester (Computer Science & Engineering)

ECPC-252, Microprocessor and Microcontroller

End Semester Examination, May 2024

Duration: 03 Hours Max. Marks: 50 Date: 27th May 2024

Marks Distribution & Mapping of Questions with Course Outcomes (COs)				
Question Number	1	2	3	4
Marks	4	17	20	9
CO No.	1,3,4	1,3,4	1,2,3,4	2,3,4
Cognitive Level	R,U,	R,U,Ap,An	U,Ap,An,E	Ap, An, C
Section/Chapter/Unit	2,5,6	1,2,3,4,5,6	1,2,3,4,5,6	1,6

Note:

1. Attempt all the questions.
2. Assume suitable data, if anything found missing

Q1 **(0.5 marks each)**

a) What is the highest value that an 8051 timer can count to?

b) How do you use the timer 0 of 8051 as a counter of external events?

c) How the baud rate of UART serial communication is programmed in 8051?

d) Which type of serial communication does the 8051's serial port support? Simplex, half or full duplex?

e) Assume the first instruction executed following a system reset is a subroutine call. At what memory address in internal RAM of 8051 is the program counter value saved before branching to the subroutine?

f) Which bits in which register must be set to give the serial data interrupt of 8051 the highest priority?

g) What is the byte address of PCON special function register of 8051?

h) How will you provide more that 8 interrupt lines to an 8086 based system?

Q2 **(1 marks each)**

a) When do you use P3.2 pin to start a timer in 8051 and how?

b) Find the TMOD value for both timer 0 and timer 1 to be programmed in mode 2, gate=0 and with clock coming from the 8051's crystal.

c) In 8051 what is the significance of the Transmit flag, TI, when it is cleared to 0? When set to 1?

d) What is the status on TCON.6 and TCON.4 bits for timer 1 runs and timer 0 stops in 8051?

e) What are the bye addresses of TH1 and TL1 registers of 8051? And what is the purpose of these registers?

f) When an 8051 is to be interfaced with a common external ROM chip for the program and data, how the $\overline{PSEN}$ *and* $\overline{RD}$ signals are used and what is their significance.

g) What are the interrupt vector addresses of the following interrupts in the 8086 interrupt table (i) INTO (ii) INT 32

h) How do you set and clear the interrupt flag? What is its importance in interrupt structure of 8086?

i) What is the maximum memory addressing and I/O addressing capability of 8086 microprocessor? And how?

j) How does 8086 microprocessor differentiate between an opcode and instruction data?

k) What is the function of opcode prefetch queue in 8086?

l) Show the 8253 control word you would use to initialize its counter 1 for read/write LSB and then MSB, mode 3, and BCD countdown.

m) How does 8259 differentiates between an 8-bit and 16-bit processors?

n) Describe the effect that a control word of 00000000 sent to 8253 will have?

o) Describe the control word format of 8255 in BSR mode.

p) What are the most prominent features of 8087?

q) What is the function of EOP signal of 8237?

Q3 **(2 marks each)**

a) Write 8051 assembly instruction sequence to initialize the serial port of 8051 to operate as an 8-bit UART at 2400 baud.

b) Write a single 8051 instruction to perform each of the following tasks (i) Read SBUF and store in A (ii) Test whether port 2 bit 5 is set (iii) Move bit 2 of port 3 into C (iv) Complement bit 3 of internal RAM location 21h.

c) With the help of 8051 assembly language instructions, show how to set INT0 and INT1 as edge triggered interrupts without affecting any other interrupt?

d) Write 8086 instructions to perform each of the following tasks (i) Store the number 1234h in absolute memory address 60000h (ii) Rotate carry bit into bit 4 of DX, assume carry is 1 initially.

e) Draw and discuss the flag register of 8086 microprocessor.

f) The contents of different registers of 8086 are given below. Form the effective addresses and physical addresses for the following two instructions. Use DS as default segment. (i) MOV AX, [BX] [SI] & (ii) MOV AX, 5000 [BX] [SI]

AX=1000H, BX=2000H, SI=3000H, DI=4000H, BP=5000H, SP=6000H, CS=0000H, DS=1000H, SS=2000H, IP=7000H & Offset=5000H

g) Explain the initialization sequence of 8259.

h) What is the function of pin A0 in conjunction with pins $\overline{CS}$, $\overline{RD}$, & $\overline{WR}$ in 8259.

i) What is the advantage of DMA controlled data transfer over interrupt driven or program controlled data transfer? Why the DMA controlled data transfers faster?

j) What are SRAMs and DRAMs?

Q4 **(3 marks each)**

a) What are the operations in 8051, when there is a return from a called routine using RET and when there is a return from an interrupt service routine using RETI. Further what happens, if RET instead of RETI is used as last instruction of the interrupt service routine.

b) Write an 8086 assembly language program to interface an 8-key keyboard and 8 LEDs with 8086 using 8255. The 8255 is to be programmed in mode 0 in such a way that data entered from the keyboard is to be displayed on LEDs. An 8-key keyboard is connected across port A and 8 LEDs are connected across port B. Assume port C is to be used as output port. Addresses of port A, B, C & CWR are 00h, 01h, 02h & 03h respectively.

c) What is the difference between NEAR and FAR call procedures of 8086? Also discuss the role of stack in calling these procedures and returning from these procedures.