CA INNOVATIVE ASSIGNMENT

REGISTER REFERENCE INSTRUCTION

FACULTY: KRUTI MA'AM

21BCE257 – RIDHDHI SANGANI

21BCE267 – AASHNA SHAH

21BCE272 – NIR SHAH

21BCE273 – SHRUTAM SHAH

16*1 MUX FOR ACCUMULATOR

SELECTION BITS	OPERATION	LOGIC USED
0000	CLA	Constant 0 is used
0001	CLE	Same output as input
0010	CMA	NOT gate used
0011	CME	Same output as input
0100	CIR	Shifter used
0101	CIL	Shifter used
0110	INC	Adder used with its second input as constant 1
0111	SPA	Same output as input
1000	SNA	Same output as input
1001	SZA	Same output as input
1010	SZE	Same output as input

16*1 MUX FOR ENABLE BIT

SELECTION BITS	OPERATION	LOGIC USED
0000	CLA	Same output as input
0001	CLE	Constant 0 is used
0010	CMA	Same output as input
0011	CME	NOT gate used
0100	CIR	Same output as input
0101	CIL	Same output as input
0110	INC	Same output as input
0111	SPA	Same output as input
1000	SNA	Same output as input
1001	SZA	Same output as input
1010	SZE	Same output as input

16*1 MUX FOR PROGRAM COUNTER

SELECTION BITS	OPERATION	LOGIC USED
0000	CLA	Same output as input
0001	CLE	Same output as input
0010	CMA	Same output as input
0011	CME	Same output as input
0100	CIR	Same output as input
0101	CIL	Same output as input
0110	INC	Same output as input
0111	SPA	Comparator is used
1000	SNA	Comparator is used
1001	SZA	Comparator is used
1010	SZE	Comparator is used

16*1 MUX FOR SEQUENCE COUNTER

SELECTION BITS	OPERATION	LOGIC USED
0000	CLA	AND gate is used with its second input as 0
0001	CLE	AND gate is used with its second input as 0
0010	CMA	AND gate is used with its second input as 0
0011	CME	AND gate is used with its second input as 0
0100	CIR	AND gate is used with its second input as 0
0101	CIL	AND gate is used with its second input as 0
0110	INC	AND gate is used with its second input as 0
0111	SPA	AND gate is used with its second input as 0
1000	SNA	AND gate is used with its second input as 0
1001	SZA	AND gate is used with its second input as 0
1010	SZE	AND gate is used with its second input as 0