Ans-1

$UBRRn = 111010100101$

$= 3749$

$f_{osc} = 24MHz$

For asynchronous normal mode:

$$\text{Baud rate} = \frac{f_{osc}}{16(UBRRn+1)}$$

$$= \frac{24 \times 10^6}{16(3749+1)}$$

$$= 400 \text{ bps}$$

$$\text{Baud rate error} = \frac{\text{Standard Baud rate} - \text{Calculated Baud rate}}{\text{Standard Baud rate}}$$

$$= \frac{300 - 400}{300} \times 100\%$$

$$= -33.33 < \pm 2\%$$

∴ There will be no communication error

Ans-2

Fast PWM Mode,

Inverting: (Using Timer0)

COM0A0 = 1

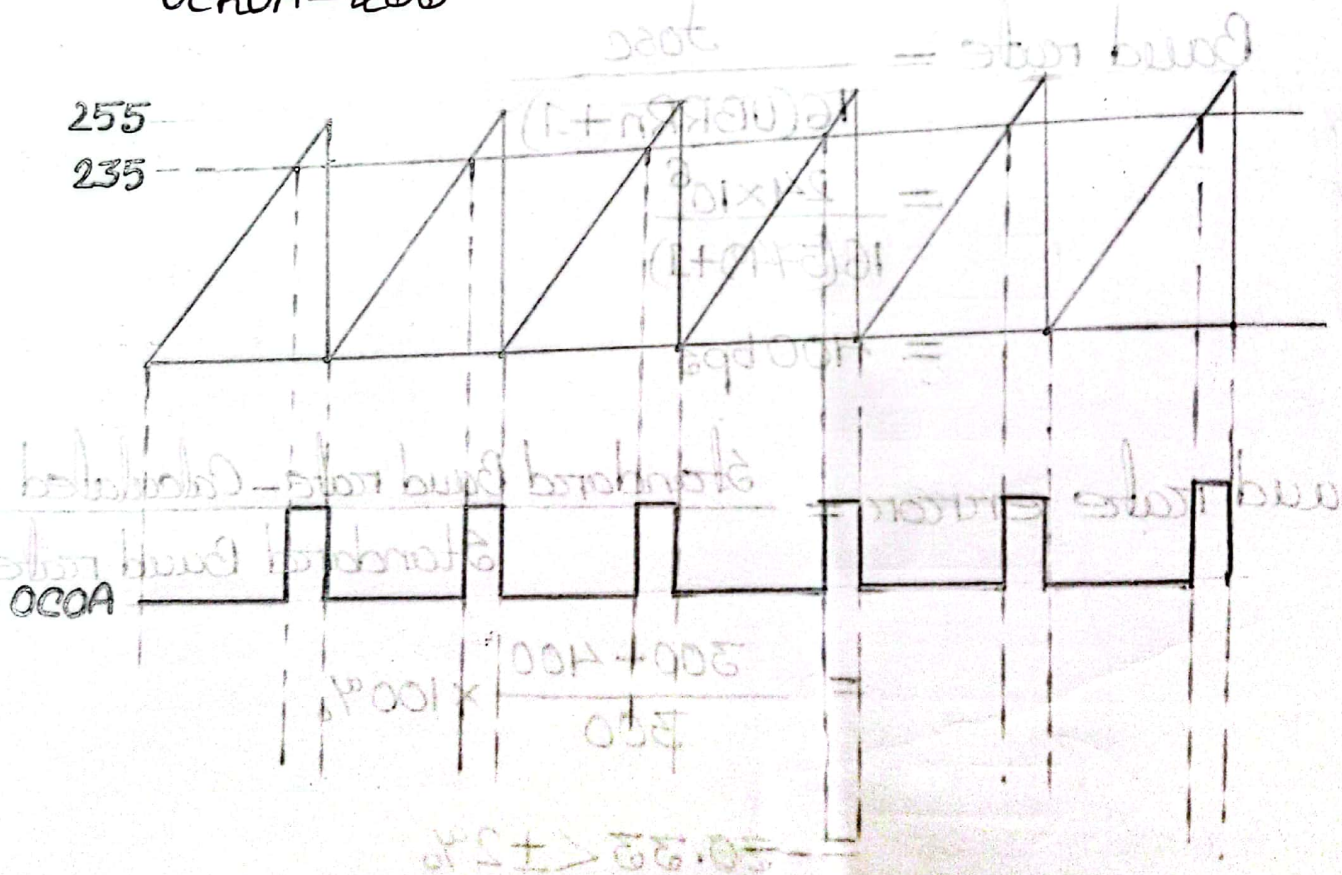
COM0A1 = 1

OCR0A = 235

WGM00 = 1

WGM01 = 1

WGM02 = 1



Ans-3

Given, OCR0A = 200

OCR0B = 141

From the program,

Prescalar = 64

Non-Inverting Mode

Mode of operation : Mode 7

Fast PWM Mode

Duty Cycle: OCR0B = 141

$$D = \left(\frac{OCR0B}{256} \times 100\right) + 1$$

$$= \left(\frac{141}{256} \times 100\right) + 1$$

$$= 56\%$$

Frequency:

$$f_{OC0APWM} = \frac{f_{clk\_IO}}{2N(1+OCR0A)}$$

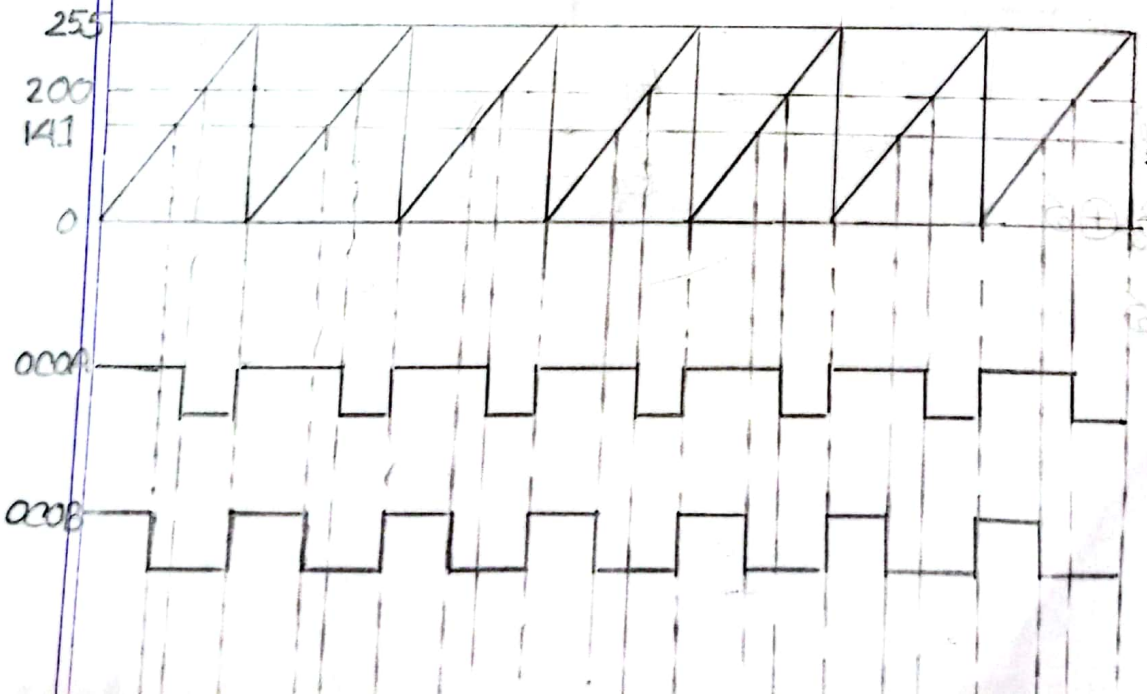
$$= \frac{8 \times 10^6}{2 \times 64 (1+200)}$$

$$= 311\ Hz$$

$$f_{OC0BPWM} = \frac{f_{clk\_IO}}{2N(1+OCR0B)}$$

$$= \frac{8 \times 10^6}{2 \times 64 (1+141)}$$

$$= 441\ Hz.$$



Ans No-4

Two input 'A' & 'B'

when $s=0$; $F=A+B$

$s=1$; $F=A-B$

Table

s	F	X	Y	C_{in}
0	A+B	A	B	0
1	A-B	A	B'	1

Truth Table:

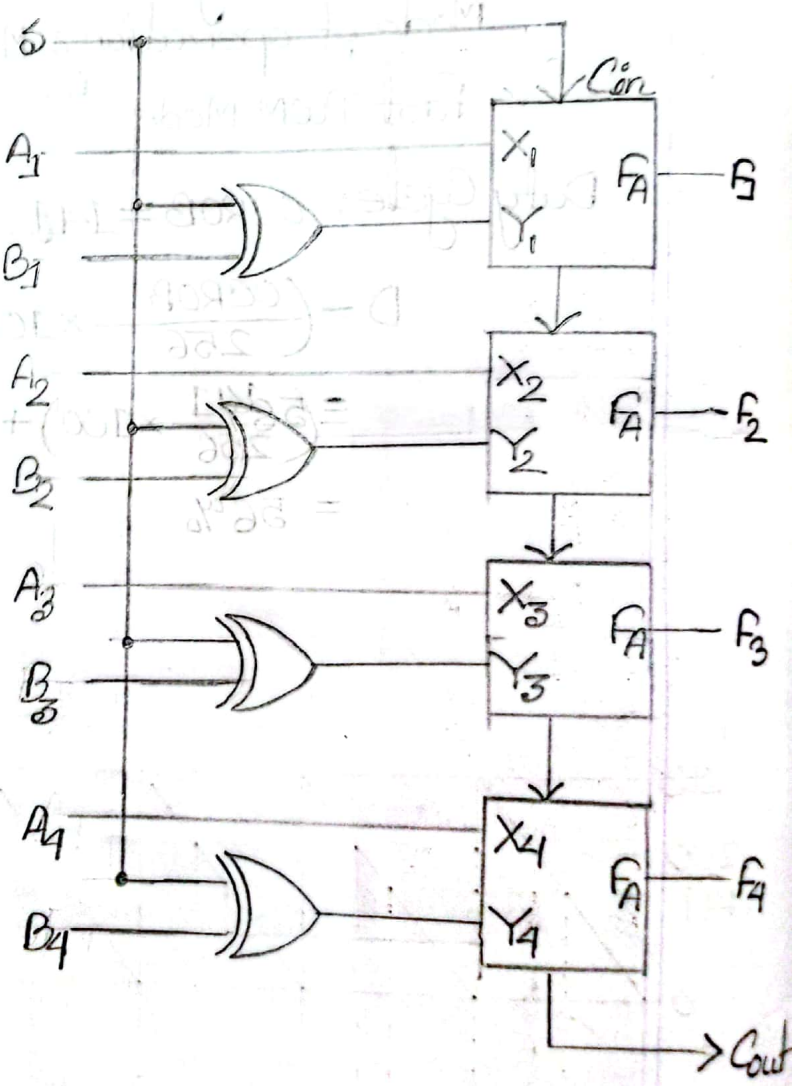
s	A_i	B_i	X_i	Y_i
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

$X_i = A_i$

$Y_i = B_i \oplus s$

$C_{in} = s$

Circuit Diagram:



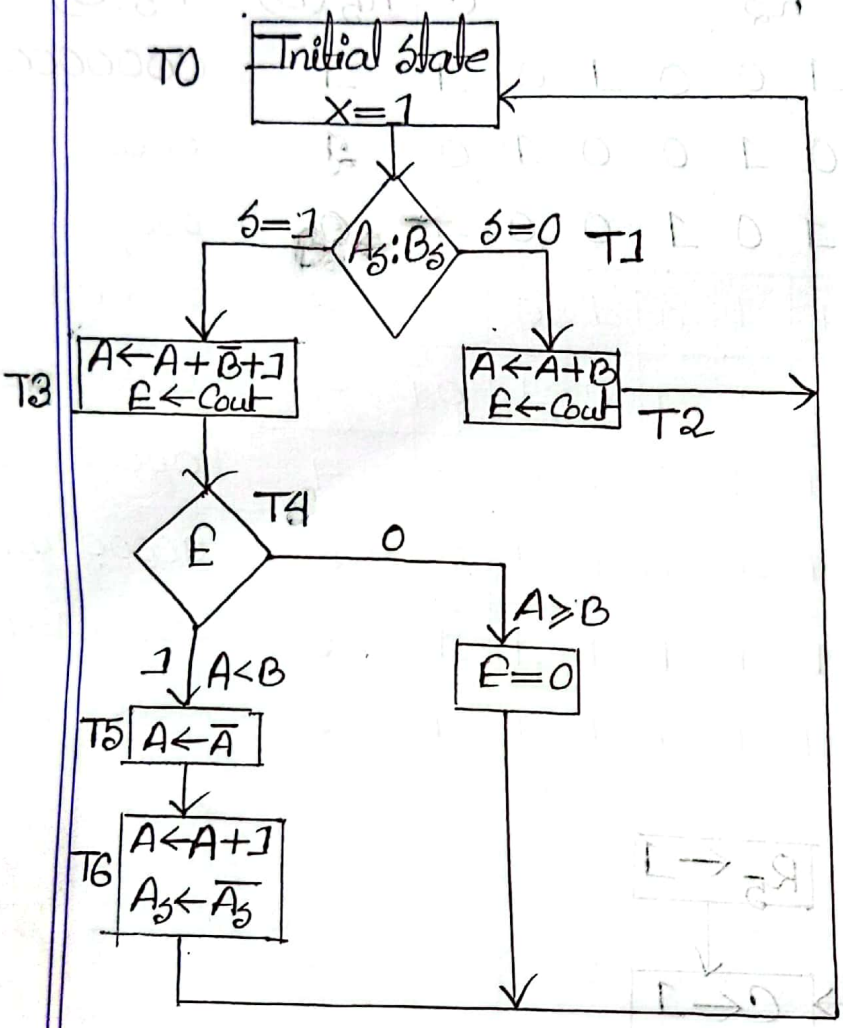
Ans No-5

	Micro-operation	A	B	D	F	C_{in}	H	In Hex
I)	$R7 \leftarrow R3 + R4$	011	100	111	001	0	010	7392
II)	$R3 \leftarrow SHL\ R3$	011	011	011	111	0	001	6DF1
III)	$R5 \leftarrow R1$	001	000	101	000	0	010	2282
IV)	$R2 \leftarrow SHR\ R5$	101	101	010	111	0	111	B577
V)	$R3 \leftarrow CRC\ R7$	111	111	011	111	0	110	FDF6

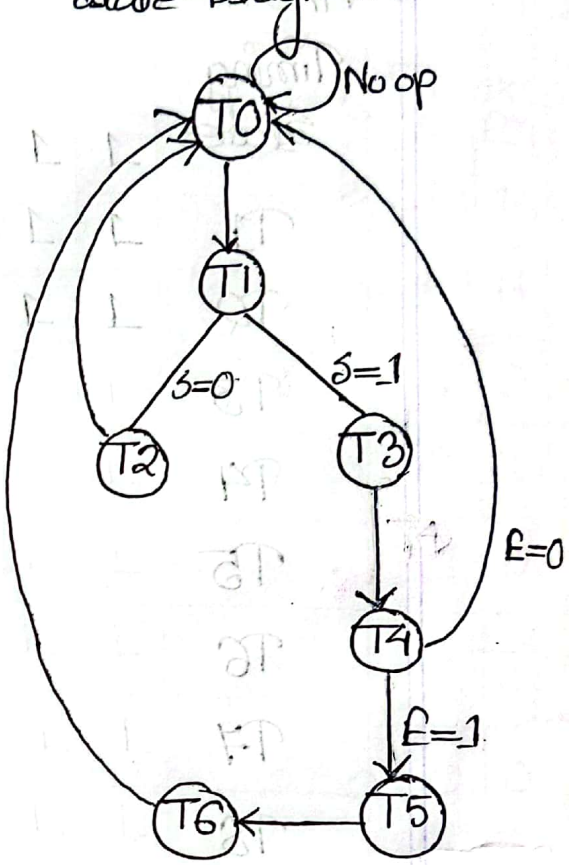
Ans No-6

	ROM Address			Control Word									Address			MUX SELECT	
	A2	A1	A0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
				x	S2	S1	S0	Cin	L	y	z	w	A2	A1	A0	H1	H0
T0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0
T1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1
T2	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0
T3	0	1	1	0	0	1	0	1	1	0	0	0	1	0	0	1	0
T4	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
T5	1	0	1	0	1	0	0	0	1	0	0	0	1	1	0	1	0
T6	1	1	0	0	0	1	1	1	1	0	1	0	0	0	0	1	0

*Flowchart



State Diagram



x (Initial state)

S2 (Mode select)

S1, S0 } function select

Cin (Input Carry)

L (Load A & E)

Y (Complement B_5)

Z (Complement A_5)

C (Clear E)

Ans No-4.

Micro-operations	Carry Bit C	Sign Bit S	Zero Bit Z	Overflow Bit V
R4 ← R3+R4	0	0	0	0
R3 ← SHL R3	x	x	0	x
R5 ← R1	x	x	x	x
R2 ← SHR R5	x	x	0	x
R3 ← CRC R4	x	x	0	x

I) R3 = 011

R4 = 100

R3+R4 = 011 + 100

= 111

II) R3 = 011

SHL = 110

IV) R5 = 101

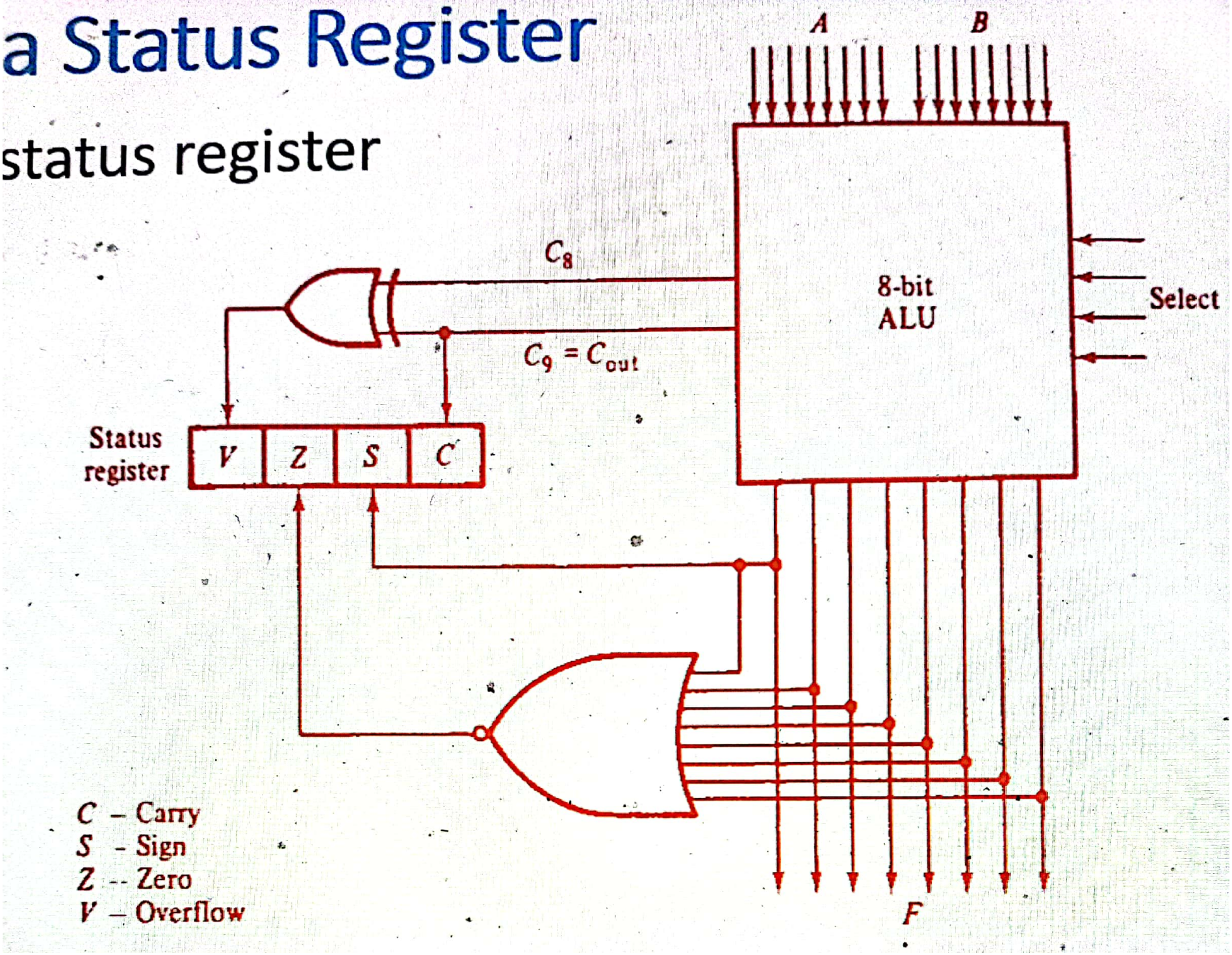
SHR R5 = 110

V) R4 = 111

CRC R4 = 111

a Status Register

status register



Ans No-8

Timing states	R_2								C	R_5(D)	R_5(B)
	1	1	0	1	0	0	1	0	1	1	00000001
T1	1	1	1	0	1	0	0	1	0→1	2	00000010
T2	1	1	1	1	0	1	0	0	1	2	00000010
T3	1	1	1	1	1	0	1	0	0→1	3	00000011
T4	1	1	1	1	1	1	0	1	0→1	4	00000100
T5	1	1	1	1	1	1	1	0	1	4	00000100
T6	1	1	1	1	1	1	1	1	0→1	5	00000101
T7	1	1	1	1	1	1	1	1	1	5	00000101
T8	1	1	1	1	1	1	1	1	1	5	00000101

Flowchart: