BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
CSE 404 JANUARY 2018 SEMESTER
DIGITAL SYSTEM DESIGN SESSIONAL

Assignment on 4-bit PC Design and Simulation

July 11, 2018

1 DESIGN SPECIFICATION

- The Address bus will be of 8-bit
- The Data bus will be of 4-bit
- The Control unit should be microprogrammed. The control signals associated with the operations should be stored in a special memory (you can use a separate ROM for this purpose) units as Control Words.
- Marks will vary according to the efficiency of design. Efficiency will be judged based on two principles:
  1. The number of the T-states of instruction cycle
  2. The MSI/LSI chips requirement

  For both the principles, the lower the number, the better the design

2 Instruction Set Description

Table 2.1: A simple longtable example

Instruction	**Description**
LDA address	$Acc \leftarrow Memory[address]$
STA address	$Memory[address] \leftarrow Acc$
MOV Acc, B	$Acc \leftarrow B$
MOV B, Acc	$B \leftarrow Acc$
MOV Acc, Immediate	$Acc \leftarrow Immediate$
ADD B	$Acc \leftarrow Acc + B$
ADC B	$Acc \leftarrow Acc + B + Carry$
ADD address	$Acc \leftarrow Acc + Memory[address]$
ADC address	$Acc \leftarrow Acc + Memory[address] + Carry$
ADD Immediate	$Acc \leftarrow Acc + Immediate$
ADC Immediate	$Acc \leftarrow Acc + Immediate + Carry$
SUB B	$Acc \leftarrow Acc - B$
SBB B	$Acc \leftarrow Acc - B - Carry$
SUB address	$Acc \leftarrow Acc - Memory[address]$
SBB address	$Acc \leftarrow Acc - Memory[address] - Carry$
SUB Immediate	$Acc \leftarrow Acc - Immediate$
SBB Immediate	$Acc \leftarrow Acc - Immediate - Carry$
INC	$Acc \leftarrow Acc + 1$
DEC	$Acc \leftarrow Acc - 1$
IN	$Acc \leftarrow Input\_port$
OUT	$Output\_port \leftarrow Acc$
PUSH	Pushes the content of the Accumulator to the Stack
POP	Pops off top element of stack to Accumulator
AND B	$Acc \leftarrow Acc.B$
AND address	$Acc \leftarrow Acc.Memory[address]$
AND Immediate	$Acc \leftarrow Acc.Immidiate$
OR B	$Acc \leftarrow Acc \vert B$
OR address	$Acc \leftarrow Acc \vert Memory[address]$
OR Immediate	$Acc \leftarrow Acc \vert Immidiate$
XOR B	$Acc \leftarrow Acc \oplus B$
XOR address	$Acc \leftarrow Acc \oplus Memory[address]$
XOR Immediate	$Acc \leftarrow Acc \oplus Immidiate$
NOT	$Acc \leftarrow !Acc$
NEG	$Acc \leftarrow -Acc$
XCHG	$Acc \Longleftrightarrow B$ [Exchanges the content of Accumulator and B]
CMP B	Accumulator will be unchanged. Set flags according to $(Acc - B)$

TEST B	Accumulator will be unchanged. Set flags according to ($Acc.B$)
SHL	$Acc \leftarrow Acc << 1$, $Carry \leftarrow Acc[MSB]$, $Acc[LSB] \leftarrow 0$
SHR	$Acc \leftarrow Acc >> 1$, $Carry \leftarrow Acc[LSB]$, $Acc[MSB] \leftarrow 0$
ROL	$Acc \leftarrow Acc << 1$, $Carry \leftarrow Acc[MSB]$, $Acc[LSB] \leftarrow Acc[MSB]$
ROR	$Acc \leftarrow Acc >> 1$, $Carry \leftarrow Acc[LSB]$, $Acc[MSB] \leftarrow Acc[LSB]$
RCL	$Acc \leftarrow Acc << 1$, $Acc[LSB] \leftarrow Carry$, $Carry \leftarrow Acc[MSB]$
RCR	$Acc \leftarrow Acc >> 1$, $Acc[MSB] \leftarrow Carry$, $Carry \leftarrow Acc[LSB]$
JMP address	Jumps to the $address$
JC address	Jumps to the $address$ if Carry flag is set
JNC address	Jumps to the address if Carry flag is not set
JZ address	Jumps to the $address$ if Zero flag is set
JNZ address	Jumps to the $address$ if Zero flag is not set
JO address	Jump if Overflow
JNO address	Jump if no Overflow
JE address	Jump if equal
JNE address	Jump if not equal
JG address	Jump if greater
JL address	Jump if less
CALL address	Calls a subroutine (at the specified $address$) unconditionally
RET	Returns from current subroutine to the caller unconditionally
CMC	Complements the Carry flag
CLC	Clears the Carry flag
STC	Sets the Carry flag
CLZ	Clears the Zero flag
STZ	Sets the Zero flag
CLS	Clears the Sign flag
STS	Sets the Sign flag
HLT	Halts execution
NOP	No Operation

3 Instruction Set Assignment

Group ID	Instructions to be Implemented
A1 G1	STA address; MOV B, Acc; ADC address; ADC Immediate; SBB address; SBB Immediate; DEC; IN; OUT; PUSH; POP; AND Immediate; XOR address; XOR Immediate; XCHG; NOT; CMP B; SHL; ROL; JMP address; JE address; JG address; CLC; CLZ; HLT;
A1 G2	LDA address; STA address; MOV B, Acc; MOV Acc, Immediate; ADD B; ADC Immediate; SUB B; INC; OUT; PUSH; POP; OR B; OR address; NOT; CMP B; ROR; RCR; JMP address; JC address; JG address; CALL address; RET; CMC; CLS; HLT;
A1 G3	LDA address; STA address; MOV Acc, B; ADD B; ADC Immediate; SBB B; SUB address; SBB address; SUB Immediate; OUT; OR B; OR address; NEG; NOT; TEST B; SHL; RCL; JMP address; JZ address; JNE address; CALL address; RET; STC; STS; HLT;
A1 G4	LDA address; STA address; MOV B, Acc; MOV Acc, Immediate; ADC B; ADC address; SBB address; OUT; PUSH; POP; AND B; OR address; OR Immediate; NOT; XCHG; CMP B; TEST B; ROL; RCL; JMP address; JNZ address; CLC; CLS; HLT; NOP;
A1 G5	LDA address; STA address; ADD B; ADC address; ADD Immediate; SUB address; SUB Immediate; INC; IN; OUT; PUSH; POP; AND Immediate; OR address; NOT; NEG; CMP B; SHL; SHR; JNC address; JNZ address; CALL address; RET; CMC; HLT;
A1 G6	MOV B, Acc; ADD B; SUB B; SBB B; SUB address; SBB Immediate; DEC; OUT; PUSH; POP; AND B; XOR Immediate; NOT; XCHG; TEST B; SHR; ROL; JNC address; JG address; CALL address; RET; CMC; CLZ; HLT; NOP;
A2 G1	STA address; MOV Acc, B; ADC B; ADD address; SUB B; IN; OUT; PUSH; POP; AND B; AND address; OR B; NEG; XCHG; CMP B; SHL; ROL; JC address; JNZ address; JE address; CALL address; RET; CLC; HLT; NOP;
A2 G2	STA address; MOV Acc, Immediate; ADC address; ADD Immediate; ADC Immediate; INC; IN; OUT; PUSH; POP; AND Immediate; OR address; XCHG; TEST B; SHR; ROR; RCR; JE address; JG address; CALL address; RET; CLC; STZ; HLT; NOP;
A2 G3	STA address; MOV B, Acc; ADD B; SBB B; SBB Immediate; OUT; PUSH; POP; AND address; OR B; XOR B; XOR address; NOT; TEST B; XCHG; SHR; ROR; RCL; JNZ address; JG address; CALL address; RET; CLS; STS; HLT;
A2 G4	ADC B; ADC address; ADD Immediate; ADC Immediate; SUB B; SUB address; OUT; PUSH; POP; AND B; XCHG; CMP B; SHL; SHR; ROL; ROR; JZ address; JE address; JNE address; JG address; CALL address; RET; CMC; CLZ; HLT;

A2 G5	MOV Acc, B; ADD B; ADD address; ADC address; ADC Immediate; SBB address; OUT; PUSH; POP; AND B; AND address; AND Immediate; XOR B; XOR address; NOT; NEG; XCHG; CMP B; RCL; JNC address; CMC; STZ; CLS; HLT; NOP;
A2 G6	STA address; MOV Acc, B; MOV Acc, Immediate; ADD address; SUB B; SUB address; OUT; PUSH; POP; AND B; OR B; OR address; XOR B; XOR Immediate; NEG; TEST B; SHL; ROL; RCR; JNC address; JNE address; CMC; STS; HLT; NOP;
B1 G1	LDA address; STA address; MOV B, Acc; ADC B; ADD address; SUB address; SBB address; OUT; OR B; OR address; OR Immediate; XOR B; XOR address; NOT; CMP B; SHR; RCR; JC address; JE address; JG address; CALL address; RET; CLZ; STS; HLT;
B1 G2	MOV Acc, Immediate; ADC address; ADD Immediate; ADC Immediate; SUB B; SBB B; SBB address; SUB Immediate; DEC; OUT; AND Immediate; XOR B; XOR address; NEG; CMP B; SHL; ROL; RCL; JMP address; JC address; JG address; CMC; STC; CLZ; HLT;
B1 G3	LDA address; STA address; MOV Acc, B; ADD Immediate; ADC address; SBB address; DEC; OUT; PUSH; POP; OR B; XOR B; XOR Immediate; NOT; TEST B; ROL; ROR; JZ address; JE address; JNE address; JL address; CMC; STC; CLS; HLT;
B1 G4	LDA address; STA address; MOV B, Acc; ADD B; ADC B; ADC address; SUB address; SUB Immediate; OUT; PUSH; POP; AND B; AND Immediate; OR Immediate; NOT; CMP B; ROL; RCL; RCR; JG address; CALL address; RET; CMC; CLS; HLT;
B1 G5	LDA address; STA address; ADD B; ADC B; ADD address; SBB Immediate; INC; DEC; OUT; AND B; OR address; XOR address; NOT; NEG; TEST B; SHL; ROR; RCR; JMP address; JNZ address; CALL address; RET; CLC; CLZ; HLT;
B1 G6	STA address; ADD B; ADD address; IN; OUT; PUSH; POP; AND B; AND Immediate; OR address; NOT; CMP B; XCHG; SHL; SHR; RCR; JNC address; JZ address; CALL address; RET; CLC; STC; STZ; HLT; NOP;
B2 G1	STA address; MOV Acc, B; ADC B; ADD Immediate; SUB B; SBB address; SUB Immediate; SBB Immediate; IN; OUT; PUSH; POP; AND B; AND address; OR address; XOR B; NOT; CMP B; SHL; JZ address; JE address; JL address; CMC; STS; HLT;
B2 G2	LDA address; MOV B, Acc; MOV Acc, Immediate; ADD B; ADC address; ADD Immediate; ADC Immediate; SUB B; SBB B; SUB Immediate; OUT; DEC; IN; OR Immediate; NOT; CMP B; TEST B; SHL; SHR; RCL; JC address; JE address; CLS; HLT; NOP;

B2 G3	STA address; MOV Acc, B; ADD B; ADD address; SUB B; SBB B; SBB address; SUB Immediate; SBB Immediate; DEC; OUT; AND B; OR address; OR Immediate; XOR address; NEG; XCHG; CMP B; TEST B; ROL; RCL; CALL address; RET; CLC; HLT ;
B2 G4	LDA address; STA address; MOV Acc, B; MOV Acc, Immediate; ADC B; ADD address; ADC address; SBB B; SUB address; OUT; AND Immediate; OR B; XOR B; XCHG; CMP B; SHL; ROR; JMP address; CMC; CLC; CLZ; STS; HLT; HLT; NOP;
B2 G5	STA address; MOV Acc, B; MOV B, Acc; ADC B; SUB B; SBB address; SBB Immediate; IN; OUT; PUSH; POP; AND B; OR address; OR Immediate; XOR address; CMP B; SHL; ROR; JMP address; JNC address; JG address; JL address; CMC; CLC; HLT;
B2 G6	LDA address; MOV Acc, Immediate; ADC B; ADC address; SUB address; OUT; INC; PUSH; POP; AND Immediate; OR B; OR Immediate; XOR B; NOT; TEST B; ROL; ROR; JZ address; JE address; JG address; CALL address; RET; CMC; STS; HLT;

4 Report Content

Contents of the report are recommended as follows:

- Introduction
- Instruction Set
- Block Diagram
- Brief Description of Blocks
- Circuit Diagram printed in drawing paper
- Complete Cycle Descriptions of all the Instructions
  - Micro Operations associated with each Macro Instruction
  - The Active Signals
- Timing diagram of at least 5 instructions including *CALL address/ADC address* operation
- How to write and execute a program in this machine
- Special Features Implemented if any (may carry bonus marks)
- ICs used with their count
- Discussion

N.B. Both hardcopy and softcopy of the report along with all the necessary Proteous file should be submitted.