



North South University
Department of Electrical & Computer Engineering
LAB REPORT-3

Course Code: CSE231L

Course Title: Digital Logic Design

Section: 8

Experiment Number: 3

Experiment Name:

Combinational Logic Design

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Objectives:

- We have to become familiarized with the analysis of combinational logic networks.
- Then we have to learn the implementation of networks using the two canonical forms.

Apparatus:

- Trainer Board
- 1 x IC 7411 Triple 3-input AND gates
- 2 x IC 4075 Triple 3-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)

Theory:

Min terms and Max terms:

Min terms are basically product terms, where all the variables appear either in normal form or in complement form & Max terms are the sum terms, where all the variables appear either in normal or in complement form.

Analysis of Combinational Logic Design:

A combinational logic design is designing a circuit with certain number of inputs and outputs. And analysis of these circuits is determining the input-output relationship (truth tables in most of the case) of the circuit then knowing how the circuit is operating and then verifying if the truth table holds.

Canonical Forms:

There are two canonical forms. One expresses a Boolean function as a Sum of Min terms or we could say Sum of Products (SOP). Example.

$$F = \Sigma(m_0, m_1, m_2, m_3)$$

And the other expresses the function in Product of Min terms also known as Product of Sums (POS) form. Example.

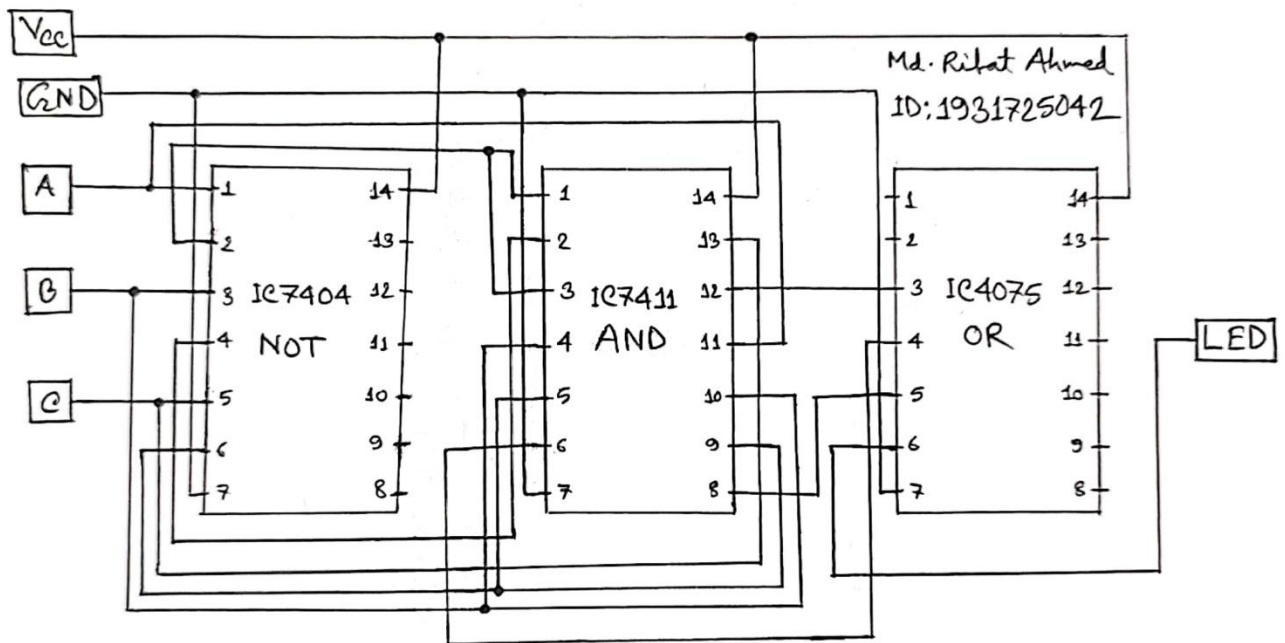
$$F = \Pi(M_0, M_2, M_4, M_6, M_8)$$

Experimental Procedure:

- At first, we need to write all the min terms and max terms for three inputs.
- Then we have to write the function F in 1st and 2nd canonical forms.
- After that we have to draw the circuits for the two canonical forms.
- Then finally, we need to construct the 1st and 2nd canonical form of the circuit.

Question/Answer:

IC Diagram:



IC Diagram for the 1st Canonical Form
of the circuit

Discussion:

Through this lab we learned about min terms and max terms, combinational logic designing and canonical forms. We started out with completing the Table 1 where we filled the Min terms and Max terms for a three-input case. After that we saw two canonical forms made from Table 1 in Table 2, which was derived from the output of the first table. Then we build both the circuits and then we used Logisim to simulate our both circuit which is of 1st and 2nd canonical forms and then verified its result using the truth table. Then in class we talked about what we should do if our circuit isn't working properly or if any of the gates or all the gates of an IC is not working. Then we also saw how we can convert a 3-input gate into a 2-input gate just by shorting a circuit or we can also set the 3rd input or the Vcc of an AND and NAND gate to 1 to make them work like 2-input gates. And for OR and NOR gate we can set the 3rd input or the ground (GND) to 0 to make them work like 2-input OR and NOR gates.

So overall, in this experiment we learned many new things like min term, max terms, canonical forms, designing combinational circuits then converting a 3-input gate into a 2-input gate. The only drawback of this experiment is that we couldn't do the experiment in physical lab.

Data Sheet & Circuit Diagrams:

Input Reference	$A B C$	F	Min term	Max term
0	0 0 0	0	$A'.B'.C'$	$A+B+C$
1	0 0 1	1	$A'.B'.C$	$A+B+C'$
2	0 1 0	1	$A'BC'$	$A+B'+C$
3	0 1 1	0	$A'BC$	$A+B'+C'$
4	1 0 0	0	$AB'C'$	$A'+B+C$
5	1 0 1	0	$AB'C$	$A'+B+C'$
6	1 1 0	1	ABC'	$A'+B'+C$
7	1 1 1	0	ABC	$A'+B'+C'$

Table 1: Truth Table to a Combinational Circuit

	Shorthand Notation	Function
1st Canonical Form	$F = \Sigma(m_1, m_2, m_6)$	$F = A'B'C + A'BC' + ABC'$ (SOP)
2nd Canonical Form	$F = \Pi(M_0, M_3, M_4, M_5, M_7)$	$F = (A+B+C).(A+B'+C').(A'+B+C).(A'+B+C').(A'+B'+C')$ (POS)

Table 2: 1st and 2nd Canonical Forms of the Combinational Circuit of Table 1

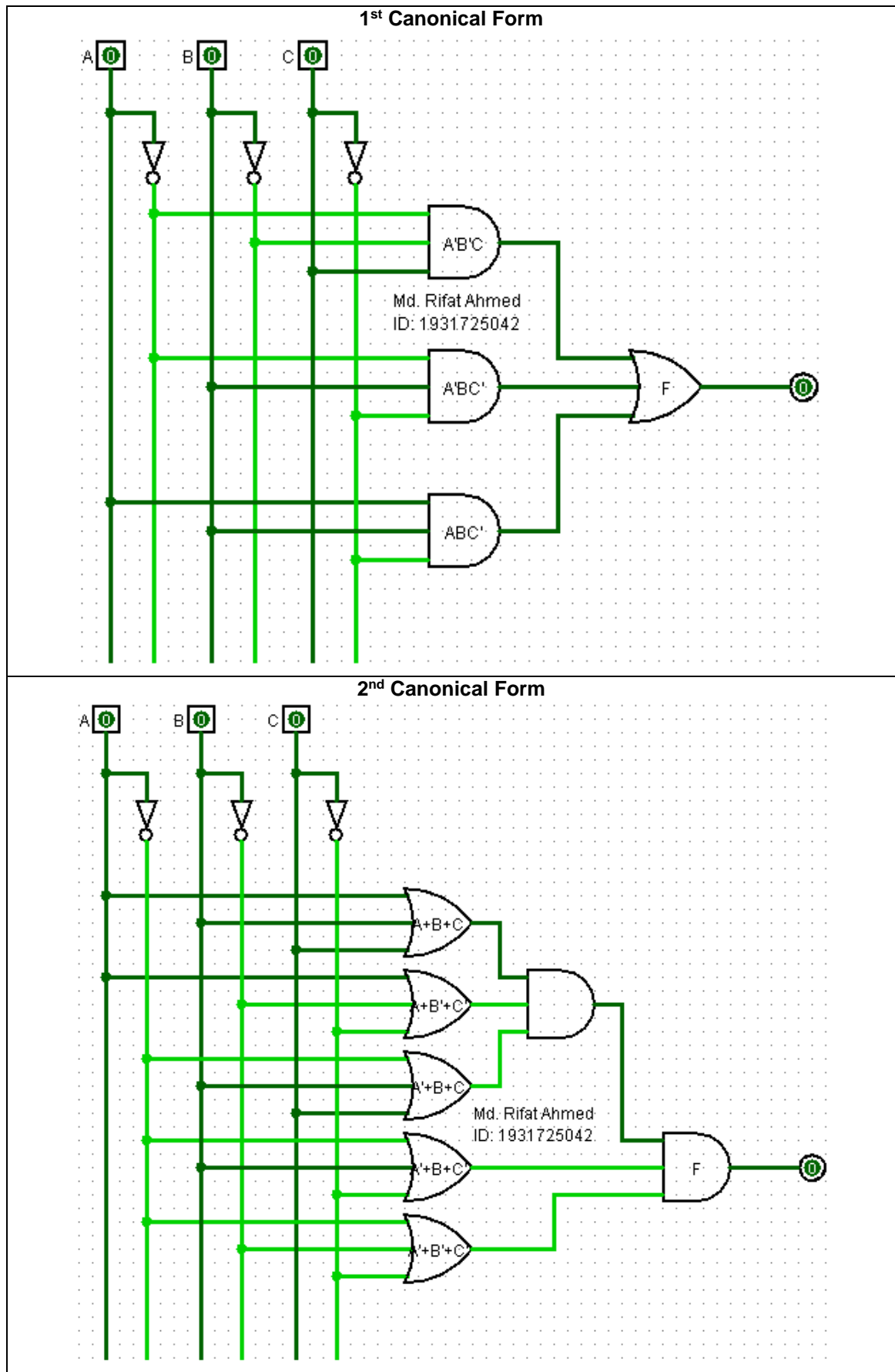


Figure 1: 1st and 2nd Canonical Circuit Diagrams of the Combinational Circuit of Table 1

Simulation:

Simulating the 2nd Canonical Circuit:

