

North South University Department of Electrical & Computer Engineering

LAB REPORT-4

Course Code: CSE231L

Course Title: Digital Logic Design

Section: 8

Experiment Number: 4

Experiment Name:

Combinational Logic Design

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Objectives:

- At first, we have to design a complete minimal combinational logic system from specification to implementation.
- Then we have to minimize combinational logic circuits using Karnaugh maps.
- After that we have to learn various numerical representation systems.
- Finally, we have to implement the circuits using canonical minimal forms.

Apparatus:

- Trainer Board
- 1 x IC 4073/7411 Triple 3-input AND gates
- 1 x IC 4075 Triple 3-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)
- 1 x IC 7400 2-input NAND gates
- 2 x IC 7408 2-input AND gates

Theory:

BCD Number System:

BCD means Binary Coded Decimal and this number system was created to represent a decimal number (from 0 to 9) using a 4-bit Binary number like (9)_{Decimal} = (1001)_{BCD}.

However, as it can represent only 0 to 9 of decimal the way we write 10 would be,

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(10)_{Decimal} = (0001\ 0000)_{BCD}
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where (0001)_{Binary} represents (1)_{Decimal} and (0000)_{Binary} represents (0)_{Decimal}.

And thus, a BCD and Binary number system has a bit of a difference. The number 10 in BCD is 00010000 but it's 16 in Binary and so we need to add an extra 6 to the Binary number to get the BCD number whenever the Decimal number is more than 9. I.e.

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(10)_{Decimal} = (1010)_{Binary} = (0001\ 0000)_{BCD}
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Excess-3 Number System:

Excess-3 number system is just like the binary number system except it starts from 3 so it's like a binary system where each binary number is added with an extra 3.

Karnaugh Map (K-map):

Karnaugh map or in short K-map is used to minimize Boolean functions by forming various patterns of the 1s in the diagram where each of the box in the diagram represents a minterm.

WX YZ	00	01	11	10
00	m ₀	m ₁	m ₃	m ₂
01	m ₄	m ₅	m ₇	m ₆
11	m ₁₂	m ₁₃	m ₁₅	m ₁₄
10	m ₈	m ₉	m ₁₁	m ₁₀

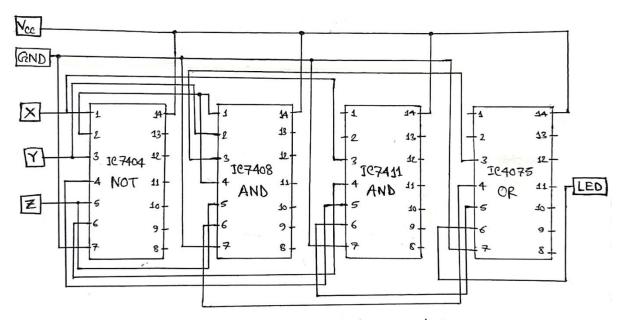
Fig: A 4 variable K-map

Experimental Procedure:

- At first, we need to complete Table 1 and identify out inputs and outputs.
- Then we have to complete the K-maps for each of variable of the outputs to find the minimal 1st canonical functions.
- Then we need to draw the circuit using the functions we got after completing the K-maps and verify the output using the truth table.
- Then finally, we have to construct the circuit again but this time using universal gates only.

Question/Answer:

IC Diagram:



IC Diagram for output B=X'Z+X'Y+XY'Z' of the BCD to Excess-3 converter

Discussion:

Through this lab we learned about BCD number system, Excess-3 number system and how to minimize a function using K-map. In this lab we started out with completing the K-maps for 4 output variables. Then we built a circuit using the 4 functions that we got from the K-maps. Then we saw how we can display our output using a LED matrix in Logisim. This way we can see the output together for all the variables as a whole. Then we also talked about how to implement the circuit using only universal gates.

So overall, in this experiment we learned how to minimize a function using a K-map without much hassle like gate-level minimization. Then we also learned how to use splitter and led matrix in Logisim. And as for the drawbacks of this experiment there wasn't any expect for doing the experiment in physical lab.

Data Sheet & Circuit Diagrams:

Decimal	Binary Coded Decimal (BCD)				Excess-3			
Digit	W	Х	Υ	Z	Α	В	С	D
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table 1: Truth table - BCD to Excess-3

Number of inputs bits:	4	Input variables:	4
Number of outputs bits:	1	Output variables:	4

Table 2: System analysis

	Kmap for A:					Kmap for B:		
	Y'Z'	Y'Z	YZ	YZ'	0	I	1	1
W'X'	0	0	0	0	1	0	0	0
W'X	0	i	1	1	X	X	X	X
WX	X	X	X	X	0	1	X	X
WX'	1	1	X	X		<u> </u>		
	A=W+ XY+X Z	1				B+X'Z +X'Y+ XY'Z'		
	Kmap for C:					Kmap for D:		
	1	0	i	0	1	0	0	1
	1	0	i	0	1	0	0	1
	X	X	X	X	X	X	X	X
	1	0	X	X	1	0	X	X

Figure 1: K-Maps

D=Z'

C = YZ+Y'Z'

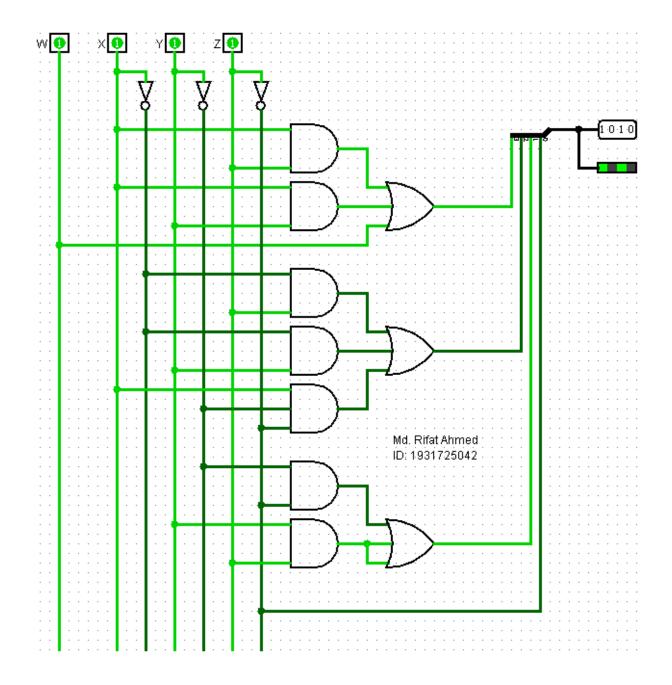


Figure 2: Minimal 1st canonical circuit of BCD to Excess-3 converter

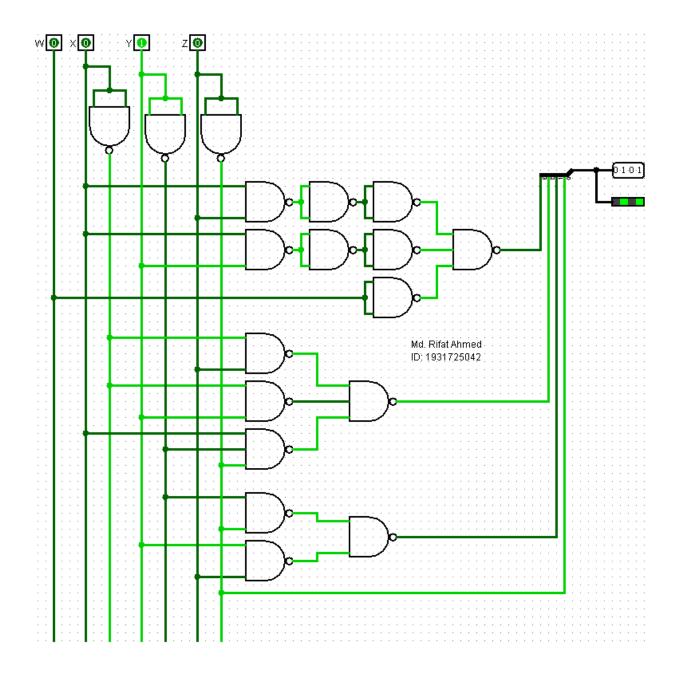


Figure 3: Minimal universal gate implementation of BCD to Excess-3 converter

Simulation:

Simulating the BCD to Excess-3 Converter Circuit:

