Lab 7: Introduction to Flip-Flops and Shift Registers

A. Objectives

- Learn about the concept of states in digital logic and how Flip-Flop circuits can be used to store state information.
- Understand the internal logic of J-K Flip-Flops and implement one using basic logic gates.
- Understand the relationship between J-K, T and D Flip-Flops and observe the characteristics of all three.
- Implement a shift register using D Flip-Flops and analyze its operation.

B. Theory

Flip-Flops: Digital logic circuits can be divided into two types: combinational logic, whose output signals are dependent only on its present input signals, and sequential logic, whose outputs are a function of both the current inputs and the past history of inputs. In sequential logic, information from past inputs is stored in electronic memory elements, such as flip-flops and latches. The stored contents of these memory elements, at a given point in time, is collectively referred to as the circuit's "state" and contains all the information about the past to which the circuit has access.

A flip-flop is a binary storage device that has two stable states and is capable of storing one bit of information. In a stable state, the output of a flip-flop is either 0 or 1. The output can only change when a clock pulse is supplied to the flip-flop. The value that is stored in a flip-flop when the clock pulse occurs is determined by the inputs to the flip-flop at that time or the values presently stored in the flip-flop (or both). The new value is stored (i.e., the flip-flop is updated) when a pulse of the clock signal occurs.

JK, D (“Data” or “Delay”) and T (“Toggle”) are three common types of flip-flops used in digital logic circuits.

In case of the JK flip-flop (J=Set, K=Reset), the combination J = 1, K = 0 is a command to set the flip-flop (i.e., make the output, Q = 1); the combination J = 0, K = 1 is a command to reset the flip-flop (Q = 0); and the combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value. Setting J = K = 0 maintains the current state.

Since the output of a flip-flop may depend on more than its current inputs, a standard truth table is not enough to summarize its operations. Generally, we use two types of tables to express the behavior of flip-flops. The first one is a State Transition Table or a Characteristic Table which shows the state the flip-flop will move to based on the current state and other inputs. It’s similar to a truth table. The second one, called the Excitation Table, shows the minimum inputs that are necessary to generate a particular next state (in other words, to "excite" it to the next state) when the current state is known. **Table B.1** shows the Characteristic Table and Excitation table for the JK flip-flop.

Characteristic Table				Excitation Table			
J	**K**	**Q_{next}**		**Q**	**Q_{next}**	**J**	**K**
0	0	Q		0	0	0	X
0	1	0		0	1	1	X
1	0	1		1	0	X	1
1	1	$\bar{Q}$		1	1	X	0

Table B1: JK flip-flop: Characteristic and Excitation Tables

In the characteristic table, Q_{next} represents what the output will be for the given inputs if a clock pulse is provided. Here, for J = 0 and K = 0, the next output will be the same as the current output (Q). The excitation table shows the values of J and K required to go from Q to Q_{next}. For example, if the current output (Q) is 0 and we want to change it to 1 (Q_{next} = 1), we will have to set J to 1 and provide a clock pulse. The value of K doesn't matter because the output will change to 1 in either case (K = 0 or K = 1)

The T flip-flop changes state ("toggles") whenever the input T is high and the clock input is strobed. If the T input is low, the flip-flop holds the previous value when given a clock pulse. **Table B.2** shows the Characteristic Table and Excitation table for the T flip-flop.

Characteristic Table			Excitation Table		
T	**Q_{next}**		**Q**	**Q_{next}**	**T**
0	Q		0	0	0
			0	1	1
1	$\bar{Q}$		1	0	1
			1	1	0

Table B2: T flip-flop: Characteristic and Excitation Tables

The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. **Table B.3** shows the Characteristic Table and Excitation table for the T flip-flop.

Characteristic Table			Excitation Table		
D	**Q_{next}**		**Q**	**Q_{next}**	**D**
0	0		0	0	0
			0	1	1
1	1		1	0	0
			1	1	1

Table B3: D flip-flop: Characteristic and Excitation Tables

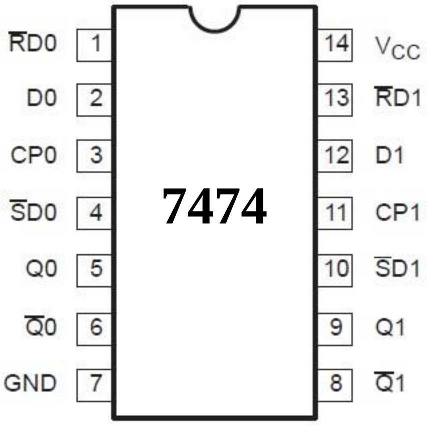
A storage element in a digital circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states. The major differences among various types of storage elements are in the number of inputs they possess and in the manner in which the inputs affect the binary state. Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches; those controlled by a clock transition are flip-flops. Latches are said to be level sensitive devices; flip-flops are edge-sensitive devices. The two types of storage elements are related because latches are the basic circuits from which all flip-flops are constructed.

Registers: A register is a group of flip-flops. Each flip-flop is capable of storing one bit of information. An n-bit register contains a group of n flip-flops capable of storing n bits of binary information. In addition to flip- flops, a register may have combinational gates that perform certain data processing tasks. In the broadest definition, a register consists of a group of flip-flops and gates that effect their transition. The flip-flops hold binary information and the gates determine how the information is transferred into the registers.

A register that is capable of shifting its binary information either to its right or its left is called a shift register. The logical configuration of a shift register consists of a chain of flip-flops connected in cascade, with the output of one flip flop connected to the input of the next flip-flop. All flip-flops receive a common pulse which causes the shift from one stage to the next.

New Apparatus:

IC 7474 (Dual D Flip-Flops):



PINS	DESCRIPTION
D0, D1	Data inputs
CP0, CP1	Clock inputs (active rising edge)
$\overline{SD}0$, $\overline{SD}1$	Set inputs (active low)
$\overline{RD}0$, $\overline{RD}1$	Reset inputs (active low)
Q0, Q1, $\overline{Q}0$, $\overline{Q}1$	Data outputs

Figure B1: Pinout of IC7474

The 7474 is a 14 pin IC which requires a Ground connection at pin 7 and V_{CC} at pin 14. Pins 2 and 12 serve as the inputs for the two Flip-Flops and pins 5 and 9 act as the corresponding outputs. Pins 6 and 8 provide the inverse of the outputs. Pin 3 is the clock input for the first Flip-Flop and pin 11 is the clock input for the second Flip-Flop.

Experiment 1: Constructing a JK Flip-Flop using AND and NOR gates

C.1 Apparatus

- Trainer board
- 1 x IC 7402 2-input NOR gates
- 1 x IC 7411 3-input AND gates

D.1 Procedure

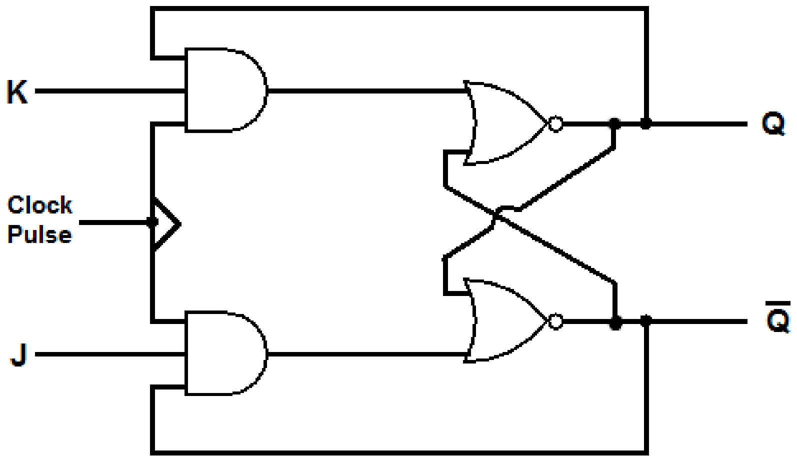


Figure D.1.1 JK Flip-Flop implemented using AND and NOR gates

1. Construct the circuit for the JK Flip-Flop shown in **Figure D.1.1**.
2. Complete the truth table (**Table F.1.1**) as instructed below. In each step, after you set the values for J and K, send one clock pulse first and observe the output. Then, send several more clock pulses and see if the output changes for each pulse.
   - Set both J and K to 0.
   - Set J to 1 (keep K at 0)
   - Once again, set both J and K to 0
   - Now, set K to 1 (keep J at 0)
   - Finally, set both J and K to 1
   - Use your observations to complete the truth table.
3. **Do not** dismantle the circuit after the experiment is complete.

Experiment 2: Using a JK Flip-Flop to construct T Flip-Flop and D Flip-Flop

C.2 Apparatus

- Trainer board
- 1 x IC 7402 2-input NOR gates
- 1 x IC 7411 3-input AND gates
- 1 x IC 7404 Hex Inverter (NOT gates)

D.2 Procedure

1. Use the logic diagram in **Figure D.2.1** to convert your already constructed JK Flip-Flop into a T Flip-Flop. This is done by connecting the J and K input terminals of the J-K Flip-Flop to the same switch (T).
2. Complete the truth table (**Table F.2.1**) as instructed below:
    - First, set the input (T) to 0 and send several clock pulses. Observe the output for each pulse.
    - Now, set T to 1 and send several more clock pulses. Once again, observe the output for each pulse.
    - Then, set T to 0 **while the output is 1** and observe what happens to the output in response to subsequent clock pulses.
    - Finally, set T to 1 and send **only one clock pulse** to set the output to 0.
    - Repeat these four steps if necessary.
    - Use your observations to complete the truth table.

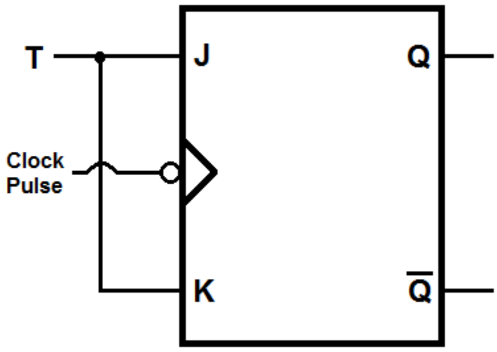


Figure D.2.1: T flip-flop constructed using JK flip-flop

3. Now, use the logic diagram in **Figure D.2.2** to convert the JK Flip-Flop into a D Flip-Flop using a NOT gate. This is done by connecting an input switch to the J terminal and connecting the inverse of that input to the K terminal. The input switch, in this case is called D.
4. Complete the truth table (**Table F.2.2**) as instructed below:
    - First, set the input (D) to 0 and send several clock pulses. Observe the output for each pulse.
    - Now, set D to 1 and send several more clock pulses. Once again, observe the output for each pulse.
    - Then, set D to 0 and send several more clock pulses. Once again, observe the output for each pulse.
    - Repeat these three steps if necessary.
    - Use your observations to complete the truth table.

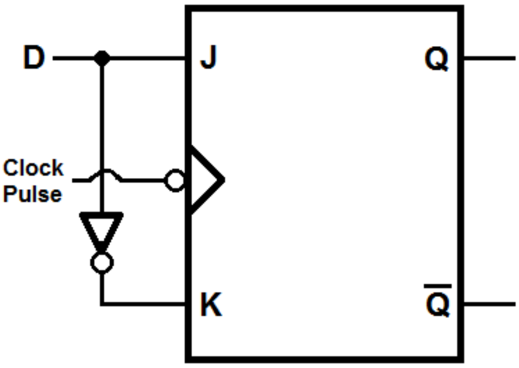


Figure D.2.2: D flip-flop constructed using JK flip-flop

E.2 Report

1. Briefly explain the difference between T and D Flip-Flops.

Experiment 3: Constructing a right shift register using D Flip-Flops

C.3 Apparatus

- Trainer board
- 2 x IC 7474 (D Flip-Flop)

D.3 Procedure

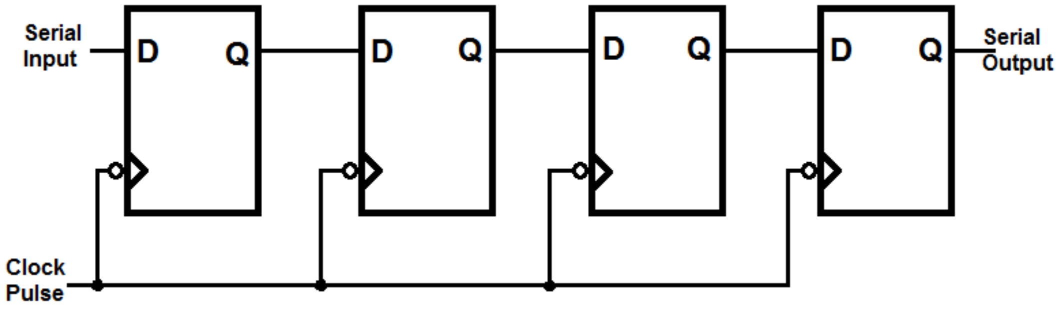


Figure D.3.1: Right Shift Register

1. Use the circuit diagram in Figure D.3.1 to construct the Right Shift Register. Each 7474 IC contains two D Flip-Flops so you will need 2 ICs to implement the circuit. Wire up the IC 7474 using the diagram in **Figure B1** as your reference. Connect the output (Q) of each of the four Flip-Flops to a separate LED. Connect the input switch to an LED as well.
2. Use the following steps to determine how the shift register works. For each step, observe which LEDs light up.
   a) Set the input to 1 and send a clock pulse. Now, set the input to 0 and send several more clock pulses.
   b) Once again, set the input to 1 and send clock pulses until all the LEDs are lit.
   c) Set the input to 0 and send clock pulses until all the LEDs are turned off once more.
   d) Try to find a combination of inputs and clock pulses that will produce an ON-OFF-ON-OFF sequence in the four output LEDs.
   e) Use this knowledge to complete the State Table in **Table F.3.1.**

E.3 Report

1. Why do we need shift registers?
2. What would happen if the output of the last D Flip-Flop in the register was connected to the input of the first D Flip-Flop?

Simulation: Experiment-3

F.1 Experimental Data: J-K Flip-Flop using AND and NOR gates

J	K	Qnext	Q′
1	0	1	
0	0	1	
0	1	0	
0	0	0	
1	1	1	
1	0	1	
1	0	1	
1	1	0	

Table F.1.1

F.2 Experimental Data: T and D Flip-Flops using J-K Flip-Flops

T	Q
0	
1	

Table F.2.1

D	Q
0	
1	

Table F.2.2

F.3 Experimental Data: Right shift register using D Flip-Flops

States	Input	Output
Initial State	X	XXXX
T1	1	1XXX
T2	0	01XX
T3	1	101X
T4	0	0101

Table F.3.1