



North South University

Department of Electrical and Computer Engineering

CSE231L - Digital Logic Design Lab Lab Outline

Instructor:

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Office hours:

Saturday: 04:10pm-06:10pm

Thursday: 04:10pm-06:10pm

Office room: LIB600(C1)

*If you need extra office hours, make an appointment by text or email.

Tentative Class Plan:

Week	Topic	Assessment
1	Digital Logic Gates and Boolean Functions	
2	Universal Logic Gates	
3	Combinational Logic Design (Canonical Form)	
4	Combinational Logic Design (K Maps)	Quiz-1
5	Binary Arithmetic	
		Midterm
6	Multiplexer and Decoder	
7	Flip-Flops - Registers	
8	Synchronous Sequential Circuits	Quiz-2
9		Final

Tentative Marking Rubric:

Category	Marks (in %)
Attendance	10
Class Performance	5
Lab Report & Simulation (Individual)	25
Quiz (Written)	20
Midterm Exam (Written)	20
Final Exam (Written)	20
Total	100

Lab Report Marks Distribution (20 Points):

- Cover Page-0.5
- Experiment Name-0.5
- Objective-0.5
- Apparatus-0.5
- Theory-1
- Circuit Diagram-1
- Experimental Procedure-1
- Results-0 (omitted for online classes)
- Question/ Answer-6
- Discussion-3
- Data Sheet-1
- Simulation-5

***Check the file-‘Lab Report Instructions’ for further details.**