Fall-2020

Final Exam

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sec: 08

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Ans.no.1

⇒ $F(A,B,C) = \Sigma(0,2,6,7)$

A	B	C	F	Data Inputs
0	0	0	1	$I_0 = 1$
0	0	1	0	
0	1	0	1	$I_1 = 0$
0	1	1	0	
1	0	0	0	$I_2 = B$
1	0	1	0	
1	1	0	1	$I_3 = B$
1	1	1	1	

AC select bit	I_0	I_1	I_2	I_3
B'	1	0	0	0
B	1	0	1	1
Input Values	1	0	B	B

2 Truth Table:

Clock	J	K	Q_{n+1}
0	x	x	Q_n } memory
1	0	0	Q_n } memory
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$ (toggle)

CH-Table:

Q_n	J	K	$Q(n+1)$
[0]	0	0	[0]
[0]	0	1	[0]
[0]	1	0	[1]
[0]	1	1	[1]
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation Table:

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

When Q_n and Q_{n+1} are [illegible]

we can conclude,
When Q_n is 00; $Q(n+1)$ is also 00. That's why it is only dependent of J and we place don't care in K in the excitation table

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Ans no. 3

$(1010)_2$

1's compliment $(0101)_2$

$+ \quad \uparrow$

2's compliment = $(0110)_2$

Now,

$$\begin{array}{r} (1100)_2 \\ +(0110)_2 \\ \hline 1010 \end{array}$$

$\therefore (1100)_2 - (1010)_2 = (10)_2$

A 4 bit adder-subtractor is a circuit that is capable of adding or subtracting 4 bit inputs A way to mark inputs output as positive or negative without using multiplexer on each bit is to use XOR gates to procede each bit. In the circuit, we will use 4 XOR gates and 4-bit adder-subtractor. Here, we will input m=1 for subtract. In the adder, we will Input A & (B⊕M) to get subtraction of B from A.

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Ans. no. 4

We can add two 8 bit numbers using two IC 7483 4 bit adder IC. IC 7483 is a 4bit parallel adder which consists of four interconnected full adder along with the look ahead. Here, IC adds the two four bit words along with input carry to produce a 4-bit sum and a one bit carry out. In first adder, the carry input is supposed to be 0. Hence the carry in pin of IC is connected to the ground. This count of adder-1 is connected to Cin input of Adder-2. The second adder adds this carry and the four bits of numbers to produce sum along with final carry out bit Cout. Thus, we can use two IC 7438 to add two 8 bit numbers.

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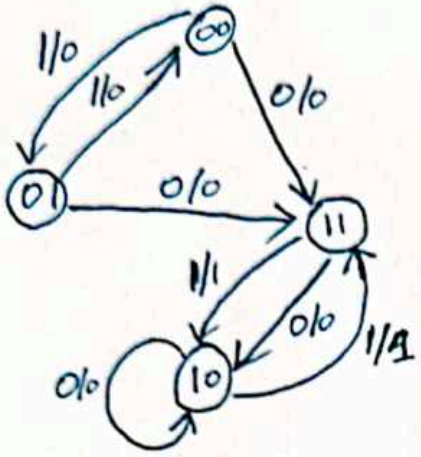
Ans. no. 5



Excitation Table

Q(t)	Q(t+1)	y	h
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Present state		Input	Next State		output	Flip Flop functions			
A	B	X	A	B	Y	y_A	k_A	y_B	k_B
0	0	0	1	1	0	1	X	1	X
0	0	1	0	1	0	0	X	1	X
0	1	0	1	1	0	1	X	X	0
0	1	1	0	0	0	0	X	X	1
1	0	0	1	0	0	X	0	0	X
1	0	1	1	1	1	X	0	1	X
1	1	0	1	0	0	X	0	X	1
1	1	1	1	0	1	X	0	X	1

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State equation

1	0	0	1	0	3	1	0
1	3	1	5	1	7	1	6

$A(t+1) = \bar{X} + A$

1	0	1	1	0	3	1	2
0	3	1	5	0	7	0	6

$B(t+1) = \bar{A}\bar{X} + \bar{B}X$

K-map

$Y_A K_A$

1	0	0	1	0	3	1	2
X_4		X_5		X_7		X_6	

$\therefore Y_A = \bar{X}$

X_0	X_1	X_3	X_2
O_4	D_5	O_7	O_6

$\therefore K_A = 0$

$Y_B K_B$

1	0	1	1	X_3		X_2	
0	4	1	5	X_7		X_6	

$\therefore Y_B = \bar{A} + X$

X_0	X_1	1_3	0_2
X_4	X_5	17	11

$\therefore K_B = X + A$

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Ans. no. 2

JK flip-flop is the same as that of the when J and K are replaced by Q and Q (Next) respectively, except for the indeterminate case.

Here, in the JK excitation table, there is a don't care term in K column. That means whether the input in 1 or 0. According to characteristic table, Q refers to the next state ~~and Q (next) refers to t~~ after the occurrence of the clock pulse.

Here, the flip flop shows that the next state is equal to the present state 0.

Thats why K's value is don't care meaning 0 or 1.

Q	Q (Next	J	K
0	0	0	X

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Circuit Diagram