



North South University
Department of Electrical & Computer Engineering
LAB REPORT-6

Course Code: CSE231L

Course Title: Digital Logic Design

Section: 8

Experiment Number: 6

Experiment Name:

Introduction to Multiplexers and Decoders

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Objectives:

- Our first objective is to understand the concept of multiplexing in the context of digital logic circuits.
- Then we need to learn about the internal logic of digital multiplexers.
- Then we have to implement digital logic functions using multiplexers.
- And finally, we have to observe and analyze the operations of the 3 to 8 Line Decoder.

Apparatus:

Experiment 1:

- 1 x IC 7404 Hex Inverter (NOT gates)
- 2 x IC 7411 3-input AND gates
- 1 x IC 7432 2-input OR gates
- Trainer Board
- Wires

Experiment 2:

- 1 x IC 74151 8:1 Multiplexer
- Trainer Board
- Wires

Experiment 3:

- 1 x IC 74138
- Trainer Board
- Wires

Theory:

Multiplexers:

Multiplexers are combinational circuits that takes information from one of its many inputs and directs it through its single output line. And the selection of the input is controlled by a set of select bits. And for n number of select bits there's 2^n number of inputs in a multiplexer.

Decoders:

Decoders are also combinational circuits but their job is to convert n number of inputs into 2^n number of outputs. And the outputs follow a pattern like binary numbers. Setting all the input value 0 gives the first output, then for the value of x , y as 0 and z as 1 it gives the next output and like this for all input values as 1 it gives the final output.

Experimental Procedure:

Experiment 1:

At first, we have to construct the 4:1 MUX shown in Figure 1. Then for the function $F(A,B,C) = \Sigma(0,1,5,7)$ we need to determine the inputs for A,B select bits and fill up all the data in Table 1.1 and 1.2 and then verify the result using the simulated circuit in Logisim.

Experiment 2:

We have to complete Table 2.1 and 2.2 for the function $F(A,B,C,D) = \Sigma(0,1,3,5,8,9,14,15)$ where we need to determine the values of 8 inputs of the MUX when using A, B and C as the select bits S_2 , S_1 and S_0 respectively. Then we have to draw the IC diagram for the 8:1 MUX using the IC 74151 in Figure 2.

Experiment 3:

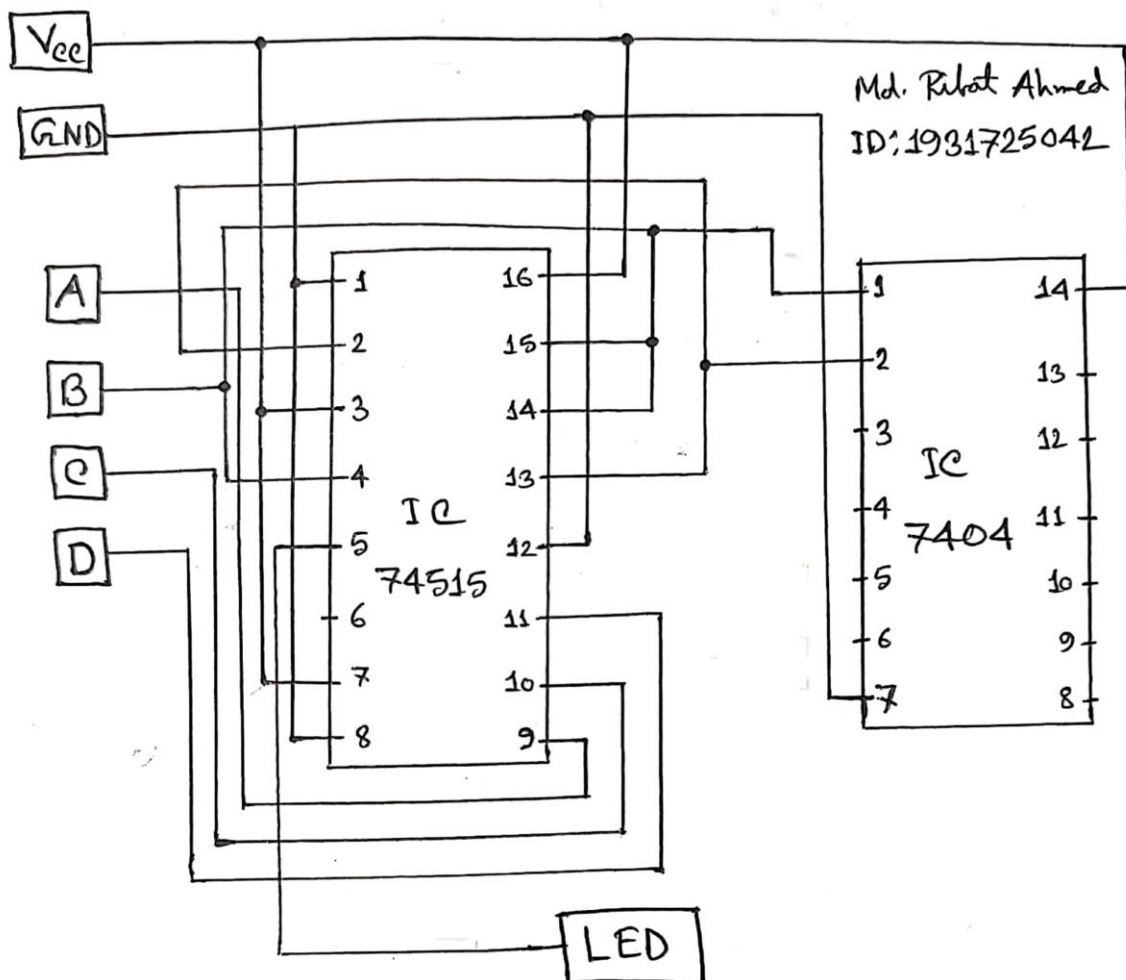
For this experiment we'll start by setting the enable inputs of 74183 IC with appropriate values where G1 should be set to High and both G2A and G2B should be set to low. Then the 3 select bits needs to be connected to 3 binary switches and the 8 outputs needs to be connected to 8 LEDs. Now for different values of the select bits we need to fill up the Table 3.

Question/Answer:

Answer to the Question No. 1 of Experiment 2:

IC diagram of the function $F(A,B,C,D) = \Sigma(1,2,4,5,10,12,13)$ taking A, C and D as the select bits S_2, S_1 and S_0 respectively:

ACD Select bits	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
B'	0(0)	1(1)	1(2)	0(3)	0(8)	0(9)	1(10)	0(11)
B	1(4)	1(5)	0(6)	0(7)	1(12)	1(13)	0(14)	0(15)
Input Values	B	1	B'	0	B	B	B'	0



Answer to the Question No. 1 of Experiment 3:

In an Active-high device the output is high when its input also high and the output is low or ground when the input is low.

And in an Active-low device, the output is high when its inactive and when its active the output is low or ground.

Discussion:

Through this lab we learned about Multiplexers and Decoders. In the first experiment we calculated the inputs for the given function for 2 select bits then built a 4:1 Multiplexer in Logisim. Then in experiment 2 we did the same things for a 4-bit function where 3 are select bits so we had to use a 8:1 Multiplexer this time. Then we drew the two IC diagram for the given functions according to the select bits one in the Question/Answer section and the other in the Circuit Diagram section using a new IC 74151 which is the IC of a 8:1 multiplexer with 16 pins. Then in experiment 3 we learned about another new IC 74183 which is an IC of 3 to 8 line decoder. Its an IC with 16 pins that's Active-low so it gives low output when its activated and high output when its inactive. Then for different values of the select bits we completed the truth table marking the end of our todays experiment. So, to sum it up our lab 6 had 3 experiments where in the first 2 we did the experiments for a 4:1 and 8:1 MUX then in the final experiment we did it for a 3 to 8 line decoder and here we learned about 2 new ICs one for MUX and another for Decoder.

Data Sheet & Circuit Diagrams:

Data of Experiment 1: Implementing a Boolean function using a 4:1 MUX:

	A	B	C	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	1	$I_0 = 1$	1
1	0	0	1	1		1
2	0	1	0	0	$I_1 = 0$	0
3	0	1	1	0		0
4	1	0	0	0	$I_2 = C$	0
5	1	0	1	1		1
6	1	1	0	0	$I_3 = C$	0
7	1	1	1	1		1

Table 1.1

AB Select bits	I_0	I_1	I_2	I_3
C'	1(0)	0(2)	0(4)	0(6)
C	1(1)	0(3)	1(5)	1(7)
Input Values	1	0	C	C

Table 1.2

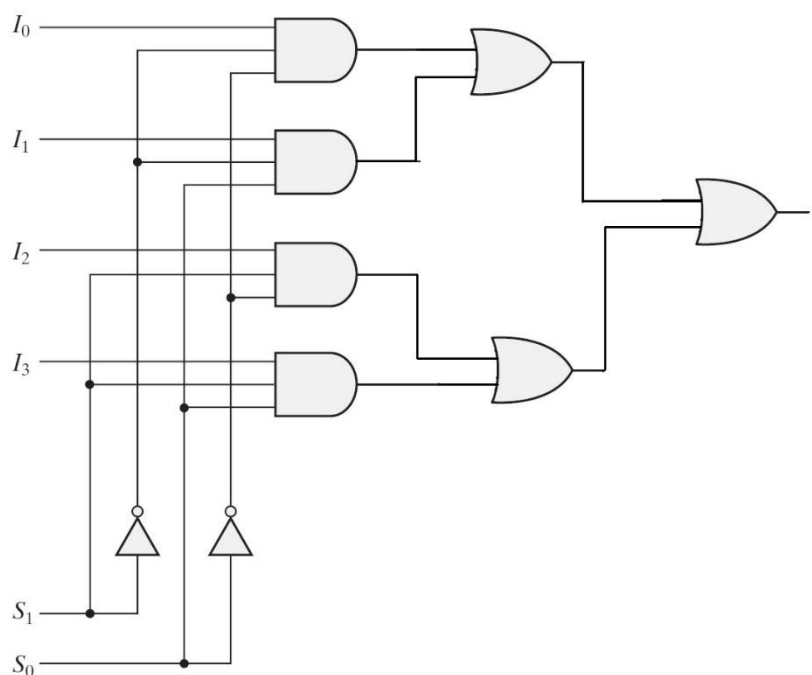


Figure 1: 4:1 Multiplexer

Data of Experiment 2: Using an 8:1 MUX to implement a Boolean function:

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	1	$I_0 = 1$	1
0	0	0	1	1		1
0	0	1	0	0	$I_1 = D$	0
0	0	1	1	1		1
0	1	0	0	0	$I_2 = D$	0
0	1	0	1	1		1
0	1	1	0	0	$I_3 = 0$	0
0	1	1	1	0		0
1	0	0	0	1	$I_4 = 1$	1
1	0	0	1	1		1
1	0	1	0	0	$I_5 = 0$	0
1	0	1	1	0		0
1	1	0	0	0	$I_6 = 0$	0
1	1	0	1	0		0
1	1	1	0	1	$I_7 = 1$	1
1	1	1	1	1		1

Table 2.1

ABC Select bits	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
D'	1(0)	0(2)	0(4)	0(6)	1(8)	0(10)	0(12)	1(14)
D	1(1)	1(3)	1(5)	0(7)	1(9)	0(11)	0(13)	1(15)
Input Values	1	D	D	0	1	0	0	1

Table 2.2

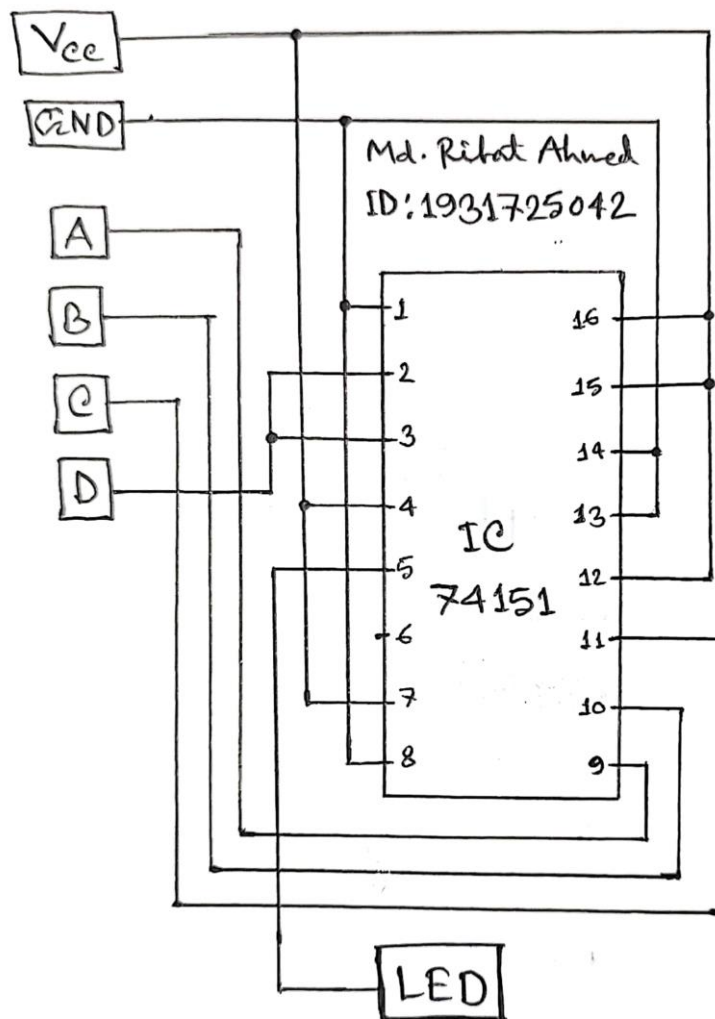


Figure 2

Data of Experiment 3: 3 to 8 Line Decoder:

Enable Inputs		Select Inputs			Outputs							
G1	G2	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Table 3

Simulation:

Simulating the circuit of Experiment 1 with a 4:1 Multiplexer taking B and C as the selection inputs, S_1 and S_0 respectively:

