North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	5
Experiment Title:	Design of a Register File
Course Code:	**CSE332L**
Course Name:	**Computer Organization & Architecture Lab**
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Date of Experiment:	30/11/2021
Date of Submission:	30/11/2021

Objectives:

* Our objective in this experiment is to study how a register file works and a build a register file that has 16 registers.

Equipments:

* Logisim Tool

Block Diagram:

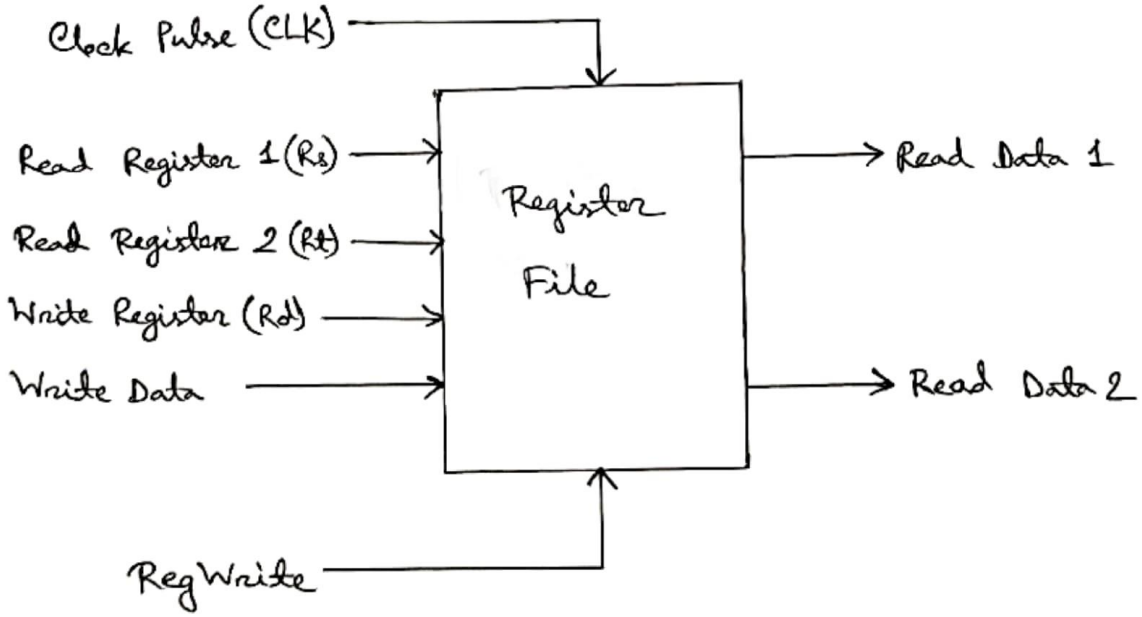

Table:

We'll be building a Register file for the 16-bit ISA with following fields where the formats of the instruction are:

R-type:

OP (4-bit)	Rs (4-bit)	Rt (4-bit)	Rd (4-bit)

I-type:

OP (4-bit)	Rs (4-bit)	Rt (4-bit)	Immediate (4-bit)

J-type:

OP (4-bit)	Target (12-bit)

Circuit Diagram:

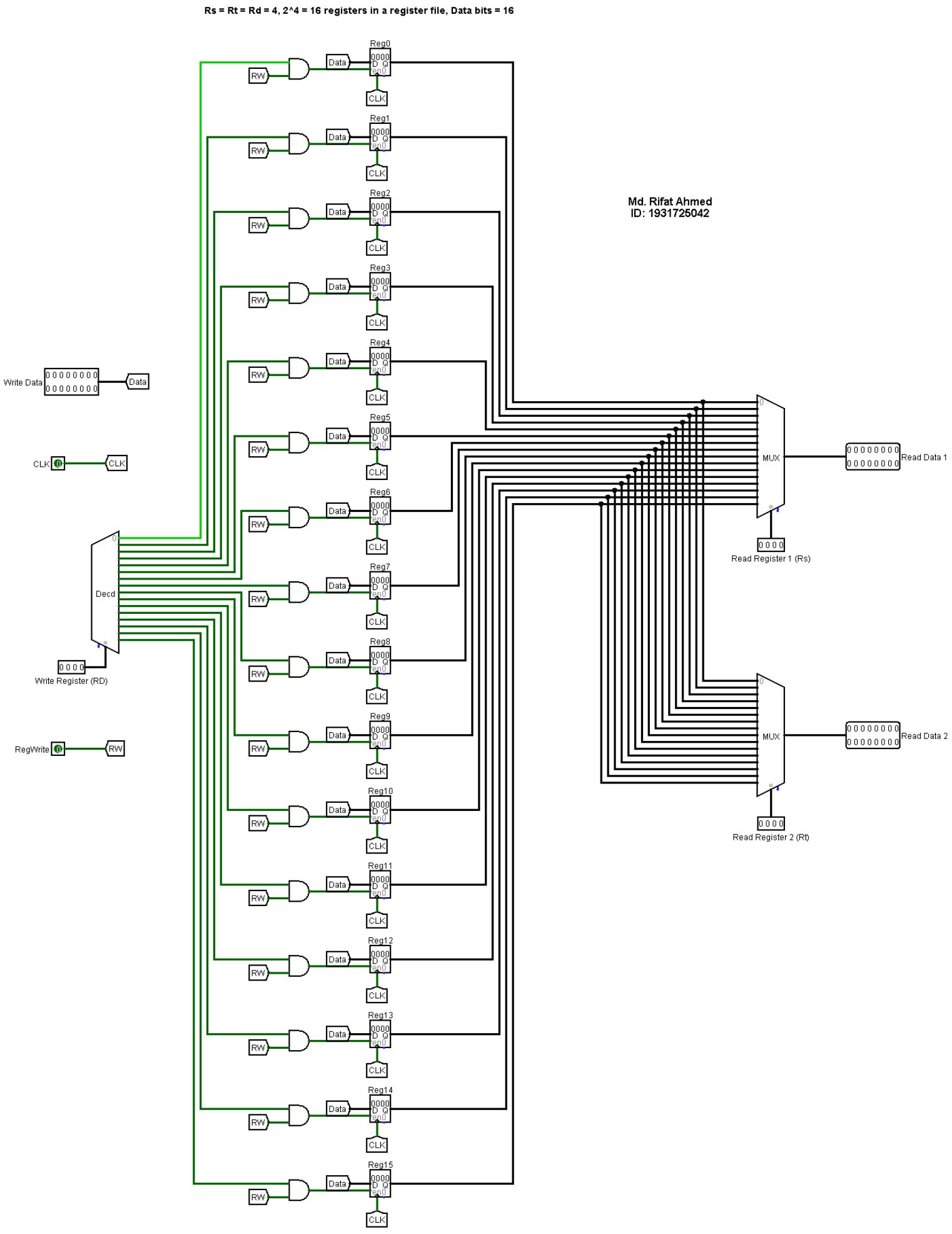

Figure – 2: Circuit diagram of a 4-bit by 4-bit Binary Multiplication Unit

Discussion:

In this experiment we learned how to a register file works and we also built a register file with 16 register where all of them are of 16-bits. To construct the circuit in logisim at first we took 16 registers then added the 'write data' in all of the inputs. Then for selecting when to work with which register we used a decoder for 'Write Register' and added it in an AND gate with the 'RegWrite' so that we can control if it should write or not. The registers won't work if we set RegWrite to 0. Then we added clock pulse, the same one to all the registers and used MUX to get the result from the registers. And it's select bit is the — 'Read Register 1', Rs. Then we added another MUX with the results to get 'Read Data 2' and the select bits of this MUX is the 'Read Register 2', Rt. And thus we get a complete Register File that has 16 registers of 16-bits.