Lab Manual

Department of Electrical and Computer Engineering
School of Engineering and Physical Sciences
North South University, Bashundhara, Dhaka-1229, Bangladesh

Experiment No: 05
Experiment Name: Design of a Register File

Introduction:

Although called a "file", a register file is not related to disk files. A register file is a small set of high-speed storage cells inside the CPU. There are special-purpose registers such as the IR and PC, and also general-purpose registers for storing operands of instructions such as add, sub, mul, etc. Since there are very few registers compared to memory cells, registers also require far fewer bits to specify which register to use. For example, the MIPS processor has 32 general-purpose registers, so it takes 5 bits to specify which one to use. MIPS is a load-store architecture, which means that only load and store instructions can access memory. All other instructions (add, sub, mul, div, and, or, etc.) must get their operands from registers and store their results in a register.

Experiment Details:

Assume, a 16 bit ISA with following fields. We need to design a register file for this ISA.

The formats of the instruction are as follows:

R-type

op (4 bit)	**rs (4 bit)**	**rt (4 bit)**	**rd (4 bit)**

I-type

op (4 bit)	**rs (4 bit)**	**rt (4 bit)**	**immediate (4 bit)**

J-type

op (4 bit)	**Target (12 bit)**

Objective:

We will have following objectives to fulfill:

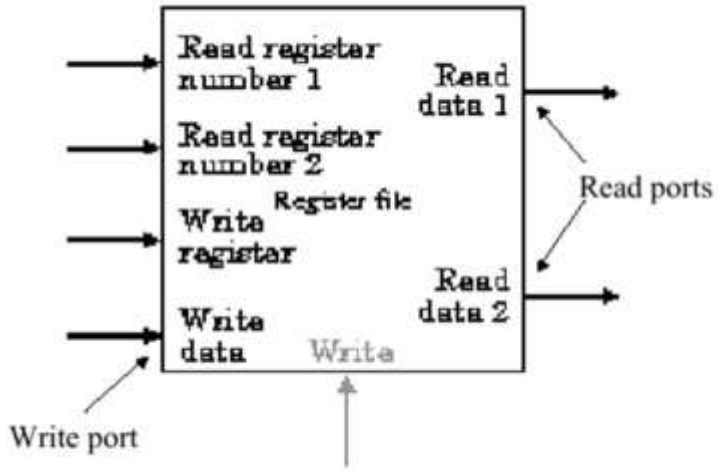
1) Design a register file that is 16 bit wide. Label properly the inputs/outputs/selections
2) Design the interfacing for reading data from any of those registers.
3) Design the interfacing for writing data to any of those registers. Make sure it has the write control signal

Equipment:

Logisim Tool

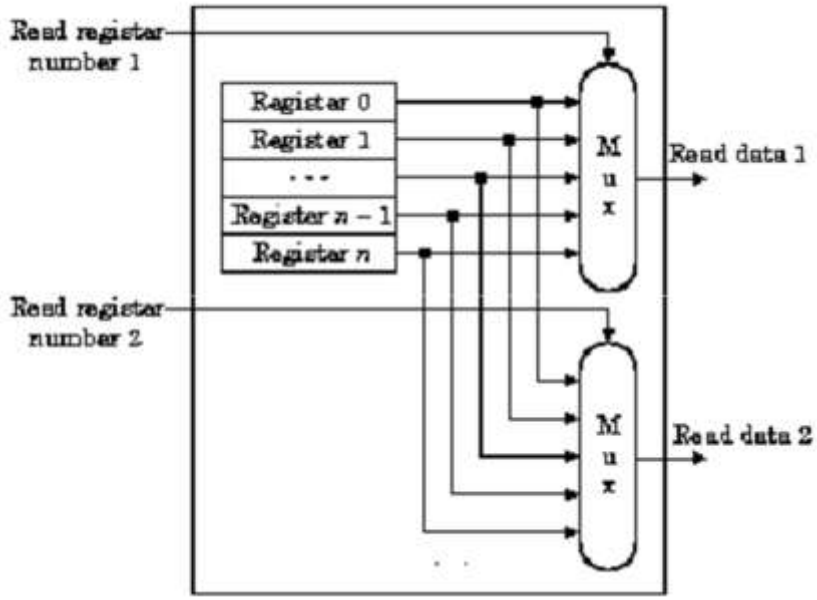
Diagram:

Following is the diagram of explaining all the necessary input/output peripherals.



Logic Diagram:

Following diagram shows the interfacing logic for reading the registers



CSE 332/ EEE 336/ ETE 336 Computer Organization and Architecture

Assignment:

1. **Implement Register File in Logisim. There will be total of 16 registers (RS=RT=RD=4, 2^4 = 16), and the data bits of each register will be 16. Submit logisim (.circ) file within the given time by your lab instructor (10 marks).**

2. **Prepare the lab report accordingly (10 marks). In the report, you have to include the *Screenshot* of the circuit as a Circuit Diagram. The screenshot must contain your name and ID along with the circuit.**

3. **HW – Designing a Register File in Logisim where there would be 32 registers and the data bits of those would also be 32 (10 marks). Submission deadline is one week from the day of experiment.**

****Plagiarism and late submission will not be acceptable.**