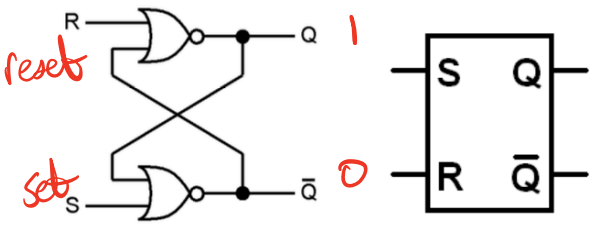
clock

S-R Latch asynchronous

The SR latch (Set-Reset) can be built from two 2-input NOR gates as shown in figure below.



S	R	Q	$\bar{Q}$
0	0	No change	No Change
0	1	0	1
1	0	1	0
1	1	0	0

memory

reset

set

Forbidden case

The circuit has two inputs (S and R), and two outputs (Q and $\bar{Q}$).

SR- latch excitation table

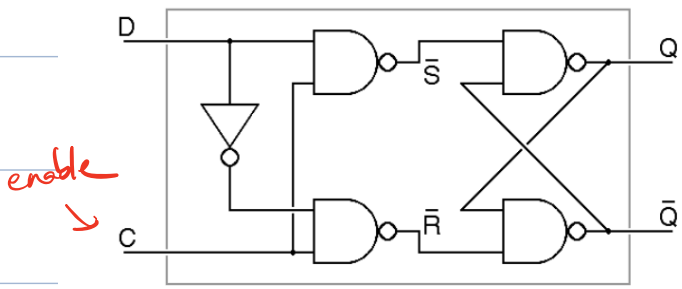
NOR

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$\longrightarrow Q^+ = S + QR'$

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

D Latch (based on NAND SR) synchronous



"enable"

C	D	Q	$\bar{Q}$
1	0	0	1
1	1	1	0
0	x	No change	No change

memory

force the inputs to be complements

D - Latch excitation table

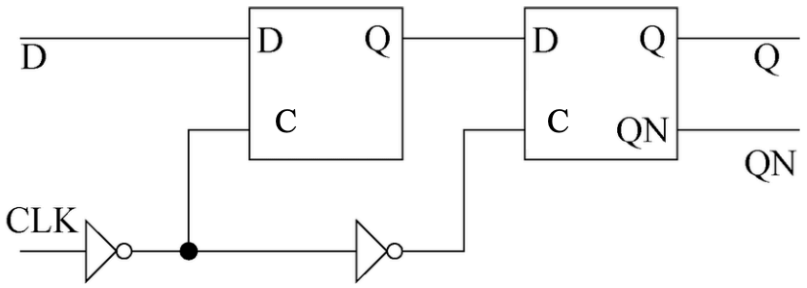
Q	Q^+	D (when C=1)
0	0	0
0	1	1
1	0	0
1	1	1

$\longrightarrow$ level-triggered

$Q^+ = D$

D flip-flop

Synchronous



D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

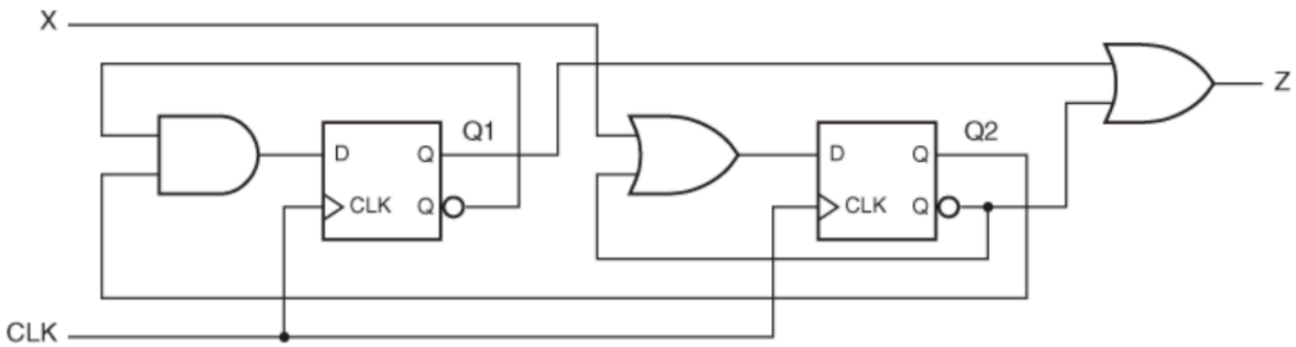
built from 2 D-Latches → edge triggered

D flip-flop excitation table

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

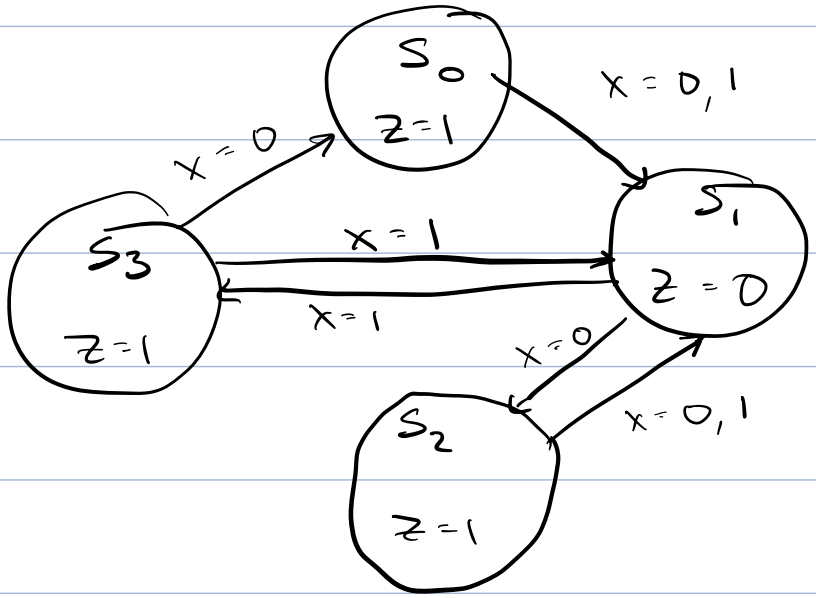
→ $Q^+ = D$

2.4



$D_2 = \overline{Q}_2 + X$ $\quad D_1 = Q_2 \cdot \overline{Q}_1$ $\quad Z = \overline{Q}_2 + Q_1$

X	Q_1	Q_2	Q_1^* (D_1)	Q_2^* (D_2)	Z
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	0	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	1	1



$S_0 = 00$

$S_1 = 01$

$S_2 = 10$

$S_3 = 11$