

# Czardas

## Liszt

8va

T  
A  
B

Po

2 5 3 2

1 0 2 3 0 0 R

1 1 3 1 0

3 3 5 5 5 R

8va

1. 3

5

T  
A  
B

Po

3 3 2 2 8

1 0 2 3 3 2 3 0 Po

3 3 2 0 2

8va

2. 3

9

T  
A  
B

Po

1 0 2 3 3 2 3 7 10 7 10 7

8va

13

Po

T  
A  
B

9 7 9 7 6 7 7 9 11 9 7 9 11 9 7 9 11 9 7

8va

17

T  
A  
B

7 5 4 5 8 10 12 10 8 10 12 10 8 10 12 10 8

8va

21

T  
A  
B

7 8 10 8 7 8 10 8 7 8 10 8 7 5 7 9 7 5 7 9 7

8va

24

5 7 9 7 5 7 5 7  $\overset{\text{SI}}{\rightarrow}$  5  $\overset{\text{SI}}{\rightarrow}$  4 5 7 10 7

8va

28

10 7 9 7 9 7 6 7 7 9 11 9 7 9 11 9

Po

8va

32

7 9 11 9 7 7 5 4 5 8 10 12 10 8 10 12 10

36

8va

T  
A  
B

40

8va

T  
A  
B

46

8va

T  
A  
B

The diagram illustrates a 52-bit bus architecture. At the top, a horizontal line represents the 52-bit bus, with a '52' label at the left end. Below this line, several control signals are indicated: '10', '12', '10-12-10', '10-12-10', '8', and '7'. Above the bus line, two pairs of signals are labeled 'H' and 'Po', each with a curved line connecting them. Below the bus line, three horizontal lines represent registers: 'T', 'A', and 'B'. The 'A' register has a '11' label. The 'B' register has a '11' label. Below the registers, a horizontal line represents the data path, with a '11' label. At the bottom, a horizontal line represents the output, with a '11' label. The diagram shows the flow of data from the registers through the bus to the output, with various control signals and labels indicating the architecture.

[illegible][illegible][illegible]

68

8va

T [14] -7 12 10 10 11 10 8 8 7 7 5 5 6 5 0

A

B

74

8va

T 5 6 5 0 7 10 7 9 8 9 10 7 10 7 9 8 9 10 7

A

B

X3

78

8va

T 10 12 11 12 10 7 0 0

A

B