Experimental extraction of relevant MOSFET parameters

We require for drain-to-source resistance calculations and for MOSFET calculations in general an accurate characterisation of MOSFET parameters.

Theoretical determination and experimental approximation of parameters

At a purely theoretical level I_D will be a function of two variables: V_{GS} and V_{DS}. We take for example R_{DS} in the Triode Region.

To determine its formula and value we need to take the partial derivative of I_D with respect to V_{DS} and voila. But there's a problem, we can't take the derivative when measuring currents and voltages with a multimeter.

So instead of taking the derivative we will be calculating the slope of the curve, as we assume the IV characteristic of the FET to be mostly linear. After all, should we take two point infinitesimally close to each other, the resulting slope would have the same value as the derivative.

Note that for the parameter extraction we'll be doing, the selected transistor will be an IRF830.

Measuring VT

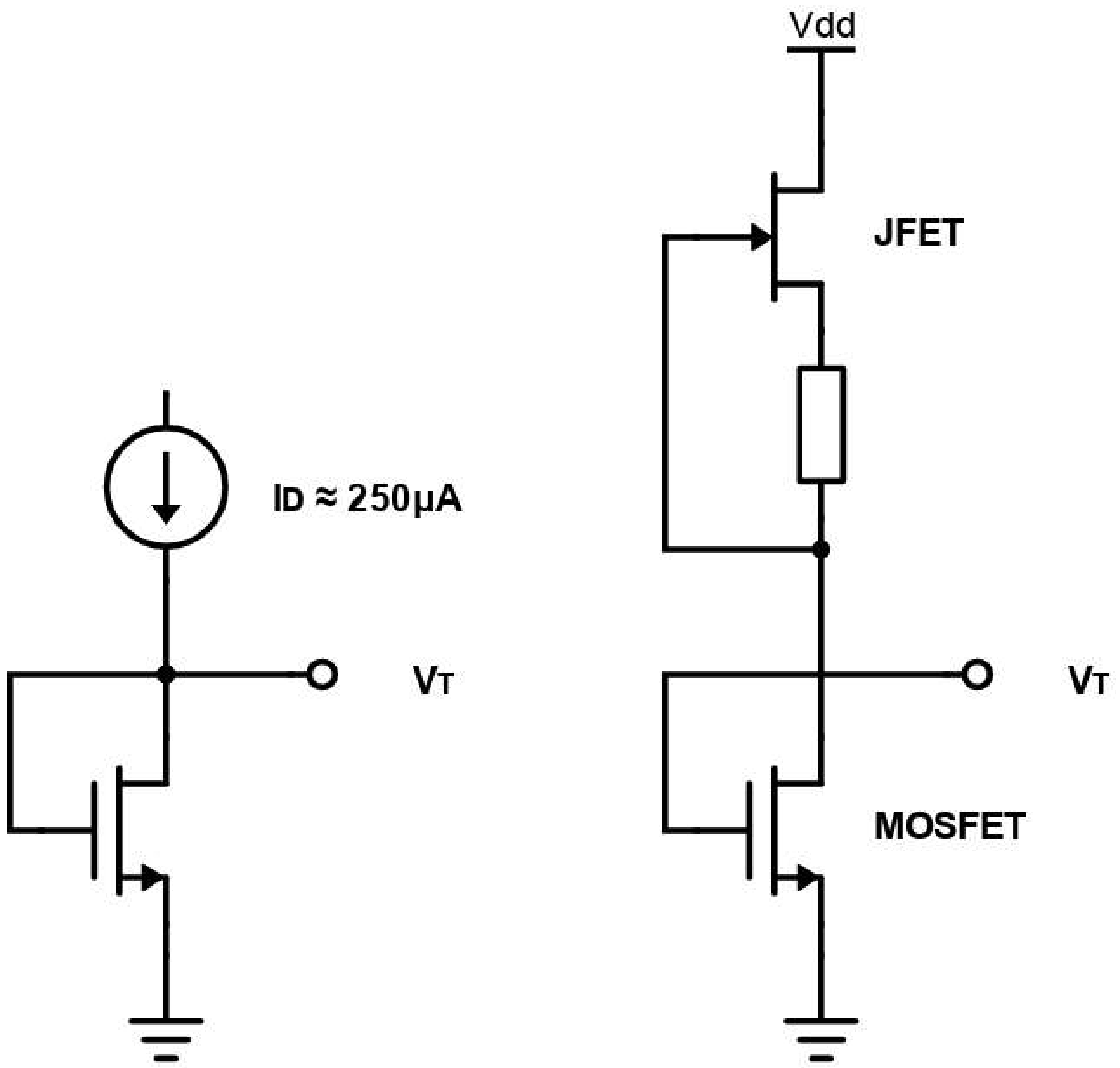
Threshold voltage can be defined in many ways, it all depends on what "threshold" current we decide to set as a benchmark.

I attempted to determine the value of V_T with the help of several distinct testing methods:

- Constant Current Method: Biasing the FET with a constant current I_D = 250 μA and measuring V_{GS}
- Linear Extrapolation in Saturation Region: Diode-connected FET is biased by a variable voltage source and the threshold voltage is subsequently graphically determined
- Extraction from characteristic FET equation

The Constant Current Method

This method works by setting a current source to output a constant, voltage independent drain current I_D = 250 μA into the Drain, which is shorted to the Gate of the device.



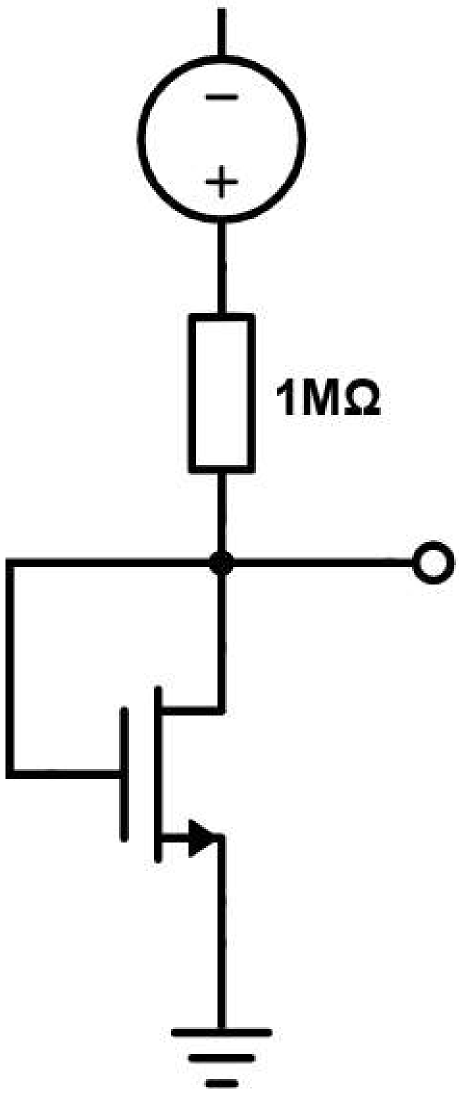
CCS implementation

The CCS was built from a JFET and a resistor, a combination also called "constant current diode", as it can be seen in the figure from above. The output current of the source is dictated by the resistance, which for a desired current I_D has this formula: $R_S = \frac{V_{GS(off)} \cdot \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)}{I_D}$. On the bench the fixed resistor was supplanted by a potentiometer to avoid having to extract the values of I_{DSS} and $V_{GS(off)}$ for the specific transistor in use.

In our specific example the potentiometer was set to 2.922 $K\Omega$ and I_D reached 255.6 μA, giving us the value of the threshold voltage as V_T = 2.97V.

Notes on alternative arrangements for a CCS

An active device is not always required for this method, as a quicker, bench-friendlier method is to just measure V_{GS} when the FET is supplied through a 0.1/1/10 $M\Omega$ resistor and the current is closer to another industry-standard current benchmark: $I_{test} = 100nA \cdot \frac{W}{L}$



Simpler bench-friendly test method

Linear Extrapolation in Saturation Region

This method necessitates the use of a diode-connected MOSFET and a variable supply voltage. Whilst performing the measurement and calculations, we must acknowledge that above the threshold voltage the FET is saturated because: $V_{GS} = V_{DS}$, $V_{GS} - V_T = V_{DS} - V_T < V_{DS}$ While varying the gate voltage we monitor the increase in current. After we gather all the data we graph I_D vs V_{GS}.

We can observe two distinct regions in the graph, above the threshold and below threshold (subthreshold region). In the above-threshold region the characteristic equation for the FET is valid, whilst in the subthreshold region the current ceases to obey the usual characteristic equations.

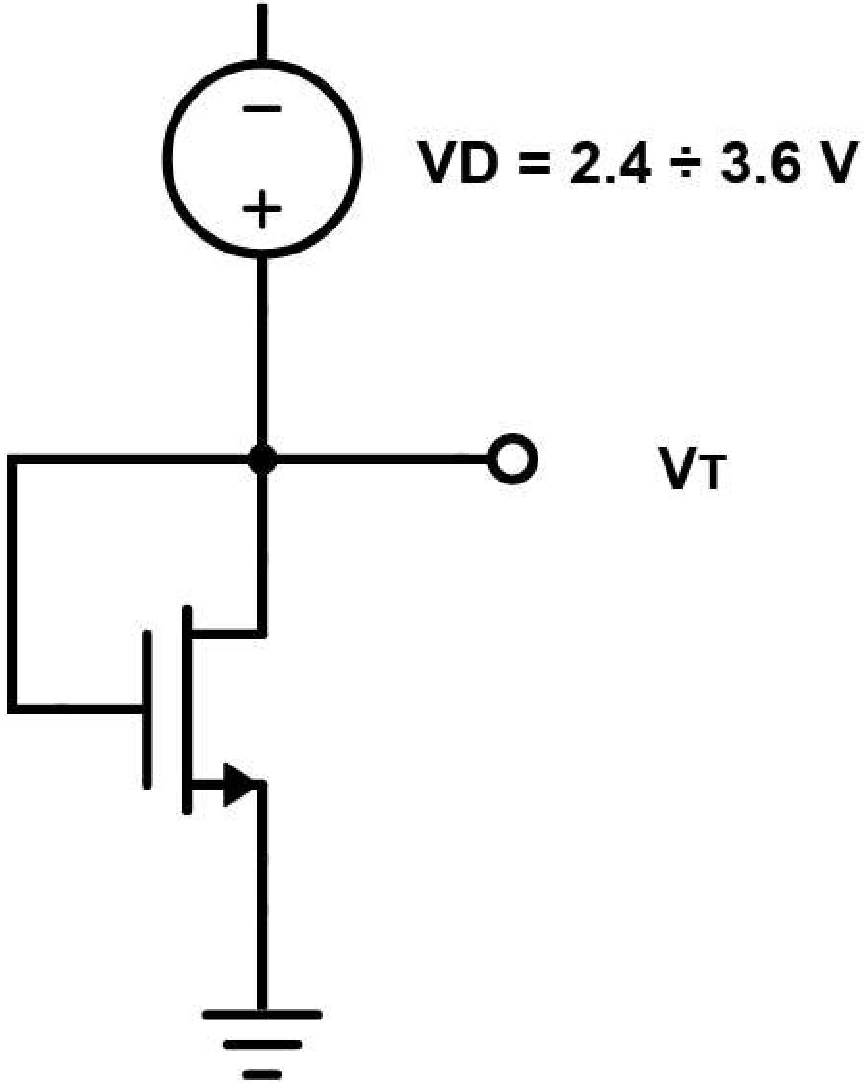
We come up with another proper formula for the variation of I_D in terms of V_{GS} and V_{DS}:

$$I_D = I_S \cdot e^{\frac{V_{GS}}{\zeta U_t}} \cdot \left(1 - e^{-\frac{V_{DS}}{\zeta U_t}}\right)$$

For $V_{DS} > 4 \cdot U_t$ the formula simplifies to: $I_D = I_S \cdot e^{\frac{V_{GS}}{\zeta U_t}}$, where U_t is the thermal voltage and ζ is the non-ideality factor. In our test circuit V_{DS} and V_{GS} will be equal.

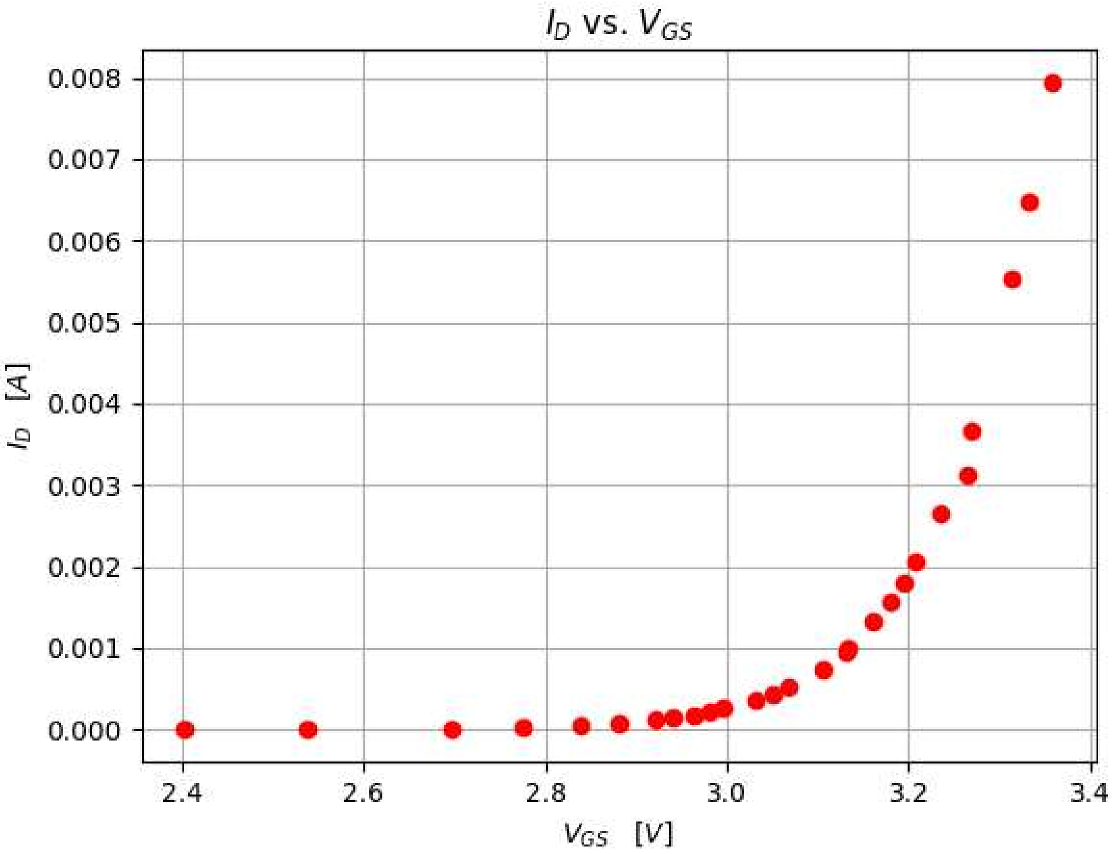
Above V_{GS} = V_T, $\sqrt{I_D}$ will be linear and equal to $K \cdot (V_{GS} - V_T)$. We take two points in the linear region of the graph and define the line passing through, where V_T is to be its X-intercept.

The test circuit looks like this:



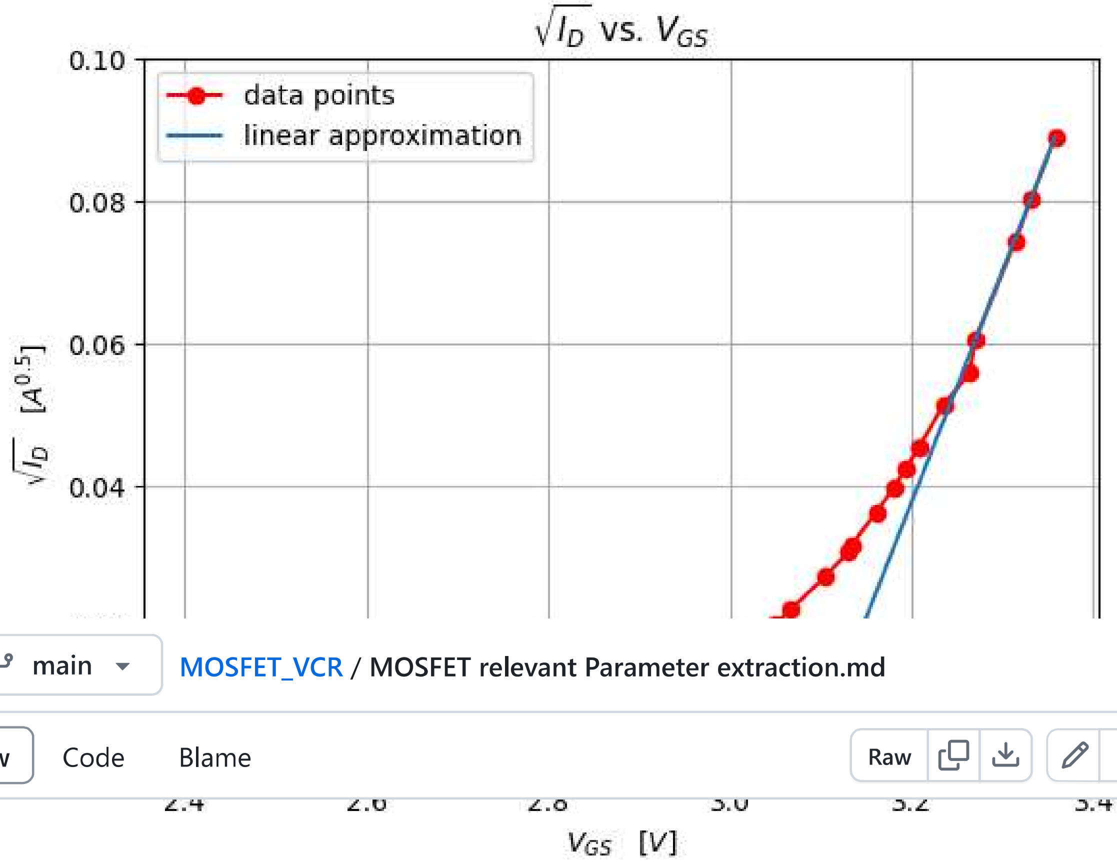
Linear Extrapolation in Saturation Region test circuit implementation

The gathered data points are represented below:



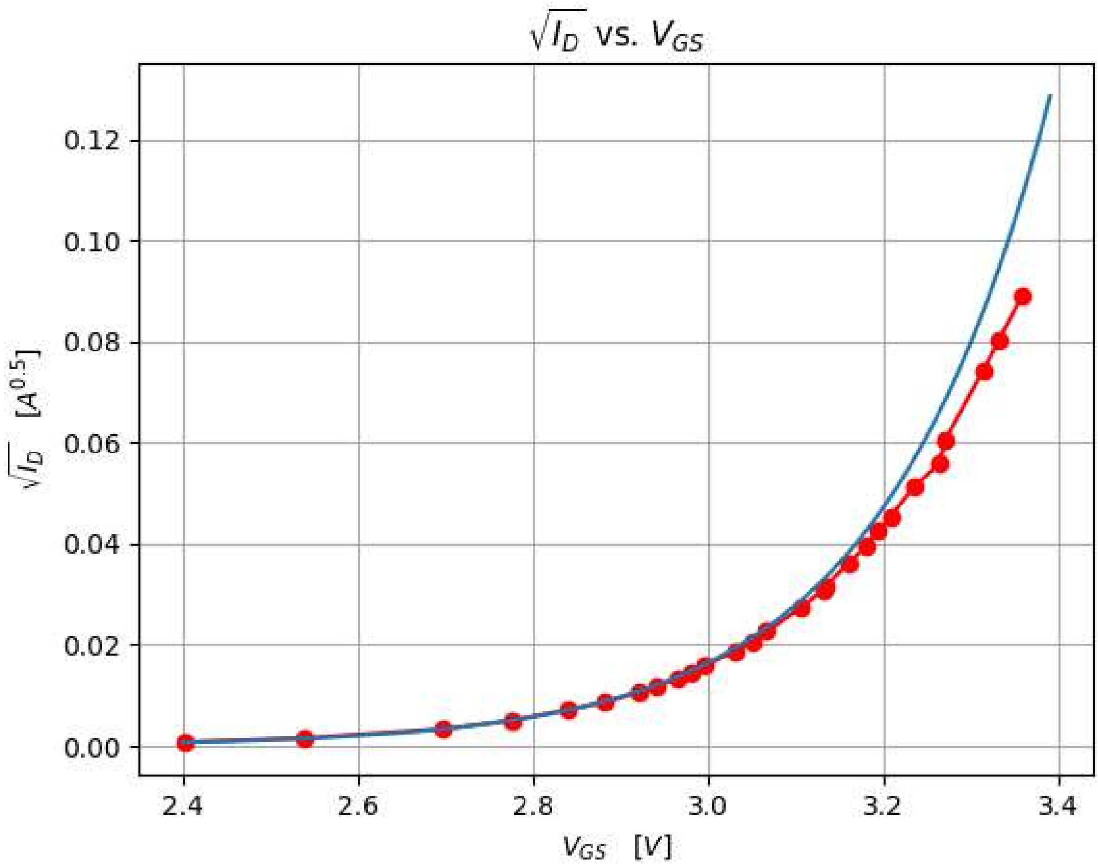
Experimentally obtained data points

And this is how the threshold voltage is determined graphically:



Linear approximation and graphical threshold voltage determination

And here we have an approximation for the characteristic equation in the subthreshold region:



Subthreshold Region and characteristic equation

The parameters needed for plotting the IV characteristic can be extracted with the help of the formulas presented below:

$$\begin{cases} I_{D1} = I_S \cdot e^{\frac{V_{GS1}}{\zeta U_t}} \\ \\ I_{D2} = I_S \cdot e^{\frac{V_{GS2}}{\zeta U_t}} \end{cases}$$

$$\zeta = \frac{V_{GS1} - V_{GS2}}{U_t \cdot ln\left(\frac{I_{D1}}{I_{D2}}\right)}$$

$$I_S = \frac{I_D}{e^{\frac{V_{GS}}{\zeta U_t}}}$$

Extraction from characteristic FET equation

We take two bias points and with the help of characteristic equation we find an expression of the form $V_T = f\left(V_{GS1}, V_{GS2}, I_{D1}, I_{D2}\right)$. One important contstraint that we must impose is that the value of the threshold voltage is smaller than both V_{GS}

$$\frac{I_{D1}}{I_{D2}} = \frac{K(V_{GS1} - V_T)^2}{K(V_{GS2} - V_T)^2}$$

$$I_{D1}{V_{GS}}^2 - 2V_{GS2}V_T I_{D1} + {V_T}^2 I_{D1} = I_{D2}{V_{GS1}}^2 - 2V_{GS1}V_T I_{D2} + {V_T}^2 I_{D2}$$

which resolves to this:

$${V_T}^2(I_{D2} - I_{D1}) + V_T(2V_{GS2}I_{D1} - 2V_{GS1}I_{D2}) + I_{D2}{V_{GS1}}^2 - I_{D1}{V_{VGS2}}^2 = 0$$

The equation has the following solutions:

$$V_T = \frac{-2(V_{GS2}I_{D1} - V_{GS1}I_{D2})}{2(I_{D2} - I_{D1})} \pm \frac{\sqrt{(2V_{GS2}I_{D1} - 2V_{GS1}I_{D2})^2 - 4(V_{GS2}^2 I_{D1} - V_{GS1}^2 I_{D2})(I_{D2} - I_{D1})}}{2(I_{D2} - I_{D1})}$$

After we numerically determine the solutions, we check that V_T is to the left of both V_{GS} values used.

Determination of Channel Length Modulation Factor

To find the value of λ we pick two bias points inside the saturation region and create a system of two equations and one unknown, the CLM Factor. We keep V_{GS} constant and sweep V_{DS} to find the two suitable measurement points.

$$\begin{cases} I_{D1} = K \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS1}) \\ I_{D2} = K \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS2}) \end{cases}$$

$$\frac{I_{D1}}{I_{D2}} = \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}}$$

And so the formula for λ is $\lambda = \frac{I_{D1} - I_{D2}}{I_{D2}V_{DS1} - I_{D1}V_{DS2}}$.

The CLM Factor can also be derived from the formula for the static resistance of the FET in the saturation region. R_{DS} can be approximated as $\frac{1}{\lambda I_D}$, the FET's equivalent resistance can be graphically determined from the IV characteristic by taking the slope of the graph. So λ will be equal to $\frac{1}{R_{DS}I_D}$.

Determination of Technology Constant "K"

For a quick and dirty solution, we just bias the FET into the saturation region and input into the characteristic equation the now known values of V_T and λ, then K is $\frac{I_D}{(V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})}$.

Conclusions

- There are a **lot** of testing methods for V_T
- Linear interpolation and log-fitting are better options for parameter extraction, but require more time and resources
- Rough values are better than no values
- Better equipment, better results

Sources and Useful Resources

- https://www.scirp.org/journal/paperinformation.aspx?paperid=72393
- http://web02.gonzaga.edu/faculty/talarico/EE303/HO/squarelawIssues.pdf
- https://2n3904blog.com/sub-threshold-conduction-of-a-power-mosfet/
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