Comprehensive-COA-Question-Bank

Qno	Question	Answer
1	What is not similar between single bus and multiple bus structures? a) Cost b) Performance c) Transfer d) All of the above	D
2	The circuit used to store one bit of data is known as? A) Encoder B) Flip flop C) Or gate D) Decoder	B
3	In assembly language programming,minimum number of operands required for an instruction is/are: A)Zero B)One C)Two D)Both (B) and (C)	A
4	The technique where the controller is given complete access to main memory is __ a) Cycle stealing b) Memory stealing c) Memory Con d) Burst mode	D
5	The addressing mode used in an instruction of the form ADD X Y is: A) Absolute B) Index C) Indirect D) None of these	B
6	The program written and before being compiled or assembled is called A. Start Program B. Intermediate program	C

Qno	Question	Answer
	C. Source Program D. Natural Program	
7	When CPU is executing a Program that is part of the OS,it is said to be in: A.Interrupt mode B.System mode C.Half mode D.Simplex mode	B
8	The interrupt servicing mechanism in which the requesting device identifies itself to the processor to be serviced is a) Polling b) Vectored interrupts c) Interrupt nesting d) Simultaneous requesting	B
9	Floating point representation is used to store a)boolean values b)whole numbers. c)real integers d)integers	C
10	The primary function of the BUS is _____ a) To connect the various devices to the cpu b) To provide a path for communication between the processor and other devices c) To facilitate data transfer between various devices d) All of the mentioned	A
11	The following are some events that occur after a device controller issues an interrupt while process L is under execution. (P) The processor pushes the process status of L onto the control stack. (Q)The processor finishes the execution of the current instruction. (R) The processor executes the interrupt service routine. (S) The processor pops the process status of L from the control stack. (T) The processor loads the new PC value based on the interrupt.	A

Qno	Question	Answer
	Which one of the following is the correct order in which the events above occur? (A) QPTRS (B) PTRSQ (C) TRPQS (D) QTPRS	
12	Cache memory acts between: A)CPU & RAM B) RAM & ROM C) CPU & HDD D) NONE	A
13	The _____ is the computational center of the CPU. A. Registers B. ALU C. Flip-Flop D. Multiplexer	B
14	In DMA transfers, the required signals and addresses are given by the a) Processor b) Device Drivers c) DMA Controllers d) The program itself	C) DMA Controllers: acts as a processor for DMA transfers and overlooks the entire process
15	Consider the control function x T1 : A ← B Here, transfer occurs when a) x=0 and T1=1 b) x=1 and T1=1 c) x=1 and T1=0 d) Both a and c	A
16	Which format is used to store data? A. BCH B. BCD C. Binary D. Decimal	B
17	The address mapping is done, when the program is initially loaded is called: A) Dynamic Relocation B) Relocation C) Dynamic as well as Static Relocation D) Static Relocation	D

Qno	Question	Answer
18	The key feature of the RAMBUS tech is _____ a) Greater memory utilisation b) Efficiency c) Speed of transfer d) None of the mentioned	C
19	_____ bus structure allow two or more transfer at a time a) Single bus structure b) Data bus structure c) Address bus structure d) Multiple bus structure	D
20	A device/circuit that goes through a predefined sequence of states upon application of input pulses is called….. A)register B)flip flop C)transistor D)counter	D
21	The condition flag Z is set to 1 to indicate _____ a) The operation has resulted in an error b) The operation requires an interrupt call c) The result is zero d) There is no empty register available	C
22	In a program using subroutine call instruction it is necessary to (a)initialize program counter (b)clear accumulator (c)reset micro processor (d)clear instruction register	D
23	Which of the following is used to choose between incrementing the PC or performing ALU operations? A. Conditional Units B. Multiplexer C. Control Codes D. Memory bus	B
24	A Stack-organised Computer uses instruction of (A) Indirect addressing (B) Two-addressing	C

Qno	Question	Answer
	(C) Zero addressing (D) Index addressing	
25	The addressing mode where you directly specify the operand value is A) Immediate B)Direct C)Definite D)Relative	A
26	_____ register keeps tracks of the instructions stored in program stored in memory. (A) AR (Address Register) (B) XR (Index Register) (C) PC (Program Counter) (D) AC (Accumulator)	C
27	The average time required to reach a storage location in memory and obtain it's contents is called a) Seek time b) Turnaround time c) Access time d) Transfer time	C
28	What characteristics of RAM memory makes it not suitable for permanent storage? a) Too slow b) Unreliable c) It is volatile d) Too bulky	C
29	Micro program is A)the name of a source program in micro computers B)set of micro instructions that defines the individual operations in response to a machine-language instruction C)a primitive form of macros used in assembly language programming D)a very small segment of machine code	B

Qno	Question	Answer
30	Memories that consists of circuits capable of retaining their state as long as power is appkied are known as a)Dynamic b)Static c)SRAM d)DRAM	B
31	When a subroutine is called, the address of the instruction following the CALL instructions stored in the? A) Stack pointer B) accumulator C) program counter D) stack	D
32	The computer architecture aimed at reducing the time of execution of instructions is _____ a) CISC b) RISC c) ISA d) ANNA	B
33	Which of the following are not a machine instructions a) MOV b) ORG c) END d) B and C	D
34	MFC stands for _____ a) Memory Format Caches b) Memory Function Complete c) Memory Find Command d) Mass Format Command	B
35	The decoded instruction is stored in _____ a) IR b) PC c) Registers d) MDR	A
36	The main memory location which contains the effective address of the operand is	pointer
37	Which memory unit has the lowest access time? a) cache b) registers c) magnetic disk d) main memory	B

Qno	Question	Answer
38	Bandwidth of system RAM is approximately a)19200MB/s b)9200MB/s c)192000MB/s d)920MB/s	A
39	Cache memory works on the principle of _____. A)Locality of data B) Locality of memory C)Locality of reference D) Locality of reference & memory	C
40	The circuit used to store 1 bit of data is known as A) encoder B) OR gate C) flip flop D) decoder	C
41	The location to return to, from the subroutine is stored in _____ a) TLB b) PC c) MAR d) Link registers	D
42	The instruction, Add #45,R1 does _____ a) Adds the value of 45 to the address of R1 and stores 45 in that address b) Adds 45 to the value of R1 and stores it in R1 c) Finds the memory location 45 and adds that content to that of R1 d) None of the mentioned	B
43	An address in main memory is called A. Physical address B. Logical address C. Memory address D. Word address	A
44	In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____ a) EA = 5+R1 b) EA = R1	D

Qno	Question	Answer
	c) EA = [R1] d) EA = 5+[R1]	
45	Which of the following is the important characteristics of computers? A.Speed B.Accuracy C.Storage D.All of the above	D
46	Which bus is used to connect the monitor to the CPU? A. Single Bus B. SCSI Bus C. Multiple Bus D. Rambus	B
47	The addresing modes which uses the PC instead of a general purpose register is (A) Indexed With offset (B) Relative (C) Direct (D) Both indexed with offset and direct	B
48	Which of the following is true about Computer Architecture? A. It acts as the interface between hardware and software. B. Computer Architecture tells us how exactly all the units in the system are arranged and interconnected. C. Computer Architecture is concerned with the structure and behaviour of a computer system as seen by the user. D. It involves Physical Components	A
49	The I/O devices are connected to the CPU via _____ . A. SDRAM's B. Control circuits C. Signals D. BUS	D
50	The input devices use _____ to store the data received A. Primary Memory B. Secondary Memory	C

Qno	Question	Answer
	C. Buffer D. External Memory	
51	In the case of, Zero-address instruction method the operands are stored in _____ a) Registers b) Accumulators c) Push down stack d) Cache	C
52	The amount of ROM needed to implement a 4-bit multiplier is	2 Kbits
53	Match the following (a) Immediate address mode (1) Local variables (b) Direct address mode (2) Relocatable programs (c) Indirect address mode (3) Pointer (d) Index addressing mode (4) Locality of reference (e) Base address mode (5) Arrays (f) Relative address mode (6) Constant Operands	Immediate Address Model -> Constant Operand Direct Address mode -> Local Variables Indirect address mode -> Pointer Index addressing mode -> Arrays Base address mode -> Relocatable programs Relative address mode -> Locality of reference
54	Register renaming is done in pipelined processors	to handle certain kinds of hazards
55	Memory interleaving is done to	Reduce memory access time
56	In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer) can be accessed is	after effective address calculation has completed

Qno	Question	Answer
57	The correct matching for the following pairs is (A) DMA I/O (1) High speed RAM (B) Cache (2) Disk (C) Interrupt I/O (3) Printer (D) Condition Code Register (4) ALU	DMA I/O -> Disk Cache -> High speed RAM Interrupt I/O -> Printer Condition Code Register -> ALU
58	The technique whereby the DMA controller steals the access cycles of the processor to operate is called	Cycle Stealing
59	For the daisy chain scheme of connecting I/O devices, which of the following statement is true?	It gives non-uniform priority to various devices
60	A machine with N different opcodes can contain how many different sequences of micro-operations	N
61	A cache has a 64 KB capacity, 128 -byte lines (blocks), and is 4 -way set associative. The system containing the cache uses 32 -bit addresses. How many lines (blocks) and sets does the cache have?	128
62	A processor has an instruction cache with hit rate of 90% and access time of 1 ns, if cache miss penalty is 20 ns, what is the average memory access time?	2.2ns
63	A computer system uses a direct mapped cache with a cachesize of 8 KB and a block size of 32 bytes. How many bits are needed for the cache index?	7 Bits
64	Which emory type is the closest to the CPU and provides fast access to frequently used data	Cache memory
65	Which addressing mode uses a base register plus an offset to calculate memory address?	Indexed addressing mode
66	A computer system uses a 32 bit virtual address and a 4KB page size. How many entries are there in the page table?	1024 entries
67	In a pipelined processor, which hazard occurs when the current instruction depends on the result of previous instruction that has not yet completed	Data hazard
68	Which cache mapping technique provides the fastest access time but has limited capacity?	Fully associative mapping
69	Which technique is used to reduce the effect of memory latency in a pipelined processor?	Out of order execution

Qno	Question	Answer
70	Which technique is used to minimize the impact of control hazards in a pipelined processor	Branch prediction
71	Example of immediate addressing mode is	SUB A, #10
72	The main virtue for using single bus structure is	Cost effective connectivity and ease of attaching peripheral devices.
73	Memory buffer register(MBR) is connected to	System bus
74	The basic component of arthmetic circuit is	Full adder
75	When we use auto increment or auto decrements, which of the following is true 1) In both, the address is used to retrieve the operand and then the address gets altered 2) In auto increment, the operand is retrieved first and then the address altered 3) Both of them can be used on general purppose registers as well as memory locations	Option 2 is true: In auto increment, the operand is retrieved first, and then the address is altered.
76	When we perform subtraction on -7 and -5 the answer in 2's compliment form is a) 11110 b) 1110 c) 1010 d) 0010	A
77	The instruction -> Add LOCA, R0 does ___ a) Adds tge value of LOCA to R0 and stores in temp register b) Adds the value of R0 to the address of LOCA c) Adds the values of both LOCA and R0 and stores it in R0 d) Adds the values of LOCA witha value in accumulator and stores it in R0	C) Adds the values of both LOCA and R0 and stores it in R0
78	Suppose after analyzing a new cache design you discover that the cache has far too many conflict misses, and this needs to be resolved. You know that you must increase associativity in order to decrease the number of cache misses. What are the implications of increasing associativity a) Slower cache access time b) Increase index bits c) Increase block size d) All of these	D

Qno	Question	Answer
79	Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is ___ a) Horizontal organization b) Vertical organization c) Diagonal organization d) None of the mentioned	B
80	DMA interface unit eliminates the need to use CPU registers to transfer data from a) MAR to MBR b) MBR to MAR c) I/O units to memory d) Memory to I/O units	C