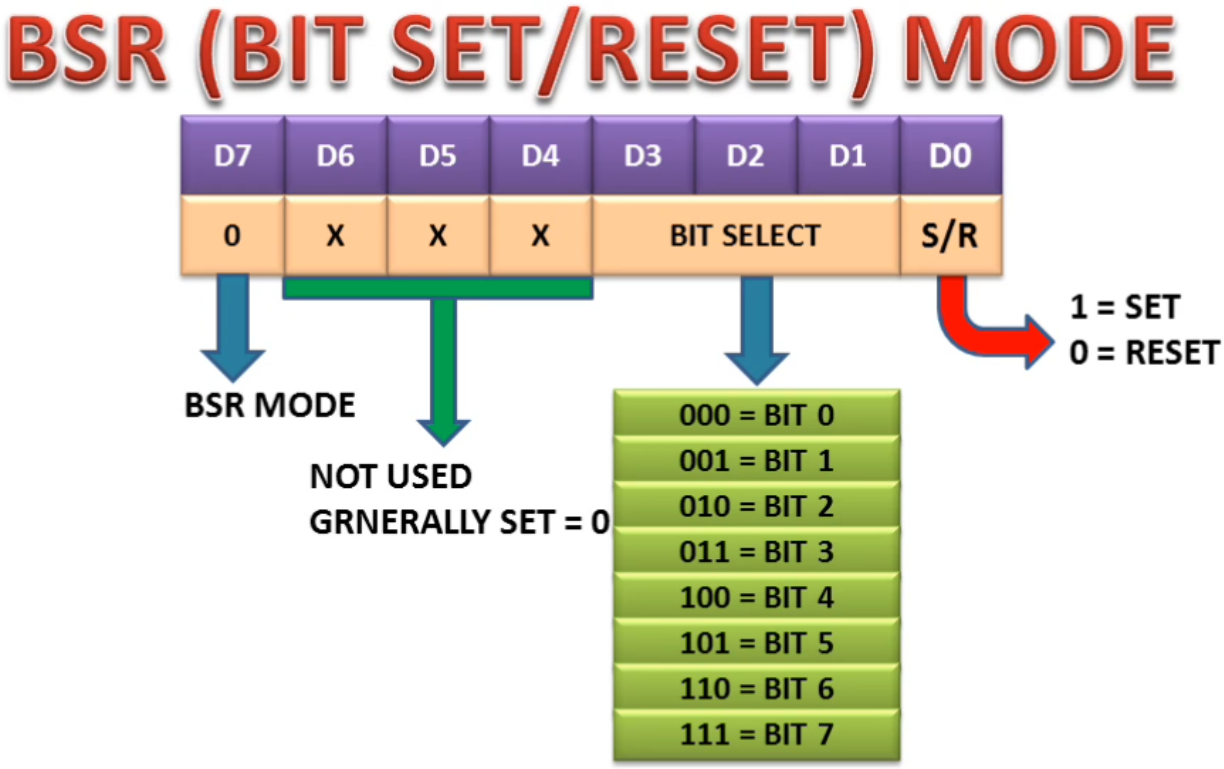
Microprocessors Module 4 Questions

Part A

1. Interpret the mode and configurations of 8255 after its control word register is loaded with 86H.

- First we need to get the Binary value of 86H
  - (86)H = (0101 0110)B
- The most significant bit D7 is 0, this implies 8255 operates in BSR Mode
  - This mode is used to set or reset the bits of port C, When D7 = 0
- Now we just need to substitute each of the binary values in the below figure



- It would be assigned like
  - D7 D6 D5 D4 D3 D2 D1 D0
  - 0 1 0 1 0 1 1 0
- Here D3D2D1 = 011 = 4
  - so PC4 is to be set or reset
- We can figure out whether its to be set or reset by looking at the D0 value
  - Here D0 = 0

- Which means PC4 is to be reset to 0

2. Explain the features of 8257 DMA Controller

The features of 8257 DMA Controller are

- It has four channels which can be used over four I/O devices.
- Each channel can transfer data up to 64kb
- Each channel can be programmed independently.
- It operates in 2 modes, i.e., Master mode and Slave mode.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It requires a single-phase clock.

3. Write the function of the following control signals in 8255. RD, WR, Ao, Ai, RESET, CS

- CS
  - Chip Select is an active low pin which selects the chip and enables communication between 8255 and CPU.
- WR
  - WR (write) is an active low pin that enables the microprocessor to write into a selected I/O port or control register.
- RD
  - RD (Read) is an active low pint that enables the microprocessor to read data from the selected I/O port of 8255
- A0 and A1
  - These pins work in conjunction with CS to select the port as shown

CS	A_1	A_0	Result
0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	Control Register
1	X	X	No Selection

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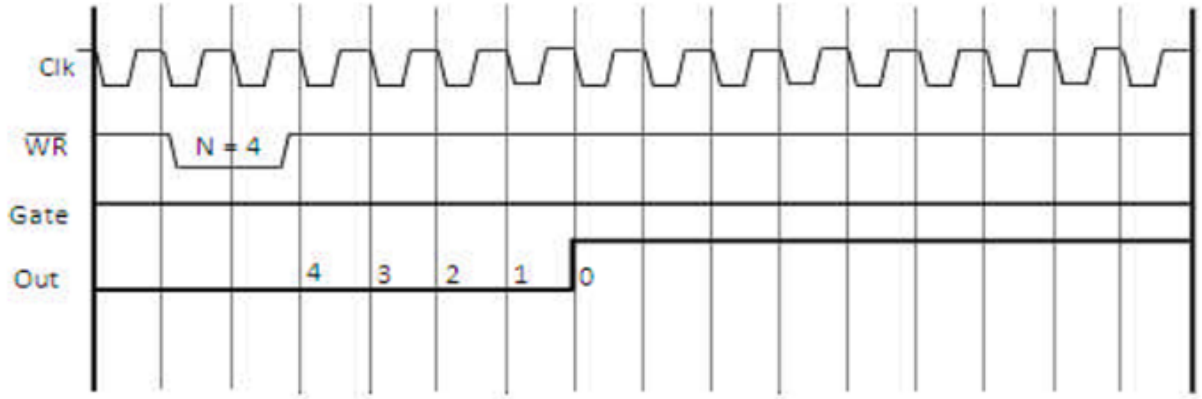
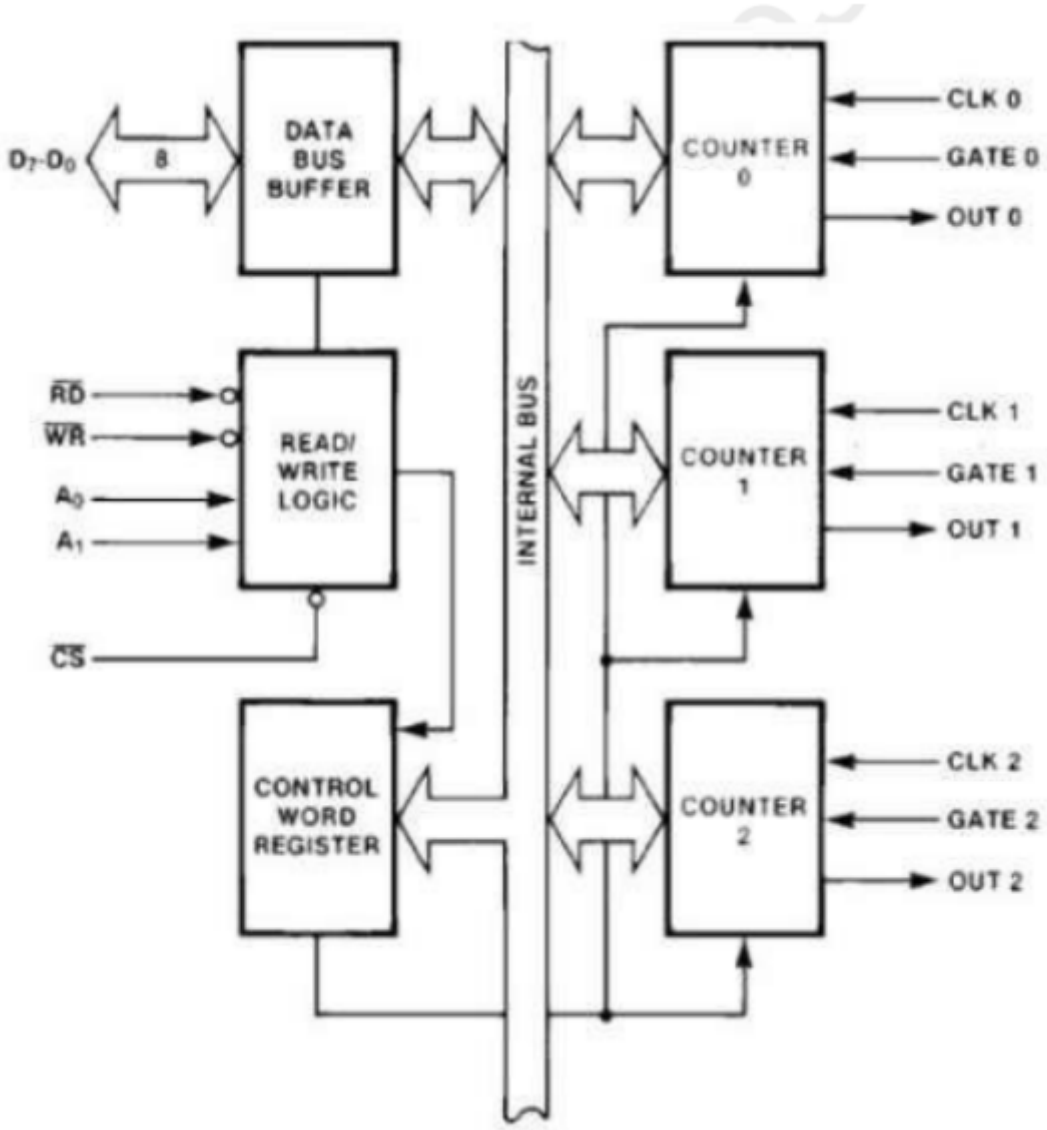
4. Draw and explain the operational waveform of 8254 in MODE 0 operation.



- Mode 0 is used for event counting
  - Event counting refers to the process of counting events or occurrences over time using a counter or a counting device
- This mode is selected if (D3 D2 D1) of the control word register is (0 0 0)
- When this mode is selected, the OUT pin is initially low.
- The GATE pin is made high, so counting is enabled.
- The count value is loaded (We are writing N=4), and the counting starts after the next high to low transition of the clock pulse.
- During counting, the OUT pin remains low.
- On terminal count (0), the OUT pin goes high, and it remains high until a new count is written into the counter
- During counting, if the gate goes low then counting is terminated and the current count is latched till the GATE goes high again
  - "latched" refers to the process of capturing or storing the current value of the counter at a specific moment.

Part B

1. Explain the 8254 programmable timer and its operation modes with a neat block diagram.

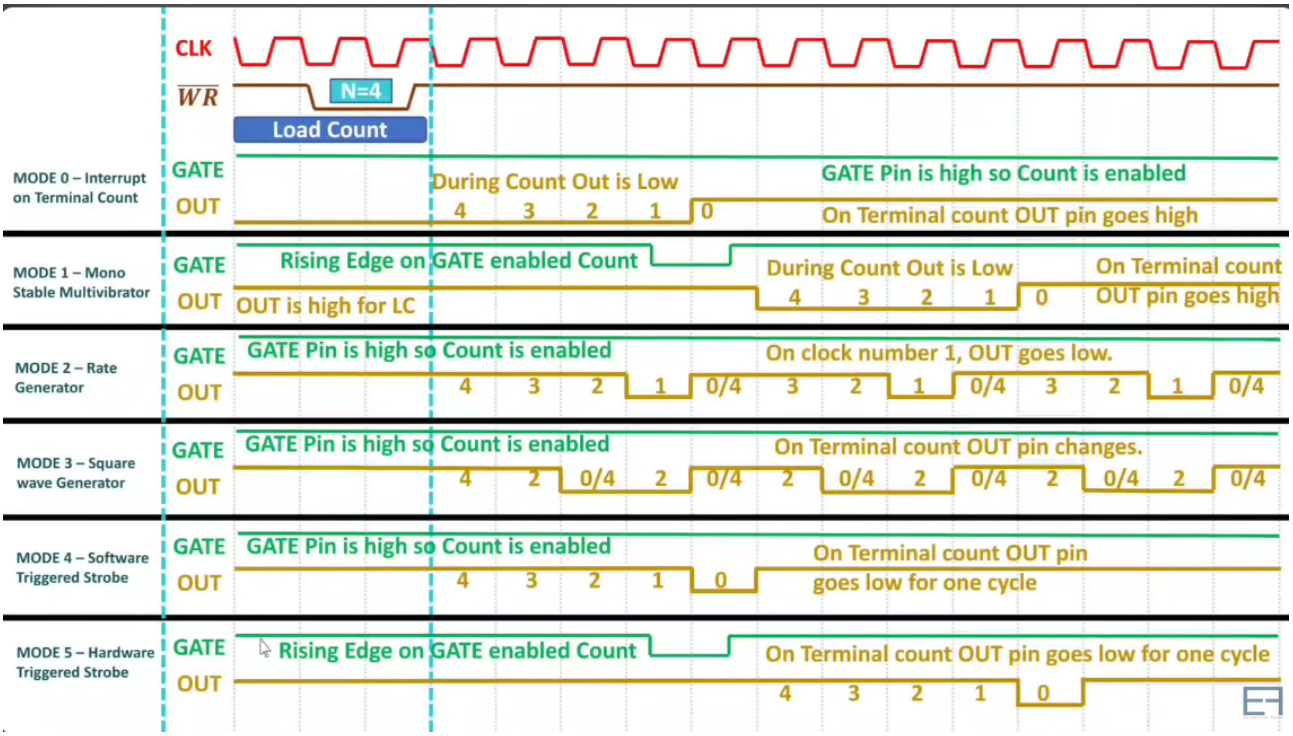


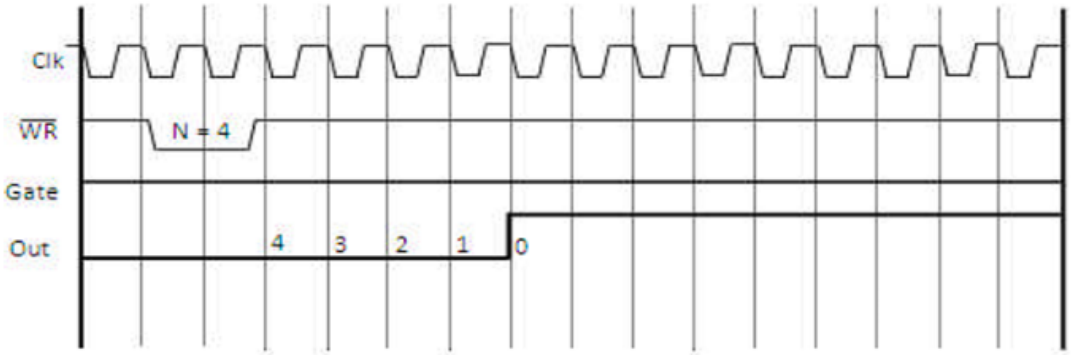
- The 8254 is a Programmable Interval Timer designed for microprocessors to perform timing and counting functions using three 16-bit registers.
- Each Counter has 3 pins: Clock, Gate and OUT.
- It has 3 independent 16-bit down counters.
- These 2 counters can be programmed for either binary or BCD Count.

To operate a counter

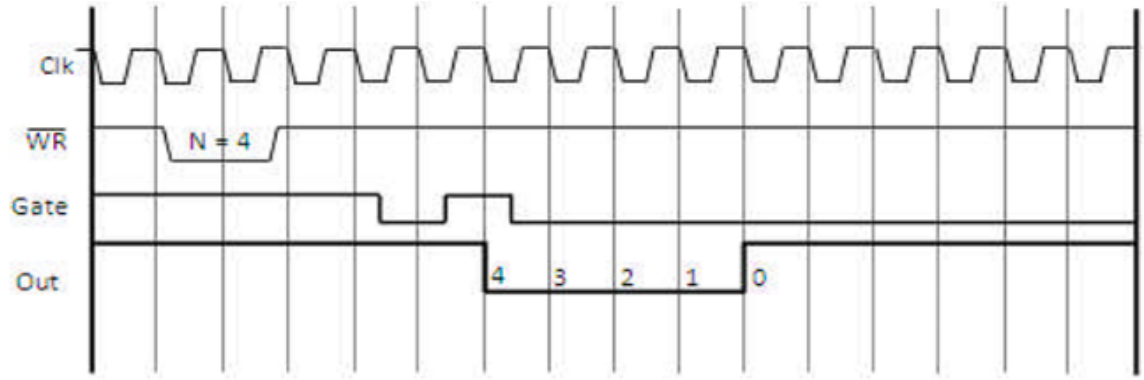
- A 16-bit count is loaded into its register.
- Counting starts after the next high to low transition of the clock pulse.
- Counter decrements for every clock pulse until it reaches Terminal Count (0).
- Once TC is reached, OUT signal is generated to interrupt the CPU.

Operation modes

- 8254 can be operated in 6 different modes
- 

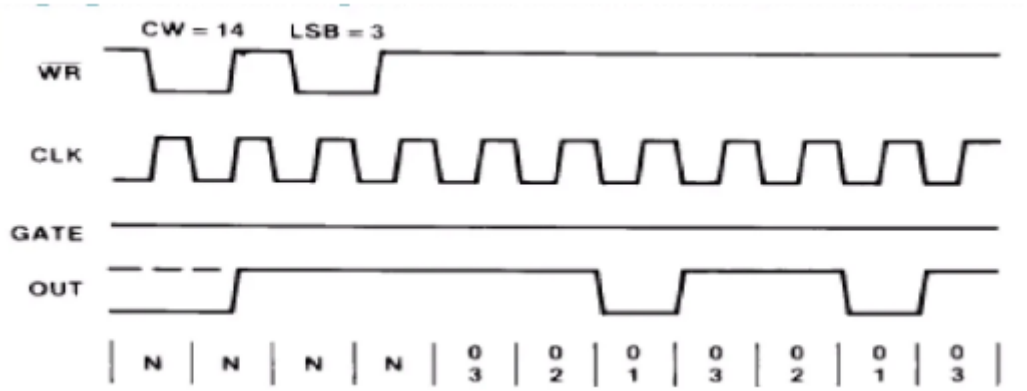
- Mode 0: Interrupt on terminal count
- 

  - Used for event counting
  - This mode is selected if (D3 D2 D1) of the control word register is (0 0 0)
  - When this mode is selected, the OUT pin is initially low.
  - The GATE pin is made high, so counting is enabled.
  - The count value is loaded, and the counting starts after the next high to low transition of the clock pulse.
  - During counting, the OUT pin remains low.
  - On terminal count (0), the OUT pin goes high, and it remains high until a new count is written into the counter.
  - During counting, if the gate goes low then counting is terminated and the current count is latched till the GATE goes high again.
- Mode 1 - Hardware Retriggerable one shot



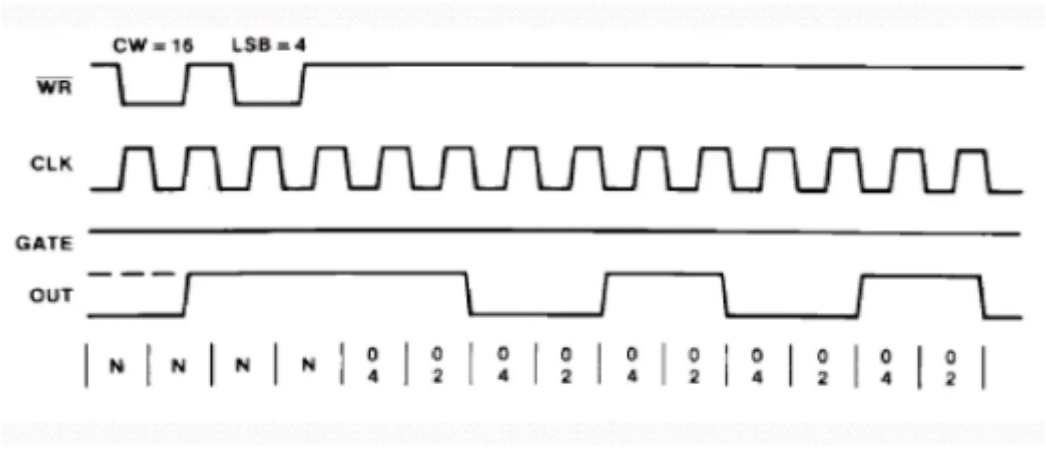
- This mode id selected if (D3 D2 D1) of CWR is (00 1).
- When this mode is selected OUT pin is initially high.
- The count value is loaded. Counting begins ONLY when a rising edge is applied to the GATE.
- OUT pin goes low and remains low during counting.
- During counting if GATE is made low, it has no effect on the Counting.

- Mode 2 - Rate Generator



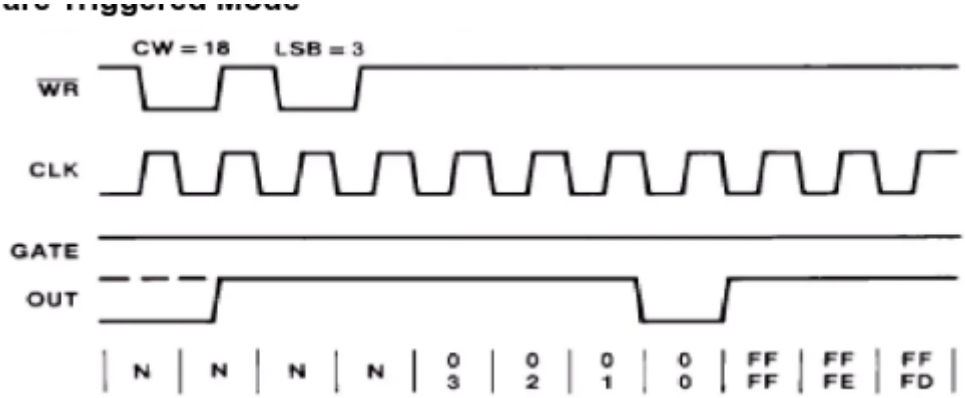
- Also known as divide by N counter.
- OUT pin is initially high.
- if N is loaded as count values then after N - 1 cycle, the output becomes low only for one clock cycle
  - If N = 4, after 3 cycles, output becomes low
- After that counter is reloader, OUT pin is set high and counting starts once more

- Mode 3 - Square Wave Generator



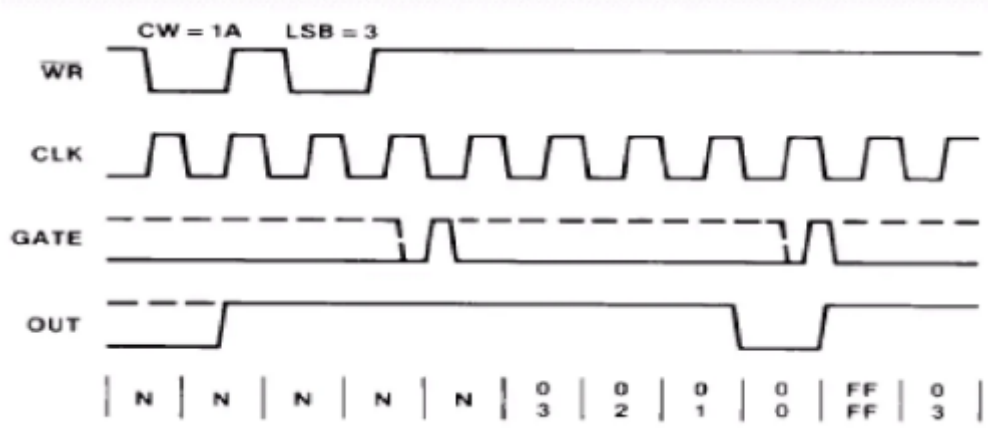
- Similar to Mode 2 except the OUT remains low for half of the timer period and high for the other half of the period.
- If the count loaded is odd, the first clock cycle decrements it by 1 resulting in an even count.
- This process is repeated continuously, generating a square wave.

- Mode 4 - Software Triggered Mode



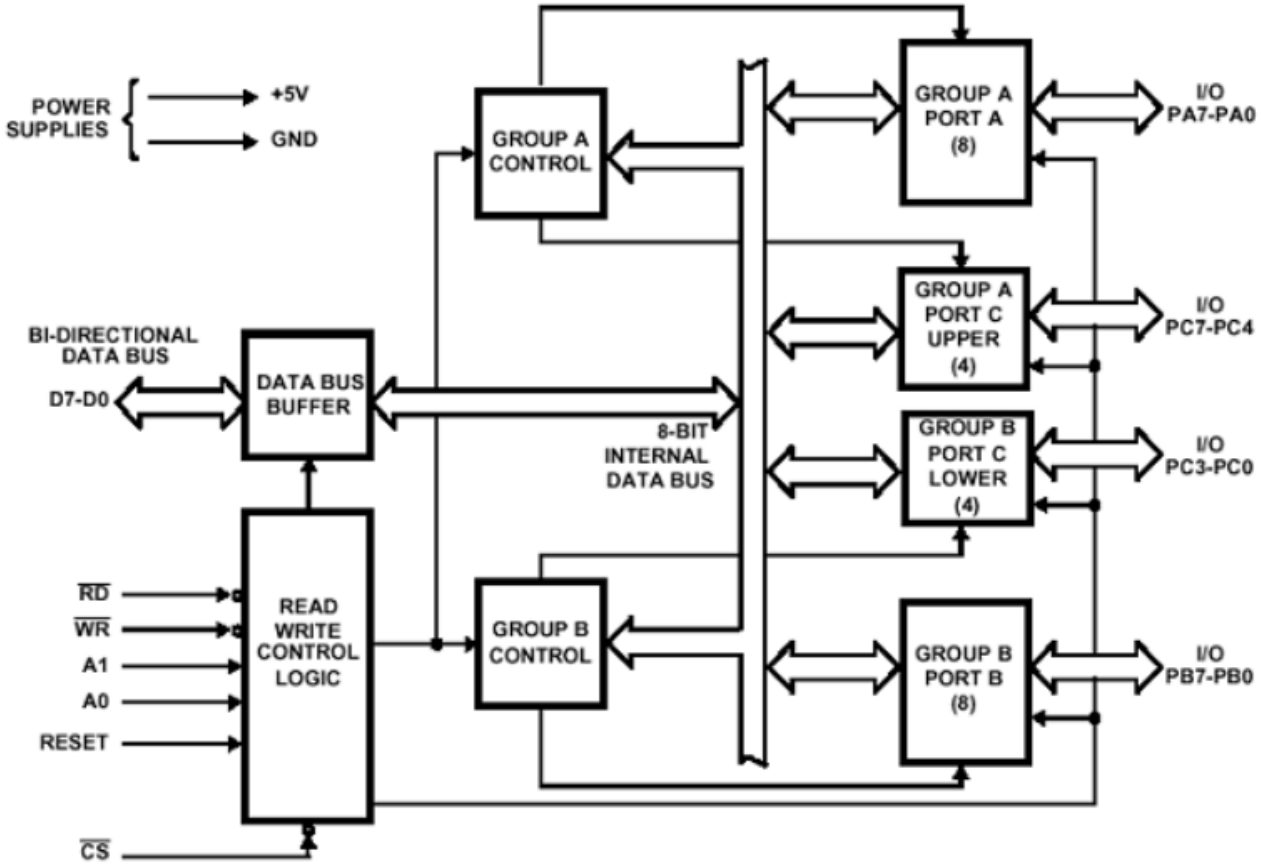
- Intially OUT remains high.
- On last count, the output goes low for one clock cycle and then goes HIGH.

- Mode 5 - Hardware triggered mode



- Similar to mode 4 except that the counting is initiated by a signal at the gate input.
- This means it is hardware triggered.

2. With a neat diagram, describe the architecture of 8255 PPI.



- 8255 PPI is designed by Intel corporation for interfacing I/O devices (Peripheral devices) with microprocessor
- Basically 8255 will function in two modes:
  - BSR Mode
  - I/O Mode
- BSR mode is also known as bit reset mode is using for setting or resetting port C bits
- I/O Mode is also known as Input/Ouput mode will function in 3 different modes:
  - Mode 0
    - In mode 0, all ports (Port A, Port B, Port C) are using for input/output data transfer without handshaking.
    - It is also known as basic I/O mode
  - Mode 1
    - In mode 1, only port A, B are using for input/output data transfer.
    - Port C pins are using for handshaking operation

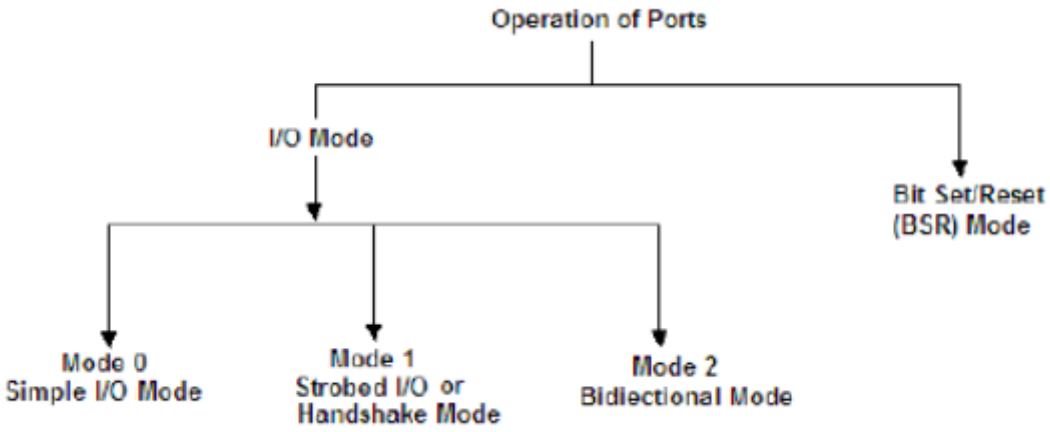
        - The upper port C bits (PC4 - PC7) are using for handshaking operation of Port A.
        - The lower port C bits (PC0 - PC3) are using for handshaking operation of port B. It is also known as strobed I/O mode
    - Mode 2
        - In mode 2, only port A is using for I/O data transfer (Bi-directional data transfer)
        - port C pins are using for handshaking operation of port A
        - It is also known as strobed bidirectional I/O mode
    - in 8255 IC, there are 40 pins
    - 24 pins are for port A, port B and port C
    - D7 bit of control register will decide the different operations of 8255 (BSR Mode and I/O mode)
        - if D7 bit = 0, then 8255 will function in BSR mode
        - If D7 bit = 1, then 8255 will function in I/O mode
        - D_3-D_6 bits of control word are using for mode selection and I/O data transfer direction of port A
          D_0-D_2 bits of control word are using for mode selection and I/O data transfer direction of port B
          D_0-D_3 pins of control word are using for direction of data transfer of port C (Mode 0)

3. Give the registers available in 8257 DMA Controller. Explain their functions.

- The 8257 performs DMA operation over four independent DMA channels with the following Registers.
- DMA Address Register
    - The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel.
    - The device that wants to transfer data over a DMA channel, will access the block of the memory with the starting address stored in the DMA Address Register.
- Terminal Count Registers
    - Each of the four DMA channels of 8257 has one terminal count register (TC).
    - This 16-bit register is used for ascertaining that the data transfer through a DMA channel cease or stops after the required number of DMA cycles
- Mode Set Register
    - The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation. The bits Do-D3 enable one of the four DMA channels of 8257.
- Status register

- The lower order 4-bits of this register contain the terminal count status for the four individual channels. If any of these bits is set, it indicates that the specific channel has reached the terminal count condition

4 .Explain the different modes of operation of 8255 in detail.

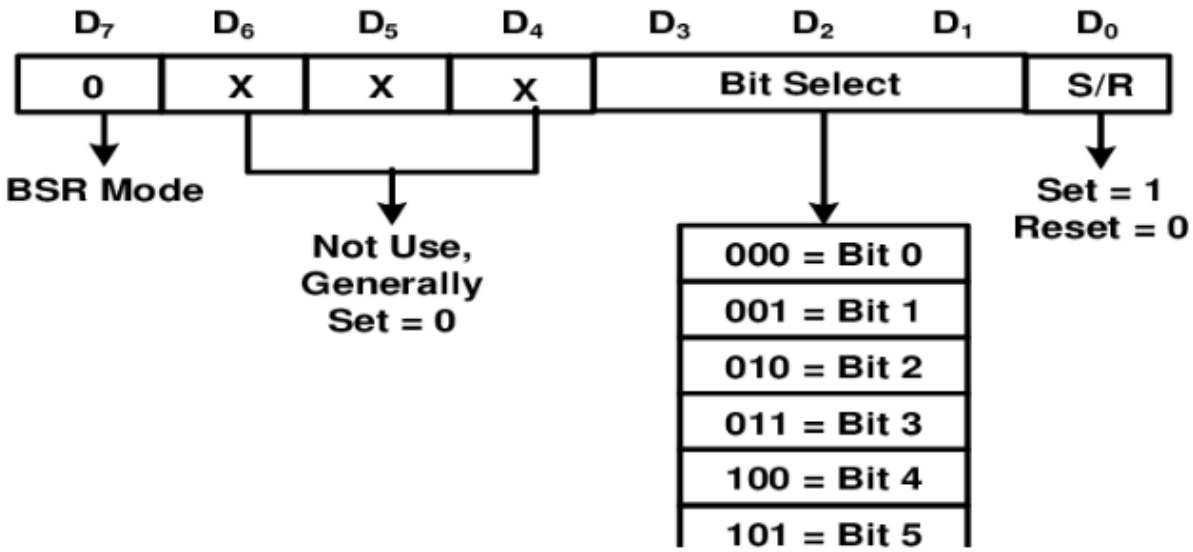


1. Input/Output Mode

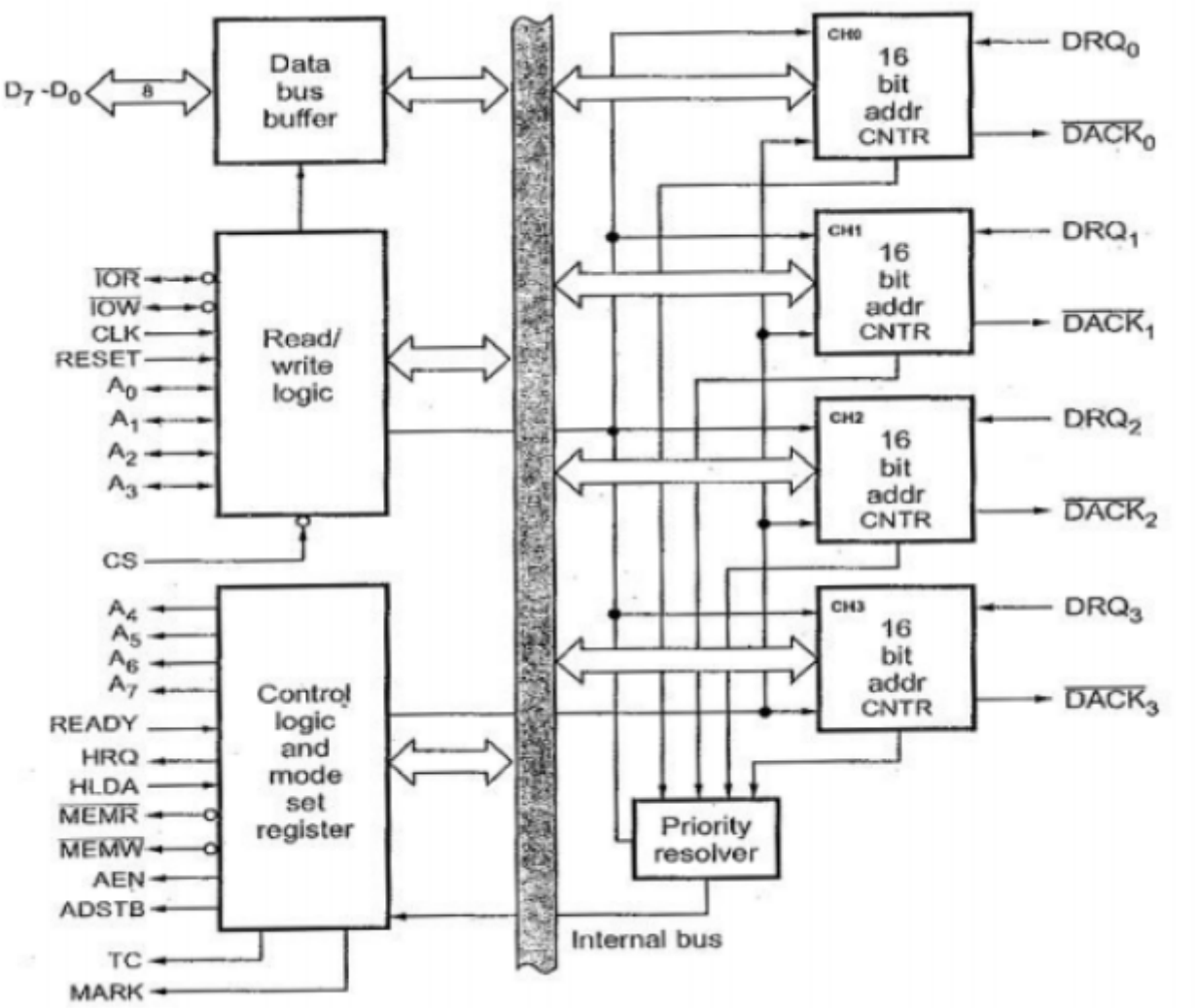
- Mode 0 - Basic input/output
  - In this mode, Port A and B is used as two 8-bit ports and Port C as two 4- bit ports.
  - Each port can be programmed in either input mode or output mode.
  - Ports do not have interrupt capability.
  - Port C is divided into two nibbles - upper and lower. Both upper and lower can now be programmed to use as input or output.
  - Mode 0 is also known as input/output mode (1/0 mode).
- Mode 1 - Strobed Input/Output
  - In mode 1 each group can be used as 8-bit input or output data bus and the remaining 4-bits (of Port C) are used as handshaking and interrupt control signals.
  - Port A is used with port C upper three bits and port B is used with port c lower 3 bits. The remaining 2 bits of port C can be used as control signals.
- Mode 2 - Bi-directional Bus
  - In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1.
  - In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1.
  - Port A uses five signals from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/0 or as handshake for port B.

2. Bit set/Reset (BSR) Mode

- In this mode only Port B can be used (as an output port).
- Each line of port C (PC0 - PC7) can be set/reset by suitably loading the command word register.
- The figure shows the control word format in BSR mode. This mode is selected by making D7='0'.
- D1, D2, D3 are used to select a particular port C bit whose value may be either set or reset.
- D0 is used for bit set/reset. When D0 = 1, the port C bit selected is SET and when D0 = 0, the port C bit is RESET.



5. Draw and explain internal architecture of 8257



- DRQ0−DRQ3: These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ0 has the highest priority and DRQ3 has the lowest priority among them.
- DACKo − DACK3: These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.
- Do − D7: These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller.
- IOR: used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle
- IOW: used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.
- CLK: It is a clock frequency signal which is required for the internal operation of 8257.

- RESET: This signal is used to RESET the DMA controller by disabling all the DMA channels.
- A0 - A3: These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257
- CS: It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.
- A4 - A7: These are the higher nibble of the lower byte address generated by DMA in the master mode.
- READY: It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.
- HRQ: This signal is used to receive the hold request signal from the output device.
- HLDA: It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.
- MEMR: It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.
- MEMW: It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation
- ADST: This signal is used to convert the higher byte of the memory address generated by the DMA controller into the latches
- AEN: This signal is used to disable the address bus/data bus.
- TC: It stands for ‘Terminal Count’, which indicates the present DMA cycle to the present peripheral devices.
- MARK: The mark will be activated after each 128 cycles or integral multiples of it from the beginning.

8257 has 5 functional blocks

- Data bus buffer
- Control logic
  - Controls the sequences of operationss
- Priority Resolver
  - The priority resolver resolves the priority of the four DMA channels depending upon whether normal priority or rotating priority is programmed
- Read/Write Logic