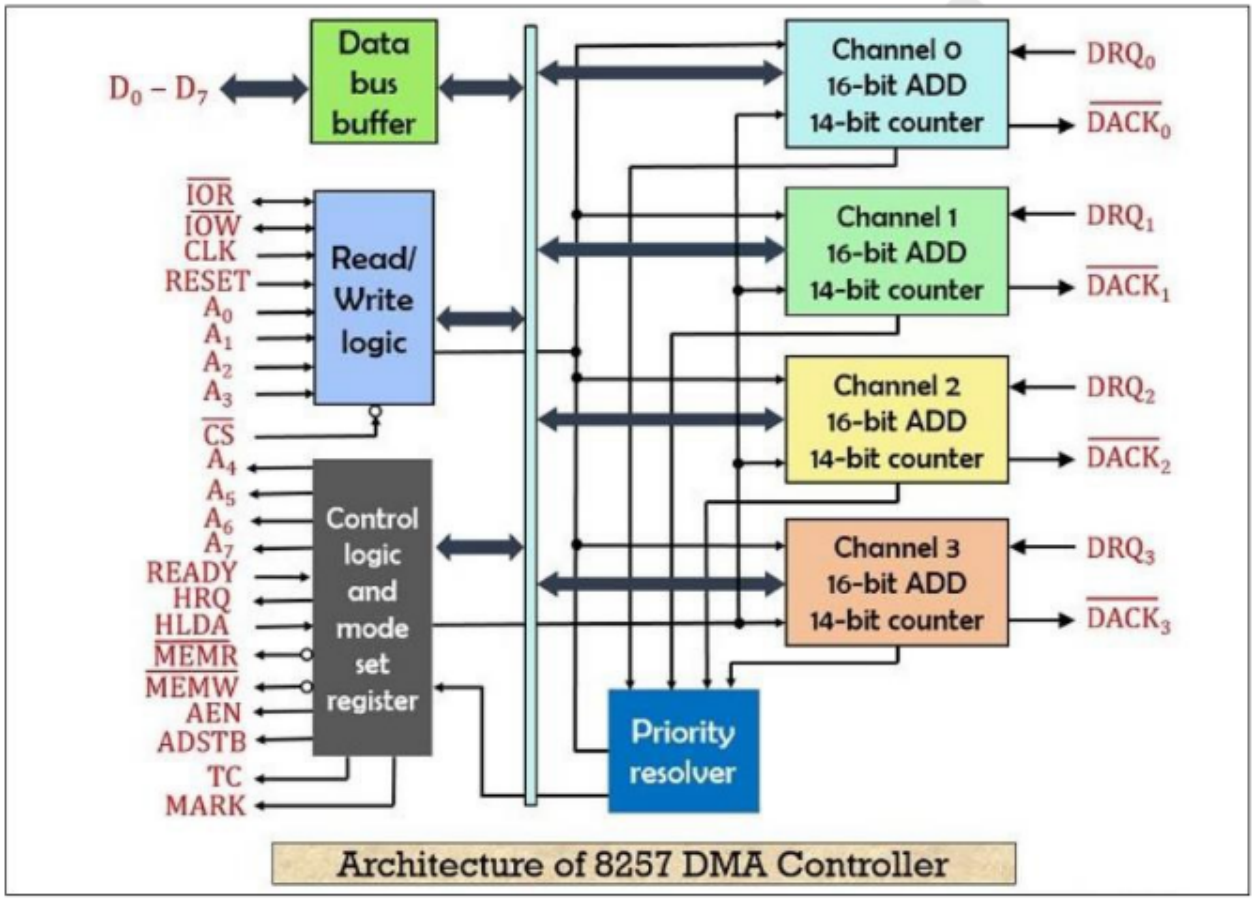
Microprocessors Module 4 Important Topics

8257 architecture

Direct Memory Access

- The DMA mode of data transfer is the fastest among all modes of data transfer
- In this mode, Device may transfer data directly to/from memory without any interference from CPU
- DMA data transfer is initiated only after receiving HLDA (Hold Acknowledge) signal from CPU



- The Chip supports 4 DMA channels
  - 4 Peripheral devices can independently request for DMA at a time
- The DMA Controller has 5 functional blocks
  - 8 bit internal data buffer
  - Read/Write Unit
  - Control Unit
  - Priority resolving unit

        - The priority resolver resolves the priority of the four DMA channels
    - DMA Channels
- Each of the 4 channels of 8257 has a pair of two 16 bit registers
    - DMA address Register
    - Terminal count register
- There are 2 common registers for all channels
    - Mode set register
    - Status Register
- So there are 10 registers in total = 4 x 2 (16 bit registers) + 2 (Common registers)
    - The CPU selects one of these 10 registers using address lines A0 - A3

Register organization of 8257

DMA Address Register

- Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel.
- When a device wants to transfer data over a DMA channel
    - It will access the block of the memory with the starting address stored in the DMA Address Register.

Terminal count register

- Each of the 4 DMA channels of 8257 has one terminal count register
- After each DMA cycle, the terminal count register content will be decremented by one
    - It becomes zero after required number of DMA cycles are over

Mode Set Register

- Used for programming 8257 as per requirements of the system
- Function of the mode set register is to enable DMA channels individually and set various modes of operation

Status Register

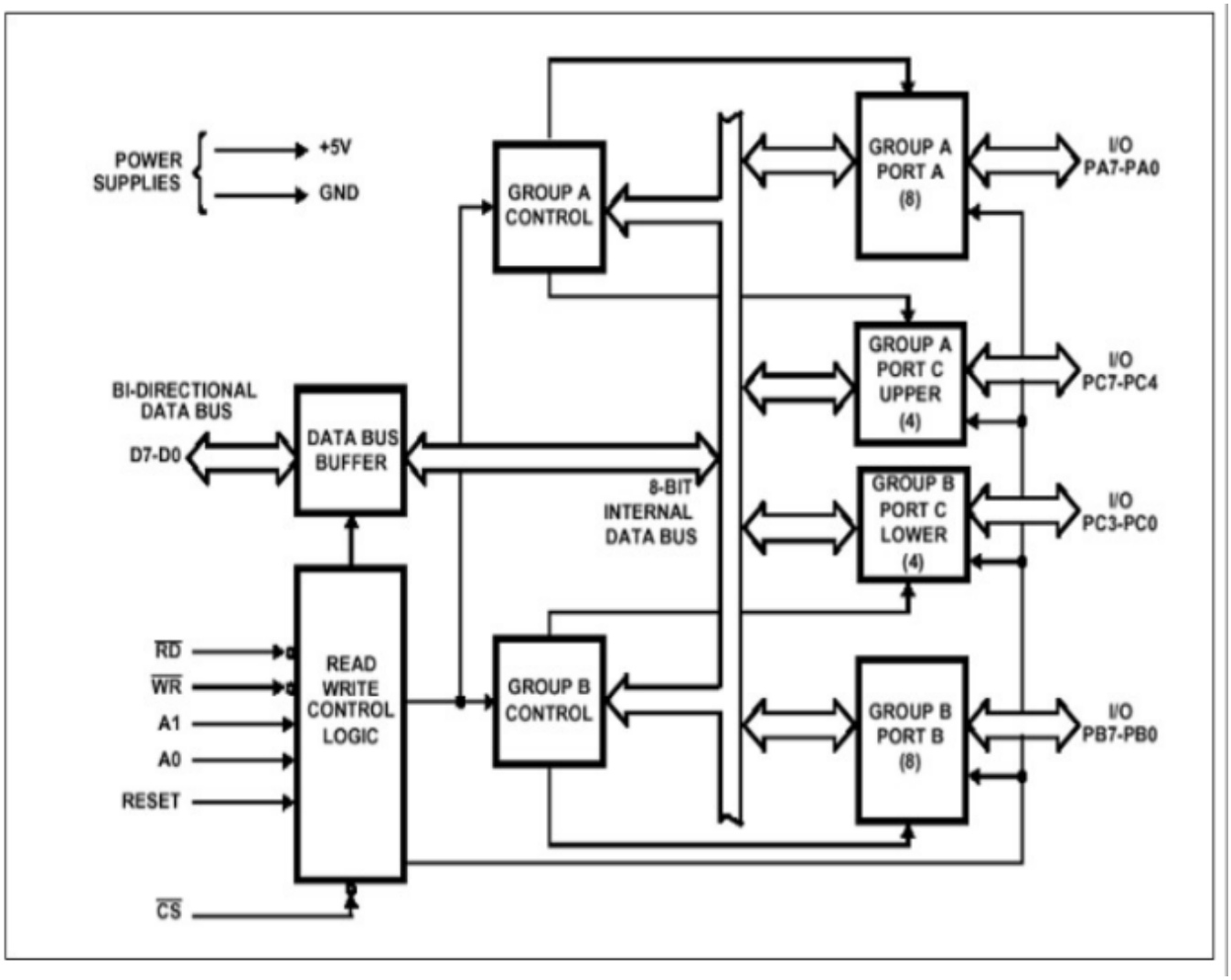
- The lower order 4-bits of this register contain the terminal count status for the four individual channels.
- If any of these bits is set, it indicates that the specific channel has reached the terminal count condition

DMA Transfer and operations

- 8257 is able to accomplish 3 types of operations
  - DMA Operation
  - Write Operation
  - Read Operation
- The operational sequence of 8257 is the following
  - **Request for Transfer:**
    - The 8257 requests any one of its DRQ (DMA Request) inputs to transfer a single byte of data.
  - **CPU Notification:**
    - In response to the request, the 8257 sends a Hold Request (HRQ) signal to the CPU at its HLD (Hold Acknowledge) input
    - The 8257 then waits for an acknowledgment from the CPU at the HLDA (Hold Acknowledge) input.
  - **CPU Acknowledgment:**
    - If the CPU acknowledges the HRQ signal by pulling the HLDA line low, it indicates that the CPU is allowing the DMA controller to take control of the system bus for data transfer.
  - **Bus Availability Check:**
    - The DMA controller, upon receiving the HLDA signal, checks if the system bus is available for the data transfer.
  - **Command Generation:**
    - If the bus is available, the DMA controller generates the necessary read and write commands to transfer the byte of data between the I/O device and memory.
  - **DACK Signal:**
    - The DMA controller pulls down the DACK (DMA Acknowledge) line of the used channel to inform the I/O device that requested the DMA transfer
  - **HRQ Line Lowering:**
    - Simultaneously, the HRQ line is lowered by the DMA controller to indicate to the CPU that it may regain control of the bus.
  - **Acknowledgment of Transfer:**
    - The DRQ line must remain high until acknowledged.
      - DRQ = DMA Request
    - In each state the DRQ lines are sampled, and the highest priority request is recognized during the next transfer.
    - The HRQ line is maintained active until all DRQ lines go low, indicating that all requested transfers are complete.
      - HRQ = Hold request

8255 architecture and modes of operation

Architecture



- It has 24 input/output lines
  - They are individually programmed to two groups of twelve lines each
  - These 2 Groups of I/O Pins are Group A and Group B
    - Each of these groups has a subgroup
    - Subgroup of 8 IO lines called 8 bit port
    - Subgroup of 4 IO lines called 4 bit port
- Group A contains
  - 8 bit port A
    - Port A lines are identified by PA0-PA7
  - 4 bit port C upper
    - Port C lines are identified by PC4-PC7
- Similarly We have Group B

    - 8 Bit port B
        - Identified by PB0-PB7
    - 4 Bit port C lower
        - Identified by PC0-PC3
- Port C upper and Port C Lower can be used in combination as 8 bit port C

Functional Description

- Data bus Buffer
    - Data is transmitted or received by buffer as per instructions by the CPU
- Read Write Control Logic
    - Responsible for controlling internal/external transfer of data/controll/status word
- CS
    - Stands for Chip select
    - LOW = Select the chip and enables communication between 8255A and CPU
- WR
    - Stands for write, Enables write operation
    - When signal is low, microprocessor writes to selected IO port/control register
- RESET
    - Clears control register
- RD
    - Read operation, When signal is low, microprocessor read the data from selected IO port

Modes of operation

- 8255A has three different operating modes
- 1. Input/Output Mode
    - Mode 0 - Basic Input/Output
        - Port A and B are used as two bit ports
        - Port C is used as two 4 bit Ports
        - Each Group can be used as input or output
            - Port A, Port B and Port C can be used as input or output
    - Mode 1 - Stored Input/Output
        - Each group can be used as 8 bit input or output data bus
        - Remaining 4 bit are used as handshaking and interrupt control signals
    - Mode 2 - Bi-directional Bus
        - Port A is Bidirectional

- Port B is either in Mode 0 or Mode 1
- Port A uses 5 signals from Port C as handshake signals for data transfer
- Remaining 3 signals from port C are used as I/O or handshake for port B
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- 2. Bit Set/Reset (BSR) Mode
  - **Port Usage:**
    - In this mode only port b can be used as an output port
    - Port C (PC0 - PC7) is exclusively used for bit manipulation (setting or resetting).
  - **Command Word Register:**
    - The BSR mode is controlled by loading a command word into the control register of the microcontroller.
  - **Bit Set/Reset Operation:**
    - D0 of the control word is dedicated to bit set/reset operations.
    - When D0 = '1', the specified bit on Port C is set.
    - When D0 = '0', the specified bit on Port C is reset.
  - **Bit Selection:**
    - The combination of D1, D2, and D3 allows you to choose one of the eight bits (PC0 - PC7) on Port C for manipulation.

BSR (BIT SET/RESET) MODE