Lattice FPGA Project Weekly Progress Report - Week 9

Report date: 2025/3/6

- **Last Week (time in hours)**
  - Team Review
    - Working through clock issues, getting building blocks ready
  - Nathaniel Fraly
    - Research into clock issues with Radiant (2)
    - Implement button in SV (2)
    - Implement PWM in SV (2)
    - Implement color change in SV (2)
  - Riley Cox
    - Looked into programming Icicle core in Radiant (1)
    - Worked on figuring out how to integrate SPI controller for Yosys (2)
  - Mohammad Alshaiji
    - Debug Clock generation issue in Lattice Radiant for SPI Controller (9)
    - Debugging issues with testing of SPI Controller (2)
  - Xiang Li
    - Code learning on Adafruit GFX library(3)
    - Understanding how to print font(3)
  - Haoyang Han
    - Completed the 3D modeling of the heart-shaped box（6）
- **Next week**
  - Team Plan
    -
  - Nathaniel Fraly
    - Begin integration of above modules in Icicle
  - Riley Cox
    - Integrate SPI controller
  - Mohammad Alshaiji
    - Determine why clock is failing to generate despite simulation working
    - Begin Integration with Riley
  - Xiang Li
    - Fix any issue that happens when using SPI commands to drive the screen
    - Figure out how to utilize FPGA to build a font table and convert
  - Haoyang Han
    - Modify 3D modeling dimensions.
- **Blocked**
  - Team Blocks
    - Radiant not behaving
  - Nathaniel Fraly
    - Issues with Radiant.
  - Riley Cox
    - Issues with Radiant / Not comfortable with it
  - Mohammad Alshaiji
    -
  - Xiang Li
    - None

- Haoyang Han
  - How to make space for buttons on the sides of a box.