

# Lattice FPGA Project Weekly Progress Report - Week 3

Report date: 2025/1/24

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- **Last Week (time in hours) (1/20-1/24)**

- Team Review
  - Finished the rough draft of Project Proposal
  - Finished setting up GitHub and the collaboration sites
  - Start trying to set up Open Source FPGA Development tools, Yosys setup
- Nathaniel Fraly
  - Yosys toolchain set up and familiarization - Was sick all week (4)
- Riley Cox
  - Set up Yosys toolchain and ran through examples to get familiar with it - in the process of moving (6)
  - Set up Github repository (1)
- Mohammad Alshaiji
  - Wrote Background and Research, Risks, and Project Management Plan for project proposal (5)
  - Created L0 and L1 diagrams for the project proposal (.5)
  - Created Preliminary Gantt Chart(3)
- Xiang Li
  - Wrote Executive Summary and Product Design Specification for project proposal (6)
  - Try to set up the development tools (1)
- Haoyang Han
  - Research projects on how to better meet low-power requirement (3)
  - Research project hardware part (2)

- **Next week(1/25-1/31)**

- Team Plan
  - Everyone should have Yosys installed and run through at least a basic design synthesis
  - Choose RISC-V core to use for design
  - Find SPI core to use for design
- Nathaniel Fraly
  - Research RISC-V core options for Yosys implementation
  - Continue Yosys familiarization
  - Look into power save of pure RTL implementation - low prio
- Riley Cox
  - Continue Yosys familiarization
  - Research RISC-V core options
- Mohammad Alshaiji
  - Install and synthesize example file in Yosys
  - Read through IEEE papers and determine pertinent info
  - Research SPI implementation
- Xiang Li
  - Set up WSL and run Yosys on Linux (2)
  - Read Yosys documentation, try examples (4)

- Search for SPI IPs (4)
- Haoyang Han
  - Set up WSL and run Yosys on computer(2)
  - Read Yosys documentation, try examples (4)
  - Begin with power monitor(4)
  - Design 3D printing case (3)
- **Blocked**
  - Team Blocks
    - Need to find a simulator; may use the school's servers for QuestaSim for preliminary, but need to see if Yosys can simulate synthesized designs. Yosys may have one built-in
  - Nathaniel Fraly
    - Need to install a different Linux distro before continuing Yosys work; Rocky distro clunky. Likely switching to Debian to match Riley's WSL environment.
  - Riley Cox
    - Need to purchase UPduino board and be able to work with it
  - Mohammad Alshaiji
    - Need to migrate to Debian
  - Xiang Li
    - Haven't successfully run Yosys on computer
    - Will try WSL and run on Linux
  - Haoyang Han
    -

# Lattice FPGA Project Weekly Progress Report - Week 4

Report date: 2025/01/31

- **Last Week (time in hours)**

- Team Review
  - Xiang and Mohammed worked on PDS to send to Roy and Rahul. Implementing feedback now
- Nathaniel Fraly
  - Yosys, Icestorm, and NextPNR tool setup (2)
  - Debian Linux environment setup (10)
- Riley Cox
  - Yosys, Icestorm, and NextPNR tool setup and working with bitstream generation (4)
  - RISC-V core research (3)
  - Icycle RISC-V core build and verification (2)
- Mohammad Alshaiji
  - Successfully completed synthesis using Yosys on WSL Debian (3)
  - Researched SPI implementation and identified some IP cores for further research (3)
  - Read further through IEEE papers (2)
- Xiang Li
  - Revise PDS(3)
  - Set up Yosys (1)
  - Research on SPI cores (3)
- Haoyang Han
  - Research power monitor (3)
  - Choose the right power monitor (1)
  - Set up Yosys (1)
  - Research on SPI cores (3)

- **Next week**

- Team Plan
  - Familiarize with Icycle RISC-V core, get SPI module implementation started
- Nathaniel Fraly
  - Get OpenSource Toolchain verified functional
  - Verify Icycle default persistence (is program stored in volatile or non-volatile memory)
  - Get Icycle core on FPGA board (Dual w/ Riley)
  - Assist w/ PDS as needed to meet the deadline.
- Riley Cox
  - Need to get Lattice Radiant setup and working
  - Need to modify current version of Icycle to work for UPduino V2.1
- Mohammad Alshaiji
  - Get Icestorm setup and read further through the documentation
  - Get upduino V2.1 and V3.1 comparison to Rahul before Tuesday
  - Assist with PDS
  - Implement SPI IP on upduino board
  - Get Radiant toolchain installed and setup
- Xiang Li
  - Finish PDS

- Figure out how to implement SPI inside a core
  - Learn about SPI core code
- Haoyang Han
  - Get power monitor and start debugging
  - Figure out how to implement SPI inside a core
  - Learn about SPI core code
- **Blocked**
  - Team Blocks
    - Differences between UPduino v2.1 and v3.0 need to be documented so implementation can move forward. Weekly progress reports being done last-minute, Nathan to implement team policy to prevent reoccurrence.
  - Nathaniel Fraly
    - Issues with Linux environment not working on personal hardware. Need to fix bootloader issues and SecureBoot issues, or move to a different environment solution. Perfect environment is useless if it doesn't start working until April.
  - Riley Cox
    - The Icicle RISC-V core for UPduino is meant for V1.0 boards, the board I have is a V2.1 so there are changes that need to be made to get it working to be able to see output on the serial monitor.
    - Need to get USB tunneling working for WSL on desktop, currently using a laptop with Arch to program board.
  - Mohammad Alshaiji
    - Need to get a test bitstream using Icestorm and Yosys and ensure functioning with arduino board.
  - Xiang Li
    - WSL can't directly visit USB device
    - ST7735R datasheet hard to read
  - Haoyang Han
    - There are so many different types of power monitors, it can be hard to find the right one

# Lattice FPGA Project Weekly Progress Report - Week 5

Report date: 2025/2/6

- **Last Week (time in hours)**

- Team Review
  - Icicle is verified functional on V2.1 boards
  - Nathan can finally stop fighting his Linux environment
  - Icicle supports UART natively, so debug messages can go out
- Nathaniel Fraly
  - Debian system setup and portable (2)
  - Work with Rahul and team on PDS (4)
  - Start project documentation requested by Rahul (1)
- Riley Cox
  - Flashed simple blinking LED bitstream to FPGA (1)
  - Migrated Icicle from UPduino V1 to V2 (3)
  - Flashed Icicle to UPduino using open source tools (1)
  - Worked on USB tunneling for WSL (1)
  - Started documentation for project setup (1)
- Mohammad Alshaiji
  - Finished V2.1 and V3.1 board comparison for Rahul (1)
  - Assisted with PDS (1)
  - Finished preliminary SPI controller Core research (2)
  - Radiant toolchain installed but setup not completed (2)
- Xiang Li
  - Revise PDS (2)
  - Collect and learn SPI modules (5)
- Haoyang Han
  - Complete power monitor research and purchase (3)
  - Radiant toolchain installed and setup (2)

- **Next week**

- Team Plan
  - Focus on SPI implementation
  - Provide Rahul with requested additional documentation
  - Work on additional future modules as able
- Nathaniel Fraly
  - Help walk Xiang and Mohammad through Icicle and how to read SV code
  - Assist with Radiant migration
  - Start on PWM module testing
- Riley Cox
  - Figure out how to flash Icicle onto FPGA using Radiant
  - Finish WSL setup and be able to work with board
  - Finish documentation for setting up project from scratch
- Mohammad Alshaiji
  - Finish Setting up radiant toolchain
  - Begin Basic SPI implementation to control LCD
  - Research and determine ideal method for interfacing with Icicle core
  - Finish Icestorm Setup
- Xiang Li

- Insert SPI module into icicle
  - Develop code for SPI module
- Haoyang Han
  - Get Power Monitor
  - Debugging Power Monitors
- **Blocked**
  - Team Blocks
    - No teamwide blocks
  - Nathaniel Fraly
    - None
  - Riley Cox
    - Icicle currently uses a Makefile with yosys and icestorm commands along with compiling the C code that the RISC-V core is running, I need to figure out how I can make that work with Radiant. This will involve getting used to Radiant and understanding the Makefile better.
  - Mohammad Alshaiji
    - Waiting on LCD order that will be beneficial for testing output from SPI
    - Need to understand SystemVerilog better
  - Xiang Li
    - Not sure about how to insert modules into icicle
    - Confused about the working principle of icicle
  - Haoyang Han
    - How to choose a more suitable microprocessor controlled power monitor

# Lattice FPGA Project Weekly Progress Report - Week 6

Report date: 2025/2/13

- **Last Week (time in hours)**

- Team Review
  - Finalize RISC-V and dependency setup for open-source
- Nathaniel Fraly
  - Test subject for Riley's setup docs (7)
  - Install and attempt to test Radiant (1)
  - Troubleshoot Icicle synthesis in Radiant (2)
  - Assist MA, XL, HH toolchain setup (3)
- Riley Cox
  - Worked on and finished WSL/toolchain setup documentation (8)
  - Installed and setup Radiant (1)
  - Helped teammates troubleshoot toolchain setup (3)
- Mohammad Alshaiji
  - Finished setting up toolchain in accordance with the toolchain Document (2)
  - Wrote preliminary SPI controller (3)
  - Setup Radiant toolchain completely and ensured functioning of Questasim (1)
  - Created Preliminary SOC block Diagram (3)
- Xiang Li
  - Review UART to SPI IP from opencores (1)
  - Setup Radiant toolchain completely following teammate's guidance(3)
  - Installed and working with Radiant (4)
- Haoyang Han
  - Setup Radiant toolchain completely following teammate's guidance(3)
  - Installed and working with Radiant (4)
  -

- **Next week**

- Team Plan
  - Rahul ordering 1.44" LCD screens; 1.8" out of stock
  - Start working on Radiant synthesis
  - Finalize SPI implementation methodology
  - SPI library skeleton
- Nathaniel Fraly
  - Work with SPI team on getting custom C library ready for SPI communication
  - Work with Roy/Rahul/Lattice resources on getting Radiant synthesis complete
- Riley Cox
  - Start working on the C code to have the RISC-V core communicate with the LCD
  - Work on synthesizing project via Radiant
- Mohammad Alshaiji
  - Run Questasim simulation of SPI controller
  - Begin Integration of SPI controller with Icicle
  - Catch up on Meeting Notes Backlog
  - Redo SOC Block Diagram and take into account Rahul's Requirements
- Xiang Li
  - Upload the documents so far
  - Research on how to write to registers inside the LCD screen

- Test the IPs on hand
- Haoyang Han
  - 3D Printing Modeling
- **Blocked**
  - Team Blocks
    - Soft Block; Radiant complaining of duplicate modules, no duplicates found.
  - Nathaniel Fraly
    - Will need SPI team to settle on implementation methodology for SPI library work to begin in earnest
  - Riley Cox
    - None
  - Mohammad Alshaiji
    - None
  - Xiang Li
    - None
  - Haoyang Han
    - None



# Lattice FPGA Project Weekly Progress Report - Week 7

Report date: 2025/2/20

- **Last Week (time in hours)**

- Team Review
  - Getting SPI module ready for integration
  - Prepare SPI library
- Nathaniel Fraly
  - Troubleshoot Radiant duplicate module error (4)
- Riley Cox
  - Researched Adafruit SPI library (2)
  - Researched ST7735 library to determine how we communicate with LCD(2)
- Mohammad Alshaiji
  - Simulate SPI controller on Questasim [3]
  - Revised SOC Block Diagram [1]
  - Synthesized SPI controller using Radiant [2]
- Xiang Li
  - Research on Adafruit ST7735 Library (2)
  - Write down the command list need to send through SPI (4)
- Haoyang Han
  - Modeling for 3D printing (4)
  - Research on debounce button (2)

- **Next week**

- Team Plan
  - Prepare accessory code
  - Continue SPI work
- Nathaniel Fraly
  - Get button interface ready
- Riley Cox
  - Work with Nathan to develop code to interface with button
  - Work on SPI library
- Mohammad Alshaiji
  - Update meeting notes on Github
  - Ensure that SPI controller Operates correctly on ICE40
  - Utilize SPI controller on ICE40 To drive LCD
- Xiang Li
  - Light up the screen
  - Find the commands for color control
- Haoyang Han
  - Improved 3D modeling
  - Solving Hardware Issues

- **Blocked**

- Team Blocks
  - Just Nathan's
- Nathaniel Fraly
  - Will need help figuring out Radiant duplicate module issue
- Riley Cox
  - None

- Mohammad Alshaiji
  - N/A
- Xiang Li
  - None
- Haoyang Han
  - N/A

# Lattice FPGA Project Weekly Progress Report - Week 8

Report date: 2025/2/27

- **Last Week (time in hours)**

- Team Review
  - Got RISC-V Core on Radiant
  - SPI module on board through Radiant!!!
- Nathaniel Fraly
  - Troubleshooting Radiant bitstream upload (3)
  - Research SPI flash chip present on UPduino devices (2)
- Riley Cox
  - Trying to put bitstream on UPduino through Radiant (4)
- Mohammad Alshaiji
  - Debugging FTDI issue in lattice Radiant (5)
  - Catching up on meeting agenda backlog 75% complete (1)
  - Begin preliminary research for implementation of SPI controller with Icicle
- Xiang Li
  - Research on Adafruit-GFX-library(3)
  - Document on how to fill in color of screen(3)
  - Learning to use Radiant tool(1)
- Haoyang Han
  - 3D modeling of the second version, Based on sponsor (5)

- **Next week**

- Team Plan
  - Continue incremental progress towards completion of phase 1
  - Figure out how to get C program on board through Radiant
- Nathaniel Fraly
  - Actually get to buttons and PWM this week. Will starve self to achieve if needed
- Riley Cox
  - Integrate SPI core with Icicle with Mohammad
  - Work on developing commands to have Icicle communicate with LCD
- Mohammad Alshaiji
  - Test initialization of screen using spi controller
  - Begin integration of SPI core with Icicle with Riley
  - test Xiang's color commands with SPI controller
- Xiang Li
  - Go back to any issues the implementation is stuck
  - Fix any bugs on lighting up the screen
- Haoyang Han
  - Continue to improve 3D modeling

- **Blocked**

- Team Blocks
  - C program on board through Radiant
- Nathaniel Fraly
  - Radiant behavior sometimes non-deterministic with FTDI driver; will cause issues persistently until a solution is found. Soft block
- Riley Cox
  - Issues with flashing bistream using Radiant

- Unsure how to put C program into memory via Radiant
- Mohammad Alshaiji
  - Experiencing FTDI issues with SPI controller, attempting to fix with documentation provided by Rahul
- Xiang Li
  - None
- Haoyang Han
  - The shape requested by the sponsor is a bit difficult to model.

# Lattice FPGA Project Weekly Progress Report - Week 9

Report date: 2025/3/6

- **Last Week (time in hours)**

- Team Review
  - Working through clock issues, getting building blocks ready
- Nathaniel Fraly
  - Research into clock issues with Radiant (2)
  - Implement button in SV (2)
  - Implement PWM in SV (2)
  - Implement color change in SV (2)
- Riley Cox
  - Looked into programming Icicle core in Radiant (1)
  - Worked on figuring out how to integrate SPI controller for Yosys (2)
- Mohammad Alshaiji
  - Debug Clock generation issue in Lattice Radiant for SPI Controller (9)
  - Debugging issues with testing of SPI Controller (2)
- Xiang Li
  - Code learning on Adafruit GFX library(3)
  - Understanding how to print font(3)
- Haoyang Han
  - Completed the 3D modeling of the heart-shaped box (6)

- **Next week**

- Team Plan
  -
- Nathaniel Fraly
  - Begin integration of above modules in Icicle
- Riley Cox
  - Integrate SPI controller
- Mohammad Alshaiji
  - Determine why clock is failing to generate despite simulation working
  - Begin Integration with Riley
- Xiang Li
  - Fix any issue that happens when using SPI commands to drive the screen
  - Figure out how to utilize FPGA to build a font table and convert
- Haoyang Han
  - Modify 3D modeling dimensions.

- **Blocked**

- Team Blocks
  - Radiant not behaving
- Nathaniel Fraly
  - Issues with Radiant.
- Riley Cox
  - Issues with Radiant / Not comfortable with it
- Mohammad Alshaiji
  -
- Xiang Li
  - None

- Haoyang Han
  - How to make space for buttons on the sides of a box.

# Lattice FPGA Project Weekly Progress Report - Week 10

Report date: 2025/3/13

- **Last Week (time in hours)**

- Team Review
  - Trying to work around clock issue UPDATE: CLOCK ISSUE RESOLVED, SPI MODULE UNIT TESTS PASSED!!!!!!!!!!!!!!!!!!!!!!
- Nathaniel Fraly
  - Troubleshooting clock instantiation with 3rd-party design modules (4)
- Riley Cox
  - Troubleshooting clock instantiation with 3rd-party design modules (4)
- Mohammad Alshaiji
  - Debugging clock generation issue (5)
- Xiang Li
  - Finished the preliminary C code for Screen Initialization and color change(6)
- Haoyang Han
  - 3D modeling improvements (4)

- **Next week**

- Team Plan
  - Integrate SPI module as time allows. Team will be focusing in finals to ensure we don't have to retake capstone next year.
- Nathaniel Fraly
  - Finals
- Riley Cox
  - Finals
- Mohammad Alshaiji
  - Finals
- Xiang Li
  - Finals
- Haoyang Han
  - Finals

- **Blocked**

- Team Blocks
  - Clock issue in SPI module
- Nathaniel Fraly
  - Can't integrate without SPI module
- Riley Cox
  - Can't integrate without SPI module
- Mohammad Alshaiji
  - Trying to integrate SPI module; clock issues
- Xiang Li
  - Can't integrate without SPI module
- Haoyang Han
  - N/A