

Lattice FPGA Project Weekly Progress Report - Week 17

Report date: 2025/05/01

- **Last Week (time in hours)**

- Team Review
 - Finishing up final touches on phase 1
- Nathaniel Fraly
 - Soldered protoboard for demo (3)
- Riley Cox
 - Assisted with soldering (3)
- Mohammad Alshaiji
 - Worked on Porting Core to Radiant (6)
- Xiang Li
 - PPT for DEMO (4)
- Haoyang Han
 - Designing PCB (5)

- **Next week**

- Team Plan
 - Start documentation, finalize Radiant port, test hardware for PCB design
- Nathaniel Fraly
 - Test battery connection
- Riley Cox
 - Update user guide on GitHub
- Mohammad Alshaiji
 - Continue Porting Core
- Xiang Li
 - Start Final Report
- Haoyang Han
 - Continue designing the PCB

- **Blocked**

- Team Blocks
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- Nathaniel Fraly
 - Need to catch up on other class
- Riley Cox
 - Need to catch up on other class
- Mohammad Alshaiji
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- Xiang Li
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- Haoyang Han
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