Lattice FPGA Project Weekly Progress Report - Week 10

Report date: 2025/3/13

- **Last Week (time in hours)**
  - Team Review
    - Trying to work around clock issue UPDATE: CLOCK ISSUE RESOLVED, SPI MODULE UNIT TESTS PASSED!!!!!!!!!!!!!!!!!!!
  - Nathaniel Fraly
    - Troubleshooting clock instantiation with 3rd-party design modules (4)
  - Riley Cox
    - Troubleshooting clock instantiation with 3rd-party design modules (4)
  - Mohammad Alshaiji
    - Debugging clock generation issue (5)
  - Xiang Li
    - Finished the preliminary C code for Screen Initialization and color change(6)
  - Haoyang Han
    - 3D modeling improvements (4)
- **Next week**
  - Team Plan
    - Integrate SPI module as time allows. Team will be focusing in finals to ensure we don't have to retake capstone next year.
  - Nathaniel Fraly
    - Finals
  - Riley Cox
    - Finals
  - Mohammad Alshaiji
    - Finals
  - Xiang Li
    - Finals
  - Haoyang Han
    - Finals
- **Blocked**
  - Team Blocks
    - Clock issue in SPI module
  - Nathaniel Fraly
    - Can't integrate without SPI module
  - Riley Cox
    - Can't integrate without SPI module
  - Mohammad Alshaiji
    - Trying to integrate SPI module; clock issues
  - Xiang Li
    - Can't integrate without SPI module
  - Haoyang Han
    - N/A