Lattice FPGA Project Weekly Progress Report - Week 3
Report date: 2025/1/24

- **Last Week (time in hours) (1/20-1/24)**
  - Team Review
    - Finished the rough draft of Project Proposal
    - Finished setting up GitHub and the collaboration sites
    - Start trying to set up Open Source FPGA Development tools, Yosys setup
  - Nathaniel Fraly
    - Yosys toolchain set up and familiarization - Was sick all week (4)
  - Riley Cox
    - Set up Yosys toolchain and ran through examples to get familiar with it - in the process of moving (6)
    - Set up Github repository (1)
  - Mohammad Alshaiji
    - Wrote Background and Research, Risks, and Project Management Plan for project proposal (5)
    - Created L0 and L1 diagrams for the project proposal (.5)
    - Created Preliminary Gantt Chart(3)
  - Xiang Li
    - Wrote Executive Summary and Product Design Specification for project proposal (6)
    - Try to set up the development tools (1)
  - Haoyang Han
    - Research projects on how to better meet low-power requirement (3)
    - Research project hardware part (2)
- **Next week(1/25-1/31)**
  - Team Plan
    - Everyone should have Yosys installed and run through at least a basic design synthesis
    - Choose RISC-V core to use for design
    - Find SPI core to use for design
  - Nathaniel Fraly
    - Research RISC-V core options for Yosys implementation
    - Continue Yosys familiarization
    - Look into power save of pure RTL implementation - low prio
  - Riley Cox
    - Continue Yosys familiarization
    - Research RISC-V core options
  - Mohammad Alshaiji
    - Install and synthesize example file in Yosys
    - Read through IEEE papers and determine pertinent info
    - Research SPI implementation

  - Xiang Li
    - Set up WSL and run Yosys on Linux (2)
    - Read Yosys documentation, try examples (4)

- - - ■ Search for SPI IPs (4)
    - ○ Haoyang Han
        - ■ Set up WSL and run Yosys on computer(2)
        - ■ Read Yosys documentation, try examples (4)
        - ■ Begin with power monitor(4)
        - ■ Design 3D printing case（3）
- **Blocked**
    - ○ Team Blocks
        - ■ Need to find a simulator; may use the school's servers for QuestaSim for preliminary, but need to see if Yosys can simulate synthesized designs. Yosys may have one built-in
    - ○ Nathaniel Fraly
        - ■ Need to install a different Linux distro before continuing Yosys work; Rocky distro clunky. Likely switching to Debian to match Riley's WSL environment.
    - ○ Riley Cox
        - ■ Need to purchase UPduino board and be able to work with it
    - ○ Mohammad Alshaiji
        - ■ Need to migrate to Debian
    - ○ Xiang Li
        - ■ Haven't successfully run Yosys on computer
        - ■ Will try WSL and run on Linux
    - ○ Haoyang Han
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