Lattice FPGA Project Weekly Progress Report - Week 1

Report date: 2025/01/17

- **Last Week (time in hours)**
  - Team Review
    - Setting up project infrastructure
  - Nathaniel Fraly
    - Researching open-source tools for synthesis (4)
  - Riley Cox
    - Researching open-source tools for synthesis (4)
  - Mohammad Alshaiji
    - Work on PDS/L0 diagram (5)
  - Xiang Li
    - Work on PDS (5)
  - Haoyang Han
    - Work on PDS (4)
- **Next week**
  - Team Plan
    - Finish PDS, have open-source selected
  - Nathaniel Fraly
    - Finish tests with Yosys
  - Riley Cox
    - Finish tests with Yosys
  - Mohammad Alshaiji
    - Finish PDS
  - Xiang Li
    - Finish PDS
  - Haoyang Han
    - Finish PDS
- **Blocked**
  - Team Blocks
    - Waiting on additional information from Rahul
  - Nathaniel Fraly
    - N/A
  - Riley Cox
    - N/A
  - Mohammad Alshaiji
    - N/A
  - Xiang Li
    - N/A
  - Haoyang Han
    - N/A