Capstone Project Proposal

Team 9 - Lattice FPGA

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Table Of Contents:

1. Executive Summary
2. Background and Research
    Research
        Open Source Projects
        Patents, Papers, White Papers, Articles, Conference Proceedings
3. Product Design Specification
    Product Overview
    Stakeholders
    Requirements
    Specifications
    Initial product design
    Verification plans
    Risks
    Deliverables
4. Project Management Plan
    Timeline, with milestones
    Budget and Resources
    Intellectual Property Discussion
    Team
    Development Tools and Process

1. Executive Summary

The goal of this project is to develop a low-power FPGA-based system that drives an SPI-based LCD display. The system will enable users to adjust brightness and cycle through colors using two buttons, showcasing the flexibility of FPGA solutions. Our team will implement three low-power design techniques and compare the outcomes of using an Open Source FPGA toolchain with the Lattice Radiant toolchain. To ensure a reliable foundation, the team will first implement the design using the well-established Lattice Radiant toolchain to verify functionality. Once a working baseline is established, the team will explore open-source alternatives and make comparisons.

The deliverables include a fully functional prototype housed in a 3D-printed enclosure, supported by SystemVerilog code, comparative analysis reports, and visualizations of power consumption. This product will serve as a demonstration tool for Lattice Semiconductor, emphasizing the potential of FPGAs in low-power, cost-sensitive applications. Development will occur over three phases, ensuring a robust and scalable outcome.

2. Background and Research

Lattice Semiconductor is an FPGA company with headquarters in Hillsboro, Oregon. They market themselves as the low-power programmable logic leader. According to their SEC 10-Q filing on November 04, 2024, their total assets as of that date totaled $853,661,000. Their total revenues for the quarter ending in September 2024 were $127,091,000. From their investor relations statements, they describe themselves as "[solving] customer problems across the network, from the Edge to the Cloud, in the growing communications, computing, industrial, automotive, and consumer markets."(Lattice)

FPGAs serve a particular niche of the market concerned with parallel processing, high-speed processing and the ability to reconfigure hardware. Such properties are leveraged by communication, automotive, aviation, and artificial intelligence systems among others. Traditionally, FPGAs stand as an alternative to the use of ASICs and microcontrollers. For this project specifically, the sponsor is interested in evaluating the trade-offs between the Lattice Radiant toolchain and open-source alternatives through the development of an FPGA-based system that controls an SPI-based LCD screen. The system will feature user interaction via two buttons for adjusting brightness and color, housed in a 3D-printed enclosure and powered by a battery. A series of power profiles, generated during different stages of development using various low-power design techniques, will be collated to compare the impact of each toolchain on key factors such as synthesis quality, and power consumption.

The team is beginning this project without having previous work to consider within our own designs. We are leveraging a previous team's toolchain experiences, as provided by Rahul, to select the open-source toolchain that supports the Upduino board, and UltraPlus FPGA we will be using.

Research

Open Source Projects

To simplify the implementation of the project and to avoid reinventing the wheel, Open-source Verilog IPs will be used instead of relying on proprietary Lattice IP. This would also simplify the comparisons between the open source and Lattice toolchain, allowing for the reduction of influences on the final power results. opencores.org has been recommended by our industry sponsor as a suitable place to explore and obtain said IPs.

Patents, Papers, White Papers, Articles, Conference Proceedings

-The IEEE paper, Development of an FPGA based low power message displaying system using scanning technique, is an exploration conducted by Ali et al. on developing techniques for the reduction of power usage in FPGAs that interface with a screen. While the system explored in the paper is more complex than the system we intend to design, it provides inspiration on potential avenues of power reduction, and could inspire the methods we utilize in developing and tracking our power profiles and their results.

-Pong game on FPGA with CRT or LCD display and push button controls, by Szabó et al, provides a useful example on where this project can take us. It provided useful information on how we could implement the push buttons for our device such that it can interface correctly with an LCD. It also provides a suitable benchmark on our progress as we proceed through the project, i.e. developing the base product, implementing low-power techniques, and the toolchain comparison

-SystemVerilog based design and implementation of LCD Controller IP Core, by Chandran O et al., provides a suitable source for examining the considerations taken in the design of an LCD controller IP. As it is written in SystemVerilog instead of Verilog, it allows us the opportunity to enhance our understanding of FPGAs by informing us of useful techniques while leaving the burden of implementation on our team. Since the IP being designed is for an LCD controller, this will be useful in determining and visualizing our own mechanism for LCD Interfacing.

3. Product Design Specification

Product Overview

This project aims to develop an FPGA-based system that controls an SPI-based LCD screen, featuring user interaction through two buttons to adjust brightness and color. The system will be housed in a 3D-printed enclosure and powered by a battery, providing a portable and functional demonstration of FPGA capabilities.

The development process is divided into several stages, with progress and results determining the final product phase achieved by the Capstone Fair at the end of Spring term. The first stage focuses on creating a fully operational product without implementing any power-saving techniques, serving as the foundation for subsequent enhancements. In the second stage, functionality will be expanded to enable the display of meaningful text on the LCD screen. The third stage will shift attention to integrating and evaluating three distinct low-power design implementations, comparing their impact on energy consumption and performance. Additionally, this phase will assess the Lattice Radiant toolchain against open-source alternatives, focusing on ease of use, workflow efficiency, synthesis quality, and power performance. If progress advances ahead of schedule, we will consider further enhancing the display capabilities to support more complex visual outputs.

The ultimate goal of this project is to analyze and compare the strengths and weaknesses of the Lattice Radiant toolchain and open-source alternatives. This comparison will focus on key aspects such as ease of use, workflow efficiency, synthesis quality, and power consumption, providing a detailed evaluation of the trade-offs between the two toolchains.

Stakeholders

1. Industry sponsor : Rahul Koche

2. Faculty Advisor : Roy Kravitz
3. User : Lattice Semiconductor
4. Project team: Nathaniel Fraly, Riley Cox, Mohammad Alshaiji, Xiang Li, Haoyang Han

Requirements

The main priority of this project is to be able to utilize off-shelf products provided by Lattice FPGA to complete a proof of concept design for an FPGA Color-mixing screen. This can be used in conjunction with an LCD screen utilizing SPI to display color/pattern changes on the press of a button, and contrast/brightness adjustments with the press of another. The proposed boards to be used are the UPduino boards using Lattice UltraPlus ICE40UP5K FPGA.

The project will start by developing a functional product without incorporating power-saving techniques, ensuring functionality. Three distinct low-power design implementations will be integrated and tested to assess their impact on performance and energy efficiency. Then a comparison of the Lattice Radiant and open-source toolchains will be conducted, evaluating usability, workflow efficiency, and synthesis quality. After finished, the product will be refined and enhanced with additional features, completing the development process.

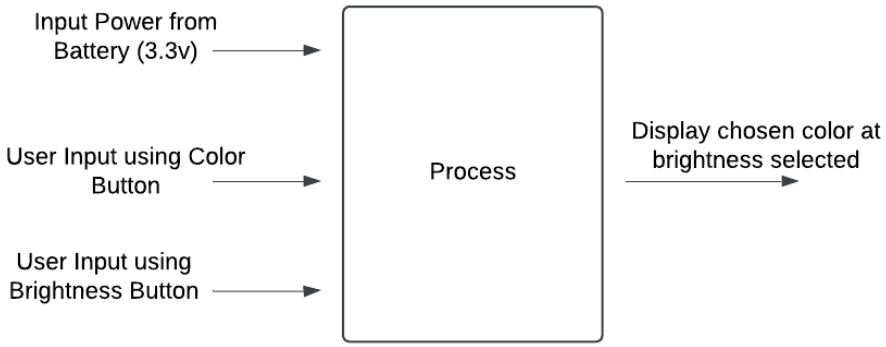
1. Must control an SPI-based LCD screen to adjust brightness and color via two buttons.
2. Must use Lattice Radiant FPGA toolchain to develop FPGA bitstream.
3. Must use at least 3 kinds of low-power design techniques.
4. Must have a working final product.
5. Must be in an enclosure.
6. Must have Phase-1 complete by April
7. Should compare the ease of use and efficiency between the open-source toolchain and the Lattice Radiant toolchain.
8. Should collect and visualize power consumption data and compare the results of the open-source toolchain and the Lattice Radiant toolchain.
9. Should be encased in a 3D-printed enclosure.
10. Should be powered by a battery.
11. May be able to show meaningful text on the screen.
12. May be able to show images on the display.
13. May be able to act as a debugging tool to show the debug messages on screen.
14. May be able to interact with other sensors.

Specifications

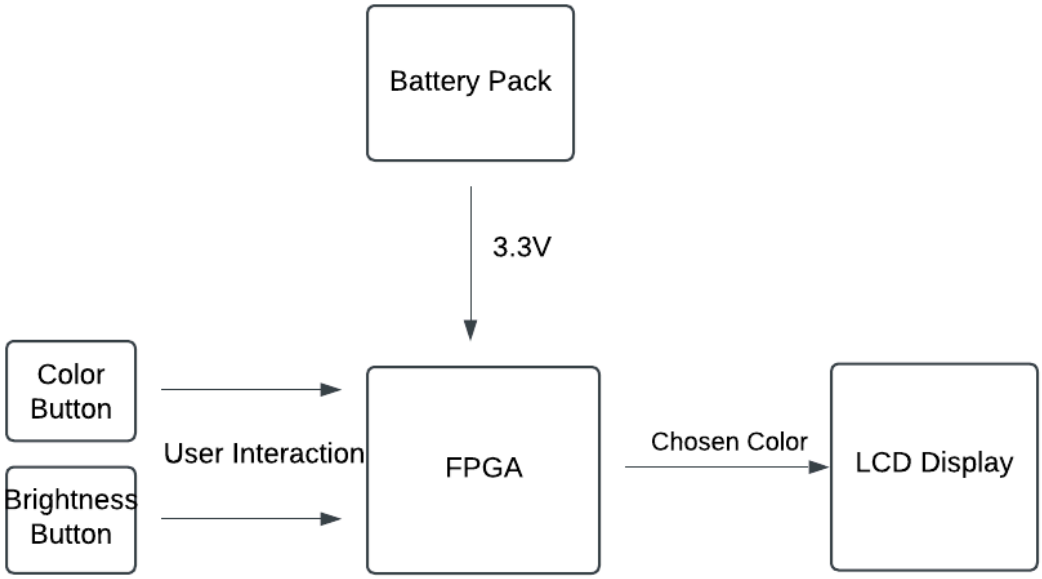
1. Must use the provided UPduino board featuring the Lattice iCE40 UltraPlus.
2. Must use Open Source FPGA toolchain to build Lattice FPGA bitstream.
3. Must use the same source code for the Open-Source FPGA toolchain and Lattice Radiant toolchain.
4. Must use Adafruit ST7735R 1.8” Color TFT LCD display with MicroSD card Breakout.
5. Should write code in Verilog.
6. May cost around $60 to produce once development is complete..

Initial product design

- Hardware architecture
    - **L0 diagram for Product:**



- **L1 Diagram for Product**:



- User interface/experience
  - At the end of phase one, the user will be able to cycle through a selection of 10-15 colors on the provided Adafruit display, with the ability to change color and brightness through the requisite buttons. This will be the base on which the low-power techniques will be applied for the examination of the two toolchains,
  - Should the techniques be properly applied and a comparison documented, there are additional avenues of functionality that could be implemented.
  - The functionality can be expanded so that it can display text. This is a useful feature as it would allow for the quick and easy display of error messages, potentially allowing the user to use the device as a debugging tool.
  - If we are further able, another avenue to explore is the display of more complex visuals on the screen, potentially allowing the user to utilize the device as a viable tester/debugger
- Other considerations
  - At least 3 kinds of low power techniques should be used
  - Collect and analyze power consumption data

Verification plans

Here is a proposed Verification test for "must" requirements:

- For the functioning of the buttons, the brightness button should increase the brightness by an increment on each button press. When the maximum brightness level is reached, subsequent presses of the button should decrease the brightness. The color button should cycle through all color selections available, and when those are done, should cycle back to the first color selection.
- The comparison and summary of the power profiles will act to ensure that each power profile utilizes at least three techniques. To confirm this, each technique will be initially implemented on its own to compare against the expected result from three implementations at a time.
- To confirm the viability of the toolchain analysis, special attention will be given to ensure that the code that is fed through both the open-source and Lattice tool is the same, containing the same IPs. The testing of the buttons and device reliability must be conducted the same for both. This is accomplished using a specific written out procedure to ensure the proper accounting of steps.
- The accuracy of resulting power consumption visualizations must be confirmed. This will be done in accordance with the specifications determined by the mechanism of data collection. It would also be prudent to have a base configuration without any power-reduction techniques to act as a control for the comparisons to be made.
- These verification steps will occur through the use of a testbench in a simulation environment (Radiant) to verify the expected outcomes. Special considerations must be given to the testcases, ensuring that all edge-cases and special cases are accounted for. These testcases will consist of a variety of "good" and "bad" cases to ensure the proper functionality of our implementation and that it meets the specifications and requirements above.

Risks

As things currently stand, our biggest risk is in ensuring that there are no issues that result from using certain SystemVerilog constructs in conjunction with the open-source toolchain Yosys, or its associated ICE40 toolchain. This should be taken into consideration when identifying suitable IP cores. PnR issues might be of concern, though we believe this to be overstated for our use-case.

Another issue is the large scope of the project, as the product is intended to be polished enough to be showcased by the industry sponsor in trade shows. To alleviate the possible issues this can cause, the full project has been divided into three stages. These stages act as checkpoints we can fall back to if our progress on a particular stage doesn't align with our expectations. As such, the product should always be transferable to future teams should the work not be completed.

Deliverables

1. A fully working SPI LCD display which uses FPGA for color-changing, two buttons for functionality and all inside a 3-D printed shell.
2. RTL source code, ideally in Verilog
3. Associated apps or software for LCD display controlling
4. Report comparing the usage of Open Source toolchain and Lattice Radiant toolchain
5. Reports with statistics and graphs on power consumption of different solutions
6. User Manual
7. Bill of Materials
8. Project proposal
9. Weekly Progress Reports
10. Final report
11. ECE Capstone Poster Session Poster

12. Documentations and source code stored in Github repository

4. Project Management Plan

Timeline, with milestones

Refer to capstone.pdf on the github repository to examine a Preliminary Gantt Chart depicting the proposed timeline of the project.

Budget and Resources

Our project operates within a budget constraint set by the industry sponsor, aiming for a final product cost of no more than $60. Key components of the project include the UPduino board with iCE40 UltraPlus FPGA and the Adafruit 1.8" Color TFT LCD display for $19.95. To stay within the remaining $7, we will carefully manage the costs of additional components such as buttons, wires, batteries, and the enclosure.

We are provided 2 sets of Adafruit LCD display with UPduino Board by our industry sponsor, and we'll use our own computer resources for program development.

Our work will primarily take place in the PSU Engineering Building (EB) and University Pointe (UP) for meetings and development. Additionally, the Electronics Prototyping Lab (EPL) will be a resource for soldering, power consumption testing, and 3D printing.

Intellectual Property Discussion

All IP is owned by the industry sponsor and is to be utilized and licensed as they see fit, within the bounds of any open-source components being used.

Team

- Nathaniel Fraly
  - Skills: (System)Verilog, leadership, adaptability
  - Responsibilities: Team leader.
    Final decision-making, guiding the team, communicating with the industry sponsor and faculty advisor, and contributing to Verilog development.
- Mohammad Alshaiji
  - Skills: Documentation, Verilog 2001, debug, soldering, research
  - Responsibilities: Doing documentation, contributing to SystemVerilog development, and supporting debugging tasks.
- Riley Cox
  - Skills: (System)Verilog, flexibility, research
  - Responsibilities: Conducting research, supporting design and synthesis improvements, managing GitHub Repo and contributing to Verilog development.
- Xiang Li
  - Skills: (System)Verilog, debug
  - Responsibilities: Managing project documentation and contributing to Verilog development.
- Haoyang Han
  - Skills: Low power reqs, physical layout, soldering
  - Responsibilities: Handling low-power requirements, physical layout, 3D printing, and contributing to Verilog development.

Development Tools and Process

Our development process will follow a spiral methodology, emphasizing iterative cycles of planning, risk assessment, development, and evaluation. We will use this methodology to address uncertainties and refine our project incrementally at every stage. Each cycle will focus on a specific set of objectives to ensure steady progress toward the goal. We will develop prototypes and perform testing during each iteration, followed by evaluations with the team, industry sponsor, and faculty advisor to gather feedback and refine our approach.

Each spiral cycle will include planning objectives, prototyping, and risk assessments. Team members will work on individual branches in GitHub, contributing to development while ensuring quality through a pull request workflow.

Collaboration will be supported by Discord for in-team communication and virtual meetings. GitHub will be our central platform for storing code, documents, and version control. Google Drive will serve as the repository for shared documents, and professional communications with stakeholders will be conducted via email, with Zoom for virtual meetings.

We will use SystemVerilog as the primary programming language for FPGA design and hardware description. Our FPGA toolchain includes an Open Source toolchain using Yosys and the Lattice Radiant toolchain.

Signature

The following signatures confirm agreement and acknowledgment of the project proposal details as outlined in this document.

Name	Signature
Rahul Koche	
Roy Kravitz	
Nathaniel Fraly	N. Fraly
Riley Cox	R. Cox
Mohammad Alshaiji	M. Alshaiji
Xiang Li	X. Li
Haoyang Han	H. Han