Lattice FPGA Project Weekly Progress Report - Week 12

Report date: 2025/3/27

- **Last Week (time in hours)**
  - Team Review
    - Get SPI integrated with Yosys core while trying to get Radiant core setup
  - Nathaniel Fraly
    - Attempt Icicle mods for Radiant (15)
    - Setup issue tracking on Github to improve Github use (3)
  - Riley Cox
    - Attempt Icicle mods for Radiant (15)
    - Integrate SPI with Yosys Icicle version (3)
  - Mohammad Alshaiji
    - Integrate SPI with Yosys Icicle version (6)
  - Xiang Li
    - Learned about icicle (1)
  - Haoyang Han
    - Study the best models and learn how to draw the pivot point between the top and bottom of the box.（6）
- **Next week**
  - Team Plan
    - Finish full system yosys integration; talk to Roy and Rahul about path forward w/ Radiant
  - Nathaniel Fraly
    - Work on integrating two button interfaces (pwm and brightness)
  - Riley Cox
    - Assist with integration of buttons
    - Add feedback from peer on user guide
  - Mohammad Alshaiji
    - Modify C code to attempt to turn on screen
  - Xiang Li
    - Documentation: add steps for verifying the SPI module independently
  - Haoyang Han
    - Improve the 3D modeling and start building the anti-shake switch circuit.
- **Blocked**
  - Team Blocks
    - Radiant and Icicle do not agree with each other; can’t integrate until this is solved
  - Nathaniel Fraly
    - Radiant full blocked for now, will move forward on Yosys integration
  - Riley Cox
    - none
  - Mohammad Alshaiji
    - none
  - Xiang Li
    - none
  - Haoyang Han
    - none

Lattice FPGA Project Weekly Progress Report - Week 13

Report date: 2025/04/03

- **Last Week (time in hours)**
  - Team Review
    - SPI integration complete with Yosys toolchain
  - Nathaniel Fraly
    - Met with Roy regarding Radiant issues (1)
    - Attempt to fix Radiant issues (1)
  - Riley Cox
    - Worked on Radiant issue (1)
    - Created GitHub Guidelines document (2)
    - Started on alternative SPI module; unit test and synthesized test show good results (12)
  - Mohammad Alshaiji
    - Continued working on integrating SPI controller (8)
    - Debugging Logic Analyzer (1)
    - Created merged c program for screen testing (1)
  - Xiang Li
    - Finished structure of SPI verification doc (2)
    - Research on functions in ST3375 Adafruit library (3)
  - Haoyang Han
    - Design push-button circuits（2）
    - design Shaft system in 3D modeling（4）
- **Next week**
  - Team Plan
    - Integrate user interface
  - Nathaniel Fraly
    - Add in button, PWM, and color change modules
  - Riley Cox
    - Help with LCD screen C program
    - Integrate button and pwm to icicle
  - Mohammad Alshaiji
    - Modify Screen program to function with pwm and button
    - Continue with unit and systemic testing of SPI controller
  - Xiang Li
    - Refine C code as needed
  - Haoyang Han
    - Completed 3D modeling (Version 3.0)
- **Blocked**
  - Team Blocks
    - Radiant still not working with icicle
    - Rahul still hasn’t dropped off hardware
    - Logic analyzers on order for Riley and Nathan
  - Nathaniel Fraly
    - Radiant. Close to beginning attempts at the RV32 IP block for Radiant.
  - Riley Cox
    - Still having Radiant issues

- Mohammad Alshaiji
  - N/A
- Xiang Li
  - N/A
- Haoyang Han
  - N/A

Lattice FPGA Project Weekly Progress Report - Week 14

Report date: 2025/04/10

- **Last Week (time in hours)**
  - Team Review
    -
  - Nathaniel Fraly
    - Attempting to integrate button module (4)
    - Rework button module for simpler integration (2)
    - Test simpler button module to find out it isn't any simpler (3)
  - Riley Cox
    - Integrating button module (4)
    - Troubleshoot button module changes via testbench and on board (4)
  - Mohammad Alshaiji
    - Integrated SPI Module (1)
    - Created unified testing program for Screen testing (1)
    - Prep for program integration with Button module (1)
  - Xiang Li
    - New C functions on text display on screen (6)
  - Haoyang Han
    - Complete 3D Printing (8)
- **Next week**
  - Team Plan
    -
  - Nathaniel Fraly
    - Get buttons working so phase 1 is complete
    - Get started on Radiant troubleshooting again
  - Riley Cox
    - Finish integrating button module
  - Mohammad Alshaiji
    - Integrate Button module with Screen Program
    - Help Xiang with text display
  - Xiang Li
    - Debug and make sure the text display functions work
  - Haoyang Han
    - Start PCB Design
- **Blocked**
  - Team Blocks
    -
  - Nathaniel Fraly
    - No screen, can't test actual output
  - Riley Cox
    - Button team only has one screen making testing slow
  - Mohammad Alshaiji
    - Waiting for Button module to be ready
  - Xiang Li
    -
  - Haoyang Han

Lattice FPGA Project Weekly Progress Report - Week 15

Report date: 2025/04/17

- **Last Week (time in hours)**
  - Team Review
    -
  - Nathaniel Fraly
    - Troubleshoot button module (17)
  - Riley Cox
    - Troubleshoot button module (17)
  - Mohammad Alshaiji
    - Troubleshooting Radiant port (7)
  - Xiang Li
    - Find out battery power supply options for Updiuno board (4.5)
  - Haoyang Han
    - Start designing PCB (4)
    - Complete the final 3D printed version（3）
- **Next week**
  - Team Plan
    -
  - Nathaniel Fraly
    - Finish up button module integration
  - Riley Cox
    - Finish button module integration
  - Mohammad Alshaiji
    - Finish porting core to Radiant
  - Xiang Li
    - Order the power components
    - Help with solving the incompatibility of icicle on Radiant
  - Haoyang Han
    - Continue to design PCB
- **Blocked**
  - Team Blocks
    -
  - Nathaniel Fraly
    - No screen; Rahul meeting on Monday to resolve issue
  - Riley Cox
    -
  - Mohammad Alshaiji
    -
  - Xiang Li
    -
  - Haoyang Han
    -

Lattice FPGA Project Weekly Progress Report - Week 16

Report date: 2025/04/24

- **Last Week (time in hours)**
  - Team Review
    - Continue phase 1 finalizing
  - Nathaniel Fraly
    - Modify SPI module to support C transaction through button press (3)
    - Add memory locations for C program to read a button press and new color data (5)
  - Riley Cox
    - Modify SPI module to support C transaction through button press (3)
    - Add memory locations for C program to read a button press and new color data (5)
  - Mohammad Alshaiji
    - Debug issues with Radiant Port of icicle (8)
  - Xiang Li
    - Documentation: Test Plan (4)
  - Haoyang Han
    - Redesigned low active anti-shake button circuitDesigning PCB (2)
    - Designing PCB (4)
- **Next week**
  - Team Plan
    -
  - Nathaniel Fraly
    - Get board ready for demo
  - Riley Cox
    - Get board ready for demo
  - Mohammad Alshaiji
    -
  - Xiang Li
    - PowerPoint for demo
  - Haoyang Han
    - Continue to adjust the design of PCB
- **Blocked**
  - Team Blocks
    -
  - Nathaniel Fraly
    -
  - Riley Cox
    -
  - Mohammad Alshaiji
    -
  - Xiang Li
    -
  - Haoyang Han
    -

Lattice FPGA Project Weekly Progress Report - Week 17

Report date: 2025/05/01

- **Last Week (time in hours)**
  - Team Review
    - Finishing up final touches on phase 1
  - Nathaniel Fraly
    - Soldered protoboard for demo (3)
  - Riley Cox
    - Assisted with soldering (3)
  - Mohammad Alshaiji
    - Worked on Porting Core to Radiant (6)
  - Xiang Li
    - PPT for DEMO (4)
  - Haoyang Han
    - Designing PCB (5)
- **Next week**
  - Team Plan
    - Start documentation, finalize Radiant port, test hardware for PCB design
  - Nathaniel Fraly
    - Test battery connection
  - Riley Cox
    - Update user guide on GitHub
  - Mohammad Alshaiji
    - Continue Porting Core
  - Xiang Li
    - Start Final Report
  - Haoyang Han
    - Continue designing the PCB
- **Blocked**
  - Team Blocks
    -
  - Nathaniel Fraly
    - Need to catch up on other class
  - Riley Cox
    - Need to catch up on other class
  - Mohammad Alshaiji
    -
  - Xiang Li
    -
  - Haoyang Han
    -

Lattice FPGA Project Weekly Progress Report - Week 18

Report date: 2025/05/08

- **Last Week (time in hours)**
  - Team Review
    - PCB work, docs, Radiant
  - Nathaniel Fraly
    - Test single cycle reset for Yosys(1)
    - Add battery power to proto board (2)
    - Test user guide (4)
  - Riley Cox
    - Implement single cycle reset for Yosys (2)
    - Test and update user guide (5)
  - Mohammad Alshaiji
    - Fixed PLL timing issues for icicle core and continued on radiant port (5)
  - Xiang Li
    - Organize and start drafting the documents (3)
  - Haoyang Han
    - Design PCB (5)
- **Next week**
  - Team Plan
    - Test PCB design, docs, Radiant
  - Nathaniel Fraly
    - Assist with PCB as needed
    - Assist with Radiant as needed
  - Riley Cox
    - Continue finalizing user guide
    - Assist with Radiant as needed
  - Mohammad Alshaiji
    - Continue working on Radiant port
    - Provide details for documentation when needed
  - Xiang Li
    - Draft the final report
  - Haoyang Han
    - Finished PCB
- **Blocked**
  - Team Blocks
    - Radiant Radiant Radiant
  - Nathaniel Fraly
    - Need to catch up on ECE510 project
  - Riley Cox
    - Need to catch up on ECE510 project
  - Mohammad Alshaiji
    - Radiant
  - Xiang Li
    - N/A
  - Haoyang Han
    - Problem with routing the traces

Lattice FPGA Project Weekly Progress Report - Week 19

Report date: 2025/05/15

- **Last Week (time in hours)**
  - Team Review
    - Focused on Docs, PCB, and Radiant
  - Nathaniel Fraly
    - Reviewed user guide and gave input(1)
    - Worked on PCB design (3)
  - Riley Cox
    - Worked on first iteration of the PCB design (4)
    - Helped Mohammad reduce the number of warnings received in Radiant port (3)
    - Updated user guide on GitHub(1)
  - Mohammad Alshaiji
    - Continued work on port of core to Radiant. Reduced number of warnings from 118 to 42. Work remains to be done (7)
  - Xiang Li
    - Finished the structure of final report, and got reviewed by Roy (5)
  - Haoyang Han
    - Designing PCB（8）
- **Next week**
  - Team Plan
    - Continue to work on PCB, Docs, and Radiant
  - Nathaniel Fraly
    - Continue to help with PCB design
  - Riley Cox
    - Continue working on PCB design implementing critiques from Andrew's design review
  - Mohammad Alshaiji
    - Continue working on Radiant port
  - Xiang Li
    - Keep on the documentation process
  - Haoyang Han
    - After getting all the parameters of the PCB, make a 3D print.
- **Blocked**
  - Team Blocks
    - N/A
  - Nathaniel Fraly
    -
  - Riley Cox
    -
  - Mohammad Alshaiji
    -
  - Xiang Li
    -
  - Haoyang Han
    -

Lattice FPGA Project Weekly Progress Report - Week 20

Report date: 2025/05/23

- **Last Week (time in hours)**
  - Team Review
    - Finished PCB and send out for design
    - Progress on Radiant Port
    - Drafting final docs
  - Nathaniel Fraly
    - Coordinated PCB design review with Andrew
    - Took notes during PCB design review meeting(2)
    - Helped with PCB design (1)
  - Riley Cox
    - Finished PCB design and ordered it through Osh Park (6)
  - Mohammad Alshaiji
    - Continued work on Radiant Port. Was able to confirm that program was loaded, that pc was coming out of reset, next_pc calculated, and ALU operations were occurring. Mem stage not working correctly. Brightness button functions(8)
  - Xiang Li
    - Making progress on the draft of the Final report and other documents (6)
  - Haoyang Han
    - Create 3D models（6）
- **Next week**
  - Team Plan
    - Finish the product and documents
  - Nathaniel Fraly
    - Solder and populate PCB when it arrives
  - Riley Cox
    - Solder and populate PCB board when it arrives
  - Mohammad Alshaiji
    - Continue Radiant Port
  - Xiang Li
    - Finish up the final report and make it reviewed
  - Haoyang Han
    - Continue to improve the 3D model
- **Blocked**
  - Team Blocks
    - Waiting on PCB
  - Nathaniel Fraly
    - Waiting on PCB
  - Riley Cox
    - Waiting on PCB
  - Mohammad Alshaiji
    - N/A
  - Xiang Li
    - N/A
  - Haoyang Han
    - N/A

Lattice FPGA Project Weekly Progress Report - Week 21

Report date: 2025/05/30

- **Last Week (time in hours)**
  - Team Review
    - Soldering the final product
    - Radiant Port progress
    - Draft final report
  - Nathaniel Fraly
    - Finished soldering and populating PCB (12)
  - Riley Cox
    - Finished soldering headers on Upduino, created debounce in the button module (12)
  - Mohammad Alshaiji
    - Continued work on Radiant Port (8)
  - Xiang Li
    - Finish up the draft of final report and send out for review (6)
  - Haoyang Han
    - Improve the 3D model and print out the enclosure(6)
- **Next week**
  - Team Plan
    - Finish the poster
  - Nathaniel Fraly
    - Helped with poster
  - Riley Cox
    - Helped with poster
  - Mohammad Alshaiji
    - Continue final attempt at Radiant Port
    - Aid in poster Design
  - Xiang Li
    - Design the poster
  - Haoyang Han
    - Helped with poster
- **Blocked**
  - Team Blocks
    - N/A
  - Nathaniel Fraly
    - N/A
  - Riley Cox
    - N/A
  - Mohammad Alshaiji
    - N/A
  - Xiang Li
    - N/A
  - Haoyang Han
    - N/A

Lattice FPGA Project Weekly Progress Report - Week 22

Report date: 2025/06/06

- **Last Week (time in hours)**
  - Team Review
    - Have the poster finished
  - Nathaniel Fraly
    - Helped with poster (2)
  - Riley Cox
    - Help with poster design (2)
  - Mohammad Alshaiji
    - Help with Poster (3)
  - Xiang Li
    - Finish the design of poster (6)
  - Haoyang Han
    - Helped with poster (2)
- **Next week**
  - Team Plan
    - Finish up documentation
  - Nathaniel Fraly
    - Finish up documentation
  - Riley Cox
    - Finish up documentation
  - Mohammad Alshaiji
    - Finish documentation
  - Xiang Li
    - Revise the poster based on feedbacks, finish up final report
  - Haoyang Han
    - Finish documentation
- **Blocked**
  - Team Blocks
    - N/A
  - Nathaniel Fraly
    - N/A
  - Riley Cox
    - N/A
  - Mohammad Alshaiji
    - N/A
  - Xiang Li
    - N/A
  - Haoyang Han
    - N/A