Lattice FPGA Project Weekly Progress Report - Week 20

Report date: 2025/05/23

- **Last Week (time in hours)**
  - Team Review
    - Finished PCB and send out for design
    - Progress on Radiant Port
    - Drafting final docs
  - Nathaniel Fraly
    - Coordinated PCB design review with Andrew
    - Took notes during PCB design review meeting(2)
    - Helped with PCB design (1)
  - Riley Cox
    - Finished PCB design and ordered it through Osh Park (6)
  - Mohammad Alshaiji
    - Continued work on Radiant Port. Was able to confirm that program was loaded, that pc was coming out of reset, next_pc calculated, and ALU operations were occurring. Mem stage not working correctly. Brightness button functions(8)
  - Xiang Li
    - Making progress on the draft of the Final report and other documents (6)
  - Haoyang Han
    - Create 3D models（6）
- **Next week**
  - Team Plan
    - Finish the product and documents
  - Nathaniel Fraly
    - Solder and populate PCB when it arrives
  - Riley Cox
    - Solder and populate PCB board when it arrives
  - Mohammad Alshaiji
    - Continue Radiant Port
  - Xiang Li
    - Finish up the final report and make it reviewed
  - Haoyang Han
    - Continue to improve the 3D model
- **Blocked**
  - Team Blocks
    - Waiting on PCB
  - Nathaniel Fraly
    - Waiting on PCB
  - Riley Cox
    - Waiting on PCB
  - Mohammad Alshaiji
    - N/A
  - Xiang Li
    - N/A
  - Haoyang Han
    - N/A