Lattice FPGA Project Weekly Progress Report - Week 18

Report date: 2025/05/08

- **Last Week (time in hours)**
  - Team Review
    - PCB work, docs, Radiant
  - Nathaniel Fraly
    - Test single cycle reset for Yosys(1)
    - Add battery power to proto board (2)
    - Test user guide (4)
  - Riley Cox
    - Implement single cycle reset for Yosys (2)
    - Test and update user guide (5)
  - Mohammad Alshaiji
    - Fixed PLL timing issues for icicle core and continued on radiant port (5)
  - Xiang Li
    - Organize and start drafting the documents (3)
  - Haoyang Han
    - Design PCB (5)
- **Next week**
  - Team Plan
    - Test PCB design, docs, Radiant
  - Nathaniel Fraly
    - Assist with PCB as needed
    - Assist with Radiant as needed
  - Riley Cox
    - Continue finalizing user guide
    - Assist with Radiant as needed
  - Mohammad Alshaiji
    - Continue working on Radiant port
    - Provide details for documentation when needed
  - Xiang Li
    - Draft the final report
  - Haoyang Han
    - Finished PCB
- **Blocked**
  - Team Blocks
    - Radiant Radiant Radiant
  - Nathaniel Fraly
    - Need to catch up on ECE510 project
  - Riley Cox
    - Need to catch up on ECE510 project
  - Mohammad Alshaiji
    - Radiant
  - Xiang Li
    - N/A
  - Haoyang Han
    - Problem with routing the traces