

Lattice FPGA Project Weekly Progress Report - Week 16

Report date: 2025/04/24

- **Last Week (time in hours)**

- Team Review
 - Continue phase 1 finalizing
- Nathaniel Fraly
 - Modify SPI module to support C transaction through button press (3)
 - Add memory locations for C program to read a button press and new color data (5)
- Riley Cox
 - Modify SPI module to support C transaction through button press (3)
 - Add memory locations for C program to read a button press and new color data (5)
- Mohammad Alshaiji
 - Debug issues with Radiant Port of icicle (8)
- Xiang Li
 - Documentation: Test Plan (4)
- Haoyang Han
 - Redesign low active anti-shake button circuit (2)
 - Designing PCB (4)

- **Next week**

- Team Plan
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- Nathaniel Fraly
 - Get board ready for demo
- Riley Cox
 - Get board ready for demo
- Mohammad Alshaiji
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- Xiang Li
 - PowerPoint for demo
- Haoyang Han
 - Continue to adjust the design of PCB

- **Blocked**

- Team Blocks
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- Nathaniel Fraly
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- Riley Cox
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- Mohammad Alshaiji
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- Xiang Li
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- Haoyang Han
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