Lattice FPGA Project Weekly Progress Report - Week 19

Report date: 2025/05/15

- **Last Week (time in hours)**
  - Team Review
    - Focused on Docs, PCB, and Radiant
  - Nathaniel Fraly
    - Reviewed user guide and gave input(1)
    - Worked on PCB design (3)
  - Riley Cox
    - Worked on first iteration of the PCB design (4)
    - Helped Mohammad reduce the number of warnings received in Radiant port (3)
    - Updated user guide on GitHub(1)
  - Mohammad Alshaiji
    - Continued work on port of core to Radiant. Reduced number of warnings from 118 to 42. Work remains to be done (7)
  - Xiang Li
    - Finished the structure of final report, and got reviewed by Roy (5)
  - Haoyang Han
    - Designing PCB（8）
- **Next week**
  - Team Plan
    - Continue to work on PCB, Docs, and Radiant
  - Nathaniel Fraly
    - Continue to help with PCB design
  - Riley Cox
    - Continue working on PCB design implementing critiques from Andrew's design review
  - Mohammad Alshaiji
    - Continue working on Radiant port
  - Xiang Li
    - Keep on the documentation process
  - Haoyang Han
    - After getting all the parameters of the PCB, make a 3D print.
- **Blocked**
  - Team Blocks
    - N/A
  - Nathaniel Fraly
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  - Riley Cox
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  - Mohammad Alshaiji
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  - Xiang Li
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  - Haoyang Han
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