Logisim Decoder and Multiplexer

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Diagram, schematic

Description automatically generated This paper is focused on the various aspects and information regarding binary decoders and binary multiplexers. This paper will demonstrate the functionality of both a 3-pin input decoder and its evolution into a multiplexer through the inclusion of screen captures from a lab environment as well as a discussion of the application of both decoders and multiplexers. To be able to build a register from gates, first the purpose of each circuit must be understood. A decoder is designed to take data as input from a specific number of input pins and output the data from one of two to the n power of outputs. One use of a decoder is to decode instructions from various memory locations on chips and circuits to pass on to other infrastructure (Takahashi, Sekine, and Yokoyama, 2009, p. 71-72). The multiplexer acts similarly to the decoder save for the fact that it includes 2 to the n additional inputs mapped to only one output. The multiplexer is essentially a switch for many inputs and allows data through a path when that path’s code is selected but can be used in any circuit where one output is required from a specified input (Thapliyal and Srinivas, 2005,). Now that the purpose of the decoder and the multiplexer have been described, their functionality can be demonstrated. Here we can see these circuits in action. At this point the multiplexer on the right of the image can be ignored. The decoder on the left of the image currently depicts a state of no input resulting in the output of NOT A, NOT B, and NOT C. If we instead choose inputs, say A and B, we should return the output A, B, and NOT C. We see in the next image that it the case.

Diagram, schematic

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If we choose another set of inputs as a code for the output, we should see another matching output. This time we will choose just B. As expected, the output is now B, NOT A, and NOT C. This system works for any code entered the input pins.

Diagram, schematic

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Now that the decoder is confidently understood, we will move on to the multiplexer and its functionality. First, we start with a blank multiplexer as pictured above and add a code into the code input pins.

Diagram, schematic

Description automatically generated

The multiplexer has B, C, and NOT A as inputs, but there is no output. As is similar to a switch, the code pathway is now unlocked, or the circuit is closed, and data can flow through that path.

Diagram, schematic

Description automatically generated

Diagram, schematic

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We see that once the path is activated, so is the output. As the decoder has shown that different paths can be specified, the multiplexer works the same way, only allowing the specific path to pass data through. If we were to use any other input instead of B, C, and NOT A the output would remain zero. The importance of this is that circuits that pass codes and data to other circuits to receive the data along a bus will often use this convention of logical path switching (Intel Corporation, 1990, p. 7). Understanding how the AND gates formed a two to the n factor series of outputs is critical to understanding the functionality of decoders and multiplexers.

**References**

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