Premier University

Department of CSE

5th Semester, Fall 2024

Complex Engineering Problem

Course Title: Computer Organization Architecture,

Course Code: CSE 3737 Course Outcome: CO2, Total Marks: 10

Problem: Designing a Pipelined Processor for a Simple Instruction Set Architecture

You are tasked with designing a pipelined processor for a simple instruction set architecture (ISA) that supports basic arithmetic and logical operations. The processor should maximize instruction throughput and minimize stalls while considering hazards that can arise in a pipelined execution.

Objectives:

Design a pipelined processor architecture that effectively utilizes instruction-level parallelism. Implement hazard detection and resolution mechanisms to handle data hazards. Minimize stalls and improve overall instruction throughput.

Investigation:

Investigate pipelining concepts, data hazards (structural, data, and control hazards), and techniques for hazard detection and resolution.

Evaluation:

Justify your processor design decisions, highlighting how the architecture addresses data hazards and improves performance.

Design:

Your solution should include the following components:

Pipeline Stages: Define the stages of the pipeline, including Fetch, Decode, Execute, Memory, and Write-back stages.

Data Hazards Handling: Describe techniques like forwarding and stalling to handle data hazards.

Hazard Detection Unit: Implement a hazard detection unit to identify and resolve hazards.

Control Unit: Explain how the control unit manages pipeline control signals and branching.

Deliverables:

Submit a detailed explanation of your pipelined processor design, including diagrams depicting pipeline stages, hazard detection, and control unit interactions.

Complex Problem-Solving Questions:

1. Does designing this pipelined processor require a solid understanding of computer organization and architecture?
2. Does the design involve trade-offs between performance optimization and complexity?
3. Is the concept of pipelining and hazard resolution well-established, or does it require creative application?
4. Are there any specific performance bottlenecks or challenges you need to consider?

   Do you need to adhere to any industry standards or guidelines for processor architecture?
5. Could there be conflicts between optimizing the pipeline for performance and maintaining correctness?

Rubrics for Assignment Marking:

Task	Criteria	Good (4-5)	Moderate (2-3)	Poor (1)
i.	Problem solution	Properly or near appropriately reasoned solution	Appropriate solution for some cases	Inappropriate or no solution
ii.	Problem analysis	In-depth analysis	Shallow analysis	Incomplete analysis