CUMEC CSiN300 Platform

Technology Handbook

Release v1.0

Chongqing United Microelectronics Center

(CUMEC)

2021.06

Document Level: (For Engineering & Quality Document) ☑ Level 1 - Manual ☐ Level 2 – Procedure/SPEC/Report ☐ Level 3 - Operation Instruction
Security Level: ☑ Security 1 - Confidential ☐ Security 2 - Restricted ☐ Security 3 - Internal

Document Change History				
Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
V1.0	1.0	2021-6-28		Initial document

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1 HANDBOOK INFORMATION

1.1 Purpose

The information in this handbook is to describe the 300nm silicon nitride photonics technology provided by CUMEC and how to use the CSiN300 technology for custom device design.

1.2 Scope

The CSiN300 process flow and the specification of process module are described in this handbook and they can be used for a wide range of applications, such as communication, biosensor, automotive and so on.

1.3 Responsibility

CUMEC will only be responsible to the process parameters which are listed in this manual, but not guarantee any device or circuit performance.

1.4 Confidential

This CUMEC CSiN300 technology handbook is only release to customers who has signed NDA for their silicon nitride photonics design with CUMEC. It should be kept in safe and secure location.

1.5 Legal disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or advise given herein, any typical values stated herein and/ or any information regarding the application of the devices, hereby disclaims all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

2 CSIN300 TECHNOLOGY OVERVIEW

CSiN300 is the silicon nitride photonics developed by Chongqing United Microelectronics Center (CUMEC). It is based on 200mm silicon substrate with 4.4μm bottom oxide, 300nm top silicon nitride and 3.5μm top oxide cladding. CSiN300 can provide the full platform silicon nitride photonics devices, including passive devices, thermal-optic phase shifter.

The process available in CSiN300:

- 1 step silicon nitride etching
- 1 level metal including heater
- Deep silicon etching

Fig 1 shows the devices available in CSiN300 technology. PDKs can provide a series of library devices, and users can complete custom device designs according to design rules.

CUMEC also provides optical and electrical packaging service, including FA packaging, DC and RF wire bonding.

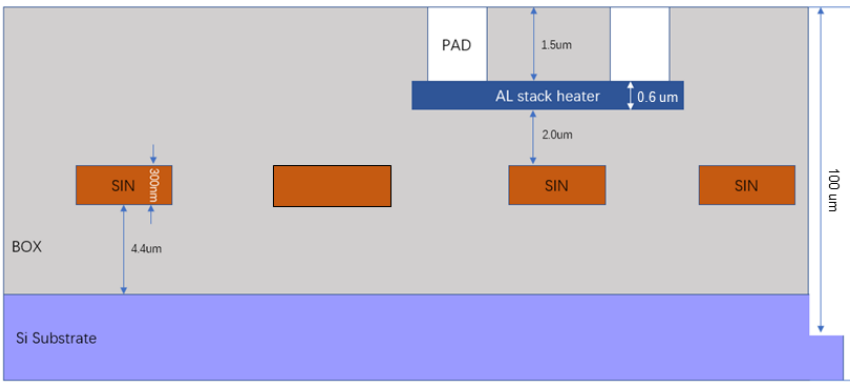

Fig. 1 Devices available (only for illustration, the size showed in this figure does not mean the real size of devices)

Layer	Thickness [μm]	Refractive index @1550nm	Remarks
Bottom oxide (BOX)	4.4	1.45	High transparency layer. SiO2 based material.
Top oxide (TOX)	3.5	1.45	High transparency layer. SiO2 based material.
Waveguide thickness	0.3	1.95	High quality low absorption nitride material. Defined by process module.
Substrate thickness	725	-	Si substrate

Refractive indices of Si_3N_4, the guiding material, and SiO_2, the clad material, are given in the Fig2.

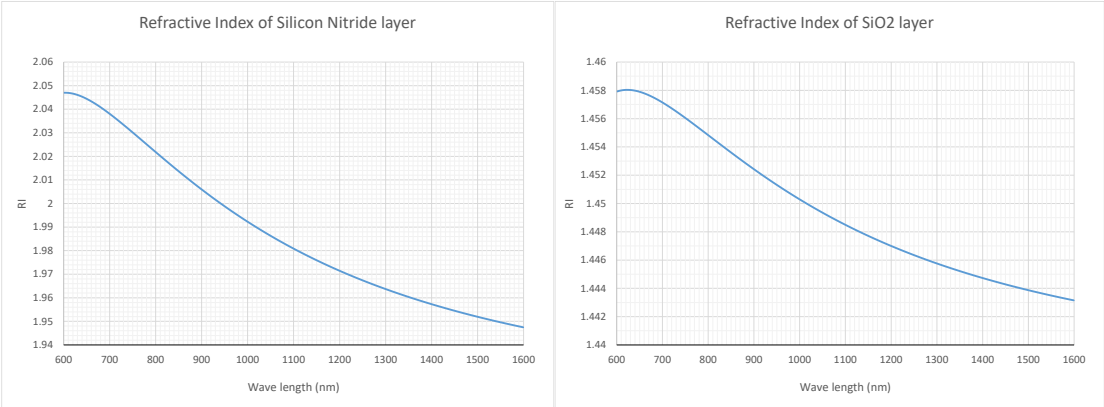

Fig.2 Material characteristics

The etched waveguide profile with side angle 87° is shown in Fig3.

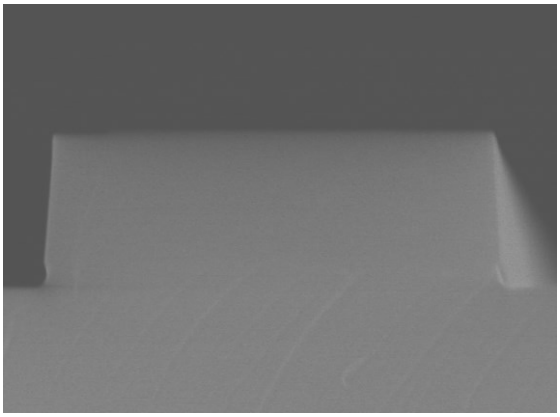

Fig.3 SEM picture of strip waveguide

3 LAYOUT DESIGN

3.1 General rules

- The layout must be submitted in GDSII format.
- Data grid must be set to 0.001μm
- Layer definition in 4.4 must be followed in layout design
- Use template provided in PDKs to begin design components/templates
- Only one top cell allowed in layout
- Use hierarchical level for design and do not flatten layout before submission
- Use uppercase or lowercase letters as initial in cell name. Do not use special symbols in cell name, such as +, -, . , / , \ , = , * , % , # , @, ! , ( )

3.2 Library cell use

There is a series of fixed cells and parameterized cells (PCells) available in CSiN300 PDK library. For fixed cells, please follow the instructions to use them.

- Do not modify the fixed cell.
- Use the right waveguide or metal definition to connect the port indicated in cell
- If you need to use the structures in library cell for custom design, please modify the cell name and ensure that the new cell name is different to the library cell name.

The PCells provided in PDKs are only to help designers simplify the design process and do **NOT** provide any guarantee of device performance. The performance guaranteed PCells will be available in next version. The descriptions of Pcells are illustrated in the “Attachment - PCells Description” at the end of the document.

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3.3 Template

Please use the templates in library to start your design. All the available templates are shown in Fig. Fig4.

- 5mm × 10mm
- 10mm × 10mm

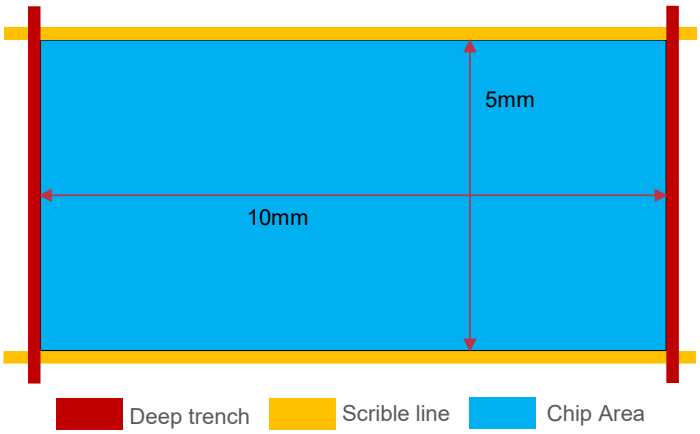


Fig. 4 Block template

3.4 GDS layers

Table. 1 defines all the layers available in CSiN300. Any layers not defined in Table. 1 will be ignored. Please find waveguides, heaters and other samples in PDKs.

Table. 1 Layer definition

No	Drawn Layer Name	Description	GDSII Layer	GDSII Data Type
1	NFE_COR	Si_3N_4 full etched waveguide: 300nm waveguide core	37	1
2	NFE_CLD	Si_3N_4 full etched waveguide: 300nm waveguide cladding	37	2
3	NFE_TRE	Si_3N_4 full etched waveguide: 300nm trenches	37	3
4	M1	Ml layer for interconnect patterning	11	0
5	PASS1	Passivation open area	60	0
6	DETCH	Deep trench area for edge coupling	64	0
7	LOGO	Logo or markers on NFE, M1	90	0
8	NOMET	No metal area	91	0
9	NOFILL	No dummy area	92	0
10	DICING	Dicing street	93	0
11	FEOL_DUM	Optical device related dummy (NFE)	94	0
12	TXT	Text label (only for indication)	96	0
13	PBOX	Black box for passive devices	97	2
14	PINREC	Pin (for port pin indications)	95	0
15	DA	Design area	100	0
16	DevRec	Device recognition	1001	0

3.5 Boolean operation

Mask layers are generated from GDS layers through boolean operations.

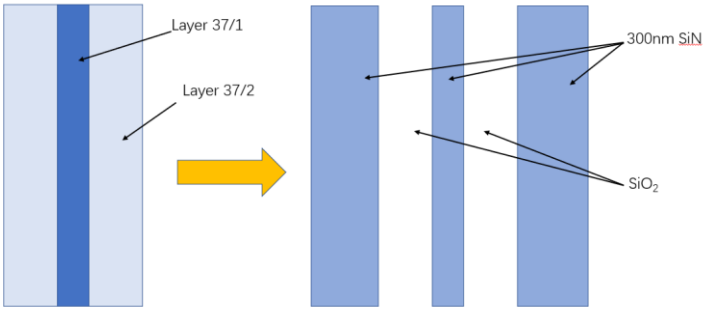
- For silicon nitride etching, shapes on clear type mask define the etching area
- For metal and heater, shapes on dark type mask define the metal line reserved

MASK	Boolean formula	Type tone
NFE	(NFE_CLD not NFE_COR) or NFE_TRE or LOGO	clear
M1	M1 or LOGO	dark
PASS1	PASS1	clear
DETCH	DETCH	clear

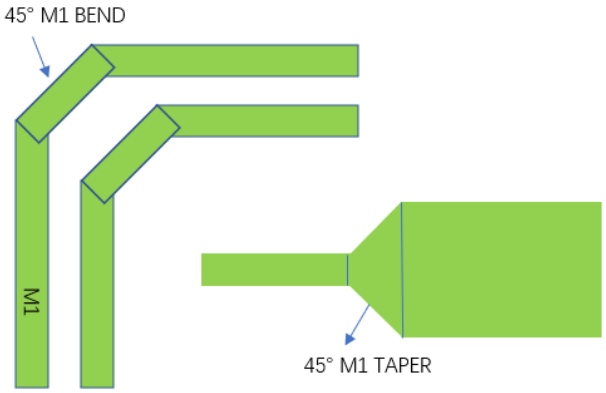
Table. 2 Mask generation

4 LAYOUT DESIGN GUIDE

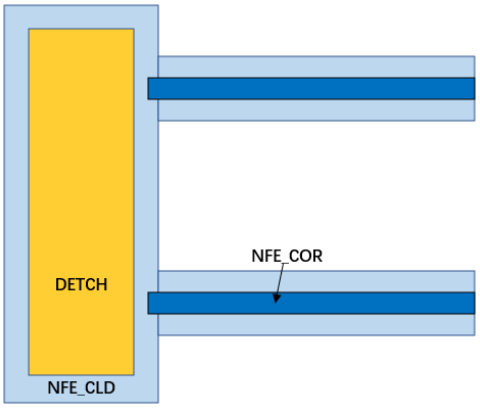
Fig5. shows design samples using the GDS layer defined in Table. 1



(a) Strip waveguide



(b) M1 bend & M1 taper



(c) DETCH used for inverted taper

Fig. 5 Layout design samples

5 LAYOUT RULE DEFINITION

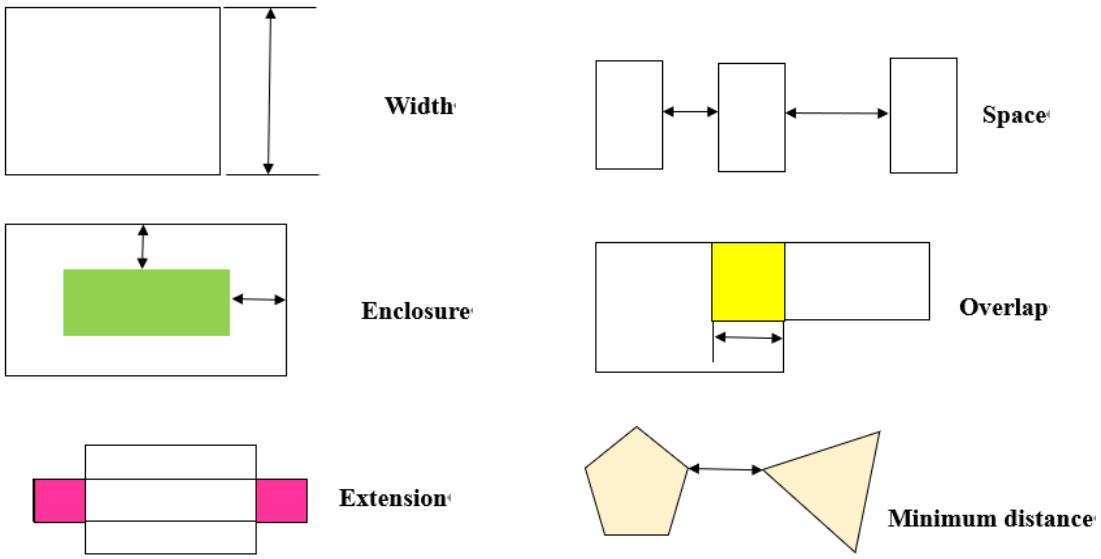


Fig.6 Rule expression definition

6 DESIGN RULE

The intersecting shapes are forbidden.

Shape with acute angle < 85° is forbidden.

6.1 NFE

The (NFE) layout layer is drawn to define strip waveguide and active area.

Rule #	Description	Layout Rule
NFE.01	Minimum width of nitride waveguides or other patterns	0.25μm
NFE.02	Minimum space between nitride waveguides or other patterns	0.22μm
NFE.03	NFE_COR outside NFE_CLD	Forbidden

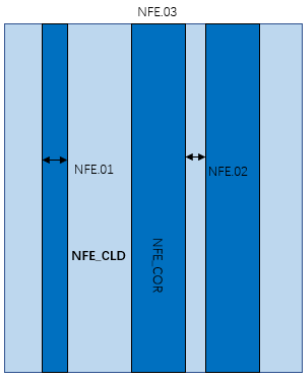


Fig. 7 NFE rules

6.2 M1

The (M1) layout layer is drawn to define metal leads and heaters.

Rule #	**Description**	Layout
M1.01	Minimum width of M1 paths or patterns	1.0 µm
M1.02	Minimum space between M1 paths or patterns	1.0 µm
M1.03	Minimum M1 to M1 space when the width of M1 is larger than 10um	5 µm
M1.04	An M1 bend should follows the 45° Manhattan routing rule.	Warning
M1.05	The connection between different M1 lines should be an 45° M1 taper	Warning

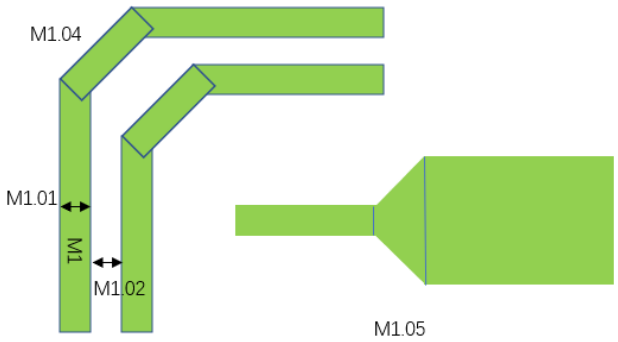


Fig. 8 M1 rules

6.3 PASS1

The (PASS1) layout layer is drawn to define passivation open area.

Rule #	**Description**	Layout
PASS1.01	Minimum width of PASS1	5µm
PASS1.02	Minimum space of PASS1	5µm
PASS1.03	Minimum enclosure of PASS1 by M1	3 µm

6.4 DETCH

The (DETCH) layout layer is drawn to define deep trench etch area for edge coupling.

Rule #	**Description**	Layout
DETCH.01	DETCH must be a rectangle with minimum width	75 μm
DETCH.02	Minimum DETCH space	20 μm
DETCH.03	DETCH layer on M1/PASS1 layers	Forbidden
DETCH.04	The minimum enclosure of DETCH by NFE_CLD	5 μm
DETCH.05	DETCH outside NFE_CLD	Forbidden
DETCH.06	The minimum distance from DETCH to NFE_COR	3 μm
DETCH.07	Overlap between DETCH and NFE_COR	Forbidden

6.5 LOGO

The (LOGO) layout layer is drawn to define LOGO on NFE, M1.

Rule #	**Description**	Layout
LOGO.01	Overlap between LOGO and NFE layer	Forbidden
LOGO.02	Overlap between LOGO and M1 layer	Forbidden
LOGO.03	Minimum space between LOGO and M1	0.5 μm
LOGO.04	Overlap between LOGO and PASS1	Forbidden

6.6 FEOL_DUM

The (FEOL_DUM) layout layer is drawn to add dummy pattern for FEOL optical layers (NFE，NSE).

Rule #	**Description**	Layout
FEOL_DUM.01	Optical layers dummy place holders are squares with a 5 um side	
FEOL_DUM.02	Minimum space between two dummy place holders	1μm
FEOL_DUM.03	Minimum distance between FEOL_DUM and NFE layer	1μm
FEOL_DUM.04	Minimum distance between FEOL_DUM and M1 layer	1μm
FEOL_DUM.05	Minimum distance between FEOL_DUM and DETCH	1μm

6.7 NOMET

The (NOMET) layout layer is drawn to define no metal area.

Rule #	**Description**	Layout
NOMET.01	Overlap between M1 and NOMET, M1 within NOMET	Forbidden
NOMET.02	Overlap between PASS1 and NOMET, PASS1 within NOMET	Forbidden

6.8 NOFILL

The (NOFILL) layout layer is drawn to define the area without dummy.

Rule #	**Description**	Layout
NOFILL.01	FEOL_DUM (NFE) within NOFILL	Forbidden

6.9 DICING

The (DICING) layout layer is drawn to define the chip's DICING street.

Rule #	**Description**	Layout
DICING.01	NFE pattern in DICING line	Warning
DICING.02	Overlap between DICING and M1	Forbidden

7 LIBRARY

7.1 Device type

Library components are available in three types:

- Fixed cells in blackbox
- Parametrized cells (PCells)

Devices provided in fixed-cell type are validated on CUMEC platform with different maturity levels. Devices provided in PCells type are to help designers simplify the construction process and do **NOT** provide any guarantee of functionality.

7.2 Library use

PINREC (layer 95/0) are used to indicate the device ports. Please use proper waveguide definition to generate the connection between devices.

Please do not modify the fixed cell, including the cell name, sub-cell names, structures, the origin, etc.

Only rotations of 90°, 180°, 270°are allowed.

7.3 Device list

The typical specifications of devices are listed in Table. 3

Table. 3 Validated devices in library

Device name	Cell name	Specification	SPEC
Waveguide	/	Propagation loss (1um width)	<= 0.1 dB/cm
Bend	/	Propagation loss (1um width, 50um radius)	<= 0.05 dB /90°
1X2 MMI	M1X2_TE_1550_SIN	Insertion loss	<= 0.3 dB
		Imbalance	±5%
2X2 MMI	M2X2_TE_1550_SIN	Insertion loss	<= 0.7 dB
		Imbalance	±10%
Edge coupler	EC_TE_1550_SIN	Insertion loss	<= 2.5 dB/facet
		1dB bandwidth	>= 40 nm
Grating coupler	GC_TE_1550_SIN	Insertion loss	<= 5.5 dB/facet
		1dB bandwidth	>= 90 nm
M1_RES	/	Metal resistance for routing and heater	0.06+/-0.01 OHM/SQ

7.4 WAVEGUIDE

8.4.1. Structure for characterization

A set of waveguides with different lengths are used to characterize the waveguide propagation loss in a specific type. The structure used for characterization is shown in Fig9.

8.4.2. Analytical method

By measuring the transmission spectrum of all the waveguide lengths, the optical waveguide propagation loss is analyzed with a cut-back method, as shown in Fig10. Please note that the transmission spectrum of grating couplers is not eliminated, and all grating couplers used in these measurements are considered identical. At the given wavelengths of 1550nm, the propagation losses are obtained from the slop of the linear fitting curves of the transmission spectrum.

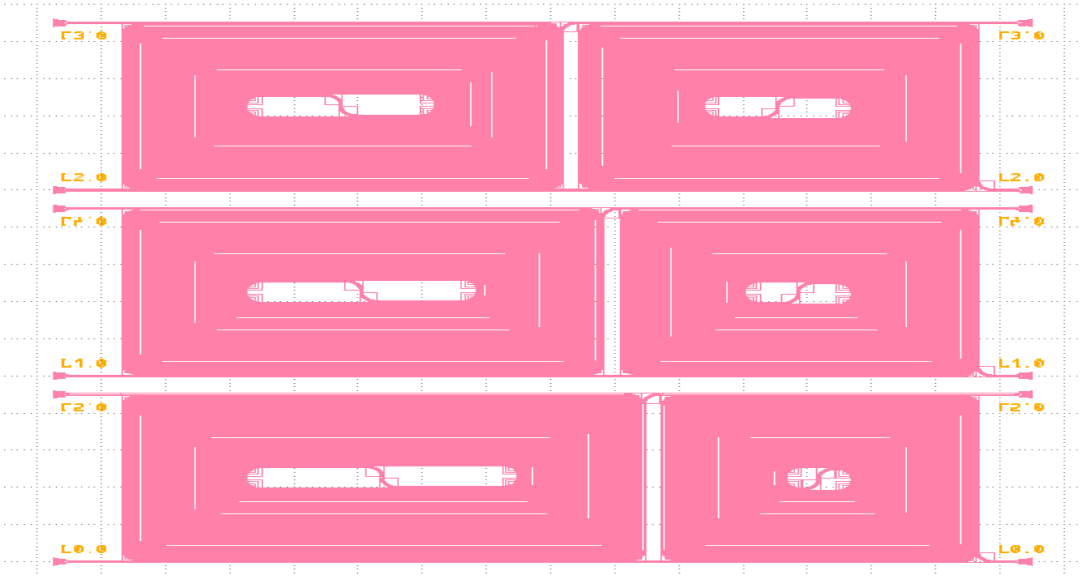


Fig. 9 A series of waveguides with different lengths in spiral way. All waveguides are set to the same numbers of bends. The lengths of waveguides are from 0cm to 35cm with 7cm step.

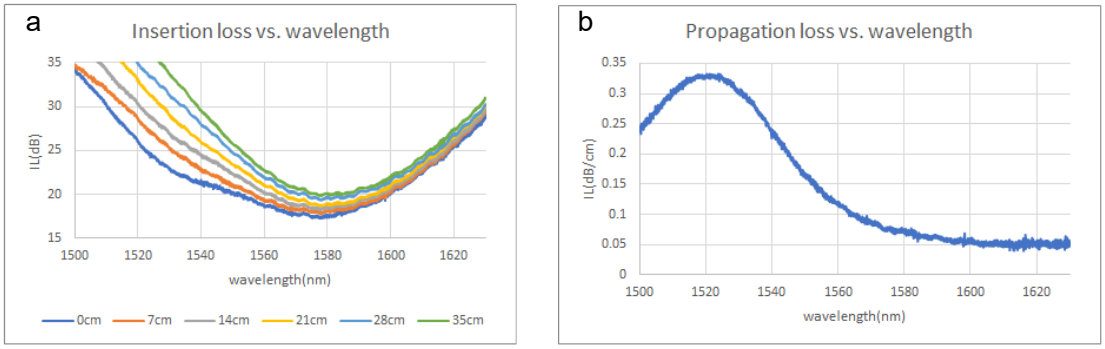


Fig.10 (a) Transmission spectrum of waveguides in different lengths. (b) Propagation loss as a function of wavelength by analyzing the slop of the linear fitting curve transmission spectrum in (a).

8.4.3. Datasheet

Device name	PCell_WG_SIN
Description	Single mode waveguide for 1550nm with 1um width.
Specification	
Propagation loss	<= 0.1 dB/cm
Effective index	
Group index	

7.5 Grating coupler

The grating coupler is designed for coupling the light into or out of the silicon nitride photonics chips.

8.5.1. Structure for characterization

A series of grating coupler pairs is designed to determine the specification of grating couplers. As shown in Fig11, each type of test grating coupler consists of identical input and output grating couplers connected by a short, straight waveguide, which is used to characterize the key specifications, such as the peak wavelength(λ_{peak}), the peak insertion loss and the 1 dB-bandwidth.

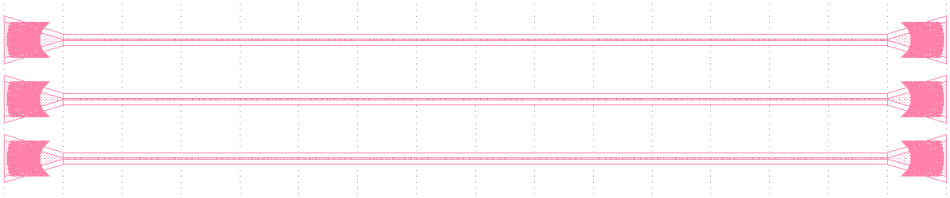


Fig. 11 Test structures of grating couplers

8.5.2. Analytical method

The test grating couplers are designed for 10° incident angle in air or 8° in fiber array (FA) packaging. The maximum is used to determine the peak wavelength and the peak insertion loss. As shown in Fig12Fig. , a transmission spectrum of a grating coupler used for TE@1550nm is given. The insertion losses are 4.65dB@1550nm and 4.64dB@1547.7nm, which are corresponded to the peak wavelength. The 1dB bandwidth (46 nm) is also extracted from the transmission spectrum.

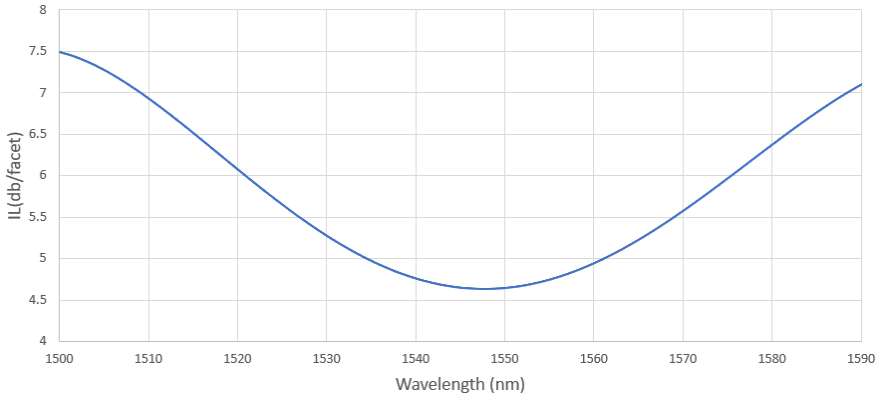


Fig. 12 Transmission spectrum of single grating coupler

8.5.3. Datasheet

Device name	GC_TE_1550_SIN
Description	Grating coupler for 1550nm and TE polarization.
Specification	
Insertion loss@1550nm	<= 5.5dB/facet
1dB bandwidth@1550nm	>= 40nm

7.6 Multi-mode interferometer (MMI)

Multi-mode interferometer (MMI) is generally used as a 50:50 power splitter or combiner.

8.6.1. Structure for characterization

In Fig13Fig. , a set of cascaded structures is used to determine the specification of MMIs. Five MMIs with one input and six output ports form the cascaded structure. From port 1 to port 5, the power difference between adjacent ports should be 3dB plus the excess loss of MMIs.

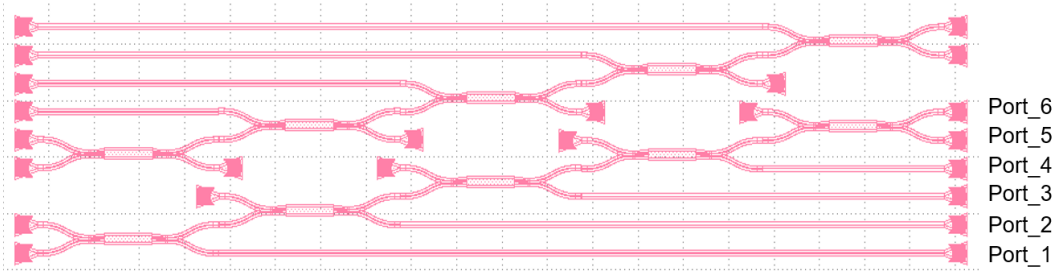


Fig. 13 Structures for MMI test

8.6.2. Analytical method

The transmission spectrum of each output port of cascaded MMIs are recorded. The excess insertion loss can be estimated through calculating the difference between the adjacent ports. The power imbalance between two output ports can be extracted from the transmission spectrum of the last two ports.

The test results of a 1x2 MMI are shown in Fig14 and Fig15. The transmission spectrum in wavelength range from 1500 nm to 1640 nm at all six output ports are recorded. In the spectrum, the influence of grating coupler is not removed, and all grating couplers in measurements are considered as identical. The excess loss of MMI is obtained by calculating the mean of all the differences between adjacent ports. The excess insertion loss is around 0.04 dB at 1550nm. The power imbalance is obtained from the difference between port-5 and port-6, which are almost the same in Fig15. After calculating the moving average of the imbalance spectrum, the imbalance around 1550nm (<5%) is achieved.

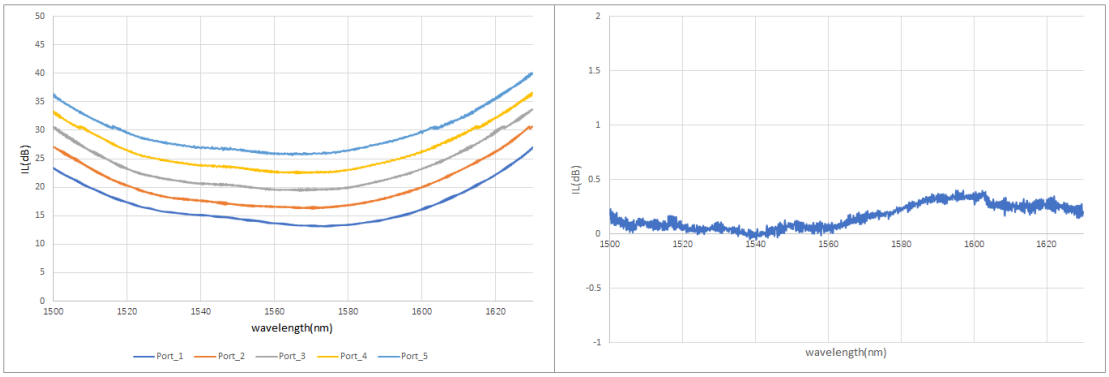


Fig. 14 Left: Transmission spectrum at output ports. Right: Excess insertion loss of a single 1x2 MMI.

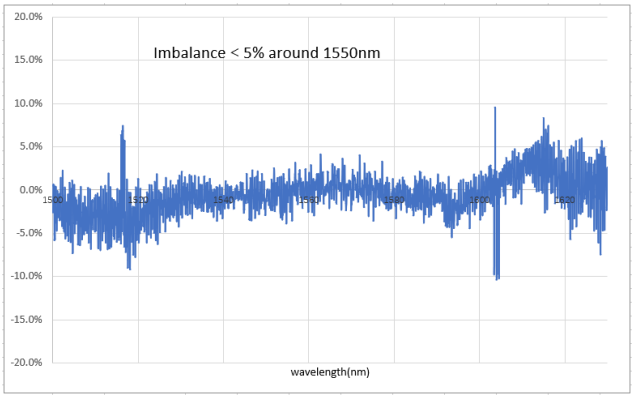


Fig.15 Imbalance spectrum and a black line indicates the average imbalance in a range of 2nm.

8.6.3. Datasheet

Device name	M1X2_TE_1550_SIN
Description	1x2 MMI used as 50:50 splitter or combiner@1550nm
Specification	
Excess insertion loss	<= 0.3 dB
Imbalance	±5%

Device name	M2X2_TE_1550_SIN
Description	2x2 MMI used as 50:50 splitter or combiner@1550nm
Specification	
Excess insertion loss	<= 0.7 dB
Imbalance	±10%

7.7 EDGE COUPLER

The edge coupler is designed for coupling the light into or out of the silicon nitride photonics chips.

8.7.1. Structure for characterization

A series of edge coupler pairs is designed to determine the specification of edge couplers. As shown in Fig16Fig. , each type of test edge coupler consists of identical input and output edge couplers connected by waveguides throughout the chip, which is used to characterize the key specifications.

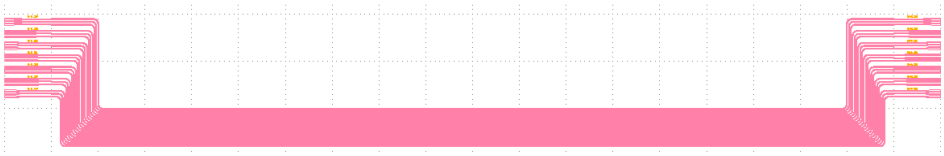


Fig. 16 Structures for edge couplers

8.7.2. Analytical method

The edge couplers are designed for fibers with a mode diameter of 3.5 μm. As shown in Fig17, a transmission spectrum of edge coupler user for TE@1550nm is given. The insertion loss is 2.01dB@1550nm. The 1dB bandwidth (more than the measurement range) is also extracted from the transmission spectrum.

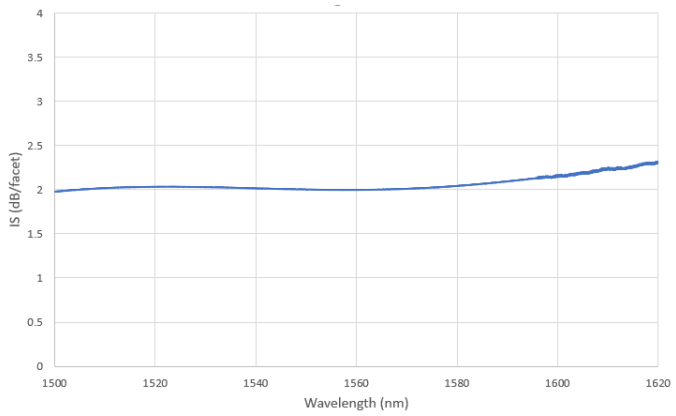


Fig.17 Transmission spectrum of single edge coupler

8.7.3. Datasheet

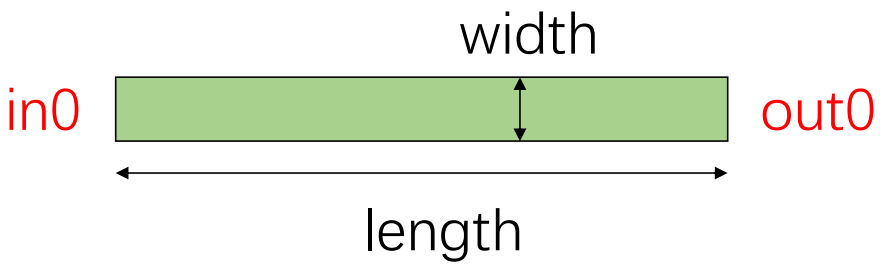
Device name	GC_TE_1550_SIN
Description	Edge coupler for 1550nm and TE polarization, MFD 3.5um
Specification	
Insertion loss@1550nm	<= 2.5 dB/facet
1dB bandwidth@1550nm	>= 90 nm

ATTACHMENT - PCELLS DESCRIPTION

Parametric cells (PCells) are provided on KLayout platform which help users draw devices in a flexible way. It's important to note that these parameters are not linked with physical performances. Additionally, the choices of parameters of each PCells are limited, i.e., not all values of parameters could generate the layout correctly. Users should carefully choose these parameters that meet the physical rules. Moreover, Users should also pay attention to the design rules since those rules are not taken into consideration in these PCells, e.g., sharp angles.

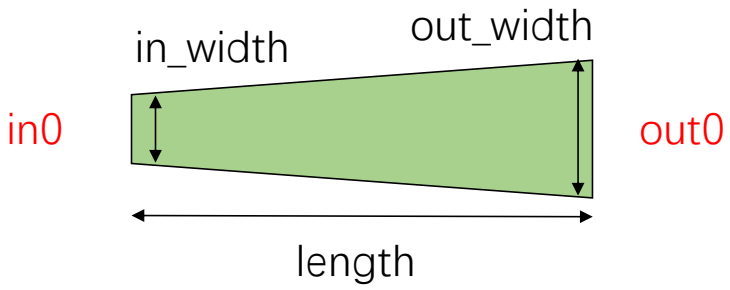
PCELL_WG_SIN

Element	PCell_WG_SIN		
Description	A straight waveguide		
Layout Parameters	Name	Parameter description	Default
	width	Waveguide width	1 [μm]
	length	Waveguide length	10 [μm]



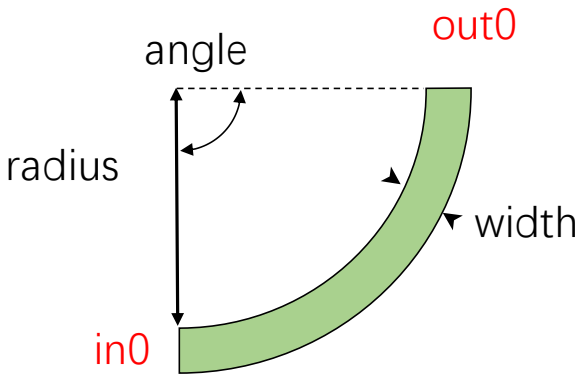
PCELL_TP_SIN

Element	PCell_TP_SIN		
Description	A taper waveguide		
Layout Parameters	Name	Parameter description	Default
	input width	Input taper width	1 [μm]
	output width	Output taper width	2 [μm]
	length	Taper length	10 [μm]
	cld_ex	Cladding width	4.5 [μm]



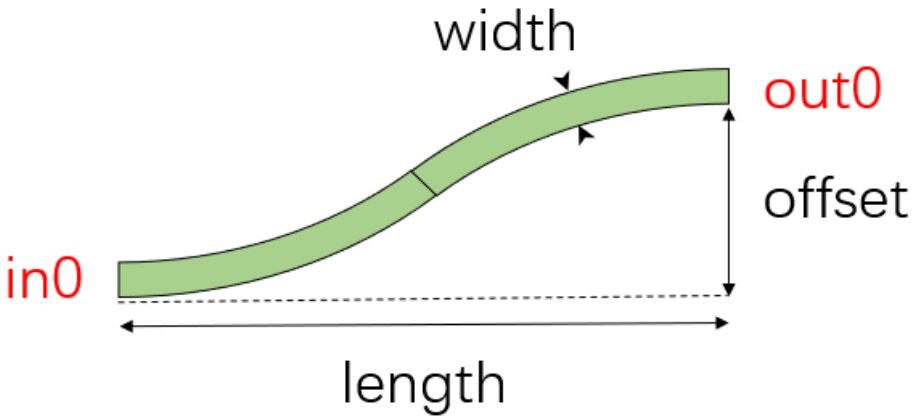
PCELL_ARC_SIN

Element	PCell_ARC_SIN		
Description	A bend SiN Waveguide		
Layout Parameters	**Name**	**Parameter description**	**Default**
	width	Core width of the bend waveguide	1 [μm]
	radius	Radius of the bend waveguide	50 [μm]
	angle	Bend angle	90 [degree]
	Number of Points	Numbers of arc points	64
	cld_ex	Cladding width	4.5 [μm]



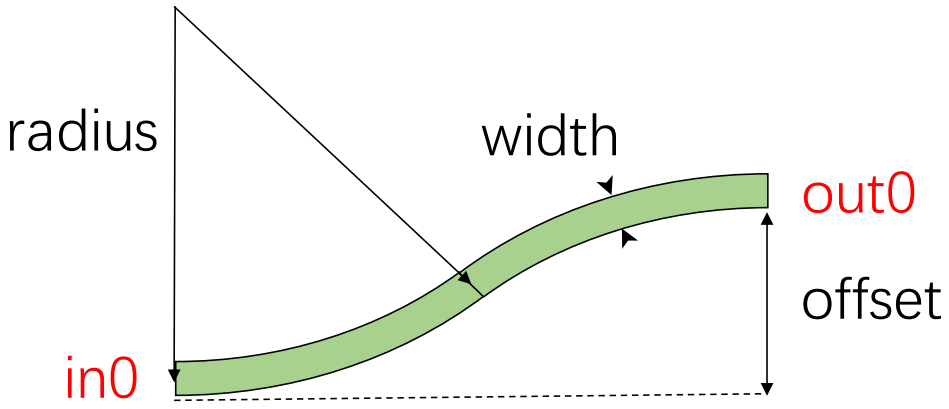
PCELL_BEND_SINE_SIN

Element	PCell_BEND_SINE_SIN		
Description	A S-bend waveguide		
Layout Parameters	**Name**	**Parameter description**	**Default**
	width	Core width of the waveguide	1 [μm]
	length	Horizontal length of the waveguide	50 [μm]
	offset	Vertical offset of the waveguide	10 [μm]



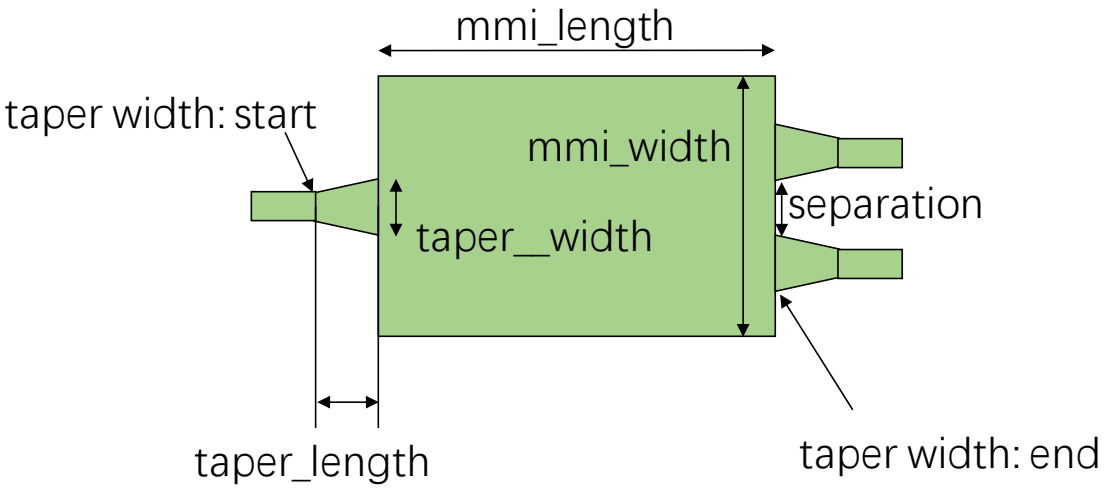
PCELL_SINE_BEND_SIN

Element	PCell_ SINE_BEND_SIN		
Description	A S-bend waveguide		
Layout Parameters	Name	Parameter description	Default
	width	Core width of the waveguide	1 [μm]
	radius	Radius of the bend waveguide	50 [μm]
	offset	Vertical offset of the waveguide	10 [μm]



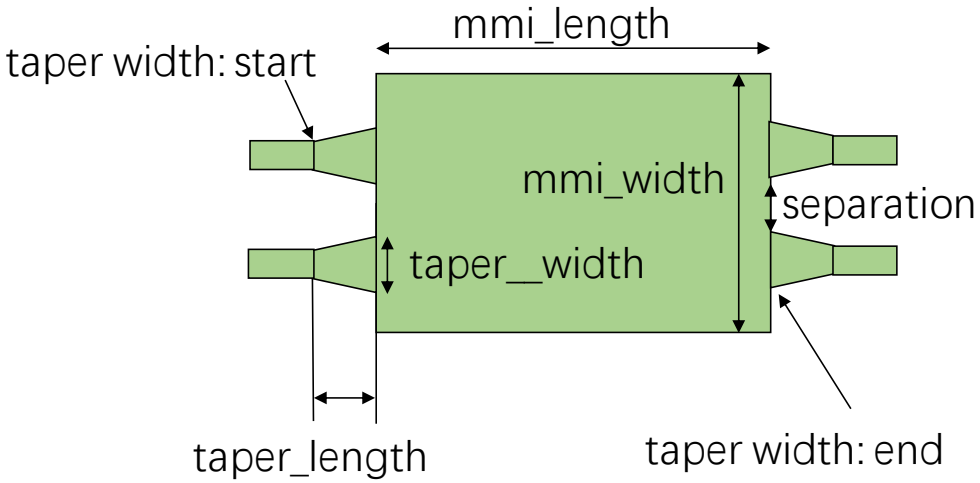
PCELL_M1X2_SIN

Element	PCell_M1X2_SIN		
Description	A 1X2 MMI		
Layout Parameters	Name	Parameter description	Default
	mmi length	Length of the mmi space	50 [μm]
	mmi width	Width of the mmi space	10 [μm]
	taper width: start	Start width of tapers	1 [μm]
	taper width: end	End width of tapers	2 [μm]
	taper length	Length of tapers	10 [μm]
	separation	Separation distance between tapers	5 [μm]



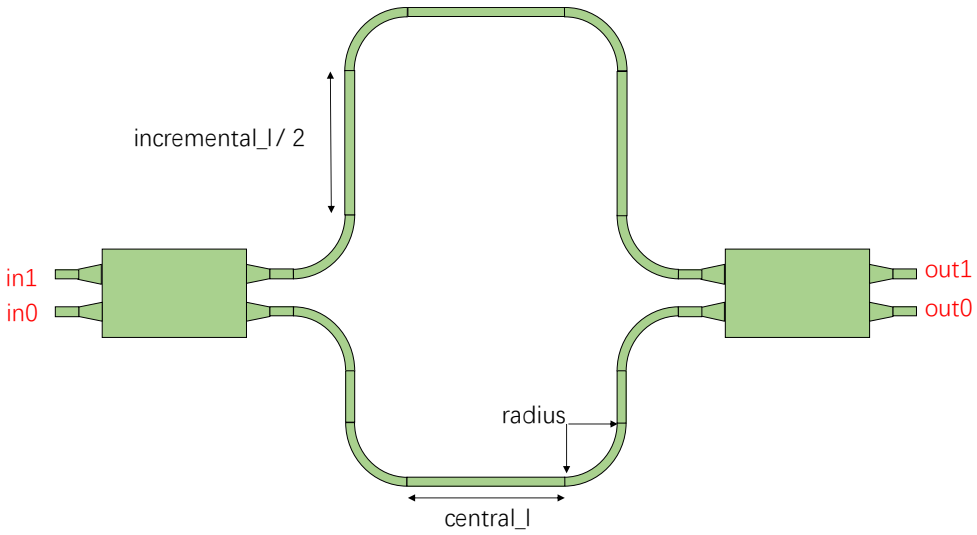
PCELL_M2X2_SIN

Element	PCell_M2X2_SIN		
Description	A 2x2 mmi		
Layout Parameters	**Name**	**Parameter description**	**Default**
	mmi length	Length of the mmi space	50 [µm]
	mmi width	Width of the mmi space	10 [µm]
	taper width: start	Start width of tapers	1 [µm]
	taper width: end	End width of tapers	2 [µm]
	taper length	Length of tapers	10 [µm]
	separation	Separation distance between tapers	5 [µm]



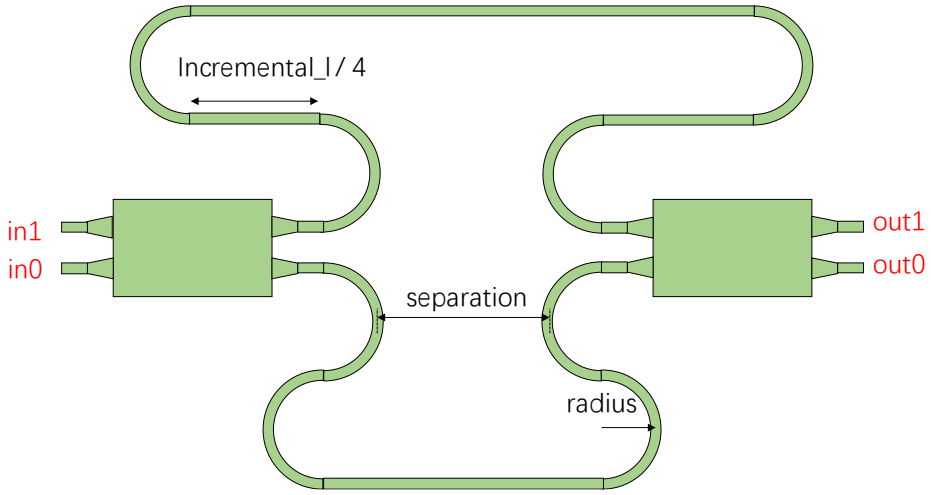
PCELL_MZI_V_SIN

Element	PCell_MZI_V_SIN		
Description	A Mach-Zehnder interferometer		
Layout Parameters	**Name**	**Parameter description**	**Default**
	incremental_l	Length difference between two arms	100 [μm]
	Central_l	Length of the central straight waveguide.	50 [μm]
	radius	Radius of bend waveguides	50 [μm]



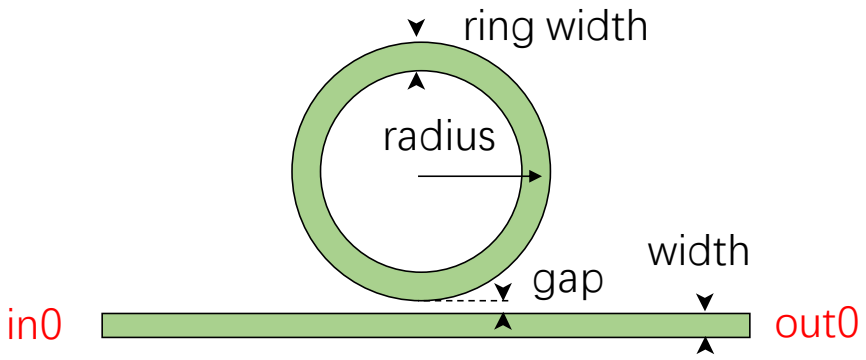
PCELL_MZI_H_SIN

Element	PCell_MZI_H_SIN		
Description	A Mach-Zehnder interferometer		
Layout Parameters	**Name**	**Parameter description**	**Default**
	incremental_l	Length difference between two arms	200 [µm]
	separation	Separation between two bend waveguides	15 [µm]
	radius	Radius of bend waveguides	50 [µm]



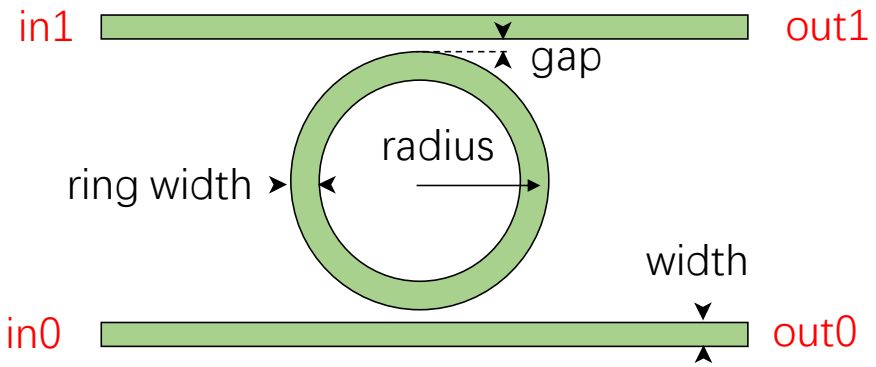
PCELL_RING1_SIN

Element	PCell_RING1_SIN		
Description	A ring resonator		
Layout Parameters	Name	Parameter description	Default
	radius	Radius of the ring	50 [μm]
	ring width	Width of the ring	1 [μm]
	gap	Gap between the ring and the bus waveguide	1 [μm]
	width	Width of the bus waveguide	1 [μm]



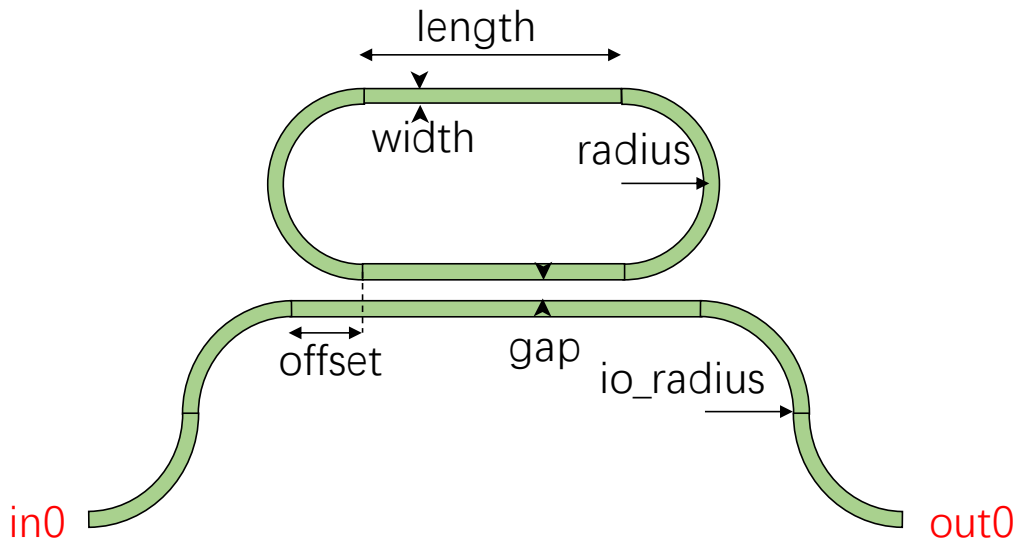
PCELL_RING2_SIN

Element	PCell_RING2_SIN		
Description	A ring resonator		
Layout Parameters	Name	Parameter description	Default
	radius	Radius of the ring	50 [μm]
	ring width	Width of the ring	1 [μm]
	gap	Gap between the ring and the bus waveguide	1 [μm]
	width	Width of the bus waveguide	1 [μm]



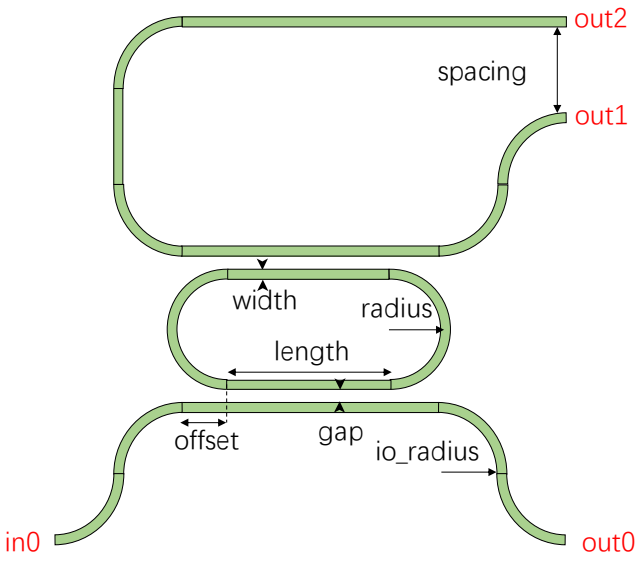
PCELL_RC_RING1_SIN

Element	PCell_RC_RING1_SIN		
Description	A ring resonator		
Layout Parameters	**Name**	**Parameter description**	**Default**
	ring radius	Radius of the ring	50 [μm]
	io radius	Radius of the io waveguide	50 [μm]
	gap	Gap between the ring and the bus waveguide	1 [μm]
	width	Width of the bus waveguide and the ring	1 [μm]
	length	Length of the straight part of the ring	100 [μm]
	offset	Offset distance between the ring and the bus waveguide	50 [μm]
	Number of Points 1	Numbers of ring points	64
	Number of Points 2	Numbers of ring points	64
	cld_ex	Cladding width	4.5 [μm]



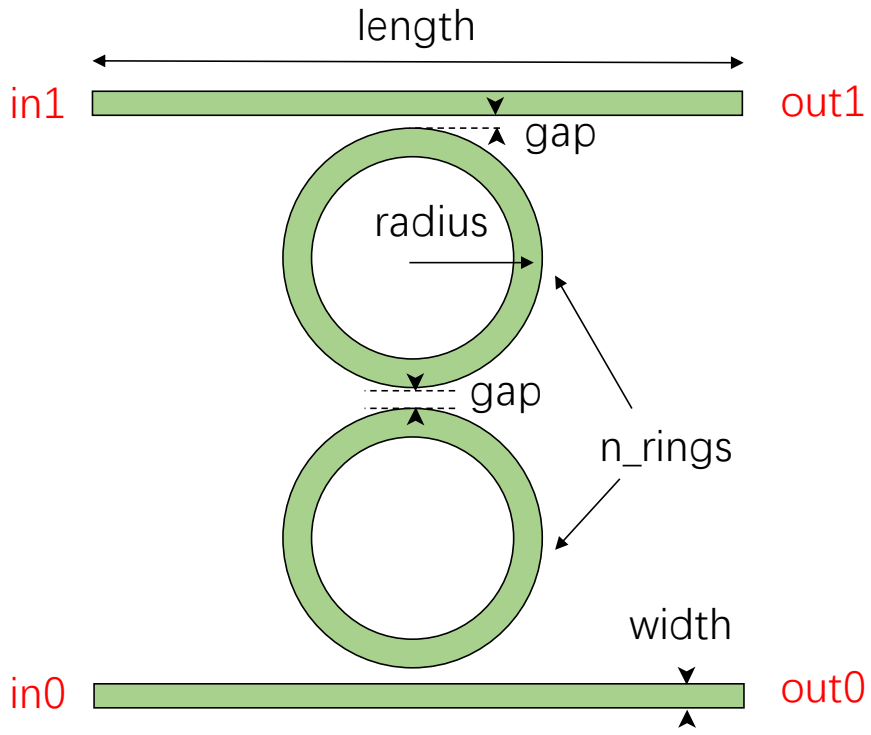
PCELL_RC_RING2_SIN

Element	PCell_RC_RING2_SIN		
Description	A ring resonator		
Layout Parameters	Name	Parameter description	Default
	ring radius	Radius of the ring	50 [µm]
	io radius	Radius of the io waveguide	50 [µm]
	gap	Gap between the ring and the bus waveguide	1 [µm]
	width	Width of the bus waveguide and the ring	1 [µm]
	length	Length of the straight part of the ring	100 [µm]
	offset	Offset distance between the ring and the bus waveguide	50 [µm]
	spacing	Spacing between ports out2 / out1	100 [µm]
	Number of Points 1	Numbers of ring points	64
	Number of Points 2	Numbers of ring points	64
	cld_ex	Cladding width	4.5 [µm]



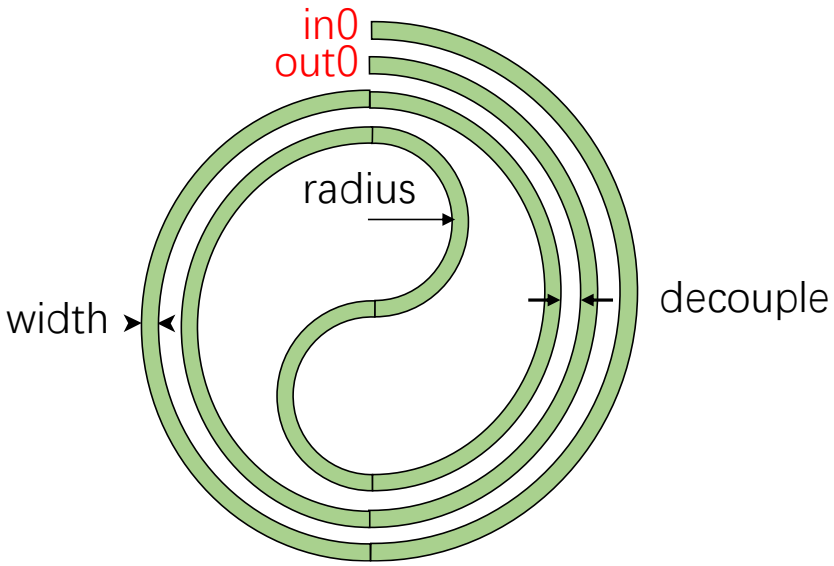
PCELL_CR_RING_SIN

Element	PCell_CR_RING_SIN		
Description	A vertical multiple loops ring resonator		
Layout Parameters	**Name**	**Parameter description**	**Default**
	radius	Bend radius for the auto-generated bends	50 [μm]
	width	Core width of the waveguide	1 [μm]
	length	Length of the bus waveguide	100 [μm]
	gap	Spacing between the two waveguide centerlines.	1 [μm]
	N_Rings	Numbers of ring	2
	Number of Points 1	Numbers of ring points	64 [μm]
	cld_ex	Cladding width	4.5 [μm]



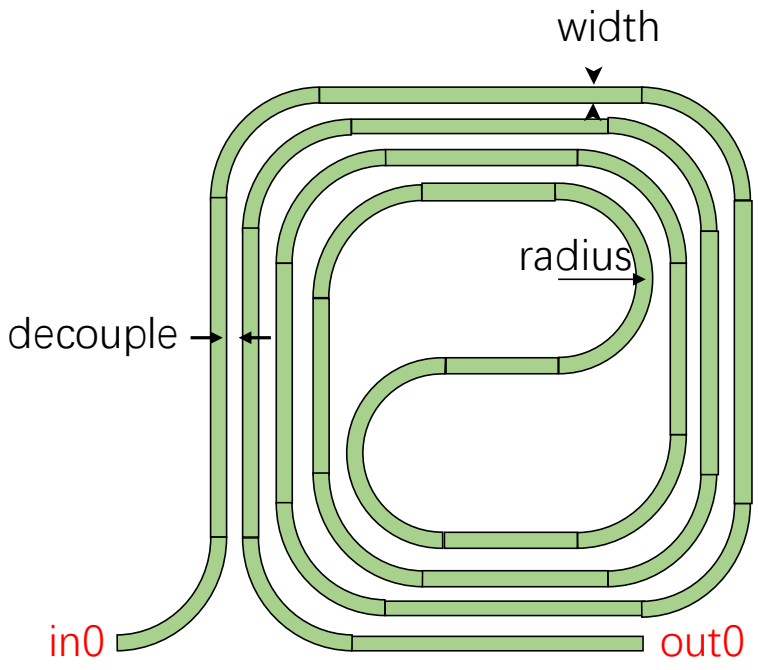
PCELL_SP_C_SIN

Element	PCell_SP_C_SIN		
Description	A rounded spiral waveguide		
Layout Parameters	**Name**	**Parameter description**	**Default**
	width	Width of the spiral waveguide	1 [μm]
	radius	Radius of round circle	50 [μm]
	decouple	Separation between adjacent waveguides	10 [μm]
	length	Length of the total spiral waveguide	1000 [μm]



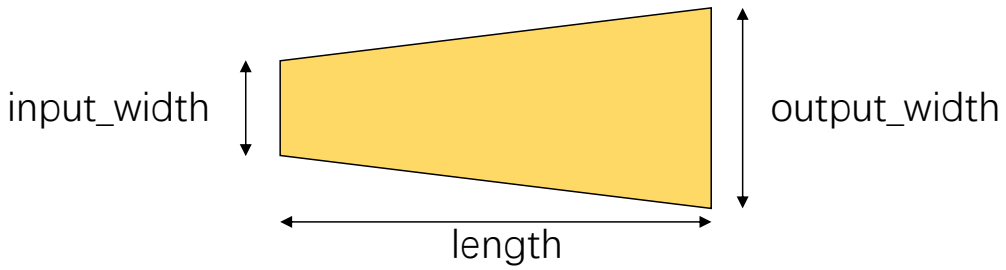
PCELL_SP_S_SIN

Element	PCell_SP_S_SIN		
Description	A direct waveguide crossing		
Layout Parameters	**Name**	**Parameter description**	**Default**
	radius	Radius of round circle	50 [µm]
	decouple	Separation between adjacent waveguides	10 [µm]
	n_o_loops	Number of loops	5
	core width	Width of the spiral waveguide	1 [µm]
	length	Length of the total spiral waveguide	6000 [µm]



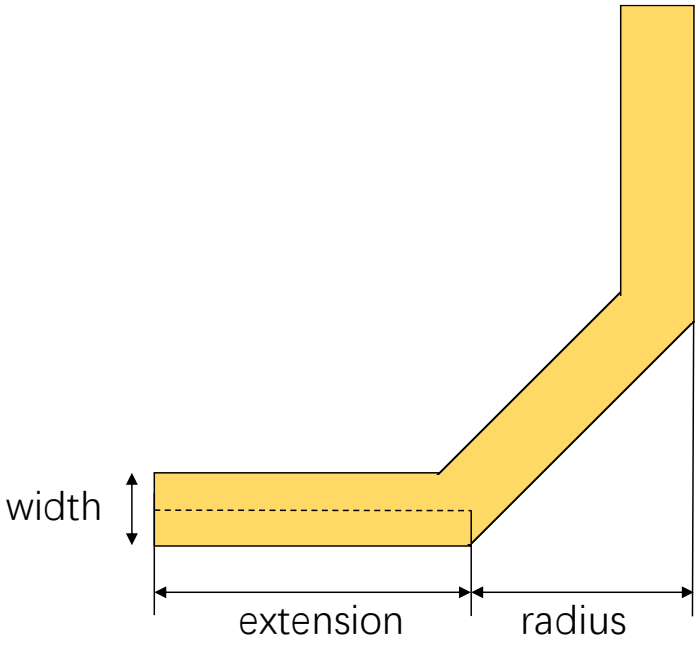
PCELL_TP_M_SIN

Element	PCell_TP_M_SIN		
Description	A metal taper		
Layout Parameters	**Name**	**Parameter description**	**Default**
	input width	Input taper width	1 [μm]
	output width	Output taper width	2 [μm]
	length	Taper length	10 [μm]



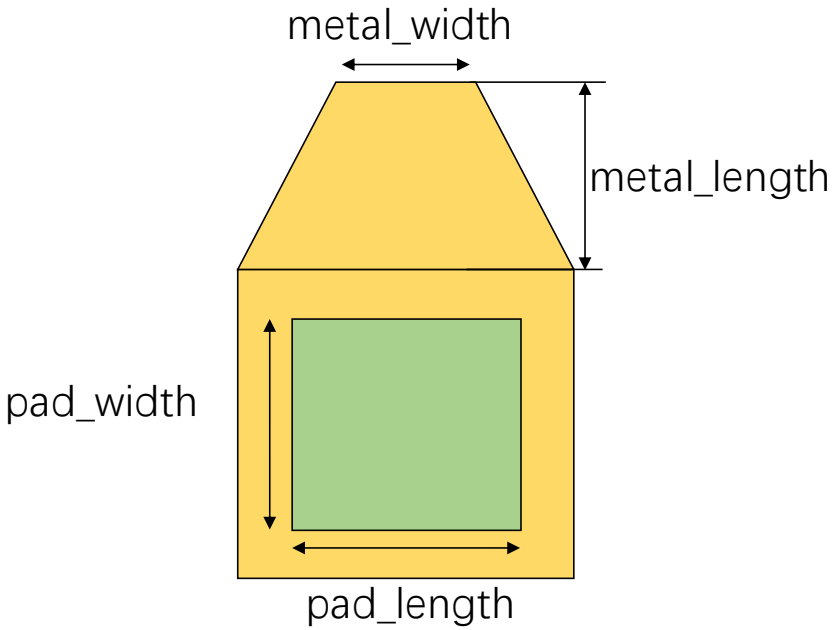
PCELL_BEND_M_SIN

Element	PCell_BEND_M_SIN		
Description	A bend metal wire		
Layout Parameters	**Name**	**Parameter description**	**Default**
	radius	Bend radius	10 [µm]
	width	Width of the metal wire	12 [µm]
	extension	Extension length	20 [µm]



PCELL_PAD_SIN

Element	PCell_PAD_SIN		
Description	A metal pad		
Layout Parameters	Name	Parameter description	Default
	pad height	Pass1 length	100 [µm]
	pad width	Pass1 width	100 [µm]
	metal width	Metal taper length	50 [µm]
	taper length	Metal taper width	10 [µm]



PCELL_PS_SIN

Element	PCell_PS_SIN		
Description	A waveguide with metal heater		
Layout Parameters	**Name**	**Parameter description**	**Default**
	width	Width of the waveguide	1 [µm]
	heater width	Width of the metal heater	2 [µm]
	length	Length of the metal heater	100 [µm]