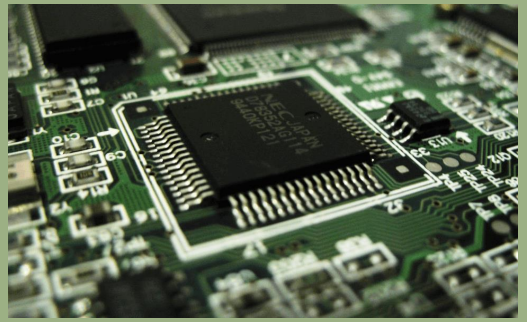

8085 Microprocessor

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Timers

- Real time applications - traffic lights, digital signals, process control.

Time delay using NOP Instruction

- NOP instruction does nothing but takes 4T states of processor time to execute. So by executing NOP instruction in between two instructions we can get delay of 4 T-State.

$$1\,T - state = \frac{1}{Operating\ frequency\ of\ 8085}$$

Time delay using counters

- Counting can create time delays. Since the execution time of the instructions used in a counting routine are known, the initial value of the counter, required to get specific time delay can be determined.
- Using 8-bit counter:

	No. of T-states
MVI C, count	7
Back: DCR C	4
JNZ Back	7/10

Maximum delay with 8-bit count is:
Let count = FF H = $(255)_{10}$
No. of T-state = (7 + (255-1)×14 + 11) × 0.5
= 1787 µsec

Total T-states required to execute the given program:
= 7 + (count-1) × (4+10) + (4+7)
Let count = 5
No. of T-state = 7 + (5-1)×14 + 11
= 7 + 56 + 11 = 74
Assuming Operating frequency of 8085A is 2 MHz.
Time required for 1 T-state = $\frac{1}{2MHz} = 0.5\ \mu sec$

Total time required to execute the given program =
$74 \times 0.5 = 37\ \mu sec$

Time delay using counters contd.

- Using 16-bit counter:

	No. of T-states
LXI B, count	10
Back: DCX B	6
MOV A, C	4
ORA B	4
JNZ Back	7/10

Maximum delay with 16-bit count is:
Let count = FFFF H = $(65535)_{10}$
No. of T-state = (10 + (65535-1)×24 + 21) × 0.5
= 786423.5 µsec = 0.786425 sec

Total T-states required to execute the given program:
= 10 + (count-1) × 24 + 21
Let count = 03FF H = $(1023)_{10}$
No. of T-state = 10 + (1022)×24 + 21
= 24559
Assuming Operating frequency of 8085A is 2 MHz.
Time required for 1 T-state = $\frac{1}{2MHz} = 0.5\ \mu sec$

Total time required to execute the given program =
$24559 \times 0.5 = 12279.5\ \mu\text{sec} = 12.2795\ msec$

Time delay using Nested loops

- In this, there are more than one loops. The innermost loop is same as explained above. The outer loop sets the multiplying count to the delays provided by the innermost loops.

	No. of T-states
MVI B, Multiplier count	7
Start: MVI C, Delay count	7
Back: DCR C	4
JNZ Back	7/10
DCR B	4
JNZ Start	7/10

T-states required for execution of inner loop:

T_{inner} = 7 + (Delay count-1) × (4+10) + (4+7)

T-states required for execution of the given program:

= 7 + (Multiplier count -1)× (T_{inner}+14) + 11

For Delay count = 65 H = $(101)_{10}$ and

Multiplier count = 51 H = $(81)_{10}$

T_{inner} = 7 + (101 – 1))× 14 + 11 = 1418

Total time required to execute the given program =

(Assuming Operating frequency of 8085A is 2 MHz)

= 7 + ((81 – 1) × (1418 +14) + 11) × 0.5 µsec

= 57.7235 msec


Thank you!