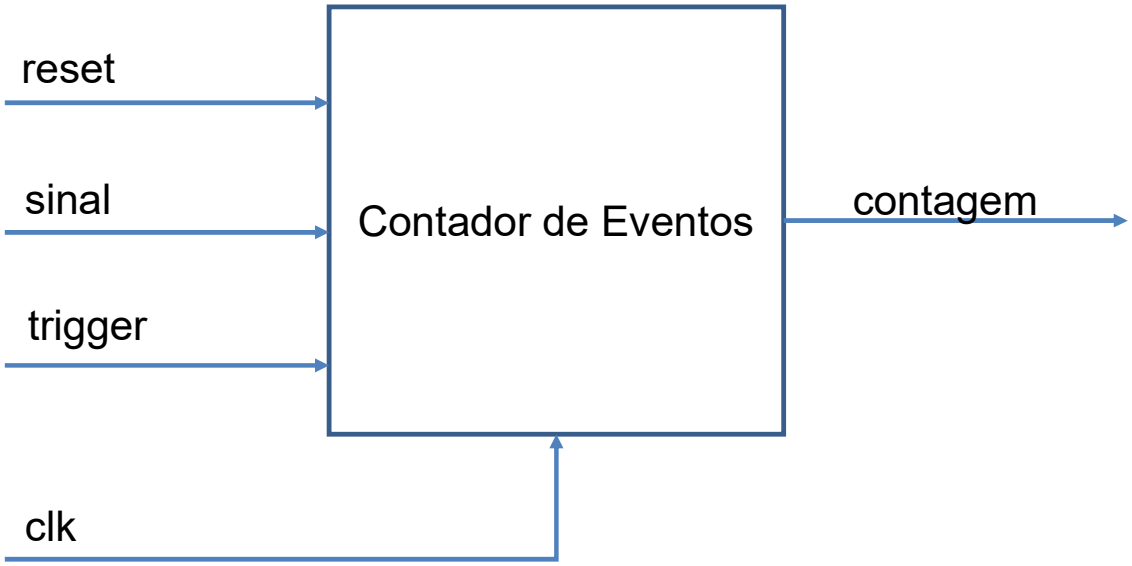
VHDL

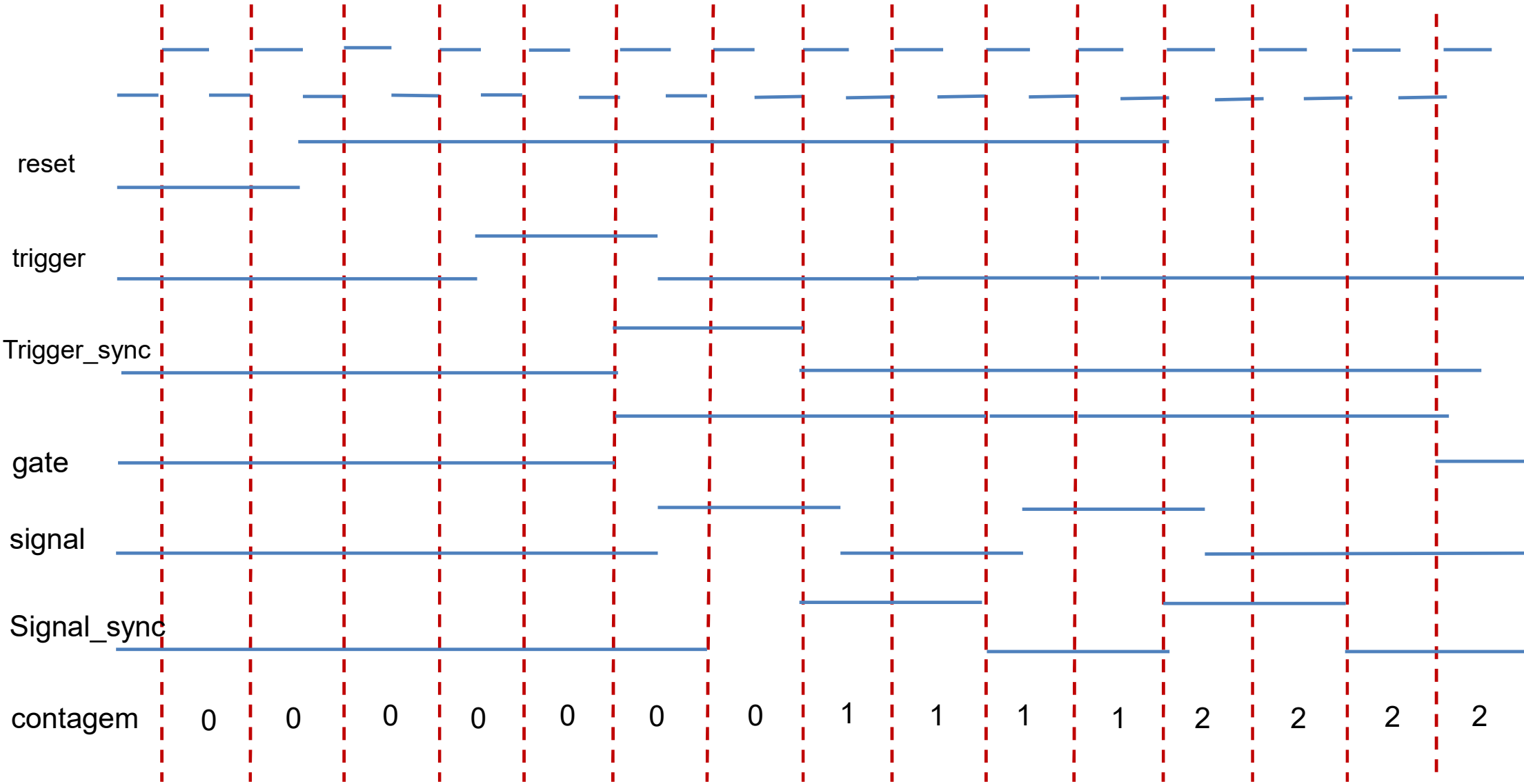
Técnicas Digitais II

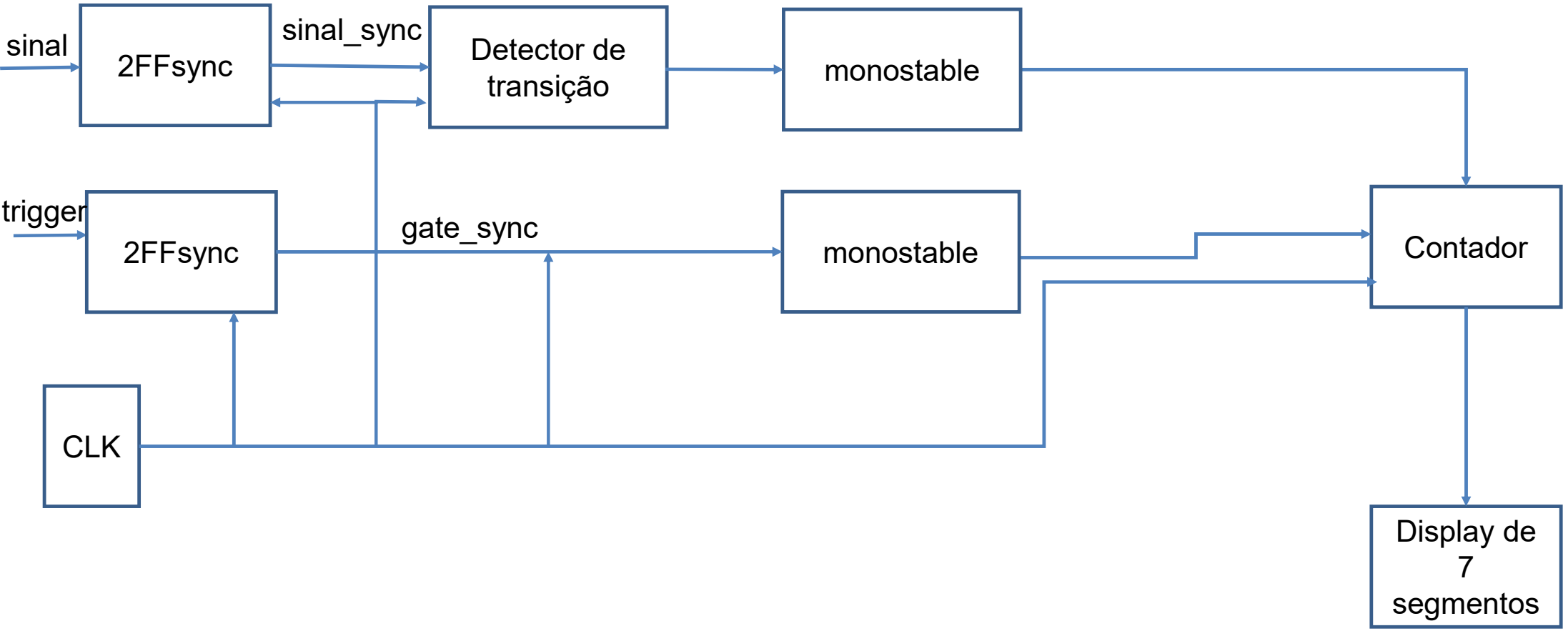
Prof. Jorge Amaral

jamaral@eng.uerj.br

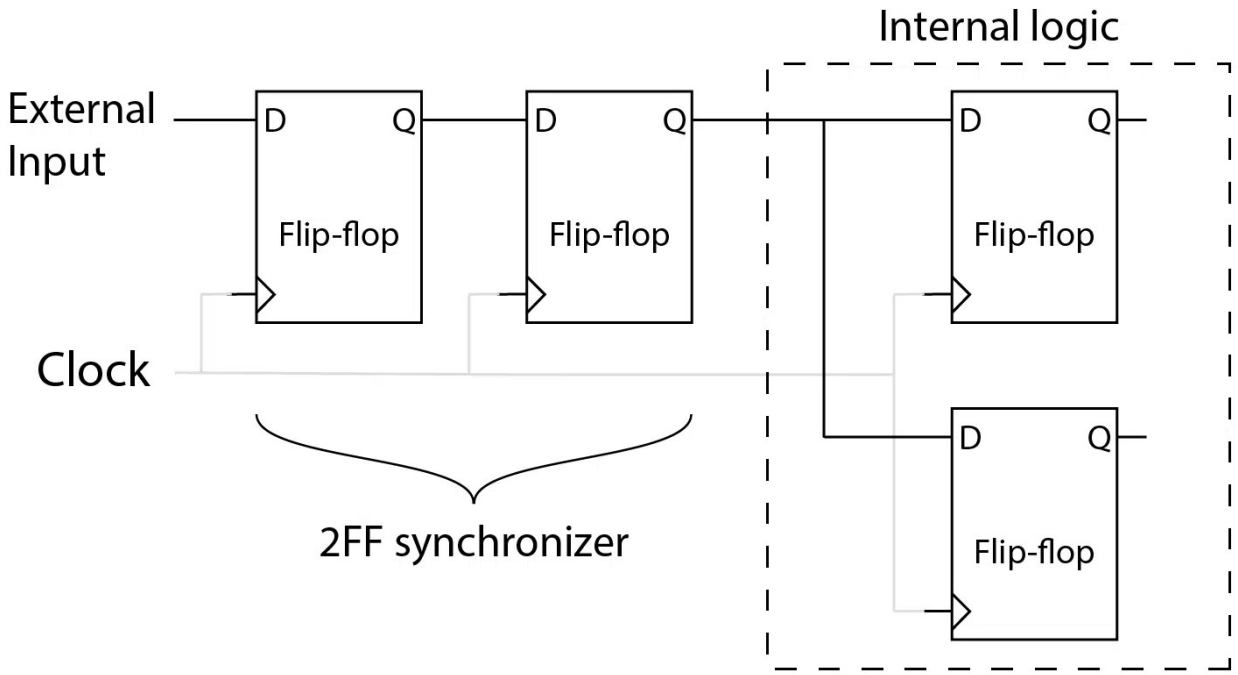
Projeto Top-down




reset
trigger
Trigger_sync
gate
signal
Signal_sync
contagem
0
0
0
0
0
0
0
1
1
1
1
2
2
2
2


sinal
2FFsync
sinal_sync
Detector de transição
monostable
trigger
2FFsync
gate_sync
monostable
Contador
CLK
Display de 7 segmentos

2FF Sync


Internal logic
External
Input
D
Q
Flip-flop
D
Q
Flip-flop
D
Q
Flip-flop
Clock
D
Q
Flip-flop
2FF synchronizer

Monoestável

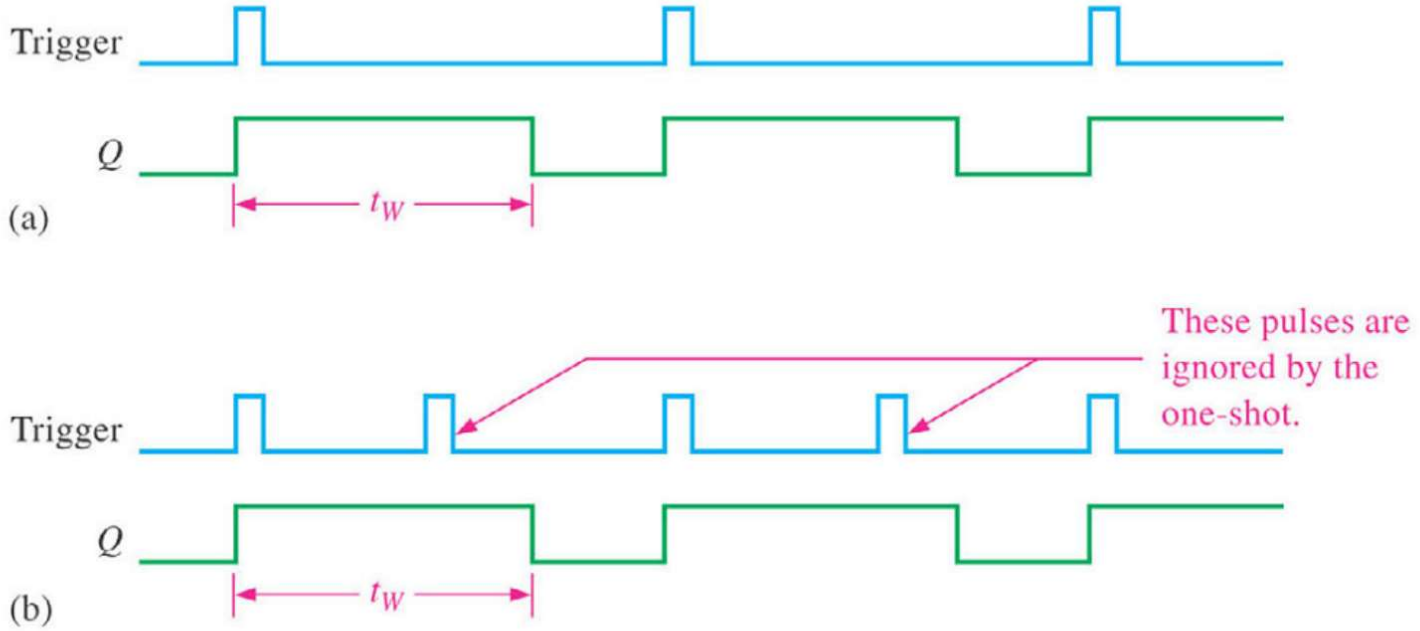


Figura 6.2 Diagrama de funcionamento de um monoestável não-redisparável.

https://www.feg.unesp.br/Home/PaginasPessoais/ProfMarceloWendling/lab.-6---circuito-monoestavel.pdf

Monoestável

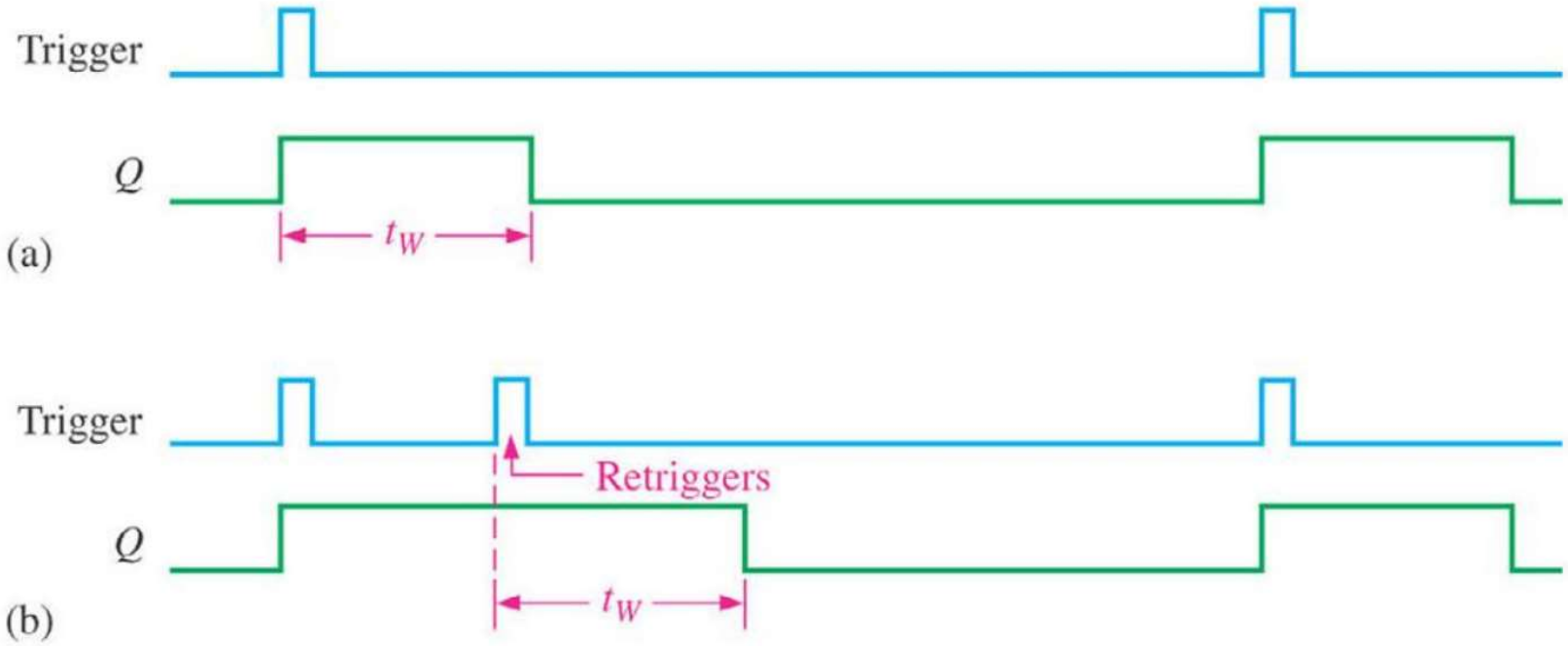


Figura 6.3 Funcionamento de um circuito monoestável redisparável.

https://www.feg.unesp.br/Home/PaginasPessoais/ProfMarceloWendling/lab.-6---circuito-monoestavel.pdf