Paper Title: **Distributed Computing in IoT: System-on-a-Chip for Smart Cameras as an Example**

Paper Link: https://drive.google.com/file/d/1WR3AxsrMBZZoyrlcLE8aqZmlq4fSfG5U/view?usp=sharing

1. Summery

1.1 Motivation

This work is motivated by the imperative role of distributed computing in addressing challenges in the Internet of Things (IoT), especially concerning large-scale data acquisition for ultra-big data analysis in video sensor networks. Recognizing the infeasibility of traditional centralized solutions on cloud servers due to significant data size and computational tasks in IoT applications, the authors advocate for distributing computation across every node in the IoT. This is further motivated by the need to reduce transmission bandwidth requirements, crucial for ultra-big data analysis in video sensor networks. The paper illustrates the concept using a video sensing network as an example and proposes a system-on-a-chip solution for distributed smart cameras with a coarse-grained reconfigurable image stream processing architecture. Emphasizing the importance of optimizing computation distribution in IoT, the authors leverage advances in silicon technology, proposing a reconfigurable smart-camera stream processor for high area and power efficiency. The motivation concludes with a commitment to ongoing research, focusing on designing a System-on-Chip for distributed video sensors in IoT applications, considering the entire network configuration for global optimization.

1.2 Contribution

The authors contribute significantly to the field of Internet of Things (IoT) by addressing the challenges associated with the four major components of IoT application systems: sensors, communications, computation, and service. In the context of large-scale data acquisition for ultra-big data analysis aimed at uncovering context information and knowledge behind signals, the authors assert the impracticality of centralized solutions on cloud servers. Leveraging the advances in silicon technology that have lowered the cost of computation, the authors propose a groundbreaking approach to distributed computing on every node in the IoT. Focusing on a video sensing network as an illustrative example, they review existing works and present the architecture of a system-on-a-chip solution designed for distributed smart cameras. This architecture incorporates a coarse-grained reconfigurable image stream processing approach, enabling the acceleration of various computer vision algorithms tailored for distributed smart cameras in the IoT. The authors' contribution lies in providing a concrete and innovative solution

that addresses the scalability and computational demands of large-scale IoT data while demonstrating the applicability of distributed computing through a practical example in the realm of video sensing networks.

1.3 Methodology

The methodology for designing a reconfigurable smart-camera stream processor (ReSSP) is outlined step by step:

1. **Design Challenges and Rationale:**
    - Highlight the design challenges for smart camera System-on-Chip (SoC) in IoT applications, emphasizing the need for programmability, power efficiency, and cost efficiency.
    - Acknowledge that ASIC and processor-based solutions have limitations in addressing all these issues, leading to the exploration of reconfigurable architectures.
1. **Coarse-Grained Reconfigurable Image Stream Processor (CRISP) Architecture:**
    - Introduce the CRISP architecture as a promising reconfigurable architecture for balancing efficiency and programmability in image processing applications.
    - Explain the components of CRISP, including reconfigurable stage processing elements (RSPE) and reconfigurable interconnection (RI).
    - Describe the role of RSPEs in performing specific operations based on the target application and the pipelined architecture for efficient data reuse.
1. **Reconfigurable Smart-camera Stream Processor (ReSSP) Proposal:**
    - Propose ReSSP as a co-processor in an SoC, based on the CRISP architecture.
    - Present 11 different types of RSPEs within ReSSP, categorized based on their functionalities, including Multiply-and-Accumulate (MAC) RSPE, Binary Morphology RSPE, CORDIC RSPE, and others.
    - Introduce reconfigurable memory and subword-level parallelism (SLP) architectures within ReSSP to support various data types in computer vision algorithms.
1. **Heterogeneous Stream Processing (HSP) and SLP Architectures:**
    - Introduce HSP and SLP architectures as extensions to CRISP, addressing the support for various data types in computer vision algorithms.
    - Provide examples, such as using 24-bit for color pixels, 8-bit for gray pixels, and 1-bit for object masks.
    - Explain the Reconfigurable Memory RSPE's role in supporting different memory usages and data types, acting as an interface between heterogeneous data streams.
1. **RSPE Designs for Smart Camera Applications:**

- Detail the design of RSPEs tailored for smart camera applications, with a focus on supporting different operations frequently used in computer vision applications.
- Illustrate the architecture of a Binary Morphology RSPE as an example, demonstrating its ability to process 64 1-bit input data at each cycle.

The methodology showcases a systematic approach to designing ReSSP, addressing specific challenges in smart camera SoC for IoT applications through the utilization of CRISP, HSP, and SLP architectures.