JMicron Technology Corporation

DATASHEET

JMB585
PCIe Gen3x2 to 5 SATA 6Gb/s Bridge

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Revision History

Revision Number	Effective Date	Description of Revision		Author
		Reference	Description of the Change	
0.1	02/26/2018	-	Draft release	Steven Lin
0.2	10/05/2018	-	1. rename JMS585 to JMB585 2. remove GPIO0 3. rename Signal Name in 5 Package pin-out 4. swap PCIe Lane0 and Lane1	MD Lin
1.0	11/01/2018	Chapter 7	Update Electrical characteristics	MD Lin
1.1	12/14/2018		Change core power to 1.25V	MD Lin

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1 Introduction

The JMB585 is a bridge controller between the PCIe host and the storage devices with SATA/AHCI interface. Its upstream port provides a PCIe which data transmission rate for PCIe Gen 3x2 specification. Meanwhile, its downstream port can connect to SATA/AHCI storage devices, such as a solid-state drive (SSD). The data speed of each port for the SATA port can arrive at 6Gb/s.

Also, the JMB585 SATA Host provides five ports and supports Port Multiplier. JMB585 supports command-based switching (CBS) and FIS (Frame Information Structure)-based switching (FBS). The default communication method between the SATA Host and the port Multiplier is CBS. FBS allows the Host controller to issue multiple commands that send and receive data simultaneously from any drive.

The JMB585 supports TRIM to the SSD and can transmit and receive data by both of AHCI mode and legacy IDE mode to and from the host respectively.

JMB585 is highly integrated with JMicron PCI Express and SATA self-designed PHYs.

Finally, the JMB585 is a new product that almost reaches PCIe Gen3x2 line bandwidth. JMB585 can be applied on PC. Mobile, severs, IPC, consumer electrical devices, storage device, and NVR/DVR system.

2 Features

General Features

- 15 GPIOs for customization.
- SPI interface for external SPI Flash (Option ROM).
- Supports Windows 7, Windows 10 and Linux-base OS
- Supports 3.3V I/O and 1.25V core power.
- 25MHz external crystal.
- 76-pin (2 lane PCIe to 5 SATA port) package.

PCI Express Features

- Supports up to two lane of PCI Express.
- Complies with PCI Express Base Specification Revision 3.1a.
- Supports PCIe link layer power saving mode.
- 100MHz differential PCI Express reference clock in.

SATA Features

- Supports 5 SATA port.
- Supports command-based and FIS-based for Port Multiplier.
- Complies with SATA Specification Revision 3.2.
- Supports AHCI mode and IDE programming interface.
- Supports Native Command Queue (NCQ).
- Supports SATA link power saving mode (partial and slumber)
- Supports SATA plug-in detection capable.
- Supports drive power control and staggered spin-up.
- Supports SATA Partial / Slumber power management state.

3 Block diagram

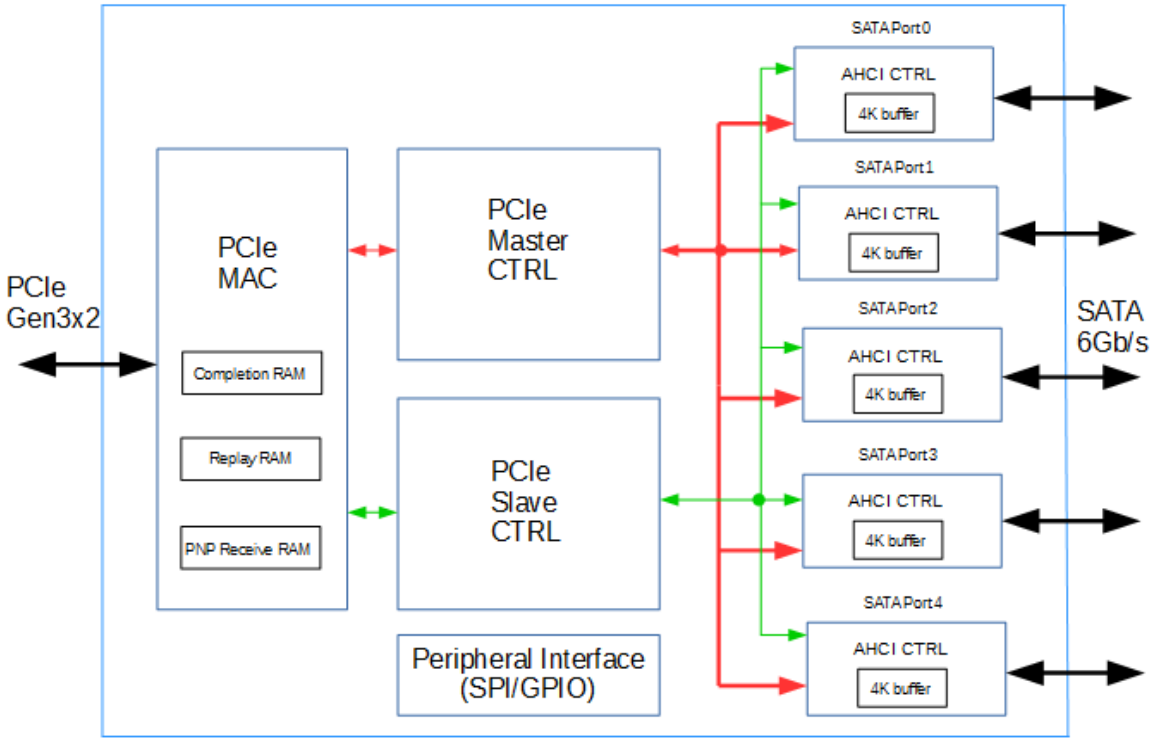
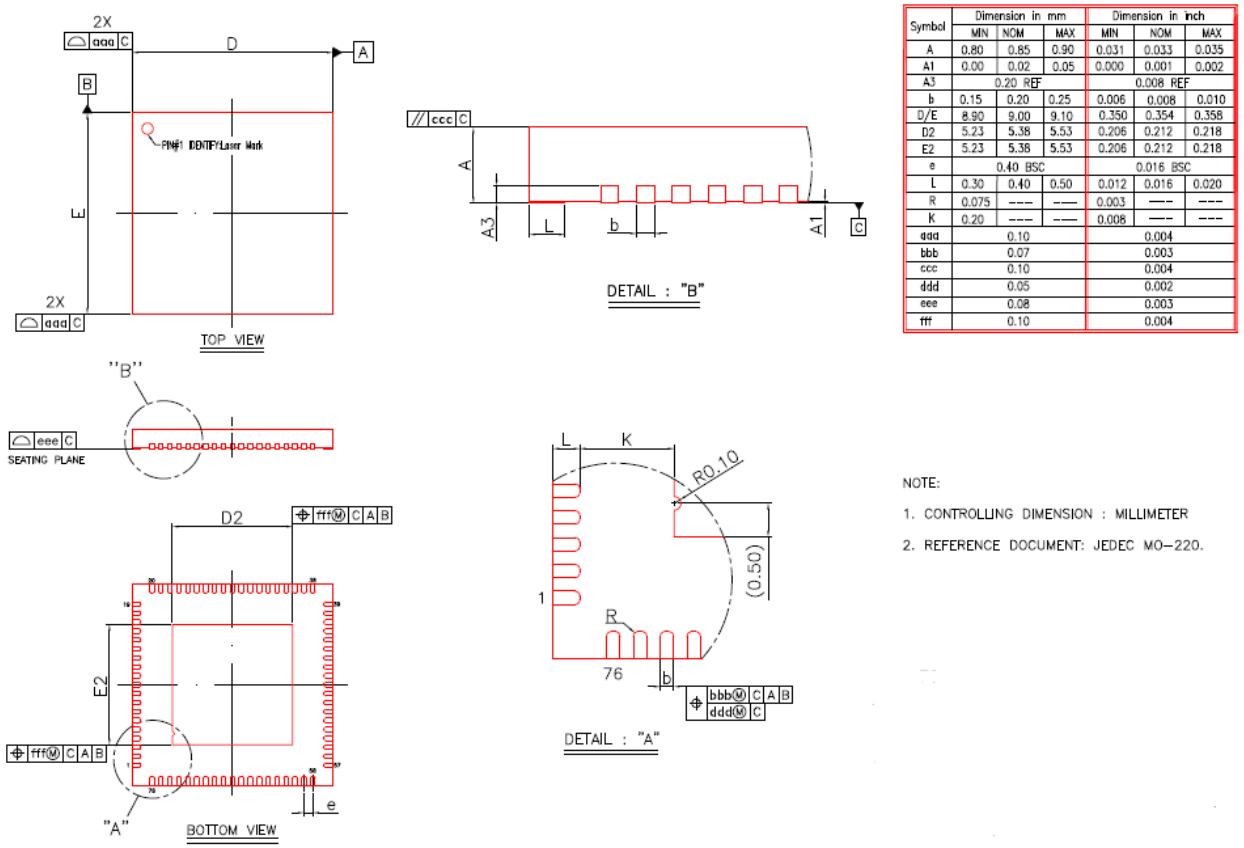


Figure 1 Block diagram

4 Package dimension



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	8.90	9.00	9.10	0.350	0.354	0.358
D2	5.23	5.38	5.53	0.206	0.212	0.218
E2	5.23	5.38	5.53	0.206	0.212	0.218
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 2 Package outline drawing of QFN76 9x9

5 Package pin-out

5.1 Pin assignment

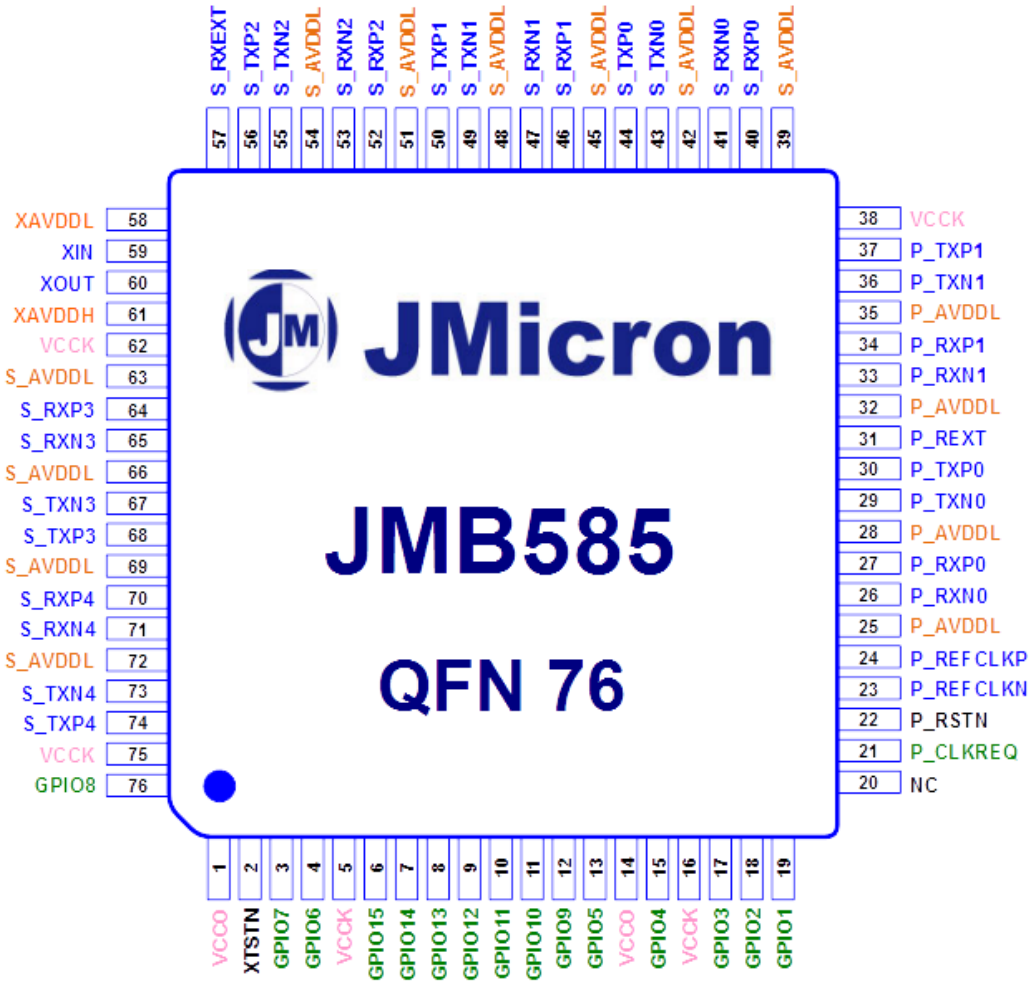


Figure 3 76-Pin assignment of JMB585

5.2 Pin type definition

Table 1 Pin type definition

Pin type	Definition
A	Analog
D	Digital
I	Input
O	Output
P	Power
IO	Bi-directional
L	Internal weak pull-low
H	Internal weak pull-high (Max. 85 kΩ, Typical 54 kΩ, Min. 36 kΩ)

5.3 Pin description

5.3.1 PCIe interface

Table 2 Pin description – PCIe interface

Signal Name	QFN 76	Type	Description
P_RXN0	26	AI	**PCIe Port RX- Signal of Lane 0**
P_RXP0	27	AI	**PCIe Port RX+ Signal of Lane 0**
P_TXN0	29	AO	**PCIe Port TX- Signal of Lane 0** A 200 nF capacitor should be connected between this pin and PCIe connector.
P_TXP0	30	AO	**PCIe Port TX+ Signal of Lane 0** A 200 nF capacitor should be connected between this pin and PCIe connector.
P_REXT	31	AI	**External Reference Resistance** A 12 kΩ±1% external resistor should be connected to this pin.
P_RXN1	33	AI	**PCIe Port RX- Signal of Lane 1**
P_RXP1	34	AI	**PCIe Port RX+ Signal of Lane 1**
P_TXN1	36	AO	**PCIe Port TX- Signal of Lane 1** A 200 nF capacitor should be connected between this pin and PCIe connector.
P_TXP1	37	AO	**PCIe Port TX+ Signal of Lane 1** A 200 nF capacitor should be connected between this pin and PCIe connector.
P_REFCLKP	24	DI	**Differential Clock P** 100Mhz reference clock from Host.
P_REFCLKN	23	DI	**Differential Clock N** 100Mhz reference clock from Host.
P_RSTN	22	DI	**PCIE Reset from Host**
P_CLKREQ	21	DIO	**This is for L1 substate**

5.3.2 SATA Gen 3 interface

Table 3 Pin description – SATA 3.1 Gen 3

Signal Name	QFN 76	Type	Description
S_RXP0	40	AI	**SATA Port0 RX+ Signal**
S_RXN0	41	AI	**SATA Port0 RX- Signal**
S_TXN0	43	AO	**SATA Port0 TX- Signal** A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP0	44	AO	**SATA Port0 TX+ Signal** A 10 nF capacitor should be connected between this pin and SATA connector.
S_RXP1	46	AI	**SATA Port1 RX+ Signal**
S_RXN1	47	AI	**SATA Port1 RX- Signal**
S_TXN1	49	AO	**SATA Port1 TX- Signal** A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP1	50	AO	**SATA Port1 TX+ Signal** A 10 nF capacitor should be connected between this pin and SATA connector.
S_RXP2	52	AI	**SATA Port2 RX+ Signal**
S_RXN2	53	AI	**SATA Port2 RX- Signal**
S_TXN2	55	AO	**SATA Port2 TX- Signal** A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP2	56	AO	**SATA Port2 TX+ Signal** A 10 nF capacitor should be connected between this pin and SATA connector.
S_RXP3	64	AI	**SATA Port3 RX+ Signal**
S_RXN3	65	AI	**SATA Port3 RX- Signal**
S_TXN3	67	AO	**SATA Port3 TX- Signal** A 10 nF capacitor should be connected between this pin and SATA connector.

S_TXP3	68	AO	**SATA Port3 TX+ Signal** A 10 nF capacitor should be connected between this pin and SATA connector.
S_RXP4	70	AI	**SATA Port4 RX+ Signal**
S_RXN4	71	AI	**SATA Port4 RX- Signal**
S_TXN4	73	AO	**SATA Port4 TX- Signal** A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP4	74	AO	**SATA Port4 TX+ Signal** A 10 nF capacitor should be connected between this pin and SATA connector.

5.3.3 Crystal interface

Table 4 Pin description – Crystal interface

Signal Name	QFN 76	Type	Description
XIN	59	AI	**Crystal Input/Oscillator Input** It is connected to a 25MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage range is 3.3V±5%.
XOUT	60	AO	**Crystal Output** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved for No Connection (NC). The output variation range is around ±30ppm (input dependent). And the output voltage range is 3.3V±5% (input dependent).

5.3.4 Control and GPIO interface

Table 5 Pin description – Control and GPIO interface

Signal Name	QFN 76	Type	Description
XTSTN	2	DI	**MP Test Mode Enable** Schmitt trigger input pin. This pin is reserved for IC mass production testing. Keep this pin to logic “1” in normal operation.
GPIO1	19	DO	**SPI SI : SPI Flash SI Pin.**
GPIO2	18	DO	**SPI CK : SPI Flash CK Pin**
GPIO3	17	DO	**SPI WP# : SPI Flash WP# Pin**

Signal Name	QFN 76	Type	Description
GPIO4	15	DI	**SPI SO : SPI Flash SO Pin**
GPIO5	13	DO	**SPI CE# : SPI Flash CE# Pin**
GPIO6	4	DO	**SATA0 LED : SATA Port 0 PWM (PHY Ready / Link Busy / Sleep Dim)**
GPIO7	3	DO	**SATA1 LED : SATA Port 1 PWM (PHY Ready / Link Busy / Sleep Dim)**
GPIO8	76	DO	**SATA2 LED : SATA Port 2 PWM (PHY Ready / Link Busy / Sleep Dim)**
GPIO9	14	DO	**SATA3 LED : SATA Port 3 PWM (PHY Ready / Link Busy / Sleep Dim)**
GPIO10	11	DO	**SATA4 LED : SATA Port 4 PWM (PHY Ready / Link Busy / Sleep Dim)**
GPIO11	10	DIO	**GPO11 : General Purpose I/O**
GPIO12	9	DIO	**GPO12 : General Purpose I/O**.
GPIO13	8	DIO	**GPO13 : General Purpose I/O**
GPIO14	7	DIO	**GPO14 : General Purpose I/O**
GPIO15	6	DIO	**GPO15 : General Purpose I/O**

5.3.5 Power supply

Table 6 Pin description – Power supply interface

Signal Name	QFN 76	Type	Description
VCCK	5,16, 38, 62, 75	PI	**1.25V core power supply**
VCCO	1,14	PI	**3.3V I/O power supply**
P_AVDDL	25,28,32, 35	PI	**Analog 1.25V power supply for PCIe**
S_AVDDL	39,42,45, 48,51,54, 63,66,69, 72	PI	**Analog 1.25V power supply for SATA**
XAVDDL	58	PI	**Analog 1.25V power supply for crystal oscillator**
XAVDDH	61	PI	**Analog 3.3V power supply for crystal oscillator**

6 Clock and reset

6.1 Crystal input

Single crystal input (25MHz) is needed.

Table 7 Crystal electrical specification

Parameter	Symbol	Min	Typical	Max	Unit
Crystal Frequency	f_{clk}		25		MHz
Long term stability (Crystal Only)	$\Delta f_{MAX\_Crystal}$	-30		30	ppm

7 Electrical characteristics

7.1 Absolute maximum rating

Table 8 Absolute maximum rating

Parameter	Symbol	Condition	Min	Max	Unit
Digital 3.3V	$VCCO_{(ABS)}$		-0.5	VCCO+0.5	V
Digital 1.25V	$VCCK_{(ABS)}$		-0.5	VCCK+0.5	V
Analog 3.3V	XAVDDH		-0.5	XAVDDH+0.5	V
Analog 1.25V	$XAVDDL_{(ABS)}$		-0.5	XAVDDL+0.5	V
Analog 1.25V	$S\_AVDDL_{(ABS)}$		-0.5	S_AVDDL+0.5	V
Analog 1.25V	$P\_AVDDL_{(ABS)}$		-0.5	P_AVDDL+0.5	V
Digital I/O input voltage	$V_{I(D)}$		-0.5	VCCO+0.5	V
Storage temperature	$T_{STORAGE}$		-40	150	^oC

7.2 Operating voltage and temperature

Table 9 Operating voltage and temperature

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO		3.0	3.3	3.6	V
Digital 1.25V	VCCK		1.20	1.25	1.30	V
Analog 3.3V	XAVDDH		3.0	3.3	3.6	V
Analog 1.25V	XAVDDL S_AVDDL P_AVDDL		1.20	1.25	1.30	V
Digital I/O input voltage	$V_{I(D)}$		3.0	3.3	3.6	V
Ambient operation temperature	T_A		0		70	^oC
Junction Temperature	T_J				125	^oC

7.3 External clock source conditions

Table 10 External clock source conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				25		MHz
Clock Duty Cycle			45	50	55	%

7.4 Power dissipation

7.4.1 PCIe to SATA mode

7.4.1.1 Operation with PCIe L0 state

Table 11 Power dissipation – Operation with PCIe L0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1		mA
Digital 1.25V	VCCK	Operate @ 1.25V		270		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1		mA
Analog 1.25V	XAVDDL	Operate @ 1.25V		18		mA
Analog 1.25V	S_AVDDL	Operate @ 1.25V		600		mA
Analog 1.25V	P_AVDDL	Operate @ 1.25V		300		mA

7.4.1.2 Idle with PCIe L0 state

Table 12 Power dissipation – Idle with PCIe L0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1		mA
Digital 1.25V	VCCK	Operate @ 1.25V		250		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1		mA
Analog 1.25V	XAVDDL	Operate @ 1.25V		18		mA
Analog 1.25V	S_AVDDL	Operate @ 1.25V		600		mA
Analog 1.25V	P_AVDDL	Operate @ 1.25V		300		mA

7.4.1.3 Suspend with PCIe L2 state

Table 13 Power dissipation – Suspend with PCIe L2 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1		mA
Digital 1.25V	VCCK	Operate @ 1.25V		100		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1		mA
Analog 1.25V	XAVDDL	Operate @ 1.25V		18		mA
Analog 1.25V	S_AVDDL	Operate @ 1.25V		330		mA
Analog 1.25V	P_AVDDL	Operate @ 1.25V		190		mA

7.5 I/O DC characteristics

Table 14 I/O DC characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	V_{IL}		-0.3		0.8	V
Input high voltage	V_{IH}		2		3.6	V
Output low voltage	V_{OL}				0.4	V
Output high voltage	V_{OH}		2.4			V
Output Current	I_{OH}		13.9	26.8	45.2	mA
Output Current	I_{OL}		9.8	14.4	19.1	mA

7.6 Power-on sequence

The power-on sequence is defined in Figure 4. Designers should follow all the rules for external power designs.

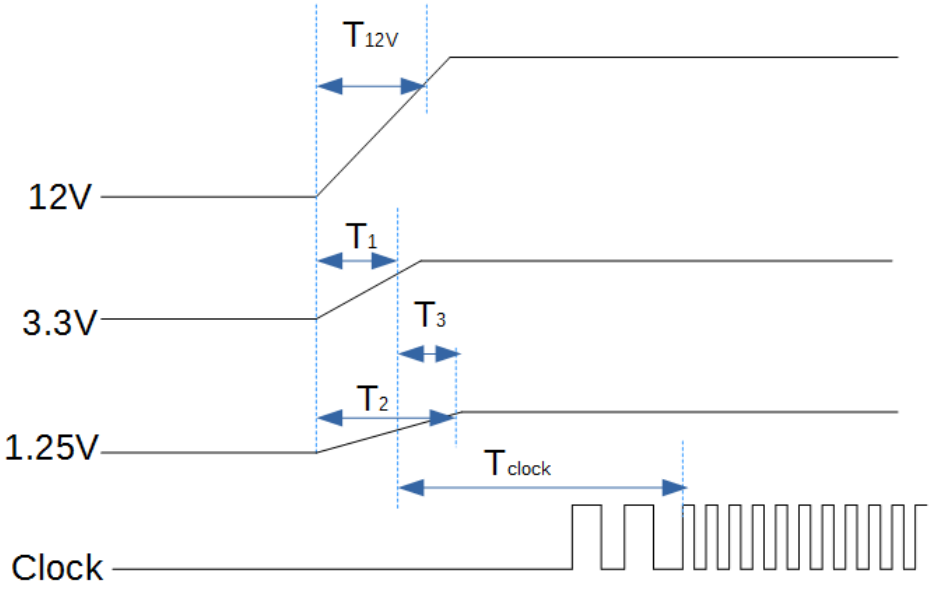


Figure 4 Power-on sequence

T_{12v}: Rise time for 12V power rail from 10% to 90%

T1: Rise time for 3V3 power rail from 10% to 90%

T2: Rise time for 1V25 power rail from 10% to 90%

T3: Time interval between 3V3 power and 1V25 Power

$T_{Clock:}$ Time interval between 3V3 and 90% clock swing

Note: Clock must meet 25MHz +/-30ppm during the sequence.

Table 15 Power-on timing requirements

Time	Minimum	Maximum
T_{12V}	-	10ms
T1	-	10ms
T2	-	10ms
T3	-5ms	5ms
Tclock	-	1ms

8 Product naming rule and identification

8.1 Format of the part number

The part number consists of the information of provider, product category, device number, package type, material type, product grade (operating temperature), mask ROM version and device version. The format of the part number is illustrated in Figure 5 below.

Figure 5 Format of the part number

8.2 Explanation of the part number

Table 17 explains each section of the part number illustrated in Figure 5 above.

Table 16 Explanation of the part number

Section	Length	Purpose	Code(s)	Meaning
a (JM)	2 digits	Brand name	JM	The provider **JM**icron
b (B)	1 digit	Product category	B	B = **B**ridge, S = **S**OC
c (585)	3 digits	Device number	585	The serial number assigned randomly to form the device name "**JMB585**" in conjunction with brand name and product category.
d (Q)	1 digit	Package type	B, L, Q, T	B = **B**GA; L = **L**QFP; Q = **Q**FN; T = **T**QFP
e (H)	1 digit	Material & grade	G, H, I, J	**G** = Gold wired RoHS compliant halogen-free green product; Ta: 0 ~ 70°C. **H** = Copper wired RoHS compliant halogen-free green product; Ta: 0 ~ 70°C. **I** = Gold wired RoHS compliant halogen-free green product; Ta: -40 ~ 85°C. **J** = Copper wired RoHS compliant halogen-free green product; Ta: -40 ~ 85°C.

Section	Length	Purpose	Code(s)	Meaning
f (B)	1 digit	Internal bonding type	A, B, C, …	A, B, C, …
g (A0)	2 digit	Version of mask ROM	A0, A1, A2, … B0, B1, B2, … Z0	Version **A0**, **A1**, **A2**, … Version **B0**, **B1**, **B2**, … Version **Z0** = no mask ROM
h (A)	1 digit	Version of the IC	A, B, C, …	Version **A**, **B**, **C**, …

8.3 Top mark

Each device has its unique top mark containing the information of provider, device name, part number, manufacturing date code, lot number and pin one identifier for identification. The top mark is illustrated in Figure 6 below.

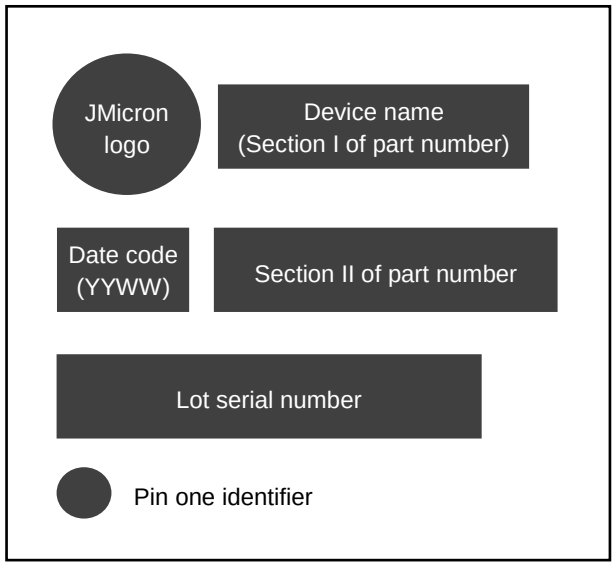


Figure 6 Illustration of device top mark