ASMEDIA TECHNOLOGY INC

ASM1064 SATA Host Controller Datasheet

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	May 2, 2019	First release
0.2	July 8, 2019	Fix pin description
0.3	July 25, 2019	1. Add strapping information in pin description 2. Change strapping pin note 3. Fix UPE_CLK* to PECLK* 4. Add chip temperature information 5. Add chip power consumption data
1.0	June 1, 2020	Remove suspend power description
1.1	Oct. 12, 2020	Change max payload size to 256Byte

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1. Introduction

ASM1064, a SATA host controller(AHCI) with upstream PCIe Gen3 x1 and downstream four SATA Gen3 ports. It's a low latency, low cost and low power AHCI controller. With four SATA ports and cascaded port multipliers, ASM1064 can enable users to build up various high speed IO systems, including server, high capacity system storage or surveillance platforms.

1.1 Features of ASM1064

PCIe interface

- 1- lane PCIe® connecting with root port
- Automatic detection of lane configuration on boot-up
- Supporting transfer rate of 2.5Gb(250MB/s), 5Gb(500MB/s) or 8Gb(1GB/s) per lane
- Support L0s/L1/L23/L3 power saving states
- Support L1 substate deep power saving mode
- Support LTR
- Support AER
- Support SRIS
- Max Payload Size = 256Byte

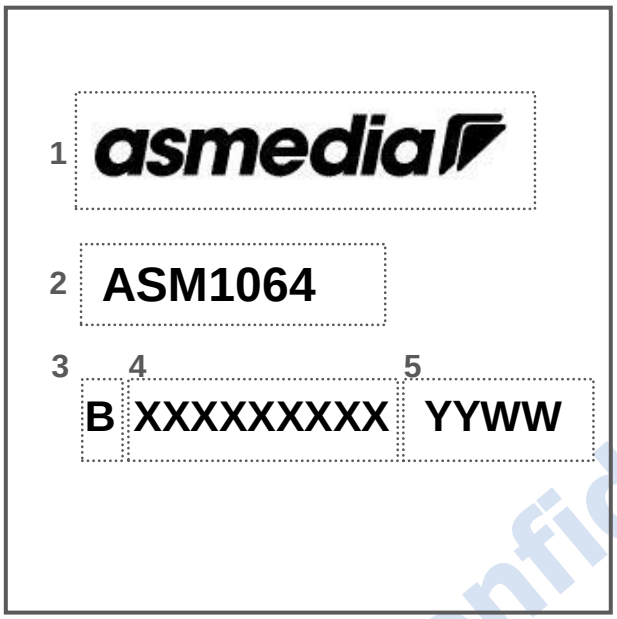
SATA interface

- AHCI SPEC Rev. 1.4
- Four SATA Gen3 (6GBps) ports
- Support NCQ
- Support SATA LED
- Supported port multiplier command based switching
- Support Partial/Slumber power management
- Support Device Sleep power management

General Features

- 25MHz Crystal
- Support SSC for both PCIe and SATA
- GPIO for extra IO control
- Package type: 8x8 QFN64

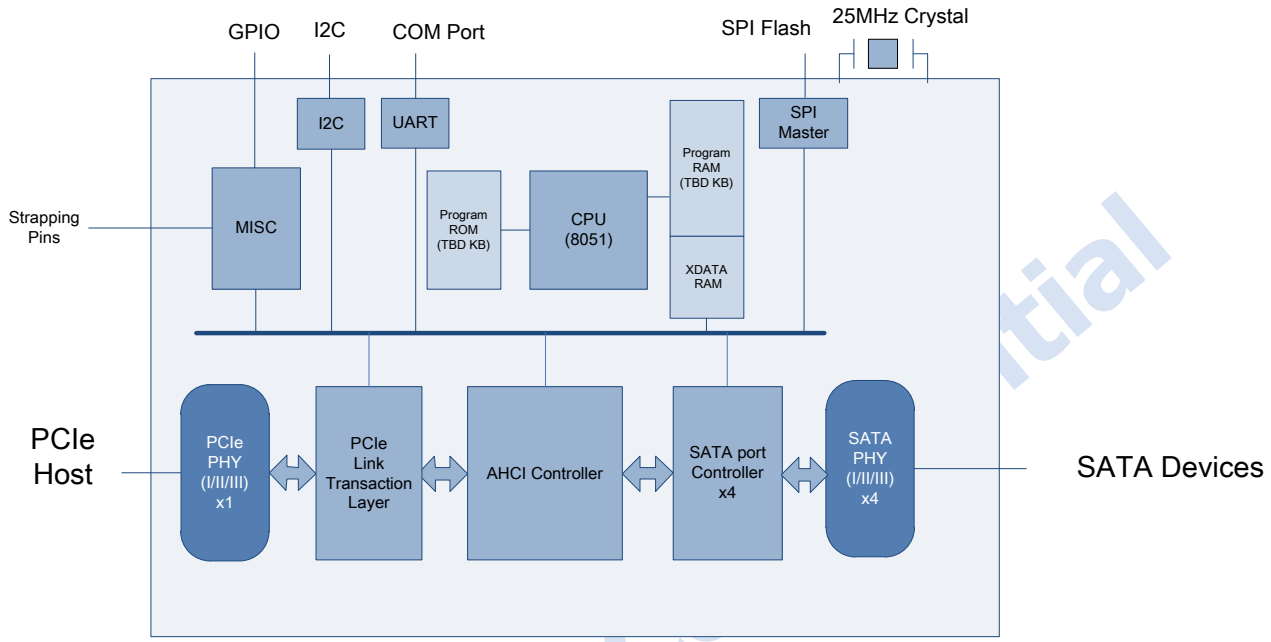
1.2 Branding and Part Number



1. asmedia: ASMedia Logo
2. ASM1064: Product Name
3. B: Version of ASMedia Logo
4. XXXXXXXXX: Serial No. Reserved for Vendor
5. YYWW: Date Code

1.3 ASM1064 Block Diagram

Figure 1 ASM1064 Block Diagram



2. Function Description

2.1 SATA port/LED/DEVSLP mapping

Table 1 SATA port / LED / DEVSLP mapping

SATA port	LED	DEVSLP
ST(R)XP(N)0	LED_S0	DEVSLP0
ST(R)XP(N)1	LED_S1	DEVSLP1
ST(R)XP(N)2	LED_S2	DEVSLP2
ST(R)XP(N)3	LED_S3	DEVSLP3

3. Pin Assignment

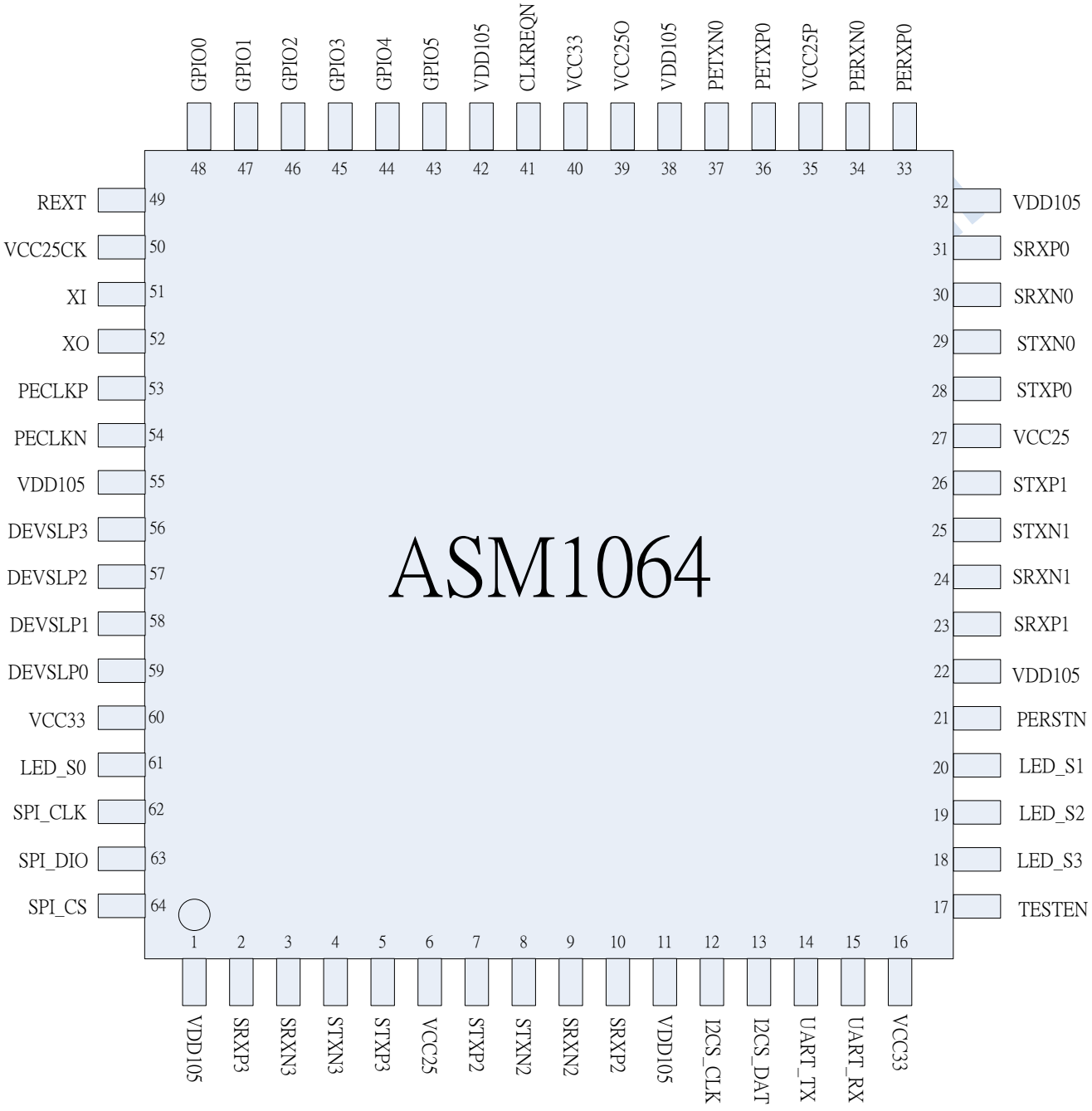


Figure 2 Pin Assignment

4. Pin Descriptions

4.1 Upstream PCI Express ® Interface

Table 2 Upstream Interface

Pin Name	Pin No.	Type	Voltage	Functional Description
PERXP0	33	A-I	VDD105 VCC25	Upstream PCIe® Lane 0 Receive positive
PERXN0	34	A-I		Upstream PCIe® Lane 0 Receive negative
PETXP0	36	A-O		Upstream PCIe® Lane 0 Transmit positive
PETXN0	37	A-O		Upstream PCIe® Lane 0 Transmit negative
PECLKP	53	A-I		PCIe® clock input positive
PECLKN	54	A-I		PCIe® clock input negative
CLKREQN	41	OD	VCC33	PCIe® clock request
PERSTN	21	I	VCC33	PCIe® reset
REXT	49	A-I	VCC25	External Reference Resistor with 12.1K ohm to GND for PCI Express

4.2 Downstream SATA Interface

Table 3 Downstream SATA Interface

Pin Name	Pin No.	Type	Voltage	Functional Description
SRXP0	31	A-I	VDD105 VCC25	SATA Port 0 Receive positive
SRXN0	30	A-I		SATA Port 0 Receive negative
STXP0	28	A-O		SATA Port 0 Transmit positive
STXN0	29	A-O		SATA Port 0 Transmit negative
SRXP1	23	A-I		SATA Port 1 Receive positive
SRXN1	24	A-I		SATA Port 1 Receive negative
STXP1	26	A-O		SATA Port 1 Transmit positive
STXN1	25	A-O		SATA Port 1 Transmit negative
SRXP2	10	A-I		SATA Port 2 Receive positive
SRXN2	9	A-I		SATA Port 2 Receive negative
STXP2	7	A-O		SATA Port 2 Transmit positive
STXN2	8	A-O		SATA Port 2 Transmit negative
SRXP3	2	A-I		SATA Port 3 Receive positive
SRXN3	3	A-I		SATA Port 3 Receive negative
STXP3	5	A-O		SATA Port 3 Transmit positive
STXN3	4	A-O		SATA Port 3 Transmit negative
LED_S0	61	OD	VCC33	SATA Port 0 LED
LED_S1	20	OD		SATA Port 1 LED
LED_S2	19	OD		SATA Port 2 LED
LED_S3	18	OD		SATA Port 3 LED
DEVSLP0	59	I/O		SATA Port 0 Device Sleep / GPIO
DEVSLP1	58	I/O		SATA Port 1 Device Sleep / GPIO
DEVSLP2	57	I/O		SATA Port 2 Device Sleep / GPIO
DEVSLP3	56	I/O		SATA Port 3 Device Sleep / GPIO

4.3 Miscellaneous Pins

Table 4 Miscellaneous Pins

Pin Name	Pin No.	Type	Voltage	Functional Description
TESTEN	17	I	VCC33	Test enable
UART_TX	14	O		UART Transmit /test purpose (Strapping of SRIS mode, SRIS_EN#)

UART_RX	15	I		UART Receive
SPI_SDIO	63	I/O		SPI Interface, Data in/out (Strapping of SATA SSC enable, SSSC_EN)
SPI_CLK	62	I/O		SPI Interface, Clock (Strapping of PCIe SSC enable, PSSC_EN)
SPI_CS	64	O		SPI Interface, Chip Select
I2CS_CLK	12	I/O		I2C clock
I2CS_DAT	13	I/O		I2C data
XI	51	I		Crystal in
XO	52	O		Crystal out
GPIO0	48	I/O		General Purpose Input/Output 0
GPIO1	47	I/O		General Purpose Input/Output 1
GPIO2	46	I/O		General Purpose Input/Output 2
GPIO3	45	I/O		General Purpose Input/Output 3
GPIO4	44	I/O		General Purpose Input/Output 4
GPIO5	43	I/O		General Purpose Input/Output 5

4.4 Power/Ground Pins

Table 5 Power/Ground Pins

Pin Name	Pin No.	Voltage/GND	Description
VCC25	6, 27	2.5V	PHY power (PCIe)
VCC25P	35	2.5V	PHY power (SATA)
VCC25CK	50	2.5V	PHY power (Clock Gen)
VCC25O	39	2.5V	LDO power output
VCC33	16, 40, 60	3.3V	Digital IO Power
VDD105	1, 11, 22, 32, 38, 42, 55	1.05V	Core Logic Power

4.5 Strap Information

Table 6 Strap Information

Strapping pins	Function
TESTEN	Test mode enable 1: Test mode 0: Function mode
SRIS_EN#	SRIS mode 1: SRIS mode disable 0: SRIS mode enable
PSSC_EN	PCIe SSC enable 1: PCIe SSC enable 0: PCIe SSC disable
SSSC_EN	SATA SSC enable 1: SATA SSC enable 0: SATA SSC disable

Note: PSSC_EN is available only when SRISP_EN# = 1'b0. If SRISP_EN# = 1'b1, PCIe SSC follows 100MHz clock source.

Strap timing requirement

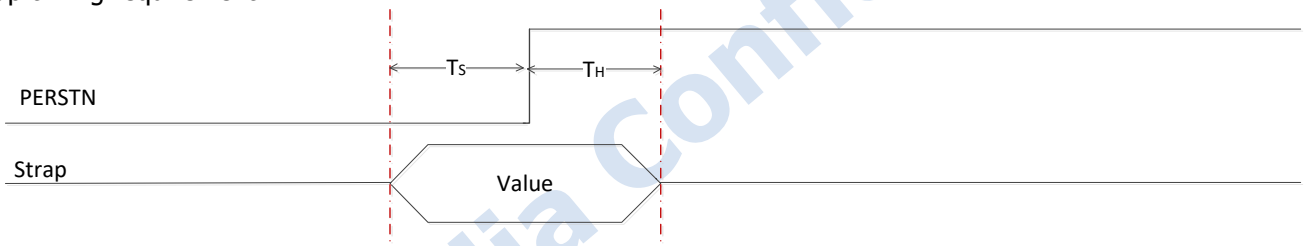


Figure 3 Strap timing diagram

Table 7 Strap timing requirement

	Parameter	Min	Max	Unit
Ts	Setup time for capture	1		ms
TH	Hold time for capture	1		ms

5. Power Sequence and Timing

Power up & Power down sequence

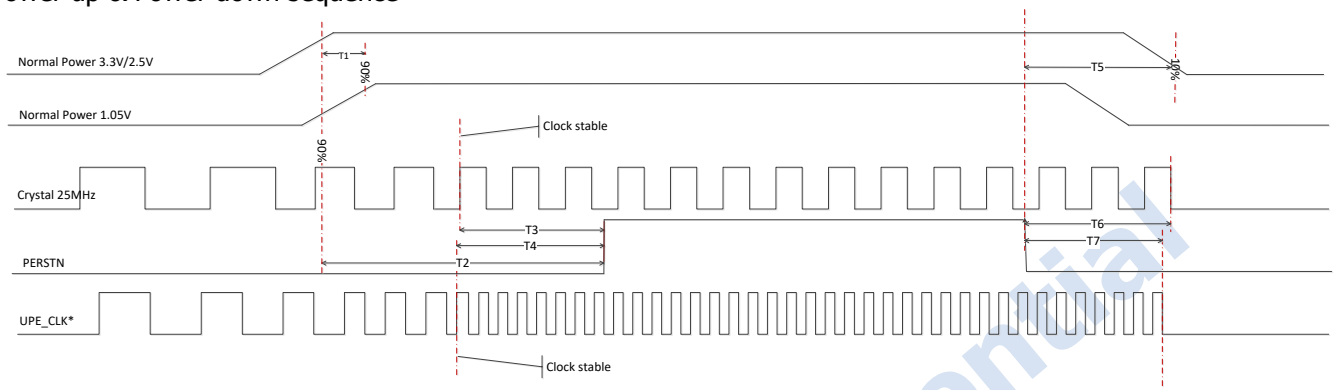


Figure 4 Power Sequence

Table 8 Power Sequence Timing

Symbol	Minimum	Maximum	Description
T1	0us	20ms	Normal power 3.3V/2.5V to Normal power 1.05V
T2	100ms		Normal power 3.3V/2.5 to PERSTN deassert
T3	1ms		Crystal stable to PERSTN deassert
T4	100us		UPE_CLK* stable to PERSTN deassert
T5	1us		PERSTN asserted to Normal power off
T6	0us		PERSTN assert to Crystal off
T7	0us		PERSTN assert to UPE clock off

6. Electrical Characteristic

6.1 Power Rail Specification

6.1.1 Absolute Maximum Ratings

Table 9 Absolute Maximum Ratings

Parameter	Range	Unit
Power Supply for Core Power	-0.5 ~ VDD105 +0.5	V
Power Supply for PHY Power	-0.5 ~ VCC25 +0.5	V
Power Supply for IO Power	-0.5 ~ VCC33 +0.5	V
DC Input Voltage for IO	-0.5 ~ VCC33 +0.5	V
Output Voltage for IO	-0.5 ~ VCC33 +0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	
HBM ESD	+/-4KV	
MM ESD	+/-200V	

6.1.2 Recommended Operating Conditions

Table 10 Recommanded Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units
VCC33	Normal Power Supply	3.0	3.3	3.6	V
VCC25	Normal Power Supply	2.25	2.5	2.75	V
VDD105	Normal Power Supply	1.00	1.05	1.1	V
Tj	Operating Junction Temperature	0	25	90	ºC
Tc	Opertating Case Temperature	0	25	85	ºC

6.2 DC Characteristic

Table 11 Electrical Characteristic of Digital Pins (GPIO, Miscellaneous)

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
V_{IH}	Input High Level	2			V	
V_{IL}	Input Low Level			0.8	V	
V_{HYS}	Input Hysteresis	0.32	0.37	0.4	V	
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.4	1.6	1.8	V	
V_{TH-H2L}	VTH of Schmitt Trigger high to low	1	1.23	1.4	V	
R_{UP}	Internal Pull-up resistance while Vin=0V	65	96	140	KΩ	
	Internal Pull-up resistance while Vin=VCCH/2 V	38	56	81	KΩ	
I_{IL-UP}	Input pull-up leakage current while Vin=0V	21	34.4	56	uA	
	Input pull-up leakage current while Vin=VCCH/2 V	18	29.4	47	uA	
R_{DOWN}	Internal Pull-down resistance while Vin=0V	59	96	142	KΩ	
	Internal Pull-down resistance while Vin=VCCH/2 V	35	55	79	KΩ	
$I_{IL-DOWN}$	Input pull-down leakage current while Vin=0V	21	34.5	60	uA	
	Input pull-down leakage current while Vin=VCCH/2 V	18	30	50	uA	
V_{OH}	Output High Voltage @IOH	2.4			V	
V_{OL}	Output Low Voltage @IOL			0.4	V	
I_{OH}	Driving Current of Output High	12			mA	
I_{OL}	Driving Current of Output Low	12			mA	

6.3 System Clock Specification

6.3.1 System Clock Description

Table 12 System Clock Description

Clock Domain	Frequency	Source
XI, XO	25MHz	25MHz Crystal
PECLKP, PECLKN	100MHz	Main Clock Generator

6.3.2 System Clock Input Frequency Specification

Table 13 Crystal AC Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{XTAL}	Frequency		25		MHz
$\triangle f_{XTAL}$	Long Term Stability (at 25^0C)	-30		30	ppm
T_C	Temperature Stability	-30		30	ppm
FA	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

Table 14 Clock Oscillator Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{CLK}	Frequency		25		MHz
$\triangle f_{CLK}$	Long Term Stability (all condition)	-150		150	ppm
C_X	External Load Capacitance (Differential mode)		8		pF
C_{TOTAL}	Total External Equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	Pf
R_{TOTAL}	Total External Equivalent Series Resistance from XI pin to XO pin			60	Ω

Table 15 UPE_CLK AC Specification

Symbol	Parameter	100 MHz Input		Unit
		Min	Max	
V_{IH}	Differential Input high voltage	+150		mV
V_{IL}	Differential Input low voltage		-150mV	mV
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV
T_{PERIOD_AVG}	Average clock period accuracy	-300	+300	ppm
$T_{CCJITTER}$	Cycle to Cycle jitter		150	ps
T_{DC}	Reference Duty Cycle	40	60	%
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns
Falling Edge Rate	falling Edge Rate	-4.0	-0.6	V/ns

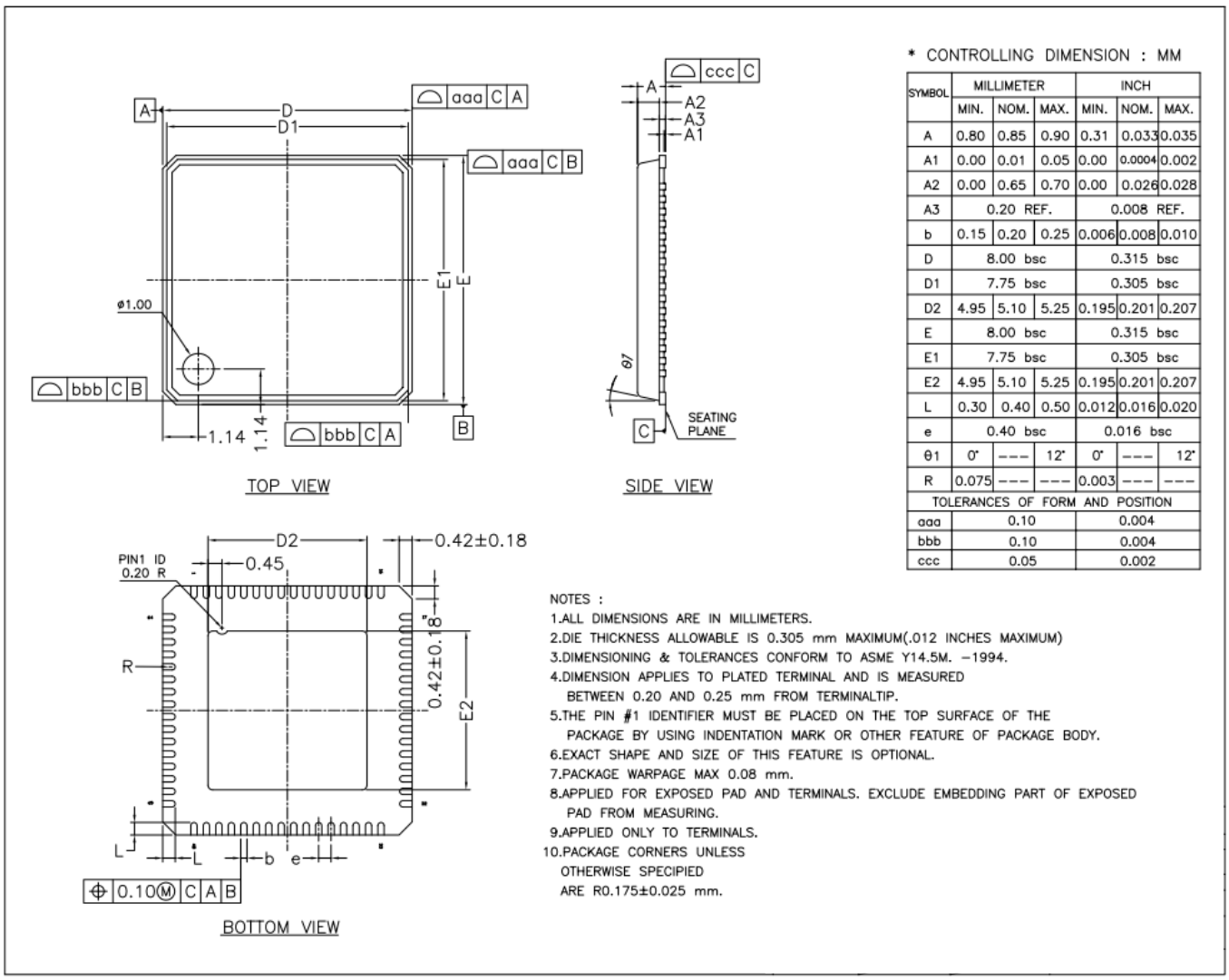
7. Power Consumption

Table 16 power consumption

	Full Running	Idle (L1 enable)	Suspend (Normal power off)
VCC33 (mA)	100	TBD	N/A
VDD105 (mA)	493		N/A
Total Power (mW)	847		0

8. Package Information

8.1 Package Overview



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.31	0.033	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	0.00	0.65	0.70	0.00	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	8.00 bsc			0.315 bsc		
D1	7.75 bsc			0.305 bsc		
D2	4.95	5.10	5.25	0.195	0.201	0.207
E	8.00 bsc			0.315 bsc		
E1	7.75 bsc			0.305 bsc		
E2	4.95	5.10	5.25	0.195	0.201	0.207
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Figure 5 Package information

8.2 Chip temperature

Table 17 Chip temperature equation

Symbol	Parameter	How to get?
Ta	Ambient temperature	Measure temperature around chip
Tj	Operating junction temperature	Tj = Θja * power + Ta
Tc	Operating case temperature	Tc = Tj - Ψjt * power
Θja	Junction to Ambient thermal resistance	Provided by package vendor: **25.8**
Ψjt	Junction to top thermal characterization	Provided by package vendor: **0.08**
Power	Chip power consumption	Measure chip power consumption (Max: 0.847 W)

- **Thermal test board condition, please refer to JEDEC JESD51-5**
- **Thermal Test Method Environmental Conditions refer JESD51-2**
- **Example: If chip power consumption is TBDW; Ta=25^{0}C**
  Tj = 25.8 * 0.847 + 25 = 46.8^{0}C
  Tc = 46.8 – 0.08 * 0.847 = 46.7^{0}C