ASMEDIA TECHNOLOGY INC

ASM1153E Datasheet

USB3.0 to SATA Bridge Controller

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	August 2, 2013	Initial Release
0.2	August 9, 2013	Add the power on sequence spec Update the Vcore spec Upadte the unit of I_{IL-UP}/I_{IL-DN} of GPIO

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1. General Description

Engaged in Universal Serial Bus I/O solution and Storage application development, ASMedia Technology is committed to expand product portfolio with introducing a new generation of USB3.0 to SATA 6Gbps bridge Products.

ASM1153E is the ASMedia third generation single chip solution, bridging the USB3.0 to Serial ATA host interface with highly integrated SuperSpeed USB3.0, High Speed USB2.0 and SATA1.5/3.0/6.0 Gbps ASMedia self-design PHYs. Along with excellent compatibility with USB3.0 hosts and SATA devices, ASM1153E uses advanced process technology to optimize the chip power consumption. Furthermore, it is also pin-to-pin backward compatible with existing ASM1053.

Customers can easily enhance their storage device performance with ASM1153E since it is also integrated 8-bit micro-processor and embedded RAM to provide a cutting edge solution in USB to SATA device enclosure market.

2. Features

- ◇ Compliant with USB3.0 Specification Revision 1.0
- ◇ Compliant with USB Specification Revision 2.0
- ◇ Support USB Super-Speed, High-Speed and Full-Speed Operation
- ◇ Support USB Mass Storage Class, Bulk-Only Transport Specification Revision 1.3
- ◇ Support USB Attached SCSI Protocol Specification Revision 1.0
- ◇ Compliant with Serial ATA Specification Revision 3.0
- ◇ Serial ATA bus up to 6Gbps Signal bandwidth
- ◇ Support Spread Spectrum Control of USB3.0 and SATA interface to improve the EMI performance
- ◇ Support ATA/ATAPI Packet Command Set
- ◇ Support ATA/ATAPI LBA48 addressing mode
- ◇ Integrated 8-bit micro-processor with embedded program RAM and ROM
- ◇ Support SPI NVRAM for Vender Specific Application of USB Device Controller
- ◇ Support multi-GPIO pins
- ◇ Support programmable PWMs
- ◇ Support 20/25/30MHz with external crystal mode or 30MHz with Clock input mode via strapping
- ◇ Integrated two internal voltage regulator for IO power and Core
- ◇ HBM ESD 2KV and MM ESD 200V

3. Package Type

- ◇ Green Package 6x6 QFN 48L (Pb-free)

4. Functional Diagram

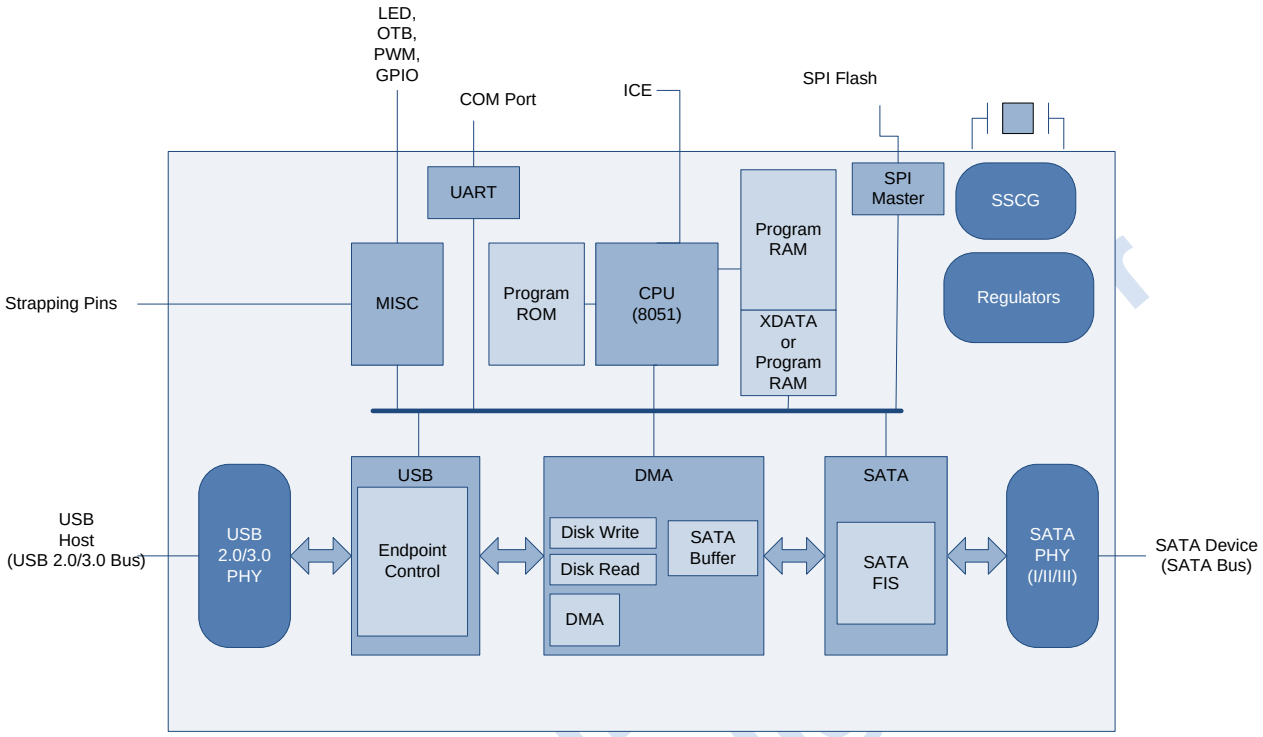


Figure 1: Functional Diagram of ASM1153E

5. Pinout Diagrams

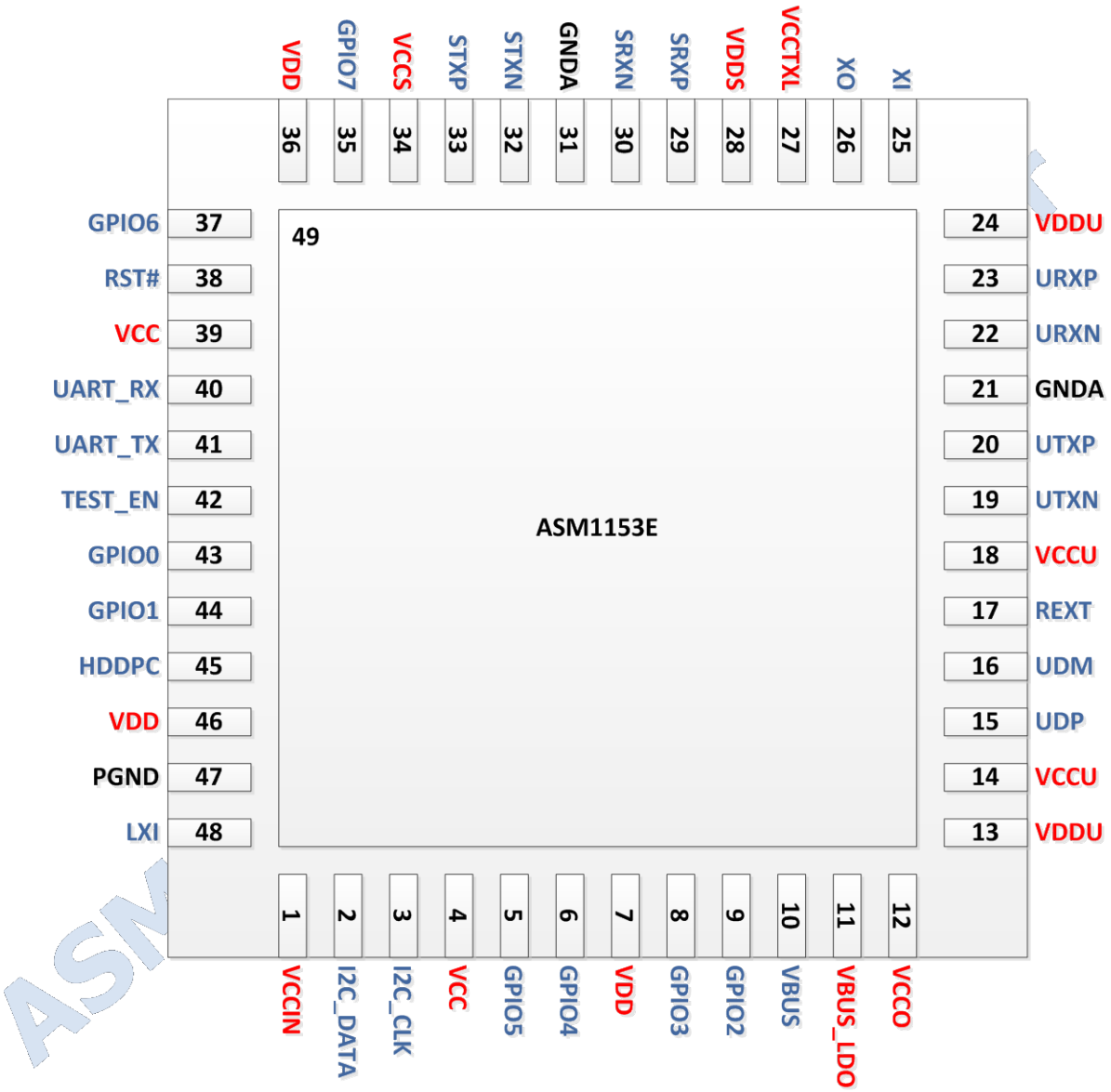


Figure 2: ASM1153E Pinout

6. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
P	Power pin
G	Ground pin
OD	Open Drain

Pin No.	Name	TYPE	Descriptions
USB interface			
16	UDM	DB	USB2.0 negative Data Signal
15	UDP	DB	USB2.0 positive Data Signal
19	UTXN	DO	SuperSpeed USB negative Transmitter Signal
20	UTXP	DO	SuperSpeed USB positive Transmitter Signal
22	URXN	DI	SuperSpeed USB negative Receiver Signal
23	URXP	DI	SuperSpeed USB positive Receiver Signal
SATA interface			
29	SRXP	DI	SATA positive Receiver Signal
30	SRXN	DI	SATA negative Receiver Signal
32	STXN	DO	SATA negative Transmitter Signal
33	STXP	DO	SATA positive Transmitter Signal
System Signals			
42	TEST_EN	I	Test Enable Signal, with internal pull-down resistor 0: Normal Mode (Default) 1: Test Mode Enable
2	I2C_DATA	B	Used as I2C_DATA signal or SPI_DI signal, defined by strapping pin 37 GPIO6. Used as General Purpose IO after power on. Integrated pull-up resistor.
3	I2C_CLK	B	Used as I2C_CLK signal or SPI_CLK signal, defined by strapping pin 37 GPIO6. Used as General Purpose IO after power on. Integrated pull-up resistor.
5	GPIO5	B	General Purpose IO, used as SPI_DO, with internal pull-up resistor.
6	GPIO4	B	General Purpose IO, used as SPI_CS0, with internal pull-up resistor.
8	GPIO3	B	General Purpose IO, used as strapping pin for clock source select while power on. Refer to the strapping table. Integrated pull-up resistor.
9	GPIO2	B	General Purpose IO, used as SPI_CS1, with internal pull-up resistor.
35	GPIO7	B	General Purpose IO, use as strapping for clock source select while power on. Refer to the strapping table. Integrated pull-up resistor.
37	GPIO6	B	General Purpose IO, used as strapping for external ROM enabling via SPI interface. Refer to the strapping table. Integrated pull-up resistor.
40	UART_RX	B	URAT_RX while debug mode, Used as General Purpose IO after power on. Integrated pull-up resistor.
41	UART_TX	B	UART_TX while debug mode, Used as General Purpose IO after power on. Integrated pull-up resistor.
43	GPIO0	B	General Purpose IO. Integrated pull-up resistor.
44	GPIO1	B	General Purpose IO. Integrated pull-up resistor.
45	HDDPC	B	HDD power control pin, use as General Purpose IO. Integrated pull-up resistor. 0: Hard Drive Power Off 1: Hard Drive Power On
10	VBUS	I	USB Cable Power Detector
17	REXT	P	External Reference Resistor with 12.1Kohm +/-1%
38	RST#	I	Power Reset pin
Clock Interface			

Pin No.	Name	TYPE	Descriptions
25	XI	I	Crystal input or Clock input pin
26	XO	O	Crystal output or Clock output pin
27	VCCTXL	**P**	Power for Crystal and PLL circuit
Voltage Regulator			
11	VBUS_LDO	**P**	Linear regulator input
12	VCCO	**P**	Linear regulator output
1	VCCIN	**P**	Switching regulator input
48	LXI	**P**	Connect with external inductor
47	PGND	**G**	Ground for voltage regulator
Power and Ground			
14, 18	VCCU	**P**	USB high power pin
34	VCCS	**P**	SATA high power pin
13, 24	VDDU	**P**	USB low power pin
28	VDDS	**P**	SATA low power pin
7, 36, 46	VDD	**P**	Core power
4, 39	VCC	**P**	IO power
21, 31	GNDA	**G**	Analog Ground
49	GND	**G**	the exposed pad connected to common ground on PCB

6.1 Strapping Table

Pin	Function	Description
GPIO6	SPI Interface Select	0: SPI for External ROM 1: I2C (Default)
GPIO[3,7]	Clock Select	00: 25MHz Crystal 01: 30MHz Clock Input 10: 20MHz Crystal 11: 30MHz Crystal (Default)

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Stresses the below parameter listed under absolute maximum rating may cause the device permanent damage. This is a stress rating only, and the function operating of the device at these or any other conditions over those parameter in the recommended operating condition is not implied. It is recommended to have a clamp circuit to protect the device with abnormal exhibit voltage spikes while power is switched on or off.

Parameter	Range	Unit
Power Supply for VCC	-0.5 ~ VCC+0.5	V
Power Supply for VDD	-0.5 ~ VDD+0.5	
DC Input Voltage	-0.5 ~ VCC+0.5	V
Output Voltage	-0.5 ~ VCC+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

7.2 Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{CC}	IO Power Supply	2.3	3.3	3.6	V
V_{CCU}	USB Analog High Power Supply	2.3	3.3	3.6	V
V_{CCS}	SATA Analog High Power Supply	2.3	3.3	3.6	V
V_{DD}	Core Power Supply	1.0	1.05	1.28	V
V_{DDU}	USB Analog Low Power Supply	1.0	1.05	1.28	V
V_{DDS}	SATA Analog Low Power Supply	1.0	1.05	1.28	V
T_C	Operating Case Temperature	0	25	95	^{0}C
T_J	Operating Junction Temperature	0	25	120	^{0}C
HBM	Human Body mode ESD		+/-2		KV
MM	Machine Mode ESD		+/-200		V

7.3 DC Electrical Characteristics for VBUS pins

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Level	2			V
V_{IL}	Input Low Level			0.8	V
V_{HYS}	Input Hysteresis	0.57	0.6	0.65	mV
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.4		1.8	V
V_{TH-H2L}	VTH of Schmitt Trigger high to low	0.85		1.10	V

7.4 DC Electrical Characteristics for GPIO pins

Symbols	Parameter	VCC=3.3V			VCC=2.5V			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input High Level	2			1.55			V
V_{IL}	Input Low Level			0.8			0.6	V
V_{HYS}	Input Hysteresis	0.57	0.6	0.65	0.47	0.52	0.57	mV
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.38	1.6	1.8	1.1	1.3	1.5	V
V_{TH-H2L}	VTH of Schmitt Trigger high to low	0.89	1.07	1.22	0.63	0.78	0.94	V
R_{UP}	Internal Pull-up resistance while Vin=0V	70	103	143	97	148	216	KΩ
	Internal Pull-up resistance while Vin=VCC/2 V	40	58.2	79.2	53	80	115	KΩ

Symbols	Parameter	VCC=3.3V			VCC=2.5V			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
R_{DN}	Internal Pull-down resistance while Vin=0V	68	109	158	91	153	230	KΩ
	Internal Pull-down resistance while Vin=VCC/2 V	39	61.7	88	49	82.7	123	KΩ
I_{IL-UP}	Input pull-up current after Vin is read, Rup is off & Iil < 1uA when VIN=0	21	32	54	10	16.8	32	mA
	Input pull-up current after Vin is read, Rup is off & Iil < 1uA when VIN=VCC/2	19	28.4	48	9.8	15.6	28	mA
I_{IL-DN}	Input pull-down current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC	19	30.2	54	15.4	27.8	32	mA
	Input pull-down current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC/2	17	26.8	48	9.6	16.4	29	mA

7.5 DC Electrical Characteristics for RST# pins

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Level	2.6			V
V_{IL}	Input Low Level			1.4	V
V_{HYS}	Input Hysteresis	0.218	0.235	0.25	V
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.88		2.58	V
V_{TH-H2L}	VTH of Schmitt Trigger high to low	1.65		2.35	V
I_{IL}	Input pull-up leakage current while Vin=0V			1	uA

7.6 External Crystal Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{XTAL}	Frequency		20/25/30		MHz
Δf_{XTAL}	Long Term Stability (at 25^0C)	-30		30	ppm
T_C	Temperature Stability	-30		30	ppm
F_A	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

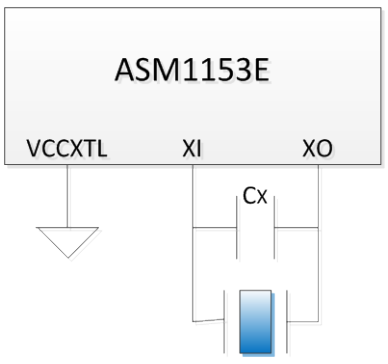


Figure 3: Differential Crystal Design

7.7 Differential Clock Oscillator Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{CLK}	Frequency		20/25/30		MHz
Δf_{CLK}	Long Term Stability (all condition)	-150		150	ppm
C_X	External Load Capacitance (Differential mode)		10		pF
C_{TOTAL}	Total External Equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	Pf
R_{TOTAL}	Total External Equivalent Series Resistance from XI pin to XO pin			60	Ω

7.8 External Clock Input Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
f_{CLK}	Frequency		30		MHz
Δf_{CLK}	Long Term Stability (all condition)	-100		100	ppm
Jitter	Input Clock cycle to cycle jitter Tolerance			150	ps
	Duty Cycle	45		55	%
t_R	Rising Edge rate	1.0		2.0	V/ns
t_F	Falling Edge rate	1.0		2.0	V/ns
V_{IH}	Clock Input High Level	2			V
V_{IL}	Clock Input Low Level			0.8	V

7.9 Internal Linear Regular Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{IN_LINEAR}	Input Voltage Range for internal linear regulator	4.5	5	5.5	V
V_{OUT_LINEAR}	Output Voltage Range for internal linear regulator	3.15	3.3	3.45	V
I_{MAX}	Maximum capacity of current output			200	mA

7.10 Internal Switching Regular Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{IN_SWITCH}	Input Voltage Range for internal switching regulator	2.3		5.5	V
V_{OUT_SWITCH}	Output Voltage Range for internal switching regulator	1.0	1.05	1.1	V
ΔV_N (p-p)	3.3V input voltage noise/ripple Range	-8		8	%
F_{OSC}	OSC frequency		1.7		MHz
I_{MAX}	Maximum capacity of current output			300	mA
$IP_{(LM)}$	P-channel current limiter		1		A

- **Strong recommend to have 10uF decoupling capacitor placed close to pin3 to filter the noise/ripple of 3.3V switching regulator input.**

7.11 Power Consumption Characteristics

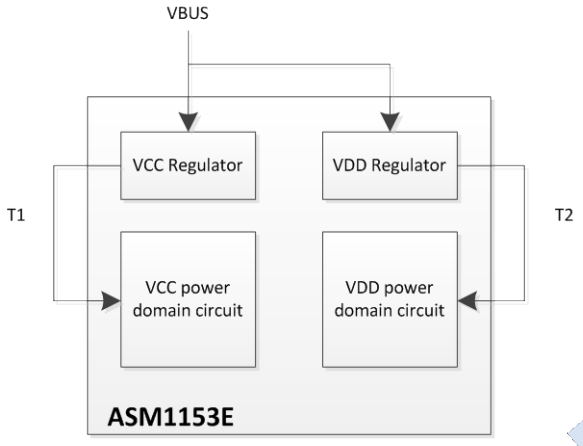


Figure 4: Test point for power consumption

Symbols	Parameter	Condition	USB3.0			USB2.0			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{VCC}	Total current consumed for 3.3V power domain (Test point T1)	Operating	30	40	50	17	27	37	mA
		Idle	30	40	50	17	27	37	mA
		suspend	1.0	1.5	2.5	1.0	1.5	2.5	mA
I_{VDD}	Total current consumed for 1.05V power domain (Test point T2)	Operating	150	170	190	83	98	113	mA
		Idle	110	125	140	83	98	113	mA
		suspend	1.5	2.5	3.8	1.5	2.5	3.8	mA

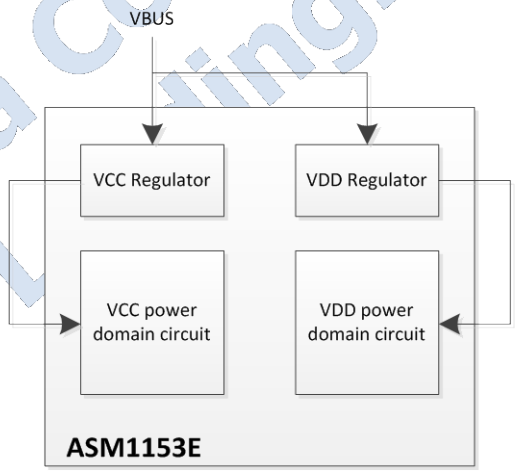


Figure 5: Test point on Type 1

Symbols	Parameter	Condition	USB3.0			USB2.0			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{VBUS}	Total current consumption for 5V (Test Point: Vbus)	Operating	75	85	95	65	75	85	mA
		Idle	65	75	85	65	75	85	mA
		suspend	1.5	2.5	3.5	1.5	2.5	3.5	mA
P_{VBUS}	Total power consumption for 5V (Test Point: Vbus)	Operating	375	425	475	325	375	425	mW
		Idle	325	375	425	325	375	425	mW
		suspend	7.5	12.5	17.5	7.5	12.5	17.5	mW

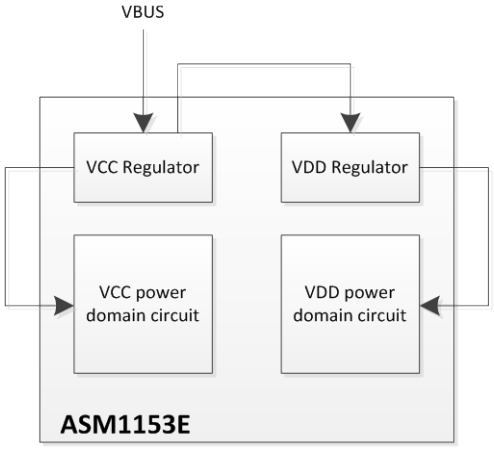


Figure 6: Test point for Type 2

Symbols	Parameter	Condition	USB3.0			USB2.0			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{VBUS}	Total current consumption for 5V (Test Point: Vbus)	Operating	95	105	115	75	85	95	mA
		Idle	75	85	95	75	85	95	mA
		suspend	1.5	2.5	3.5	1.5	2.5	3.5	mA
P_{VBUS}	Total power consumption for 5V (Test Point: Vbus)	Operating	475	525	575	375	425	475	mW
		Idle	375	425	475	375	425	475	mW
		suspend	7.5	12.5	17.5	7.5	12.5	17.5	mW

Notice: The different type of inductor for internal switching regulator will have different power consumption.

8. Power on Sequence

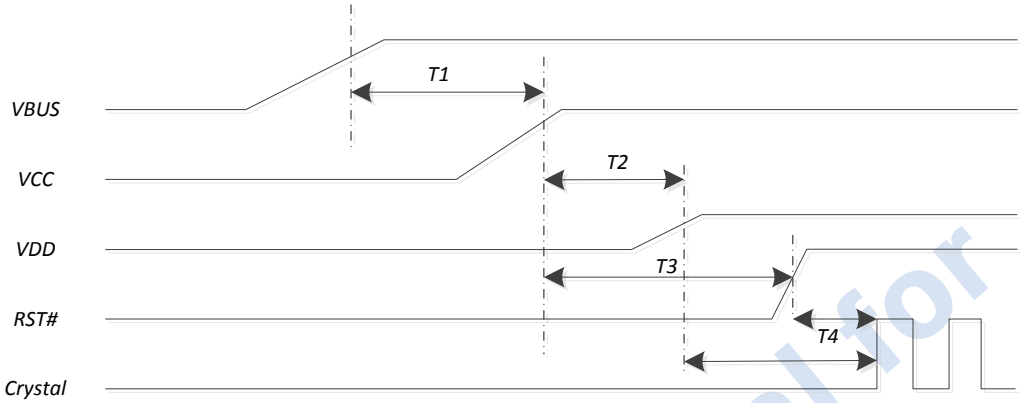


Figure 7: timing diagram

Symbols	Parameter	Min	Typ	Max	Unit	Remark
T1	The delay of VCC after VBUS is available	0	5	10	ms	Measure from 10% of VCC to 90% of VBUS For Self-powered system or external 5V to VCC regulator, this rule is not needed.
T2	The delay of VDD after VCC is available	40	64	90	ms	Measure from 10% of VCC to 90% of VDD For external VCC to VDD regulator, this rule is not needed.
T3	The delay of RST# after VCC is available	0		N/A	ms	Measure from 2V of RST# to 90% of VCC
T4	The crystal clock is stable after RST# and VDD is available	15	25	40	ms	Measure from 90% of VDD or 2V of RST#
TSLEW	Slew rate of VDD	0		10	ms	Measure from 10% to 90% of VDD

9. PCB Design Guide under Thermal Pad

To improve the thermal efficieny and signal integrity, it is recommended to place the thermal via under or near to thermal pad. To avoid the process issue, please make sure the thermal via fills with solder covering with solder mask. It is recommended to follow up the pattern on PCB as Figure 7 or Figure 8.

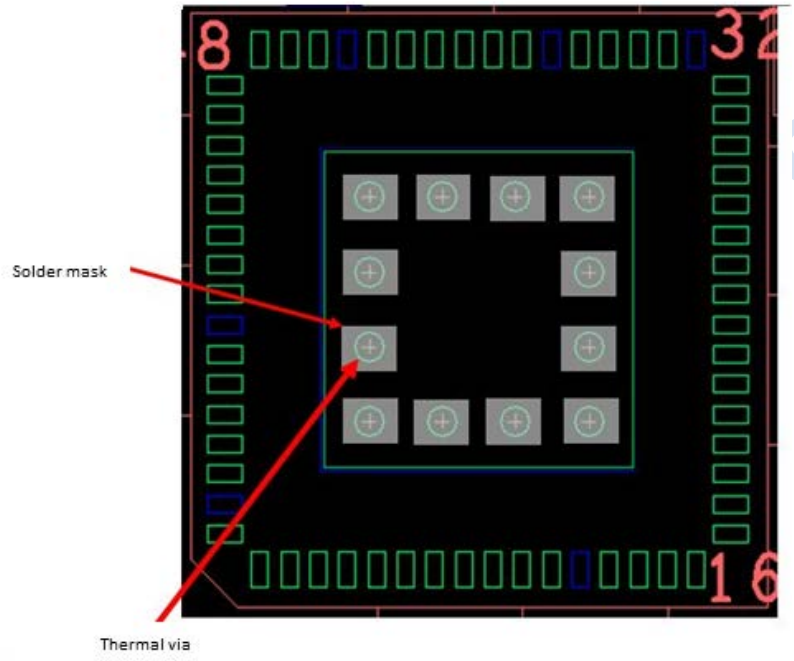


Figure 8: Symbol 1 for via design rule under Thermal pad

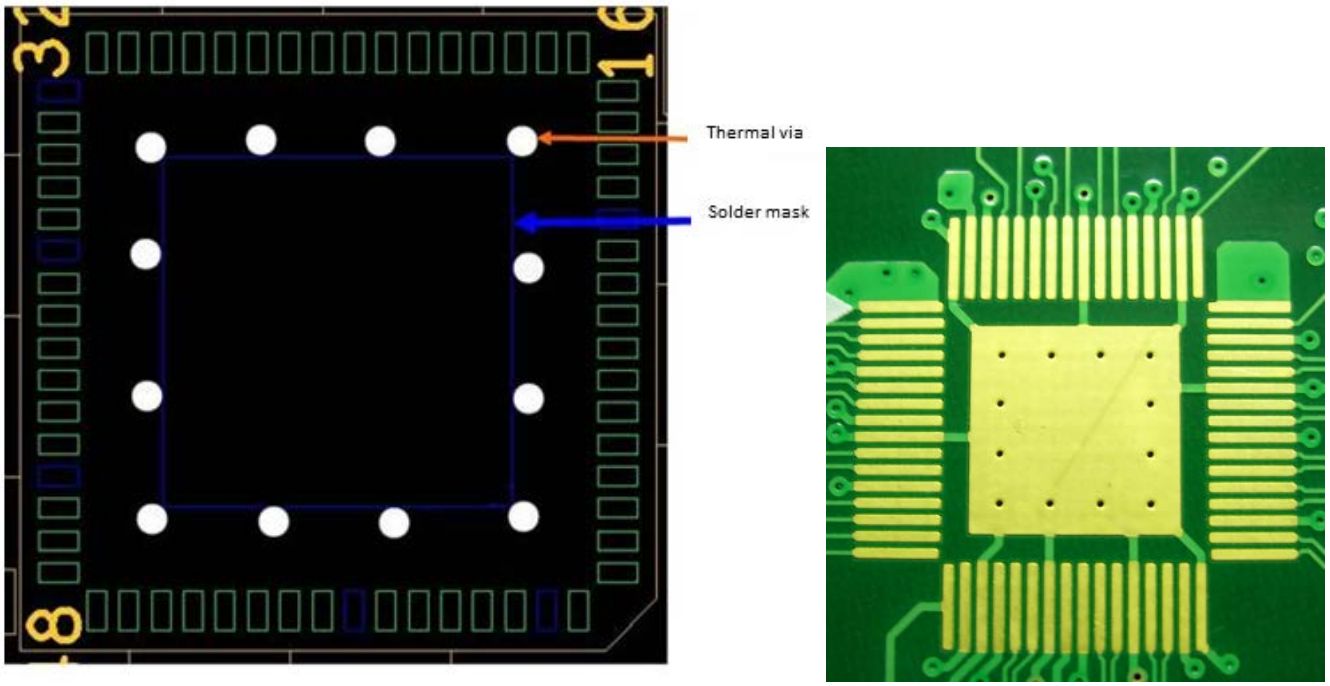
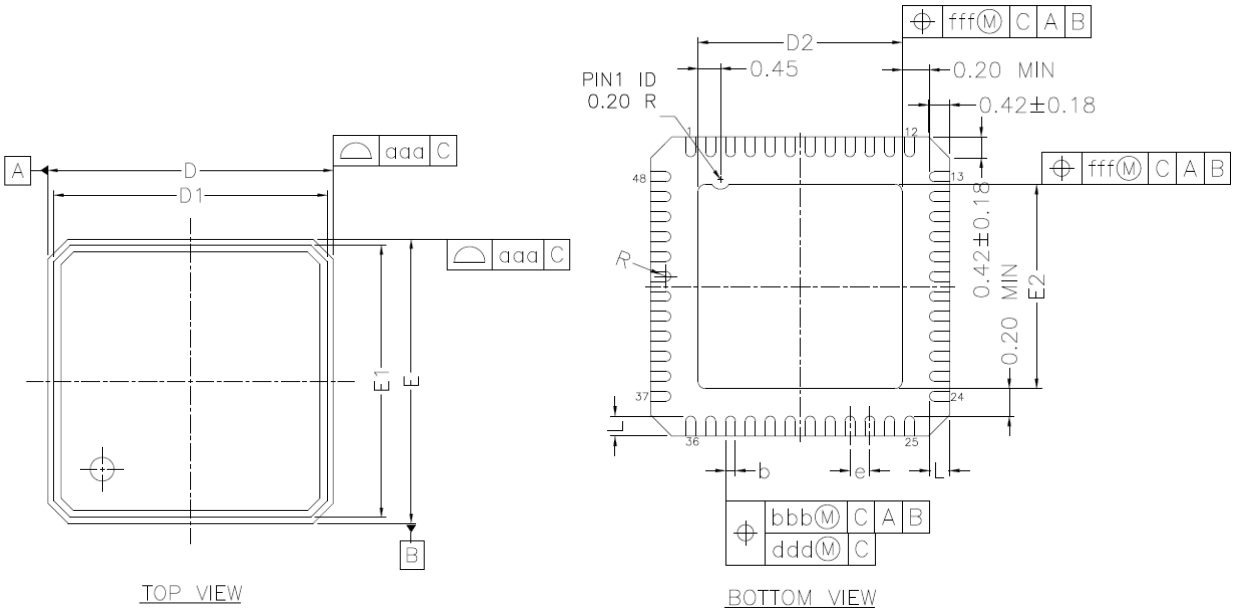


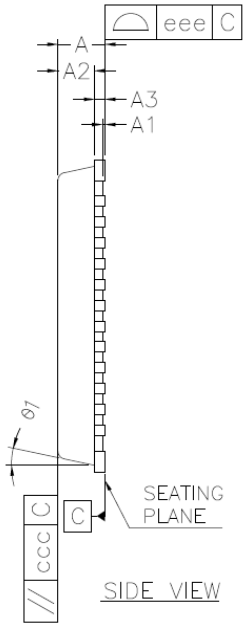
Figure 9: Symbol 2 for via design rule under Thermal pad

10. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.00	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 bsc			0.236 bsc		
D1	5.75 bsc			0.226 bsc		
D2	3.95	4.10	4.25	0.156	0.161	0.167
E	6.00 bsc			0.236 bsc		
E1	5.75 bsc			0.226 bsc		
E2	3.95	4.10	4.25	0.156	0.161	0.167
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
θ1	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	---	---	0.10	---	---	0.004
bbb	---	---	0.07	---	---	0.003
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004



NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. −1994.
4.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED
BETWEEN 0.20 AND 0.25 mm FROM TERMINALTIP.
5.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE
PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7.PACKAGE WARPAGE MAX 0.08 mm.
8.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED
PAD FROM MEASURING.
9.APPLIED ONLY TO TERMINALS.
10.PACKAGE CORNERS UNLESS
OTHERWISE SPECIPIED
ARE R0.175±0.025 mm.

Figure 10: Mechanical Specification – QFN 48L

11. Top Marking Information

TBD