Studies on Boost Topologies for High Boost Ratio

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***Abstract*—Various problems come to the fore, in order to achieve high voltage boost using the basic form of non-isolated boost converter. A number of topological improvements have been suggested by researchers to achieve higher voltage boost ratio with their inherent pros and cons. This paper presents an overall study of four such converters including the boost converter, covering their basics of operation, comparison of various aspects, simulations and implementation details of the suitable one.**

Keywords— cascaded converter, quadratic boost converter, simple boost converter, tapped inductor boost converter

I. INTRODUCTION

New and improved power electronic converters are emerging day by day to interface renewable/non-conventional energy sources to the storage capacity, distribution network, directly fed loads etc. Since most of these sources generate energy at low voltage, there is a need to create a high boost voltage for making the final output compatible to existing loads. The popular mass energy storage technology like, batteries, ultra-capacitors also operate at low voltage need either to be connected in series to add the voltages (with problems in this process) and therefore need boosting the available voltage. Thus, there is a demand for converters with high boost ratio or voltage gain, which is defined as G_v = output voltage/input voltage.

The conventional simple boost converter (SBC) for its simplicity and popularity gets the first consideration to be the basic choice for the job. However, it is very difficult to achieve high boost ratio with SBC as the duty ratio (D) becomes nearly 100%. The main goal of this paper is to find a converter with high boost ratio, along with higher efficiency, lower cost, lower size and weight and reliability, which is not dealt with in existing the research works. With the basic criteria, only single switch topologies are included. The inductor size is a deciding factor. The voltage stress across the switch, current peak through the switch should be low. Besides, the input/source current ripple should be low.

For comparison, the specifications of all the converters are considered to be as:

1) The input and output voltage of all the converters are same, therefore the boost ratio is same in all cases

2) The rated power is same for all the converters

3) Operating frequency of the converters is equal.

4) Same core material is used to implement all the inductors. This simplifies the comparison of inductor sizes which is proportional to the value given by ($LI_{rms}I_{pk}$), where, L is the inductance value, I_{rms} and I_{pk} are the rms and peak current through the inductor respectively.

As power rating and input voltage is same for all converters, the input current is similar for all the converters, considering efficiencies of similar order.

II. BOOST CONVERTER TOPOLOGIES

A. Simple Boost Converter (SBC)

Fig. 1 shows the schematic of the SBC [1]. It is well known that, the voltage gain of SBC is given by:

$$G_v = \frac{V_O}{V_{in}} = \left(\frac{1}{1-D}\right) \quad (1)$$

Where, D = (Switch ON duration)/(Switching Time Period).

Peak voltage stress across the switch is given by:

$$V_{sw\text{-}pk} = V_o. \quad (2)$$

Therefore, for SBC if, I_{av} is the input average current, I_{peak} is the input peak current, then size of inductor for SBC is:

$$LI_{peak}\sqrt{I_{av}^2 + \left(\frac{I_{peak}}{\sqrt{3}}\right)^2} \quad (3)$$

Input current ripple is given by:

$$\Delta I_L = V_{in}D \Big/ Lf \quad (4)$$

Where, f is the switching frequency.

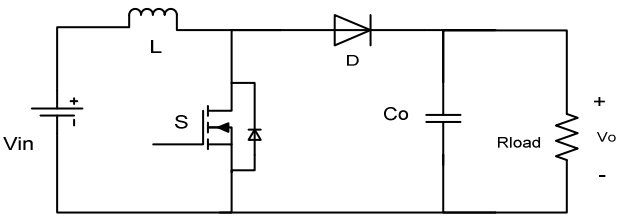

Fig 1. Schematic of the Simple Boost Converter

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From, (1), for high G_v duty ratio, D is very high, reverse recovery time available for the diode is very small, along with the high current through the diode. The voltage stress across the switch during off time is high. Along with the high current ripple this causes high switching loss. Therefore, it is very difficult to achieve high boost ratio, with SBC.

B. Quadratic Boost Converter (QBC)

QBC [2-5] is the result of two cascaded boost converters along with a topological modification to minimize number of switches. Here, the voltage gain has quadratic dependence on D, which can be given by:

$$G_v = \frac{V_o}{V_{in}} = \frac{1}{(1-D)^2} \tag{5}$$

The Peak voltage stress across the switch is

$$V_{sw\text{-}pk} = V_o. \tag{6}$$

Total size of the inductors required can be given by:

$$I_{pk1}L_1\sqrt{I_{av1}^2+\left(\frac{I_{pk1}}{\sqrt{3}}\right)^2} + I_{pk2}L_2\sqrt{I_{av2}^2+\left(\frac{I_{pk2}}{\sqrt{3}}\right)^2} \tag{7}$$

Where, I_{pk1} and I_{av1} are the peak and average current through inductor L_1, and I_{pk2} and I_{av2} are the peak and average current through inductor L_2 as shown in Fig. (2).

Input current ripple is given by:

$$\Delta I_{L1} = V_i D \Big/ L_1 f \tag{8}.$$

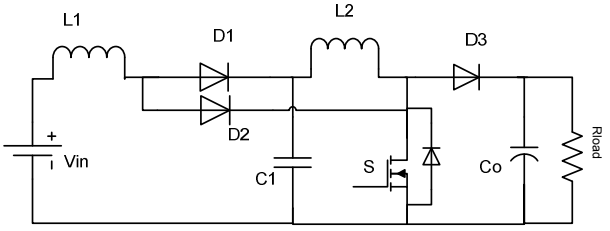

Fig 2. Schematic of the Quadratic Boost Converter.

Compared to SBC, QBC requires lower D for same G_v. However, high switch voltage rating and high peak current through the switch is becomes the limiting factors. Moreover, the inductor size in (7), is not a true value in this case as, the two inductors would be wound on separate cores.

C. Tapped Inductor Boost Converter (TIBC)

The inductor in SBC can be tapped to connect the switch [6-8] as shown in Fig. 3. If number of turns of the inductors L1 & L2 be N1 & N2 respectively, then the voltage gain of the TIBC is given by:

$$G_v = \frac{V_o}{V_{in}} = \frac{1+(N_2/N_1)D}{(1-D)} \tag{9}$$

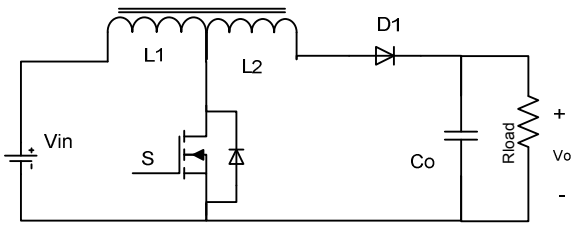

Fig 3. Schematic of the Tapped Inductor Boost Converter.

Peak voltage stress across the switch:

$$V_{sw-pk} = \frac{V_{in}}{1-D} \tag{10}$$

Size of the inductor can be given by :

$$I_{peak}L_{eq}\sqrt{I_{av}^2+\left(\frac{I_{peak}}{\sqrt{3}}\right)^2} \tag{11}$$

where, $L_{eq} = L_1 + L_2 + \sqrt{L_1 L_2}$

Input current ripple is given by:

$$\Delta I_{L1} = \left[\frac{I_{av}N_2}{N_1+N_2D}\right] - \frac{V_{in}^2 D}{L_1 f}\frac{I_{av}}{P_{in}}.\left(1-\frac{N_2}{2(N_1+N_2)}\right) \tag{12}$$

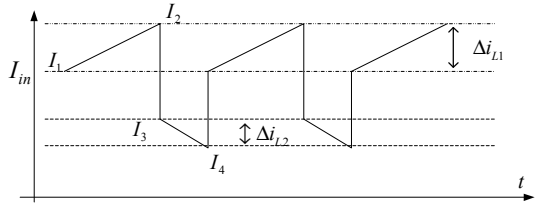

Fig 4. Theoretical Input current waveshape of the Tapped Inductor Boost Converter.

D. Cascaded Boost Converter(CBC)

The CBC [9-11], shown in Fig. 5, is the topological combination of SBC and a second stage boost converter (BC) incorporating a coupled inductor, to achieve still higher gain compared to the topologies discussed earlier.

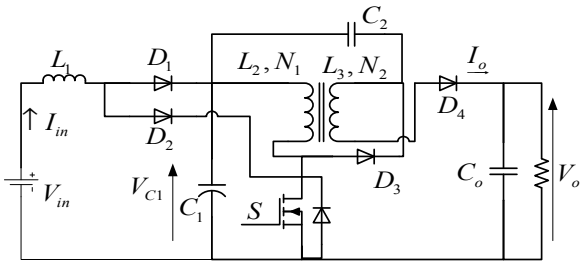

Fig 5. Schematic of the Cascaded Boost Converter.

Voltage gain of the CBC is given by:

$$G_v = \frac{V_o}{V_{in}} = \frac{1+(N_2/N_1)D}{(1-D)^2} \quad (13)$$

Peak voltage stress across the switch is given by :

$$V_{sw-pk} = \frac{V_{in}}{(1-D)^2} \quad (14)$$

Due to the presence of SBC at the first stage of CBC the input current ripple is similar to that appearing in SBC. The input current ripple is given by:

$$\Delta I_L = V_{in} D / L_1 f \quad (15)$$

Total size of the inductors required is:

$$L_1 I_{pk1} \sqrt{I_{av1}^2 + \left(\frac{I_{pk1}}{\sqrt{3}}\right)^2} + I_{pk} L_{eq} \sqrt{I_{av}^2 + \left(\frac{I_{pk}}{\sqrt{3}}\right)^2} \quad (16)$$

where, $L_{eq} = L_2 + L_3 + \sqrt{L_2 L_3}$. I_{pk} & I_{av} are the peak and average current through L_2. I_{pk1} & I_{av1} are the peak and average current through L_1.

III. Comparative Analysis

All the topologies presented in previous section can theoretically provide any amount of voltage boost. However, there are practical limits. Besides, it is preferable to obtain same amount of voltage boost at the lowest possible duty cycle. From (1), (5), (9), (13) it can be concluded that, for the same G_v, SBC would have to operate at maximum D, higher compared to QBC. As, for TIBC and CBC there is one more freedom in terms of the turns ratio of the tapped and coupled inductor respectively. However, with same turns ratio ($n = N_2/N_1$) as CBC has quadratic relation of G_v and D it would be able to supply higher voltage with lower D. Fig. 6 shows the voltage gain of the converters at different D. This figure shows that CBC provides maximum boost, which however depends on n, which in turn should be as low as possible to reduce the switch peak current.

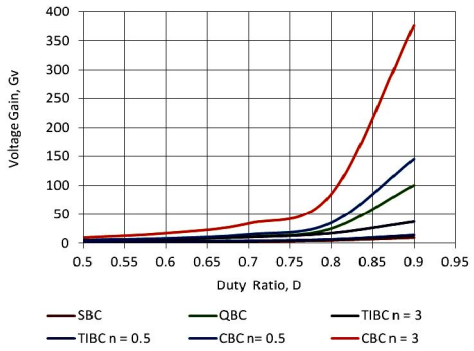

Fig 6. Achieveable voltage gain at vaious duty ratios for the boost converter topologies. n = turns ratio of the inductor

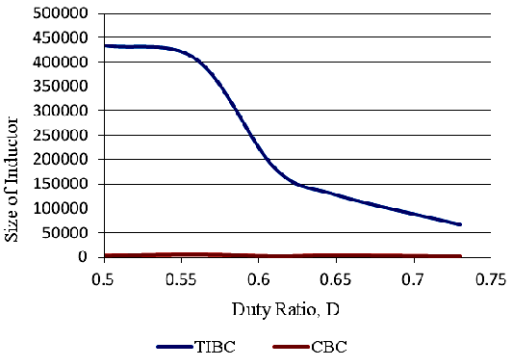

Fig 7. Total magnetics size for TIBC & CBC to achieve same voltage gain by varation of turns ratio, n and Duty ratio, D

For further comparison, various converter parameters need to be compared for equally rated converters. Therefore, the converter specification was set as following:

Rated Power, P_o = 120W, Input Voltage, V_{in} = 12V, Output Voltage, V_o = 240V, Input Peak to Peak Current Ripple = 30% of Input Average Current.

The high voltage gain has certain interdependence on the magnetics size. The total inductors size, which is a crude measure of total magnetics size in the topologies mentioned earlier should be as low as possible to reduce cost and size of the converter. Fig. 7 shows the total magnetics size ($LI_{rms}I_{pk}$) with variation of duty ratio, D. The voltage gain is maintained same by variation of number of turns, n, as D varies. As SBC and TIBC have to operate with a fixed D, they have not been considered here. Besides, the high voltage rating required for the switches in these converters is a significant problem, which restricts their usage when voltage boost requirement is high.

For the comparison depicted in Fig. 7, the source current ripple is same in all cases. However, as n increases the current ripple in the second stage increases very rapidly, thereby increasing switch current ripple. This necessitates switches of higher current rating.

Fig. 8 shows the voltage across the switch for TIBC and CBC with variation in D. Turns ratio, n is changed to maintain same voltage boost for all readings. For CBC the voltage across the switch is higher as its dependence on the duty ratio is quadratic. The switch voltage stress for SBC and QBC is

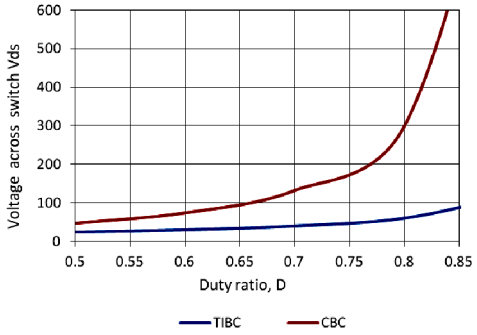

Fig 8. Voltage across the switch for TIBC and CBC with variation in D. n is vaied accordingly to achieve required voltage boost.

equal to the output voltage, which in this Fig. should stand at 240V. It can be concluded that TIBC requires switch of lowest voltage rating. However, it should be emphasized that CBC requires lower duty ratio for same G_v with same n. Therefore, the voltage stress of TIBC and CBC are comparable.

Fig. 9 depicts the peak current through the switch for TIBC and CBC with the variation in D. Here also, n is varied with D to achieve equal voltage boost. For SBC and QBC switch peak currents are 13.5A and 18.8A respectively. It is clear that the switch current rating is almost same for TIBC and CBC, which are both higher compared to SBC and QBC.

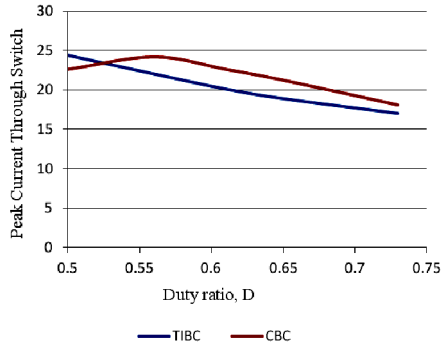

Fig 9. Peak Current through the switch for TIBC and CBC with variation in D. n is vaied accordingly to achieve required voltage boost.

Fig. 10 shows the peak input current variation for TIBC and CBC with change in D. Similar to earlier cases, n is varied with D for equal voltage boost.

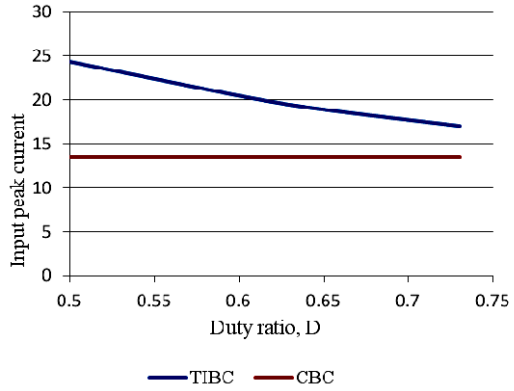

Fig 10. Peak input current for TIBC and CBC with variation in D.

Fig. 11 depicts the peak-to-peak input current ripple magnitude for TIBC and CBC. For SBC and QBC this value is 3.6A.

SBC and QBC are not suitable for high voltage boosting, due to high switch voltage rating as high voltage MOSFETs have higher Rds-on causing higher conduction loss. SBC has a practical limit of duty ratio around 0.9 mainly due to reasons like diode reverse recovery at high frequency. Besides, QBC requires higher switch peak current rating. TIBC shows either comparable or higher characteristic values as depicted in Fig. 7-11. These values can be varied by choosing proper combination of D and n for a given boost ratio. There, for high boost ratio if CBC provides lots of space for optimization.

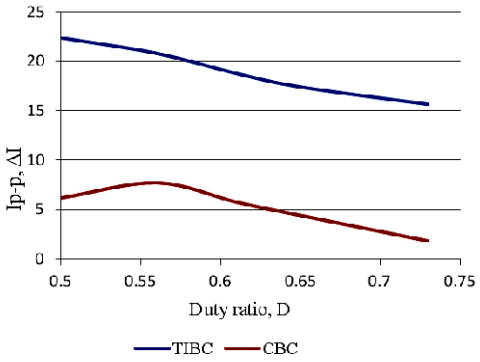

Fig 11. Peak to peak input current ripple for TIBC and CBC.

IV. Simulation Result

From the comparative study, it is apparent that CBC is well suitable for high boost ratio. It can provide maximum boost at lowest duty ratio. The switch voltage stress can be managed by proper design choice. A CBC prototype was simulated in MATLAB SIMULINK environment.

Fig. 12 shows the input current. This current is very similar to the input current of a SBC. The first stage of QBC being a SBC also shows similar input current nature.

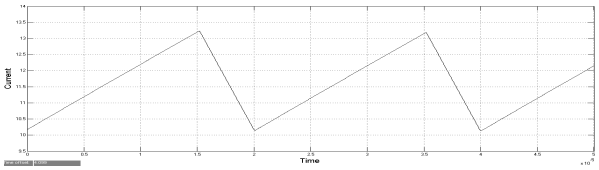

Fig 12. Source current of a CBC

Fig. 13 depicts the input current for the second stage of CBC. It should be mentioned here that these two currents get added to flow through the switch (shown in Fig. 14), thereby making the switch peak current high. The switch peak current can be managed by optimizing D and n. The current waveform through D3 is shown in Fig. 15.

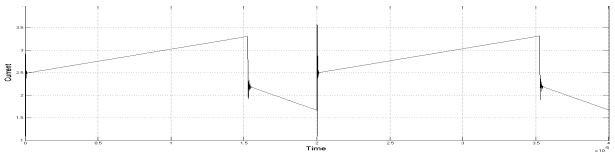

Fig 13. Current through L2 of CBC

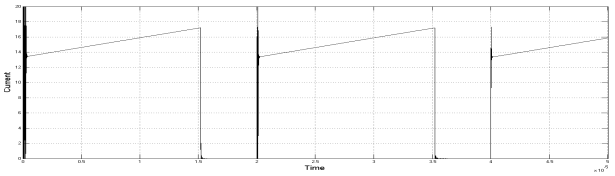

Fig 14. Current through the switch in CBC

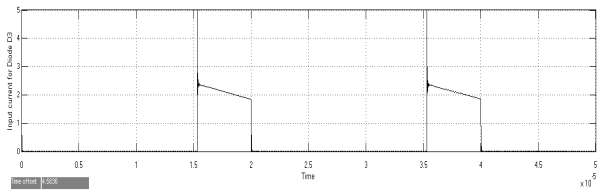

Fig 15. Current through diode D3 in CBC

V. HARDWARE IMPLEMENTATION

A prototype of CBC was implemented in the laboratory to study its features based on the specifications mentioned earlier. The design of the CBC was done first by restricting the switch voltage stress [12]. This provides the duty ratio from (14). This value of *D* along with the required voltage gain provides the value of *n*. The value of switch voltage stress and *n* can be changed to obtain optimized values of parameters like switch current peak, first stage capacitor voltage etc.

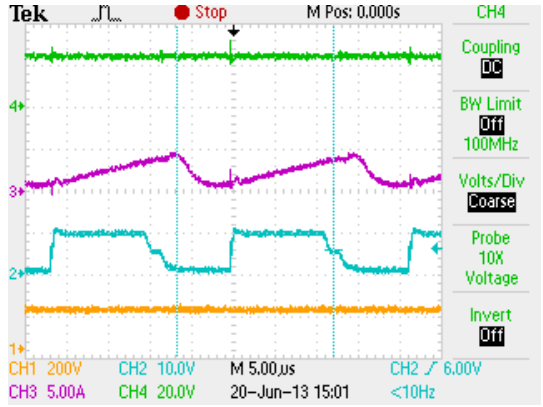

Fig 16. Voltage and Current waveforms at various points of CBC

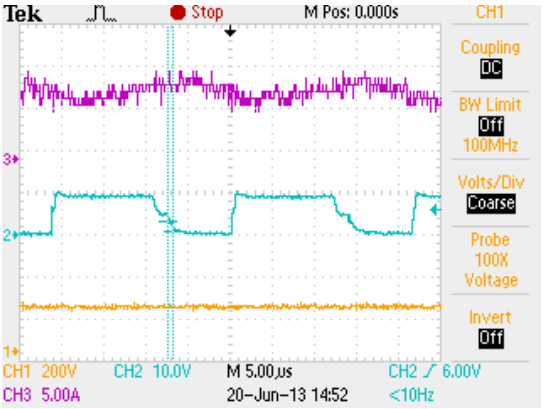

Fig 17. Input Current, Switch Gate Pulse and Output Voltage of the CBC

Fig. 16 depicts the oscillogram of CBC parameters, where, top trace (channel 4, green) shows voltage across first stage capacitor C1, channel 3 (pink) trace represents current through inductor L2, channel 2 (blue) trace is the gate pulse to the MOSFET switch, channel 1(yellow) trace is the output voltage. In practical implementation there was significant leakage inductance between windings of the coupled inductor. Therefore, a small capacitor C2 was added to limit the voltage spike across the switch due to this leakage. Value of C2 was calculated to approximately resonate with L2.

Fig. 17 shows input current to the CBC at the uppermost trace (channel 3, pink). The input current has small ripple as visible in the oscillogram. The middle trace shows the gate pulse to the switch and the lower trace shows the output voltage of the CBC.

VI. CONCLUSION

Four boost topologies are compared to find the best suitable candidate for high boost ratio. Ability to boost with a lower value of D, peak switch current and total size of the magnetics are used as the basis of comparison for a given input/output voltage and power. Although none of the converters has absolute superiority in all aspects, on the basis of various optimizations, CBC can be accepted to be better compared to other topologies. However, as always, the choice of a converter topology can be dictated by the specific application.

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