

An ultra-low noise, high-voltage piezo driver

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We present an ultra-low noise, high-voltage driver suited for use with piezoelectric actuators and other low-current applications. The architecture uses a flyback switching regulator to generate up to 250V in our current design, with an output of 1 kV or more possible with small modifications. A high slew-rate op-amp suppresses the residual switching noise, yielding a total RMS noise of $\approx 100 \mu\text{V}$ (1 Hz–100 kHz). A low-voltage ($\pm 10 \text{ V}$), high bandwidth signal can be summed with unity gain directly onto the output, making the driver well-suited for closed-loop feedback applications. Digital control enables both repeatable setpoints and sophisticated control logic, and the circuit consumes less than 150 mA at $\pm 15 \text{ V}$.

I. INTRODUCTION

Many instrumentation applications in the modern laboratory require agile, low-noise voltage sources capable of supplying hundreds of volts or more. For example, piezo-actuated mirrors and diffraction gratings play an important role in atomic physics experiments (used, e.g., in Fabry-Pérot cavities^{1,2} and external-cavity diode lasers³), while avalanche photodiodes and photomultiplier tubes require large bias voltages for proper operation. In the realm of biophysics, electrokinetic separation methods such as free-flow or capillary electrophoresis⁴ require large electric field gradients, and the recent push to develop lab-on-a-chip devices could benefit from miniaturized high-voltage sources.⁵

Laboratory devices are often operated in a closed feedback loop, where small voltage changes on top of a large DC voltage are necessary to stabilize the output of a particular system. For example, the frequency of an extended-cavity diode laser can be locked by feeding back to a piezo-actuated diffraction grating or mirror, which in turn supplies optical feedback to the diode. Commercially available piezoelectric drivers typically provide a modulation input for such closed-loop applications, but the input voltage is often gained such that it spans the entire output range of the device. Other designs separate high- and low-voltage control pathways, which can extend the bandwidth to $\approx \text{MHz}$, but the low-voltage control is AC-coupled to the output.⁶ While these designs have advantages, many applications would benefit from an architecture that provides a unity-gain, DC-coupled feedback path to the high-voltage output. This low-gain modulation input could make closed-loop systems less susceptible to noise contributions from the servo controller, which we often find in our laboratory to be a limiting factor in laser lock stability.

Instrumentation electronics capable of supplying high voltages traditionally fall under one of two architectural umbrellas: DC-DC switching converters, and linear-type amplifiers. While DC-DC converters are efficient and can

work at very high voltages, they suffer from switching noise and limited control bandwidths. Linear-type devices are typically constructed from a high-voltage operational amplifier (op-amp), powered either from a high-voltage linear regulator or more typically from a secondary switching converter. While the op-amp can provide 100 dB or more of power-supply noise rejection⁷, linear regulators must handle any excess voltage by dissipating heat and so may be more cumbersome to deploy in the laboratory.

We present a circuit with a hybrid architecture. The high voltage is generated by a galvanically isolated DC-DC converter, while a low-noise, high-slew-rate op-amp simultaneously removes noise at the output and provides a low-gain, high-bandwidth ($\gtrsim 100 \text{ kHz}$) modulation input for closed-loop feedback applications. This architecture is able to achieve extremely low noise ($\approx 100 \mu\text{V}_{\text{RMS}}$) over the entire output range, draws very little current, and fits comfortably onto a small-footprint printed circuit board (PCB). Additionally, the high-voltage output remains single-ended and referenced to ground, allowing it to drive piezo actuators with a grounded terminal. The schematic is presented in Sec. II, with a noise analysis in Sec. III and characteristic performance data in Sec. IV. Complete design files, including the schematic, bill of materials, and board layout, can be found on GitHub.⁸ The board manufacture and component cost is less than \$200, making it a cost-effective alternative to commercial options.

II. CIRCUIT DESIGN

The design principles discussed below show how we leverage the characteristics of a galvanically-isolated switching regulator without sacrificing the low-noise requirements of many laboratory applications. Our design targets a 250 V output, but we discuss straightforward modifications to the schematic that make it possible to tailor the gain and output range to a specific application. The entire electronics package fits into a compact Eurocard rack module (with the high-voltage section taking only a fraction of the PCB), and draws less than 150 mA

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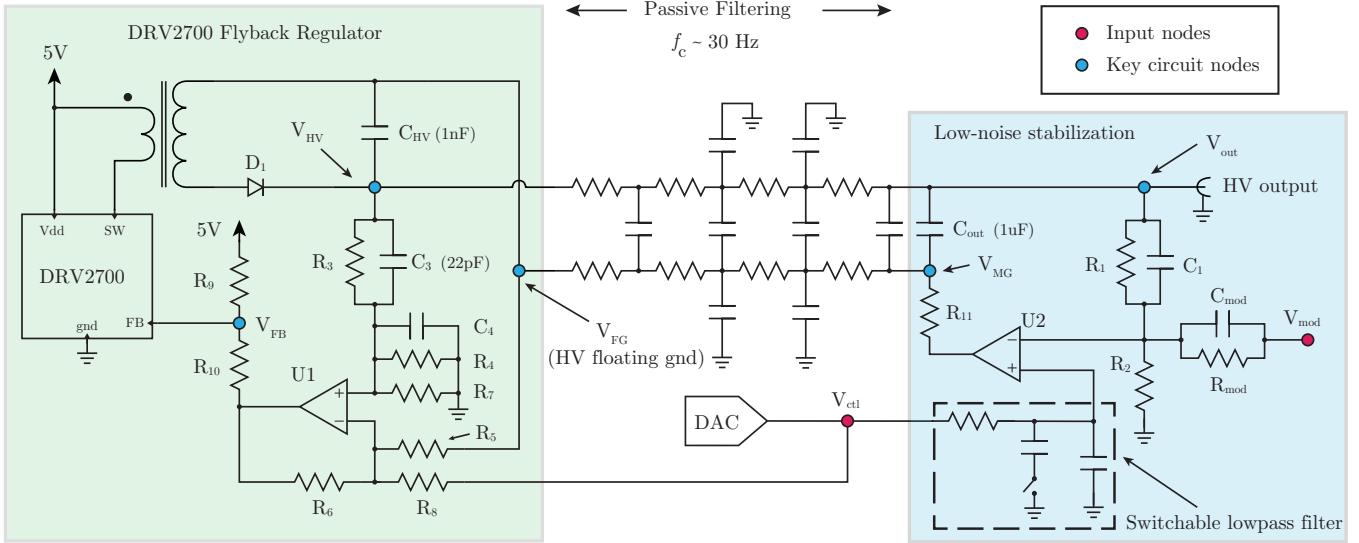


FIG. 1. Schematic of the high voltage supply and stabilization. The voltage V_{HV} is generated using a Texas Instruments DRV2700 high voltage driver in flyback configuration. A high slew-rate op-amp (U_2) senses the output voltage across R_1 and R_2 , and controls it by modulating the mid-ground node V_{MG} . The DC control signal for this op-amp, V_{ctl} , is supplied by a digital-to-analog (DAC) converter, which is passed through a switchable low-pass filter. This design allows for very heavy filtering of the DAC $1/f$ noise during steady-state operation, but the corner frequency can be increased if the output needs to be scanned more quickly. The V_{ctl} gain is set by $(1 + R_1/R_2)$, while the modulation gain is set by $-R_1/R_{mod}$. The op-amp U_2 removes residual switching noise and stabilizes the DC output according to the transfer function given in Eq. (3). A MOSFET quench circuit, shown in Fig. 2, connects at nodes V_{out} and V_{MG} .

at 15 V. The high-voltage output current will be limited by the switching regulator and by the LM7171 op-amp used for low-noise stabilization (U_2 in Fig. 1, which can supply at most $\approx 100 \text{ mA}^9$), but is sufficient for nearly all piezoelectric applications.

Fig. 1 shows an overview of the circuit schematic. A flyback regulator (Sec. II A) controls the potential between the high-voltage (V_{HV}) and floating-ground (V_{FG}) circuit nodes, while the low-noise stabilization circuitry (Sec. II B) controls the output node V_{out} relative to the true circuit ground. A digital-to-analog converter (DAC) generates a voltage setpoint, V_{ctl} , which is sent to the high-voltage flyback regulator and to the low-noise stabilization circuit. The DAC is controlled by an integrated microcontroller, and can be programmed to output slow ($\approx 10 \text{ Hz}$) rail-to-rail voltage ramps in addition to setting the DC operating point (Sec. II C). To improve the large-amplitude slew rate, a MOSFET “quench” circuit (Fig. 2) is included to reduce the RC time constant of the high-voltage node V_{out} when needed. A low-pass filter with a switchable corner frequency can be engaged during DC operation to reduce $1/f$ noise from the DAC (discussed in Sec. III). Fast output modulation between $\pm 10 \text{ V}$ can be achieved through the input node V_{mod} . This node is DC-coupled to the high-voltage output, and is useful for closed-loop feedback control.

A. Flyback regulator

The high-voltage DC-DC converter used here is based on the Texas Instruments DRV2700 piezo driver.¹⁰ This integrated circuit can be operated as a boost converter to drive an on-chip differential amplifier up to 100 V, or as a flyback converter up to 1 kV or more. In flyback configuration, the internal-boost switch of the DRV2700 (pin SW in Fig. 1) drives a step-up transformer. When the switch closes, current begins to flow through the primary coil of the transformer and induces a corresponding voltage across the secondary coil. In this state, the output diode D_1 is reverse-biased, and the capacitor (C_{HV} in Fig. 1) holds its charge. When the switch opens, the voltage across the secondary coil is inverted, putting the diode into conduction and charging the capacitor. By changing the switching duty cycle, the DRV2700 is able to regulate the voltage across the galvanically isolated output (nodes V_{FG} and V_{HV} in Fig. 1).

The DRV2700 implements output voltage control by comparing the feedback input pin at node V_{FB} with an internal (1.3 V) reference. The resistors R_9 and R_{10} are chosen such that pin FB is at 1.3 V when the output of U_1 is at ground: $R_{10}/(R_9 + R_{10}) = 1.3 \text{ V}/5 \text{ V} \approx 0.26$. The op-amp U_1 subtracts V_{FG} and $G \cdot V_{ctl}$ from the voltage at node V_{HV} , ensuring the DRV2700 regulates the output voltage such that

$$V_{HV} - V_{FG} = G \cdot V_{ctl}, \quad (1)$$

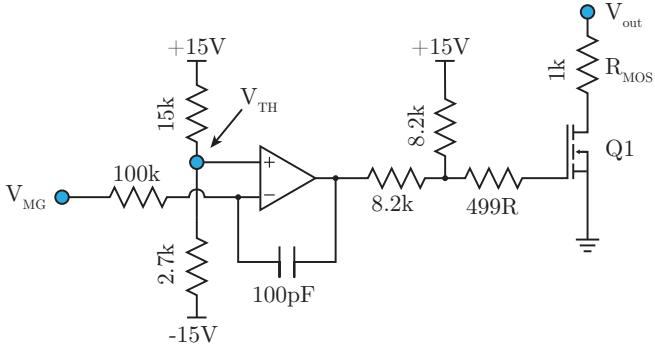


FIG. 2. MOSFET “quench” circuit. When the mid-ground node V_{MG} (also shown in Fig. 1) goes below the threshold value set at V_{TH} , the op-amp puts the HV MOSFET Q1 into conduction. When engaged, the quench time constant is given by $\tau \approx R_{MOS}C_{out}$, which for our circuit is set to 1 ms. The capacitor $C_{out} = 1\text{ }\mu\text{F}$ is shown in Fig. 1, and details of this circuit are discussed in Sec. II C.

where the gain G is set by the resistor ratio $R_3/R_4 \equiv R_5/R_6$, and V_{ctl} is the control voltage set by the DAC. The capacitors C_3 and C_4 are chosen such that $C_3 = 22\text{ pF}$ and

$$\frac{C_4}{C_3} = \frac{R_3}{R_4 \parallel R_7}, \quad (2)$$

as suggested by the DRV2700 datasheet¹¹, where $R_6 = R_7 = R_8$, and $R_i \parallel R_j \equiv R_iR_j/(R_i + R_j)$. In our implementation, we choose a gain $G \approx 50$ ($R_3 = R_5 = 499\text{ k}\Omega$; $R_4 = R_{6,7,8} = 10\text{ k}\Omega$), allowing a 5 V control signal V_{ctl} to span 250 V at the output. A different DAC and/or a different gain factor could be chosen to adjust the maximum output voltage.¹² The transformer (ATB3225, 1:10 step-up winding), diode, and RC feedback network are all based on values suggested in the DRV2700 datasheet.^{11,13}

The output of the flyback regulator is passed through a four-pole, low-pass RC filter. The corner frequency $f_c \approx 30\text{ Hz}$ is chosen to be high enough that a slow ($\approx 10\text{ Hz}$) rail-to-rail triangle ramp can be applied by the DAC at V_{ctl} (for, e.g., sweeping over a resonance in spectroscopy), but low enough that the $\approx 100\text{ kHz}$ switching noise is substantially attenuated. Additional capacitors on both the V_{HV} and V_{FG} resistor networks shunt high frequency noise to ground. This filter topology, modeled on a lossy transmission line, is sufficient for our application, but other corner frequencies or topologies could also be used.

B. Low-noise stabilization and fast modulation

The low-noise stabilization circuit is crucial to the performance of the design, as it is responsible for removing noise at the output of the flyback converter. To accomplish this, a high slew-rate op-amp (Texas Instruments

LM7171, 4100 V/ μs ; see U2 in Fig. 1) drives the galvanically isolated floating ground of the flyback converter. This op-amp senses the voltage V_{out} referenced to true circuit ground, and adjusts its output such that

$$V_{out} = \left(1 + \frac{R_1}{R_2 \parallel R_{mod}}\right) V_{ctl} - \left(\frac{R_1}{R_{mod}}\right) V_{mod}. \quad (3)$$

Here, V_{mod} is the applied modulation, which can vary between $\pm 10\text{ V}$ and is inverted before being summed onto the output. We choose $R_1 = R_{mod} = 1\text{ M}\Omega$ and $R_2 = 20.5\text{ k}\Omega$ such that the DC gain $\Delta V_{out}/\Delta V_{ctl}$ is ≈ 50 and the modulation gain $\Delta V_{out}/\Delta V_{mod}$ is unity. Depending on the application, other gain configurations could work equally well provided the non-inverting gain of U2 closely matches the gain of the flyback regulator (since they both derive from V_{ctl}).

The op-amp U2 controls V_{out} via two different feedback pathways. At low frequencies, it modifies the floating ground reference V_{FG} of the flyback converter, and the DRV2700 in turn modifies V_{HV} to maintain a constant voltage between V_{FG} and V_{HV} . At higher frequencies, U2 is decoupled from V_{FG} by the passive filtering network. In this regime, C_{out} provides a low-impedance path between U2 and the output, such that high-frequency switching noise can be directly compensated for by the op-amp. We chose a value $C_{out} = 1\text{ }\mu\text{F}$, which is a compromise between component size and the desire for a large capacitance. In addition, a small resistance $R_{11} = 50\text{ }\Omega$ is inserted between U2 and C_{out} to ensure stable operation. Smaller R_{11} and/or larger C_{out} might provide better performance, but this has not been tested.

The choice of components for resistors R_1 and R_2 is crucial for the low-noise performance of the system. Because this resistive divider is responsible for accurately sensing the voltage V_{out} , noise introduced by these resistors cannot be corrected by the op-amp. In general, resistors are fundamentally limited by Johnson noise, in which thermal fluctuations contribute to a white noise power spectrum given by $4k_B T R$, where T is the temperature and k_B is Boltzmann’s constant.¹⁴ However, resistors also exhibit $1/f$ current noise caused by equilibrium fluctuations of the resistance.^{15,16} This excess noise depends on the applied voltage, and therefore is an important consideration in a high-voltage circuit. It is also highly dependent on the resistor composition and varies from manufacturer to manufacturer. Seifert, et. al.¹⁷ characterized $1/f$ noise in a variety of resistors, and found that the Vishay TNPW 0.1% series resistors showed a noise spectrum almost consistent with Johnson noise down to 1 Hz. Our current design uses this series in a 1206 package, but we noticed low-frequency noise correlated with varying strain on the PCB, potentially due to the relatively large footprint of this package. Future boards might instead use three TNPW 0.1% 0603 resistors in series for both R_1 and R_2 to minimize strain-induced output noise.

The value of capacitor C_1 is a tradeoff between two

competing design considerations. On the one hand, a larger C_1 extends the frequency range where switching noise from the DRV2700 is suppressed. However, large values of C_1 limit the bandwidth of V_{ctl} . We empirically settled on $C_1 = 1 \text{ nF}$, which is large enough to saturate the feedback gain in the 40 kHz–100 kHz range where switching noise dominates, but not so large that it limits the bandwidth of V_{ctl} below the corner set by the switchable low-pass filter described in Sec. II C. Once C_1 was chosen, capacitor C_{mod} was calculated to match the impedances $R_1 \parallel C_1 = R_{\text{mod}} \parallel C_{\text{mod}}$. For our circuit, this means $C_{\text{mod}} = C_1$.

C. Digital control and slow modulation

The high-voltage setpoint (absent voltages summed in at V_{mod}) is controlled by a low-noise DAC. This has two advantages: digital control enhances setpoint repeatability, and simplifies the integration with computerized control electronics or sophisticated servo loops. While the modulation input V_{mod} has a limited range of $\pm 10 \text{ V}$, larger voltage swings can be achieved by reprogramming the DAC.

As discussed below in Sec. III, without modification the DAC would dominate the noise performance of V_{out} . Therefore we add a single-pole, low-pass filter between V_{ctl} and the non-inverting node of U2 to bring the DAC noise contribution below other noise sources in the circuit. This filter has a switchable corner frequency (between 165 Hz and 0.8 Hz) to optimize noise performance at DC while still permitting AC modulation when needed. It consists of a $20.5 \text{ k}\Omega$ resistor and 47 nF capacitor, with a secondary $10 \mu\text{F}$ capacitor that can be switched in to operate with the lower corner frequency.

One downside of the flyback regulator presented above is that while the switched transformer can quickly charge the output capacitors, the discharge time τ is limited to $\approx 1 \text{ s}$ by the RC time constant of the circuit. To get around this limitation, we have added an auxiliary MOSFET “quench” circuit¹⁸ to quickly shunt V_{out} to ground (see Fig. 2). This circuit works by monitoring the voltage at V_{MG} , the mid-ground node controlled by op-amp U2. If V_{MG} drops below a threshold set by V_{TH} , the comparator op-amp in Fig. 2 changes the gate voltage of the MOSFET to put it into conduction. The time constant for this configuration is given by $\tau \approx R_{\text{MOS}}C_{\text{out}}$. For our circuit, this changes τ to $\approx 1 \text{ ms}$, allowing C_{out} to be quickly discharged. The threshold is $V_{\text{TH}} = -10.4 \text{ V}$, but other values could be chosen depending on the design requirements.

The high-voltage design presented here has the flexibility to exist as a standalone circuit or be integrated with other electronics, and we have included several auxiliary features to make this more convenient. For example, the analog modulation input is differentially buffered to break ground loops (not shown in Fig. 1), and the digital portion can be interfaced with other devices in

the lab to expand conceivable control scenarios. Secondary features include a divided-down output that can be used as a monitor or fed forward to a low-noise laser diode current controller like the one in Erickson, et. al.¹⁹ Of course many variations are possible, and we refer the reader to our GitHub page for more details on our specific implementation.⁸

III. NOISE MODEL & ANALYSIS

To better understand the circuit performance and the measured output noise reported in Sec. IV, we introduce the noise model shown in Fig. 3. A summary of each noise contribution (op-amp, DAC, Johnson-Nyquist, and residual ripple from the DRV2700, all calculated at the node V_{out}) is shown in Fig. 4, along with the cumulative root-mean-square (RMS) noise estimates in different frequency bands. We will neglect noise appearing at node V_{mod} due to the external modulation because its exact character depends on the external drive.

To facilitate the noise analysis, we calculate the voltage and current (transimpedance) gains from the input nodes of U2 to the output, V_{out} . Starting with the non-inverting node, we find the voltage gain to be

$$G_+^{(v)} = 1 + Z_1 \left(\frac{1}{R_2} + \frac{1}{Z_{\text{mod}}} \right), \quad (4)$$

where Z_1 and Z_{mod} are the equivalent impedances of $R_1 \parallel C_1$ and $R_{\text{mod}} \parallel C_{\text{mod}}$, respectively. The transimpedance gain, $G_+^{(i)}$, follows by multiplying $G_+^{(v)}$ by the impedance, Z_+ , seen from that node. Thus,

$$G_+^{(i)} = G_+^{(v)} \left[\frac{R_{\text{LP}}}{1 + 2\pi i f R_{\text{LP}} C_{\text{LP}}} \right], \quad (5)$$

where the bracketed term is Z_+ , f is the Fourier frequency, and i is the imaginary unit.

We now calculate gains from the inverting node of U2. Because any currents appearing at this node will be cancelled by the feedback of U2, the transimpedance gain $G_-^{(i)}$ is simply the impedance Z_1 , given by

$$G_-^{(i)} = Z_1 \equiv \frac{R_1}{1 + 2\pi i f R_1 C_1}. \quad (6)$$

With these expressions in hand, we can calculate the output noise contribution from each source in our model.

As shown in Fig. 3, the op-amp noise is parametrized by two noise contributions: e_n , the input voltage noise spectral density, and i_n , the input current noise spectral density. For the LM7171 at 10 kHz, $e_n = 14 \text{ nV}/\sqrt{\text{Hz}}$ and $i_n = 1.5 \text{ pA}/\sqrt{\text{Hz}}$ with a $1/f$ noise character below this frequency.⁹ The voltage noise appears at the non-inverting input, while the current noise is present at both inputs. By multiplying each source by the appropriate

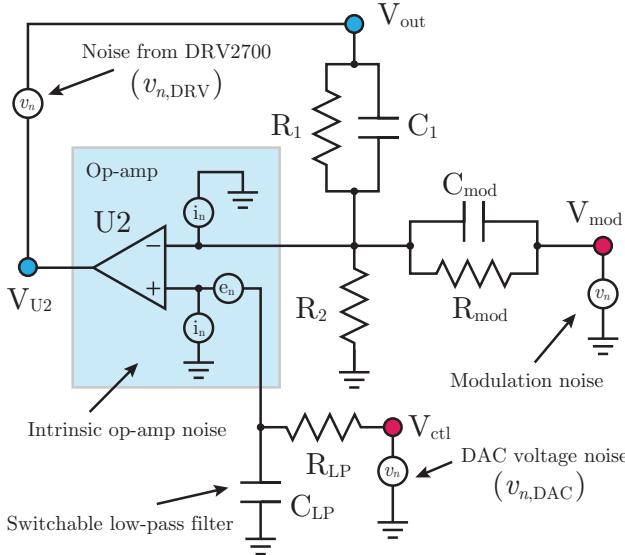


FIG. 3. Noise model, including contributions from the op-amp, DAC, DRV2700, and modulation input. The element labeled C_{LP} consists of a 47 nF capacitor in parallel with a 10 μ F capacitor connected to ground through a switch, such that the corner frequency of the filter can be changed depending on the mode of operation (see text). Though not drawn in the figure, we also consider the Johnson noise contributions from all resistors.

gain, we obtain the equivalent output-noise power spectral densities (PSD),

$$\begin{aligned} e_{v,U2}^2 &= |G_+^{(v)}|^2 e_n^2 \\ e_{i,U2}^2 &= |G_-^{(i)}|^2 i_n^2 + |G_+^{(i)}|^2 i_n^2, \end{aligned} \quad (7)$$

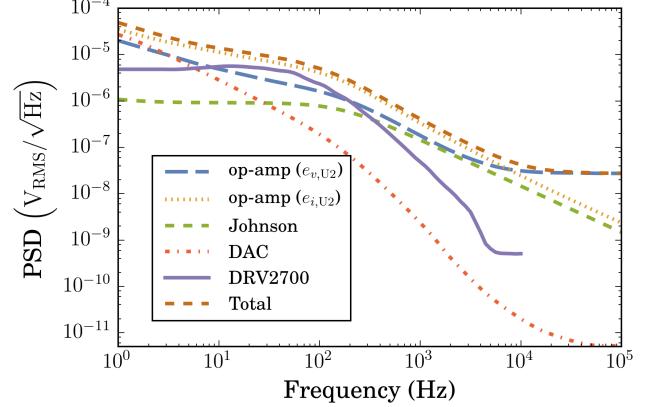
where $e_{v,U2}^2$, $e_{i,U2}^2$ are the output-referred voltage and current noise PSD, respectively (plotted in Fig. 4).

Next, we calculate the DAC noise contribution. The voltage gain from the node V_{ctl} is given by

$$G_{ctl}^{(v)} = \left[\frac{1}{1 + 2\pi f R_{LP} C_{LP}} \right] G_+^{(v)}, \quad (8)$$

where the bracketed term represents the contribution to the transfer function from the switchable low-pass filter. Without the addition of this low-pass filter, the voltage noise of the DAC would dominate both the low- and high-frequency noise performance of the circuit. A simple solution would be to place a fixed-corner filter at this node, but this would severely restrict the AC performance of V_{ctl} . Thus, we use a switchable low-pass filter (as described in Sec. II C) to achieve low-noise performance during DC operation, while still permitting the DAC to modulate V_{ctl} more quickly when needed. The non-zero resistance of the switch contributes a zero to the transfer function at ≈ 23 kHz, but has negligible effect on the performance. The DAC voltage noise contribution can now be calculated as

$$e_{n,DAC}^2 = |G_{ctl}^{(v)}|^2 v_{n,DAC}^2, \quad (9)$$



Noise source	RMS Voltage (1 Hz – 10 Hz)	RMS Voltage (10 Hz – 100 kHz)
op-amp voltage ($e_{v,U2}$)	26 μ V	31 μ V
op-amp voltage ($e_{i,U2}$)	51 μ V	73 μ V
DAC ($e_{n,DAC}$)	28 μ V	8 μ V
Johnson-Nyquist ($e_{n,JN}$)	3 μ V	14 μ V
DRV2700 ($e_{n,DRV}$)	15 μ V	43 μ V
total (calculated)	66 μ V	92 μ V

FIG. 4. Modeled noise contributions (color online). Plotted are the noise contributions from each source in our model, along with the total calculated noise. Power spectral density (PSD) is referred to the high-voltage output, and the table shows the integrated RMS noise due to each noise source in different frequency bands. The total RMS noise (summed in quadrature) over the entire 1 Hz – 100 kHz range is calculated to be 113 μ V, with the residual DRV2700 switching noise measured at 100 V as described in the text. Frequency-dependent noise spectra for the DAC and op-amp were extracted from the datasheets.

where $v_{n,DAC}$ is the frequency-dependent output voltage noise of the DAC as reported in the datasheet.²⁰ In subsequent calculations, we take the DC-mode operation ($f_c = 0.8$ Hz) for the switchable low-pass filter.

The Johnson noise contribution can be calculated by modeling each resistor with a parallel current noise given by $i_R^2 = 4k_B T/R$. Resistors R_1 , R_2 , and R_{mod} all contribute current noise at the inverting node of U2, which as discussed previously has a transimpedance gain to the output given by $G_-^{(i)}$. The resistor R_{LP} contributes current noise at the non-inverting node, which sees a transimpedance gain $G_+^{(i)}$. Thus, the total Johnson noise is

$$e_{n,JN}^2 = 4k_B T \times \left[|G_-^{(i)}|^2 \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_{mod}} \right) + \frac{|G_+^{(i)}|^2}{R_{LP}} \right]. \quad (10)$$

The low-noise stabilization circuit is limited in its ability to reject residual switching noise from the DRV2700 regulator (after the passive filtering network) by the total loop gain analyzed from node V_{out} . The LM7171 has

a reported open-loop gain of 85 dB ($\approx 1.8 \times 10^4$), with a dominant pole at ≈ 10 kHz.⁹ We can model the open loop gain, G_{OL} , as

$$G_{OL} = \frac{1.8 \times 10^4}{1 + i(f/10\text{ kHz})}. \quad (11)$$

The feedback network contributes a gain

$$G_{FB} = \frac{R_2 || Z_{mod}}{Z_1 + R_2 || Z_{mod}}, \quad (12)$$

arising from the voltage partition between V_{out} and the inverting node of U2. From these, we write down the closed-loop gain seen from V_{out} ,

$$G^{(DRV)} = \frac{1}{1 + G_{OL}G_{FB}}. \quad (13)$$

The contribution to the output from residual switching noise, $v_{n,DRV}$, is then

$$e_{n,DRV}^2 = v_{n,DRV}^2 |G^{(DRV)}|^2. \quad (14)$$

For $R_1 = 1\text{ M}\Omega$ and $C_1 = 1\text{ nF}$, $v_{n,DRV}$ is attenuated by as much as 76 dB at 6.3 kHz.

We estimate the noise spectral density $v_{n,DRV}$ by monitoring the node V_{U2} in Fig. 3, since the output of this op-amp represents the control signal required to cancel voltage fluctuations at V_{out} . The trace for $e_{n,DRV}$ plotted in Fig. 4 is derived from the results of this measurement. Because the measured $v_{n,DRV}$ drops below the noise floor of our spectrum analyzer at ≈ 10 kHz, we only plot the trace out to this frequency.

Given the noise model discussed above, our circuit is dominated by the op-amp's intrinsic current noise at

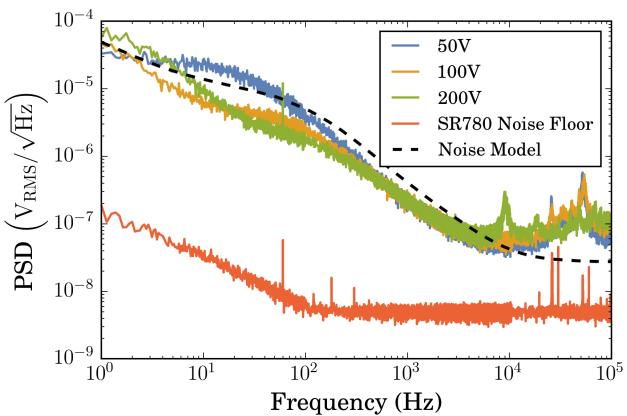


FIG. 5. Voltage noise power spectral density at various output voltages, as measured on an SR780 spectrum analyzer (color online). The integrated RMS noise (1 Hz – 100 kHz) is {138, 80, 101} μV measured at {50, 100, 200} V, with no output load. The dashed black line overlays the noise estimate from our model, calculated at 100 V (see Fig. 4).

lower frequencies, and voltage noise at higher frequencies. The op-amp current noise contribution could be suppressed by using lower resistances R_1 and R_{mod} , however one must be careful about power and current limitations when dealing with such high voltages. Each noise source is tabulated and plotted in Fig. 4, and the total voltage noise (1 Hz – 100 kHz, $V_{out} = 100$ V) is calculated to be 113 μV_{RMS} .

IV. RESULTS

The measured performance of the high-voltage piezo driver is shown in Fig. 5, where we plot the noise power spectral density measured at several different output voltages. These traces were taken on a Stanford Research Systems SR780 spectrum analyzer, with the high-

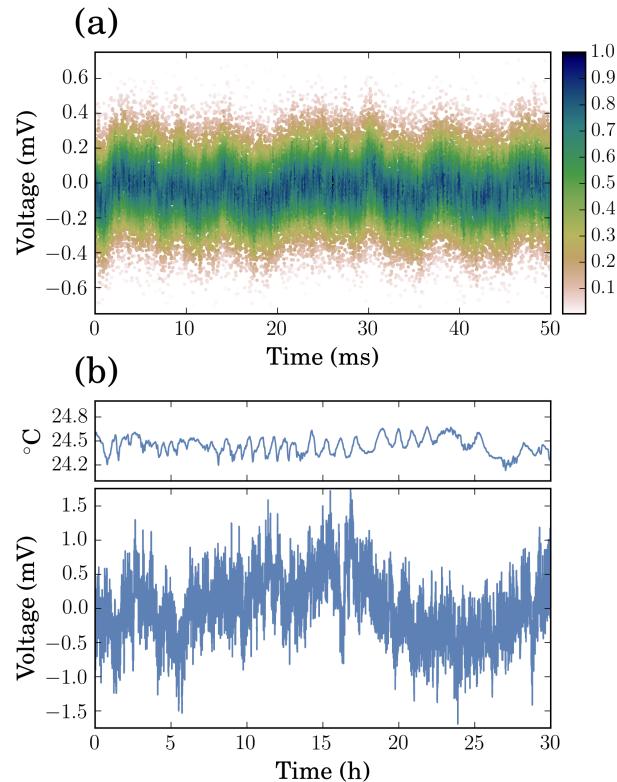


FIG. 6. Time-domain traces of the high-voltage output (100 V, color online). (a) Short-time scatterplot, measured on a PicoScope 5442B (AC coupled). The points have been down-sampled for clarity, and colored based on a normally-distributed probability of occurrence in each 100- μs timeslice (scaled to the most probable voltage). The color thus provides a visual estimation of the RMS width. (b) Long-term trace, measured on a Keithly 2010 digital multimeter. A 100 V DC offset is subtracted from the plotted values. The top panel shows the lab temperature during the same time period.

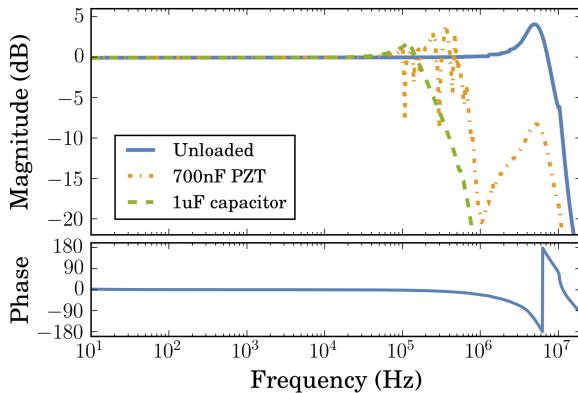


FIG. 7. Modulation input transfer function (color online). The solid blue line indicates the unloaded frequency response, with the phase plotted in the lower panel. The dash-dotted orange trace shows the response with a 700 nF piezoelectric actuator (Thorlabs PN AE0505D08F). Several mechanical resonances above ≈ 50 kHz are clearly visible. The dashed green trace shows the response under a 1 μ F capacitive load. Loaded response bandwidth is ≈ 100 kHz, and the unloaded gain is flat within 0.1 dB out to 1 MHz where the phase is -20° .

voltage output coupled through a 0.5 Hz high-pass filter and without any capacitive load. This represents a worst-case scenario, as larger capacitances at the output will reduce the noise. The integrated noise (1 Hz–100 kHz) was measured to be $\{138 \mu\text{V}_{\text{RMS}}, 80 \mu\text{V}_{\text{RMS}}, 101 \mu\text{V}_{\text{RMS}}\}$ for $\{50 \text{ V}, 100 \text{ V}, 200 \text{ V}\}$ outputs. This matches roughly with the expected total RMS noise calculated in Sec. III. The difference in noise performance at different output voltages can be traced back to the residual ripple of the DRV2700, which is larger for lower output voltages. Indeed, one can see the characteristic shape change in Fig. 5 between 100 V and 50 V as the residual ripple $e_{n,\text{DRV}}$ begins to dominate at low frequencies.

Fig. 6 shows the performance at both short- and long-time scales. At long times, voltage fluctuations on the order of a few mV can be observed. This is due generically to $1/f$ noise, but also correlates with the external temperature. A cross-correlation between the measured temperature and output voltage yields an effective temperature coefficient of $-24 \text{ ppm}/^\circ\text{C}$ at 100 V.²¹ The short-term trace was taken on a PicoScope 5442B (AC-coupled, 100 V output), and downsampled for clarity. Points are binned into 100- μs slices, and colored based on their normally-distributed probability of occurrence. The color scale is normalized to the most probable voltage in each bin.

Fig. 7 shows the measured frequency response under different load conditions. The unloaded bandwidth is as high as a few megahertz, while a 1 μ F capacitive load can still be driven at ≈ 100 kHz. Several mechanical resonances can be seen with a 700 nF piezoelectric load, as expected. In a laboratory setting, these resonances can be mitigated by using a digital feedback controller

with notch filters tuned to match the exact resonance frequencies observed in the system²², thereby extending the usable bandwidth out to ≈ 100 kHz.

V. CONCLUSION

We have designed, built, and characterized a high-voltage piezoelectric driver optimized for use in a modern atomic physics laboratory. It is based on a flyback configuration switching regulator, but is able to achieve very low noise performance by active stabilization from a high slew-rate op-amp. This hybrid architecture makes it small and easy to deploy in a variety of situations, without requiring an external high-voltage power supply. The design principles discussed here can be adapted to fit the exact application, and all design files are freely available on GitHub for others to use and modify.

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