
Flyback SMPS Using a Microcontroller as Control Unit

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INTRODUCTION

This application note describes the steps taken to design, build and test a 20W Flyback Switched Mode Power Supply (SMPS) that uses the PIC16F1769 to control the circuit. The purpose is to show how the Core Independent Peripherals (CIPs) of the microcontroller unit (MCU) can be used to implement the logic control for a SMPS while the core is free to do other functions.

The reason for changing the dedicated flyback controller to a MCU with CIPs is to gain control, monitoring, communications and automated features, which are some of the demands in a new SMPS.

The concept of CIPs can be tricky to understand for designers who have never worked with MCUs. Designers who have used only Application Specific Integrated Circuits (ASICs) may think of them as analog devices, such as op amps and comparators that are integrated in a microcontroller that does not need code supervision to work normally, but can be interconnected and configured in a sandbox-type environment.

The flyback topology was chosen because it offers a simple design with few components while providing isolation. It can be used as a reference for more complex designs.

The first part of this application note is dedicated to readers who are unfamiliar with the flyback design. It focuses on:

- Theory
- Logic
- Equations and a third-party tool to solve them
- Component design and selection
- Compensation process and filtering

For readers already accustomed to these steps the second part provides:

- Information on what a CIP is
- How CIPs are used to control the flyback SMPS
- How to use the Microchip Code Configurator (MCC) tool to configure them without writing a line of code
- The MCU on a “hot” side of a SMPS
- Limits control and examples of automated functions

The third part provides some layout tips and thermal equations while the forth part provides experimental results which demonstrate that a MCU dotted with CIPs is ready to control a SMPS and even make it “smart”.

SPECIFICATIONS

The most used power source for a SMPS is the AC wall plug. It is used for this flyback SMPS to provide a good example for most designers.

There are two basic standards for voltage and frequency in the world, one is the North American standard of 120 volts at a frequency of 60 Hz, and the other is the European standard of 220-240 volts at 50 Hz. For more related information on standards, see [1] in [Section “References”](#).

Because there are deviations from these standards (220 VAC ~ 60 Hz in Brazil, 110 VAC ~ 50 Hz in Jamaica), there is a need to have a universal input compatibility like 100 VAC - 240 VAC at 50 Hz-60 Hz with a 10% error margin. In this application note, the used input is 84 VAC - 276 VAC at 47 Hz - 63 Hz.

The design must be able to supply a maximum power of 20 Watts, and the output must be isolated from the input. The output voltage is 12 Vdc and output current up to 1.7A. There is a variety of transformers on the market that can support the input/output conditions with this power. Here, a custom one is built for educational purposes and to show size differences between the two. The transformer is built based on the input and output voltage ratio, thus the designer can calculate the turns ratio, the inductance, and later, the other variables. Depending on the application in which the design is used, the designer must be well aware that some output ripple constrictions may apply.

In this specific design, an active power factor correction (PFC) system is not implemented, but note that some applications or users may specify the need of one, so the PFC system must be included in the noise calculation of the system and can influence the stability of the design.

The flyback design presented in this application note is implemented so that it uses the current-mode control and the latest PIC16F176X microcontroller that includes comparators, op amps and COG, to ensure correct functionality and stability. The PIC16F176X microcontroller is a powerful IC that includes both the analog control system for SMPS using internal CIPs that can be configured and reconfigured during run-time, which enables the advantage of having an intelligent system to control and adapt, that the user can communicate with.

The stability of the system is verified and complies to a phase margin greater than 45 degrees and a gain margin greater than 20 dB.

Isolation must be maintained using good PCB design rules, a properly designed transformer and an optocoupler that will have the function to isolate the feedback information needed for the current-mode control loop.

Flyback Theory (What is Needed)

The flyback is the most ubiquitous in both AC/DC and DC/DC conversion with galvanic isolation between the input and any outputs. The flyback converter is a buck-boost converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with the additional advantage of isolation. The system is able to provide line isolation to maintain a safe environment for the user, thanks to the use of a transformer for power conversion and an optocoupler for output regulation.

The most common applications are:

- Low-power SMPS (cell phone charger, standby power supply in PCs)
- Low-cost multiple-output power supplies (main PC supplies < 250W)
- High-voltage generation (xenon flash lamps, lasers, copiers)

The isolation offered by the flyback transformer can also be obtained by using a transformer at the line frequency of 50-60 Hz, but this transformer's weight and dimensions are inversely proportional to the frequency, so it is more convenient to incorporate it in the converter's structure and work at tens to hundreds of kHz, thus significantly decreasing the physical dimensions.

When compared to other switching regulator topologies, the flyback has several cost and performance advantages, which can be seen below.

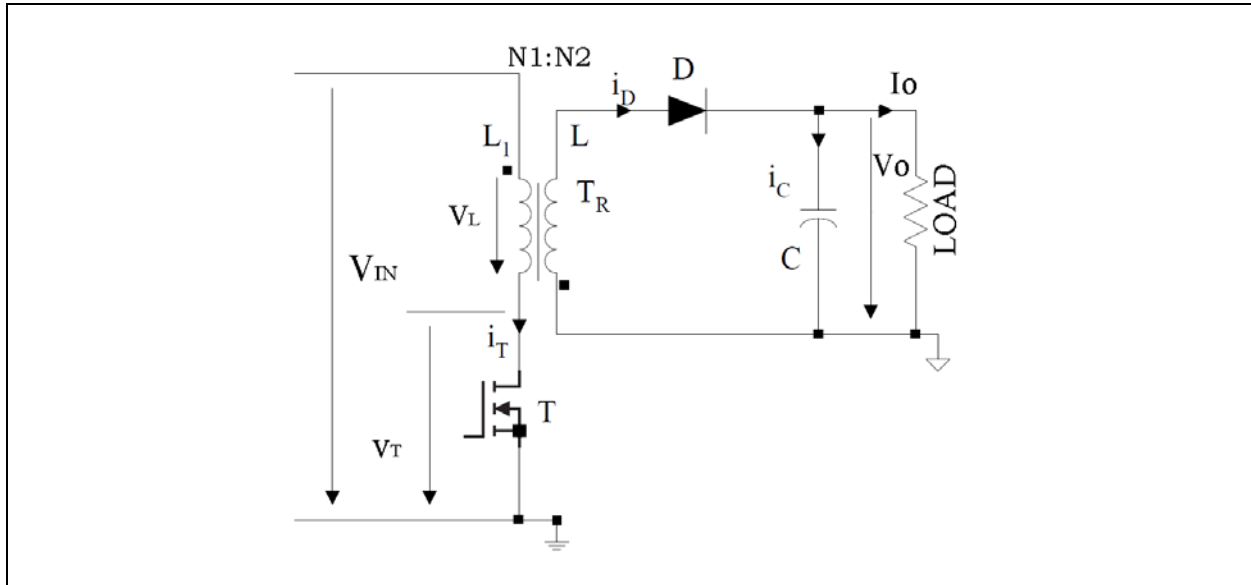
Cost Advantages

The assembly costs for the flyback regulator are low due to a low overall component count, single-magnetic element for both energy storage and transformer action, and for the ease it provides in generating multiple outputs.

Performance Advantages

1. The flyback topology offers good voltage tracking in multiple output supplies due to lack of intervening inductances in secondary circuits.
2. Since there is no need to charge an output inductor every cycle, a good transient response is achievable.
3. Easy to have input dynamic range.
4. Simple driving.

The electrical schematic of this convertor is illustrated in [Figure 1](#).

FIGURE 1: ELECTRICAL SCHEMATIC OF THE FLYBACK TOPOLOGY

A flyback converter operates by first storing energy from an input source into the transformer while the primary power switch is ON. When the switch turns in OFF state, the transformer voltage reverses, forward-biasing the output catch diode(s) and delivering energy to the output(s). With a flyback topology, an output can be positive or negative (defined by a transformer polarity dot).

There are three basic energy-transfer modes of operation:

- Continuous Conduction mode (CCM) – when a part of the energy stored in the flyback transformer remains in the transformer when the next ON period begins.
- Discontinuous Conduction mode (DCM) – in which all of the energy stored in the transformer is transferred to the load during the OFF period.
- Critical Conduction mode (CrCM), also called Transition mode (TM) – which is just at the boundary between DCM and CCM, occurring when the stored energy reaches zero at the end of the switching period. The waveforms of CCM, DCM and CrCM are shown in [Figure 2](#), [Figure 3](#) and [Figure 4](#), respectively.

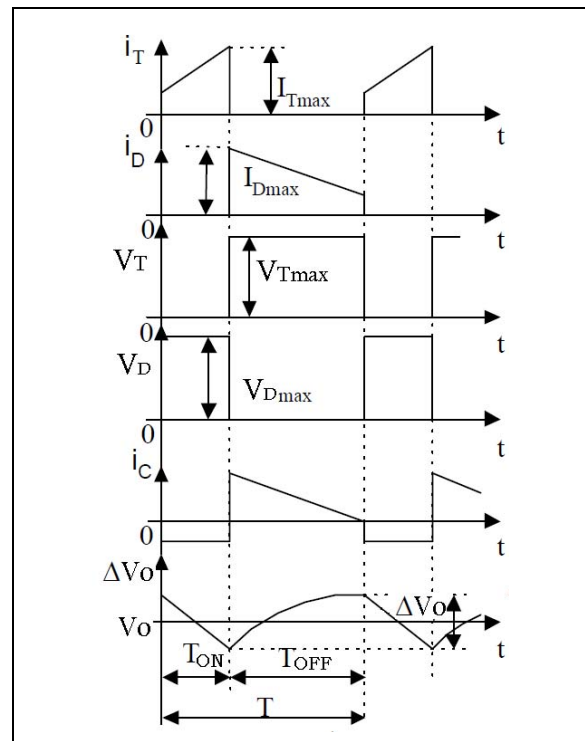
FIGURE 2: CCM OPERATION WAVEFORMS

Figure 2 and Figure 3 illustrate the current flow in CCM and DCM operation. With DCM operation, when the primary MOSFET turns on, the primary current starts at zero and rises to a peak value that can be more than twice the peak current in a comparable CCM application. At turn-off, the ampere-turns transfer to the secondary and the secondary current decreases to zero where it remains until the beginning of the next switching cycle. A flyback transformer designed for DCM operation requires a smaller inductance value than the one designed for CCM operation, since the current ripple (ΔI_L) is much higher.

FIGURE 3: DCM OPERATION WAVEFORMS

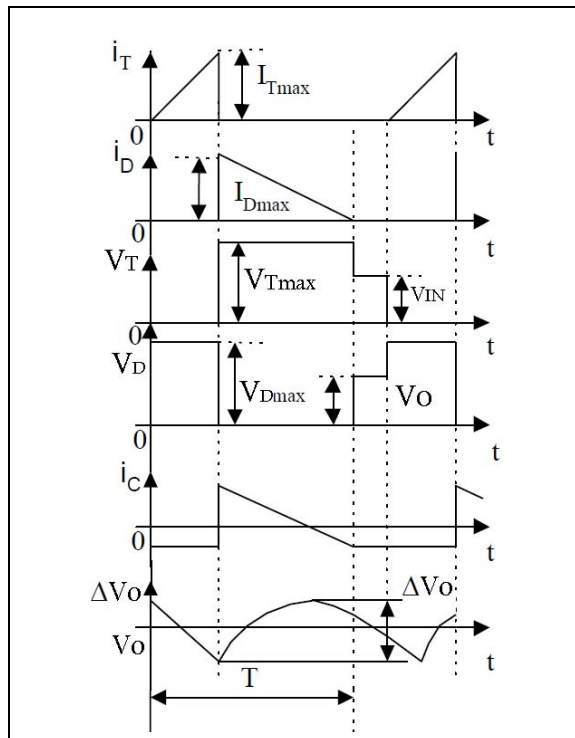
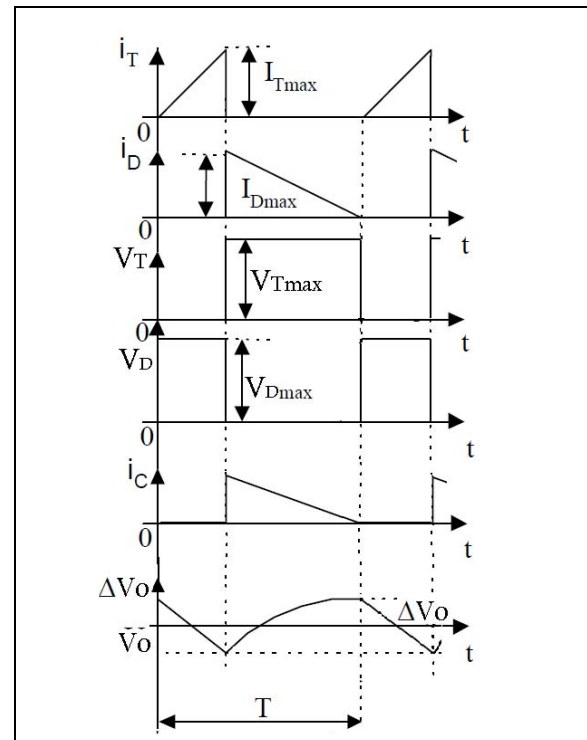


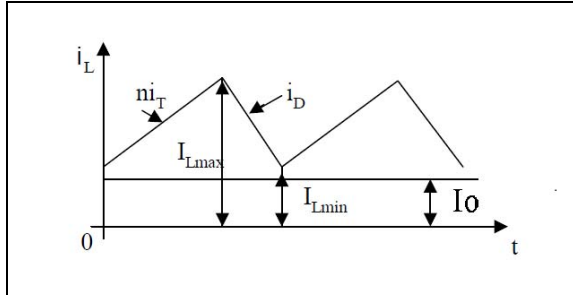
FIGURE 4: CrCM OPERATION WAVEFORMS



EQUATION 3: OFF TIME IN CCM

$$T_{OFF} = T \cdot \frac{V_{IN}}{V_{IN} + n \cdot V_O}$$

FIGURE 6: REFLECTED CURRENT IN THE SECONDARY OPERATING IN CCM



The output current represents the average current through the diode and can be calculated by using [Equation 4](#).

EQUATION 4: OUTPUT CURRENT IN CCM

$$I_O = \frac{I_{Lmin} + I_{Lmax}}{2} \cdot \frac{T_{OFF}}{T}$$

The minimum and maximum value of I_L can be calculated using [Equation 5](#) and [Equation 6](#).

EQUATION 5: MINIMUM INDUCTOR CURRENT IN CCM

$$I_{Lmin} = I_O \cdot \left(1 + \frac{n \cdot V_O}{V_{IN}}\right) - \frac{V_{IN} \cdot T}{2 \cdot n \cdot L} \cdot \frac{n \cdot V_O}{V_{IN} + n \cdot V_O}$$

EQUATION 6: MAXIMUM INDUCTOR CURRENT IN CCM

$$I_{Lmax} = I_O \cdot \left(1 + \frac{n \cdot V_O}{V_{IN}}\right) + \frac{V_{IN} \cdot T}{2 \cdot n \cdot L} \cdot \frac{n \cdot V_O}{V_{IN} + n \cdot V_O}$$

If I_O drops lower than a limit value I_{OL} , then I_{Lmin} becomes '0' and the converter will operate in CrCM as shown in [Figure 7](#). I_{OL} can be calculated using [Equation 7](#).

EQUATION 7: OUTPUT CURRENT LIMIT IN CCM

$$I_{OL} = \frac{V_O \cdot T}{2 \cdot L} \cdot \left(\frac{V_{INmax}}{V_{INmax} + n \cdot V_O}\right)^2$$

2. Discontinuous Conduction Mode

In Discontinuous Conduction mode, the reflected current in the secondary reaches zero during a commutation period, as shown in Figure 8. The rising slope does not change from CCM, but the falling slope becomes more abrupt. The flyback transformer used in the Discontinuous mode is much smaller because the inductive energy stored is only 1/5 to 1/10 of the energy required in comparable Continuous Conduction mode circuits. The turn-on circuits are simplified because load current in the power switch is zero during turn-on and there is no concern for turn-on losses or turn-on snubber circuits. Conducted Electromagnetic Interferences (EMI) are reduced because transistor turn-on occurs with zero collector current. Core loss must be considered when operating in DCM (and CrCM), given the large AC component of the magnetic field. CCM operation usually corresponds to a lower AC magnetic field; thus, the main limitation when designing the transformer becomes core saturation rather than core losses.

While in DCM, transferred energy is dictated by ON time, input voltage, and inductance value. There is always a complete energy transfer during every cycle, defined by Equation 8, where P_{DCM} is the load power while in DCM, L is the inductance value measured at primary of the transformer and f is the switching frequency.

EQUATION 8: OUTPUT POWER IN DCM

$$P_{DCM} = \frac{V_{IN}^2 \cdot D^2}{2 \cdot L \cdot f}$$

FIGURE 7: REFLECTED CURRENT IN THE SECONDARY OPERATING IN CrCM

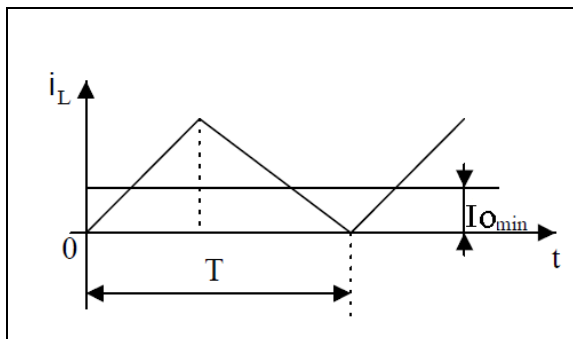
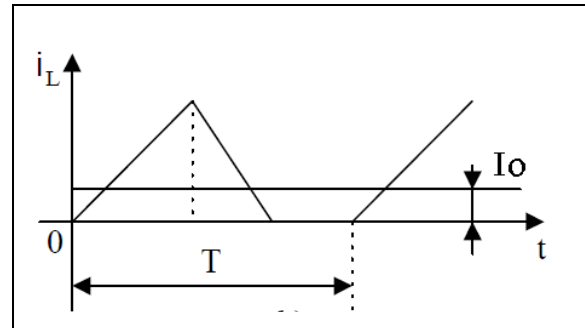


FIGURE 8: REFLECTED CURRENT IN THE SECONDARY OPERATING IN DCM



Although there is discontinuity of current on both sides of the transformer, operating in CCM generally results in better efficiency than operating in DCM. One reason supporting this fact is that a higher root mean square (RMS) current in DCM means a higher dissipation in the MOSFET, in the primary and secondary capacitors, and in the primary clamp. However, because the inductance value is lower for the DCM operation, a transformer that has the same physical size may have less conduction loss for this DCM operation than if it was designed for the CCM operation, even if its RMS current is higher. In some AC-line applications and operating conditions, the CrCM operation may be able to provide similar or even higher efficiency than CCM.

Control Aspects

The two most popular ways of controlling the operation of a flyback topology are Voltage Mode Control (VMC) and current-mode control (CMC). CMC uses the magnetizing current to define the duty cycle, while VMC does not. When operating in CCM, a design using VMC has a relatively low-frequency double pole due to the transformer's inductance and the output capacitor. It is more difficult to compensate than CMC, which basically consists of a current source driving the same capacitor. Conversely, when using CMC while operating in CCM, the comparator has to avoid sub-harmonic oscillation when the operating duty cycle exceeds or even gets near 50%. This is usually accomplished by the addition of an external ramp to the current-feedback signal, creating a composite signal.

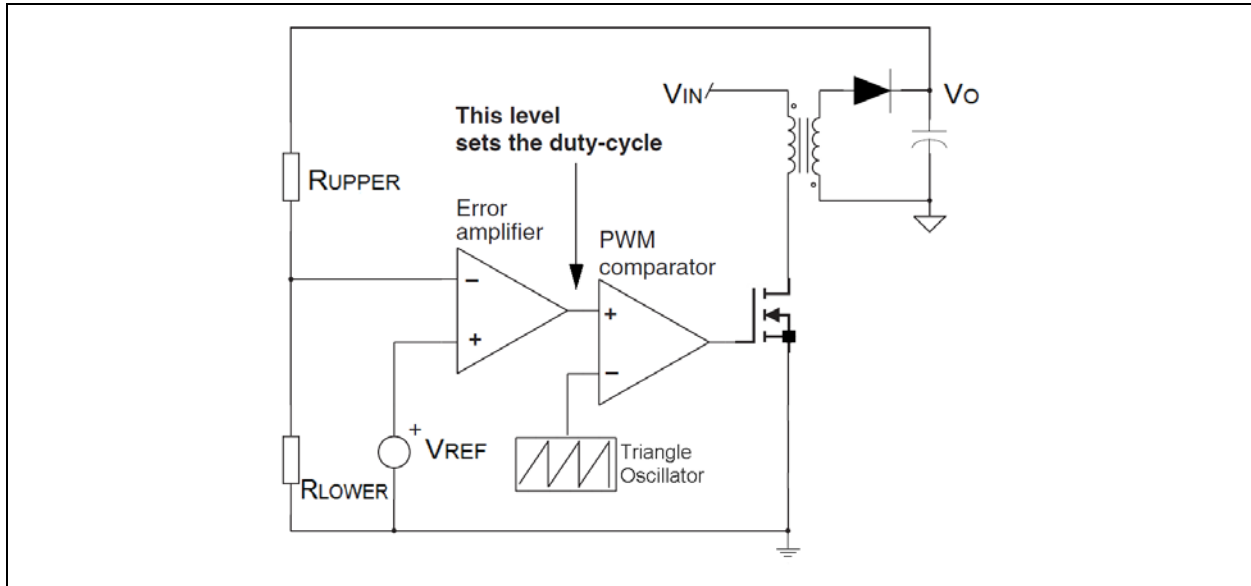
Voltage Mode Operation

The Voltage Mode Control is probably the most common way to control a power supply. An error voltage obtained from the difference between a reference voltage and a portion of the output voltage is permanently compared to a fixed-frequency and amplitude sawtooth. The crossing point between these two signals generates a transition on the comparator's output. When the output voltage deviates from its

natural target, the error voltage increases and as a result, the point at which both the error and sawtooth signals cross, naturally expands the distance between the toggling points: D is increased.

Figure 9 depicts a simple convertor operated by a Voltage mode PWM controller. Voltage mode is also called direct duty cycle control, as the error voltage drives directly the duty cycle.

FIGURE 9: PRACTICAL IMPLEMENTATION OF VOLTAGE MODE CONTROL CIRCUITRY (ERROR VOLTAGE SETS ON-TIME DURATION)



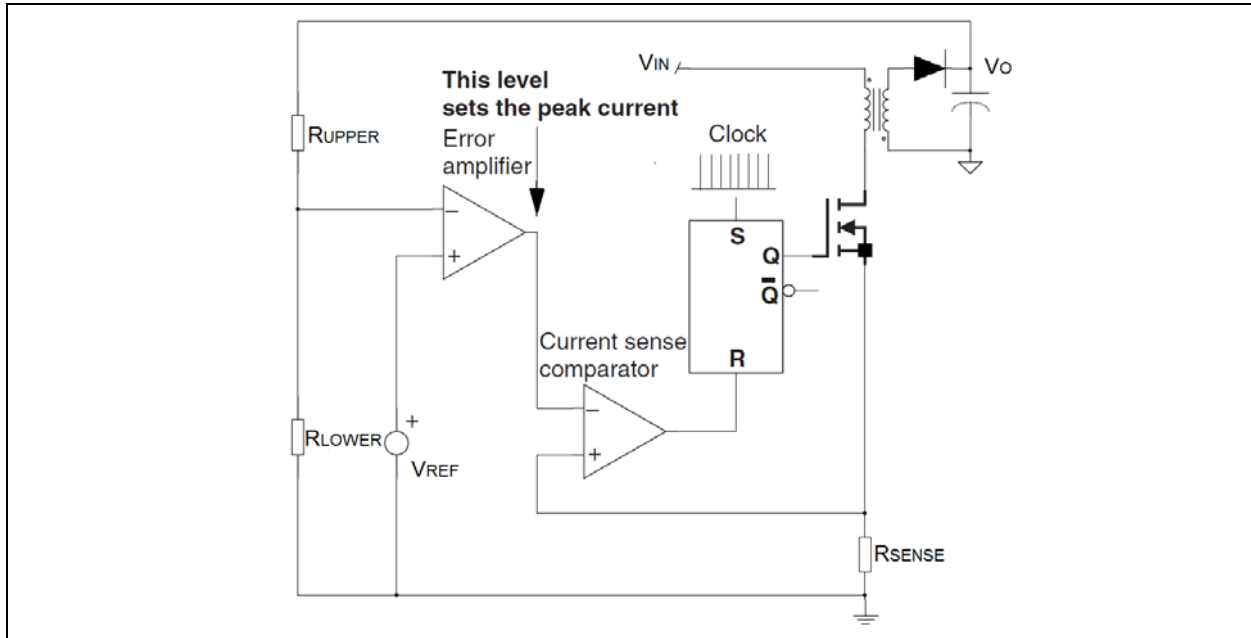
Current-Mode Operation

The current-mode modulators rely on the circulating inductor current to make the toggling decision. A clock pulse sets a latch which closes the power switch. The current ramps up in the inductor, following a V/L slope. When the current reaches a given set point value, a comparator detects it and resets the latch; the switch now opens and waits for the next clock cycle to close again; this is depicted in more detail in [Section "Flyback Logic with CIPs"](#). Figure 10 depicts a standard implementation of a current-mode controller. Current-mode control offers faster response to output changes, a more simple compensation circuit and higher bandwidth over a comparable Voltage mode circuit. An additional benefit with current-mode circuits include inherent pulse-by-pulse current limiting, and the ease of providing load sharing when multiple power units are in parallel. This design uses the current-mode control logic.

First Calculations

The first calculation for this design was done using a tool called "POWER 4-5-6". This tool has all the mathematical calculations used to get started and gives an idea of how the design will work, what values the components will have and what kind of transformer will be needed. Some laboratory time and adjustments still must happen in order to have the design work as needed.

FIGURE 10: INDIRECT CONTROL VIA INDUCTOR PEAK CURRENT



This tool provides the ability to select the specifications of the converter, as shown in [Figure 11](#). In this case, the input is of 85-264 Volts at 50 Hz, the output of 12 Volts at 1.8 ampere (~ 21W), and an auxiliary with 10 Volts at 0.2 ampere (2W). This will serve as the power source for the microcontroller and driver after the bootstrap provides enough power to start the SMPS.

FIGURE 11: INPUT AND OUTPUT SPECIFICATIONS FOR THE DESIGN

Input and Output Specifications

Flyback Converter

Clear Design

INPUT VOLTAGE RANGE

☐ 120 VAC

☐ 240 VAC

☒ 120-240 VAC

☐ DC Input

Low Line Voltage

85

Nominal Input Voltage

240

High Line Voltage

264

AC LINE FREQUENCY

☒ 50 Hz

☐ 60 Hz

☐ 400 Hz

☐ Custom Frequency

Hz

OUTPUT VOLTAGE AND CURRENT

Main

Aux 1

Aux 2

Aux 3

Aux 4

Output Voltage

12

10

Output Current

1.8

0.2

Clear Aux

POWER SUPPLY COOLING

☐ High Airflow

☐ Moderate

☐ Low Airflow

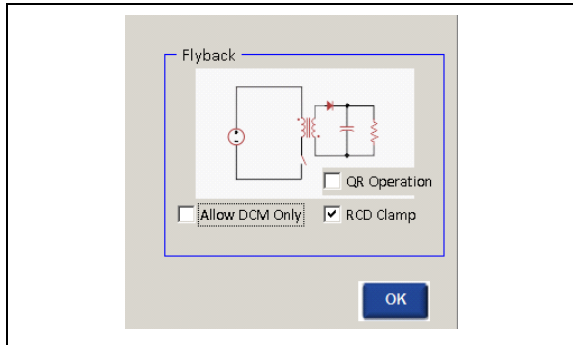
☒ None

25

Help

OK

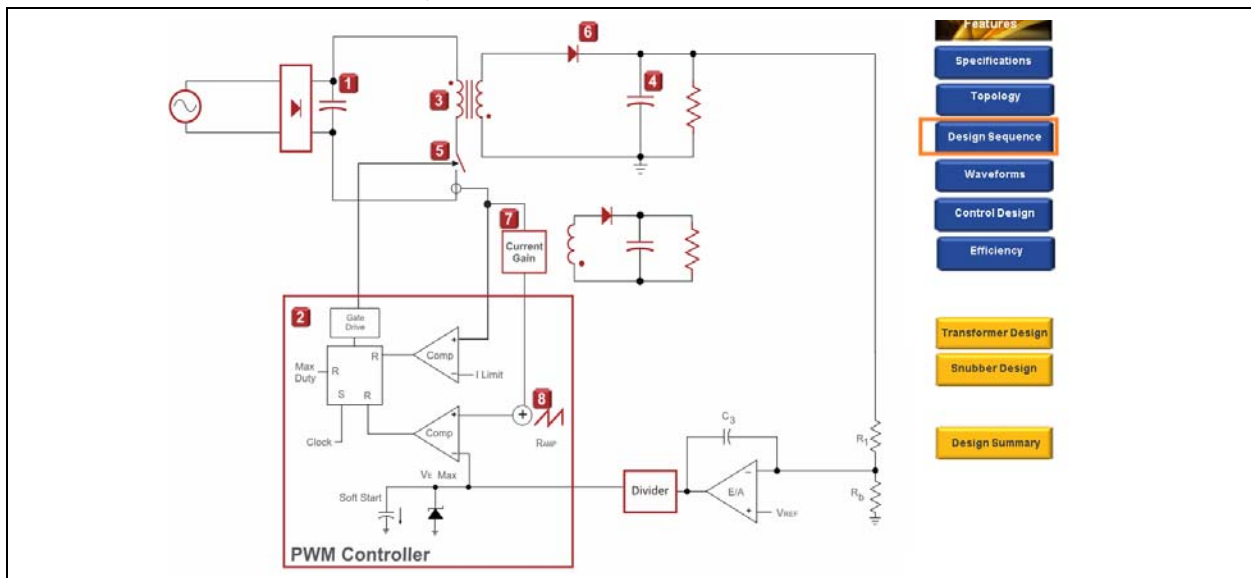
The tool will provide the option to choose from nine different topologies, depending on the specifications. The flyback topology is selected with RCD clamp, as shown in [Figure 12](#).

FIGURE 12: TOPOLOGY SELECTION

These design sequences come with suggested values by the tool, but also give the user the possibility of changing nearly everything, so that the user can apply values from the off-the-shelf components. More information about the tool and how to use it can be found at [2] in [Section “References”](#).

The component selection, control method and sensing method can be seen in [Figure 13](#). This tool shows how the topology looks, how the PWM controller is connected and how the compensation is to be placed. The design sequences are labeled from 1 to 8 as follows:

1. Input Capacitor design
2. PWM Controller design
3. Flyback Transformer design
4. Multiple-Outputs Capacitor design
5. Power Switch design
6. Diodes for Multiple Output
7. Current Sense Gain
8. PWM Ramp design

FIGURE 13: DESIGNING SEQUENCE

PWM Controller Design

The tool allows changes to the PWM controller values to get closer to the ones used, as depicted in Figure 15. It has dedicated IC in which the tool already has all the needed information, as depicted in Figure 14. The one selected is PIC16F1769.

FIGURE 14: PWM CONTROLLER SELECT STAGE

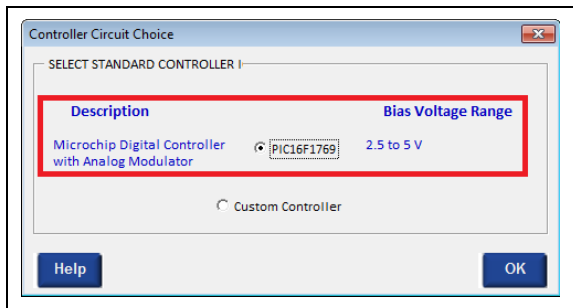
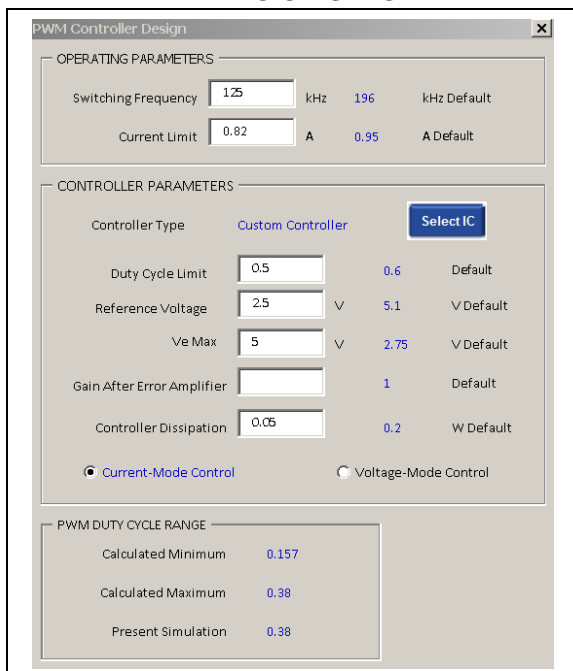


FIGURE 15: PWM CONTROLLER DESIGN STAGE



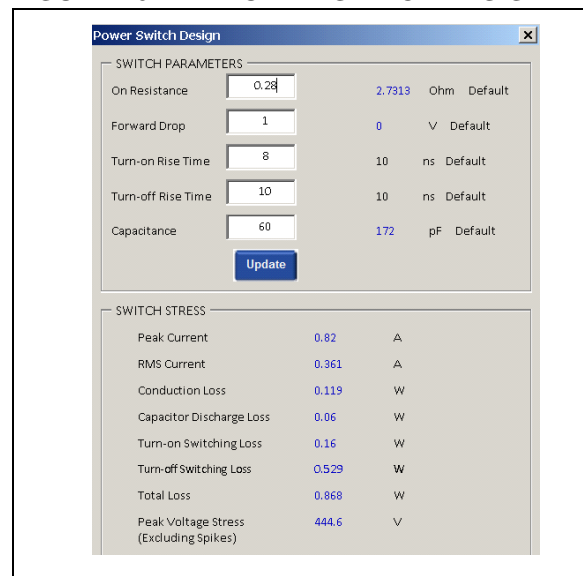
Flyback Transformer Design

The ability to change the transformer values allows for high flexibility in the design and in the choice of components. Compared to other tools, this one permits the detailed design of the transformer, the core materials and dimensions, the wire thickness, and the possibility to wind in different ways.

Power Switch Design

Figure 16 shows the parameters that need to be defined when designing the power switch. The switch stress are shown in the lower box, and can be used to check for compatibility with other off the shelf switching devices.

FIGURE 16: POWER SWITCH DESIGN



Current Sense Gain Design

Figure 17 below depicts the design of the current sense.

FIGURE 17: CURRENT SENSE GAIN DESIGN WINDOW

Current Sense Gain

☒ Use Sense Resistor ☐ Use Current Transformer

RESISTIVE SENSING

Sense Resistor: Ohm **Update** 3.327 Ω Default

Dissipation: 2.6E-01 W

CURRENT TRANSFORMER SENSING

Number of Turns: **Update** 50,000 Turns Default

Sense Resistor: Ω **Update** 166.348 Ω Default

Dissipation: 8.7E-03 W

CURRENT GAIN

3.327 V/A Recommended Value

2.000 V/A Actual Value

2.6E-01 W Current Sensing Loss

RECOMMENDED FILTER VALUES

Filter Resistor R_f	470	Ω
Filter Capacitor C_f	1.088	nF
Time Constant	0.51	μs

The tool provides the possibility to view the simulated waveforms and track the influence of different component changes, avoiding long simulation periods of other tools. This allows faster learning for new designers. Figure 18 depicts the summary of the needed SMPS project.

Mathematical Method

FIGURE 18: FIRST CALCULATION SUMMARY USING POWER 4-5-6

Project Name			Simulated Converter Loss and Efficiency		
Flyback Converter			Input Voltage	114.50	VDC
Input Specifications			Output Voltage	11.735	V
Input Voltage Type	AC		Output Power	22.95	W
Minimum AC Line	90	VAC	Semiconductor Conduction	1.100	W
Nominal AC Line	210	VAC	Switching Loss	0.689	W
Maximum AC Line	265	VAC	Actual Winding Loss	0.388	W
AC Line Frequency	50	Hz	Core Loss	0.196	W
Maximum DC Input	374.70	V	Snubbers	0.423	W
Nominal DC Input	296.90	V	Capacitor ESR Loss	0.069	W
Minimum DC Input	114.50	V	Controller, Current Sense	0.311	W
Input Rectifier Design			Total Loss	3.18	W
Rectifier Type	Full-Wave		DC-DC Efficiency	88.74	%
Input Bulk Capacitor	47.00	μF	Input filter loss not included		
Low Line Input Voltage	89.20	V	PWM Controller Values		
Output Specifications			Frequency	125.00	kHz
Output 1 (Regulated)	12.00	V	Compensating Ramp	2.64	V
Output 1 Current	1.80	A	V ref:	2.50	V
Total Load Power	24.00	W	Current Limit	0.82	A
Selected Circuit Topology			Ve Max:	5.00	V
Topology	Flyback Converter		Maximum Duty Cycle	0.50	
Control	Current-Mode		Single Capacitors for Multiple Outputs		
Control Circuit	Custom Controller		Capacitance Output 1	480.00	μF
Auxiliary Output Specifications			ESR Output 1	25.60	mΩ
Output 2	12.00	V	Capacitance Output 2	10.00	μF
Output 2 Current	0.20	A	ESR Output 2	230.40	mΩ
Input Capacitor Design			Output Diode		
Capacitance	47.00	μF	Diode Voltage Drop	0.49 V	V
ESR	26.03	mΩ	Dissipation	0.886	W
Power Dissipation	0.01	W	Peak current	4.132	A
Transformer Design			Peak voltage stress	78.900	V
Turns Ratio	5.60 : 1		Power Switches		
Magnetizing Inductance	672.36	μH	Switch Resistance	0.280	Ω
Primary Turns	28		Peak switch current	0.820	A
Primary Resistance	2.57	mOhm	Per switch rms current	0.36	A
Secondary 1 Turns	5.00		Total switch dissipation	0.87	W
Secondary 1 Resistance	5.71	mOhm	Peak voltage stress	445	V

If the tools are not at the designers disposal, the mathematical calculations can still be of help at the first designing steps. The designer needs to specify the following specs:

V_O ; V_{P_MIN} ; V_{P_NOM} ; V_{P_MAX} ; V_D ; I_{S_MAX} ; f_{SW} ; ΔV_O ; V_{T_MAX} ; V_{T_MAX*} ;

Then, the following parameters need to be calculated:

- The duty cycle: D
- Winding turns ratio: n
- Inductivities of primary NP and secondary NS winding:
 - L_{P_MIN}
 - L_{S_MIN}

- Current in primary winding:
 - I_{T_MAX}
 - I_{T_MIN}
- Current in secondary winding:
 - I_{L_MAX}
 - I_{L_MIN}
- The maximum diode breakdown voltage: V_{D_MAX}
- The output capacitance: C_S
- ESR: R_{ESR}
- Number of turns in the primary coil: N_P
- Number of turns in the secondary coil: N_S
- Ferrite core volume of the transformer: V_E

EQUATION 9: FIRST CALCULATIONS

Consider the following:

$$V'_P = V_P - V_{CEsat} - V_{Rpp}$$

Ex: $V'_{Pmin} = 110V - 1V - 0.2V = 108.8V$

$$V'_O = V_O + V_F + V_{Rps}$$

Ex: $V'_O = 12V + 0.65V + 0.2V = 12.85V$

The minimum duty cycle:

$$D_{min} = 1 - \frac{V'_{Pmax}}{V'_{Tmax}}$$

Winding turns ratio:

$$n = \frac{V'_{Pmax} \cdot D_{max}}{V'_O \cdot (1 - D_{max})}$$

(here D_{MIN} is used as initial D_{MAX})

Transistor in Conduction mode T_{ON} :

$$T = \frac{1}{f_{sw}}$$

$$T_{ON} = T \cdot \frac{n \cdot V'_O}{V'_P + n \cdot V'_O}$$

$$D = \frac{T_{ON}}{T}$$

Inductivities of primary NP and secondary NS winding:

$$L_{Smin} = \frac{V'_{Pmax} \cdot T}{2 \cdot n \cdot I_{OL}} \cdot D_{min} (1 - D_{min}) \quad (\text{here } I_{OL} \text{ will be } I_{O_MAX})$$

$$L_{Pmin} = n^2 \cdot L_{Smin}$$

Current in primary and secondary winding:

$$I_{Lmax} = \frac{I_O}{1 - D} + \frac{T \cdot V'_O}{2 \cdot L_{Smin}} (1 - D)$$

$$I_{Lmin} = \frac{I_O}{1 - D} - \frac{T \cdot V'_O}{2 \cdot L_{Smin}} (1 - D)$$

$$I_{Tmax} \geq \frac{I_{Lmax}}{n}$$

$$I_{Tmin} = \frac{I_{Lmin}}{n}$$

The maximum diode breakdown voltage:

$$V_{Dmax} = \frac{V'_{Pmax}}{n(1 - D_{min})}$$

The output capacitance:

$$C_O = \frac{T \cdot I_{Omax}}{\Delta V_O} \cdot \frac{n \cdot V'_O}{V'_{Lmin} + n \cdot V'_O}$$

Equivalent Series Resistance (ESR):

$$R_C \leq \frac{\Delta V_O}{I_{Omax}}$$

MOSFET, OUTPUT DIODE AND CAPACITOR SELECTIONS

Having a discrete MOSFET design allows greater design flexibility than having an integrated chip with driver, controller and switcher on the same package. The designer can change to a higher voltage part with the same control part.

The transistor must be chosen to support the maximum voltage that can appear during functionality, to support the maximum collector current and to have a small drain-to-source resistor to minimize losses.

The maximum current through the transistor and drain-to-source voltage can be calculated using equations [Equation 10](#) and [Equation 11](#).

EQUATION 10: MAXIMUM CURRENT THROUGH THE TRANSISTOR

$$I_{Tmax} = \frac{P_{Omax}}{n \cdot V_O} \cdot \left(\frac{n \cdot V_O + V_{IN}}{V_{INmin}} \right) + \frac{V_{INmin} \cdot T}{2 \cdot n \cdot L} \cdot \frac{n \cdot V_O}{V_{INmin} + n \cdot V_O}$$

EQUATION 11: MAXIMUM DRAIN TO SOURCE VOLTAGE

$$V_{Tmax} = \frac{V_{INmax}}{1 - D_{min}}$$

In this case, I_{Tmax} is approximately 1A and V_{Tmax} approximately 450V. The results being close to what POWER 4-5-6 suggests.

The MOSFET for this design belongs to Infineon Technologies IPP65R190C7FKSA1 and has the following values of interest, depicted in [Equation 12](#):

EQUATION 12: VALUES OF INTEREST FROM THE CHOSEN MOSFET

$V_{DSS} = 800V$; $R_{DS} = 0.45\Omega$; $I_D = 11A$; $R_W = 41W$; $R_{thj-amb} = 80 \text{ } ^\circ C/W$; $C_{OSS} = 65 \text{ pF}$

Conduction power losses $P_{CL} = I_{PRMS}^2 \cdot R_{DS} = 0.36V^2 \cdot 0.45\Omega = 58 \text{ mW}$

Commutation power loss $P_{off} = \frac{V_{INmax} \cdot I_{Tmax} \cdot t_f \cdot f_{sw}}{6} = \frac{375V \cdot 0.82A \cdot 10 \text{ ns} \cdot 125 \text{ kHz}}{6} = 64 \text{ mW}$

Capacitance loss $P_{cap} = \frac{(C_{OSS} + C_P) \cdot V_{INmax}^2 \cdot f_{sw}}{2} = \frac{(65 \text{ pF} + 20 \text{ pF}) \cdot 375V^2 \cdot 125 \text{ kHz}}{2} = 747 \text{ mW}$

Total power loss $P_{tot} = P_{CL} + P_{off} + P_{cap} = 869 \text{ mW}$

Which is close to what POWER4-5-6 suggested.

If choosing a heat sink is needed, use the formula in [Equation 13](#). When the maximum junction temperature is 150°C for MOSFET, the ambient temperature is selected by the designer, depending on the ambient where SMPS will work. The junction-to-ambient and the junction-to-radiator temperature can be found in the device data sheet. The remaining radiator to ambient can be calculated and so a decision for a heat sink can be made.

EQUATION 13: JUNCTION TEMPERATURE EQUATION

$$\frac{T_J - T_A}{P_{tot}} = R_{thj-amb} + R_{thj-rad} + R_{thr-amb}$$

The diode must be chosen in order to support the maximum current that can appear during functionality, and to support the maximum output voltage combined with the voltage seen at the transformer output. [Equation 14](#) and [Equation 15](#) show exactly how they are calculated. In this case, the maximum diode current is $I_{Dmax} = 0.82A \times 5.6 = 4.59A$, and the peak voltage stress is $V_{Dmax} = (375/5.6) + 12 = 78.9V$. When searching Digi-Key, or another supplier for a compatible part, a diode from ON Semiconductor MBR20H150CTG Schottky Rectifier is selected, since it has a forward current of 20A and a repetitive reverse voltage of 150V. Thus, the part meets the criteria and has room for safety in case the calculated limits are surpassed in practical implementation.

EQUATION 14: MAXIMUM CURRENT ON THE OUTPUT DIODE

$$I_{Dmax} = I_{Tmax} \cdot n$$

EQUATION 15: MAXIMUM VOLTAGE ON THE OUTPUT DIODE

$$V_{Dmax} = \frac{V_{INmax}}{n} + V_O$$

The value of the output capacitor is calculated based on the permitted output ripple and transient response. The designer must verify if the effective current value through the capacitor does not exceed the permitted value given in the data sheet. [Equation 16](#) can help decide the proper value. If the voltage variation at the output might be 10-20 mV, a capacitor value of 280 uF to 560 uF is resulted. When choosing the capacitor, select a voltage that will cover at least from 1.5 or 2 times the chosen voltage; for this project, the choice is a value of 660 uF with maximum voltage support of 35V.

EQUATION 16: OUTPUT CAPACITANCE EQUATION

$$C = \frac{I_{Smax} \cdot T}{\Delta U_S} \cdot \frac{U_S \cdot n}{U_{Imin} + U_S \cdot n}$$

CURRENT SENSING

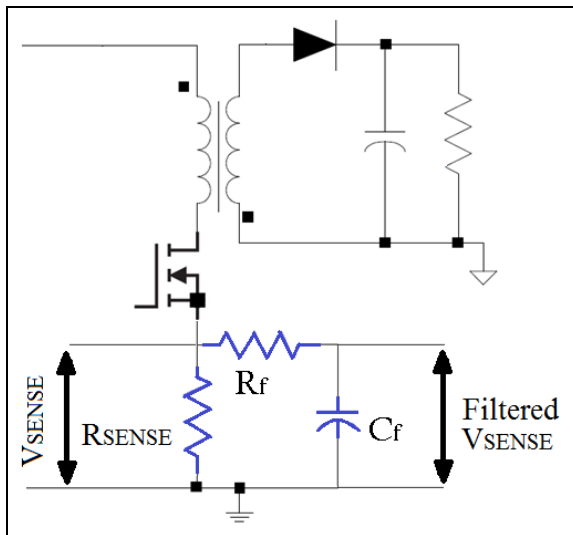
A very important step when designing SMPS is the control waveform sensing. Be it the output voltage, output current, input voltage or inductor current needing attention, since depending on the control method, the sensed waveforms will be compared and some control decisions will be taken based on their value. If they are not correct, the whole control system will fail to work as expected.

Regardless of the type of feedback control, almost all DC-DC converters and linear regulators sense the inductor current for overcurrent (overload) protection. Additionally, the sensed current is used in current-mode control DC-DC converters for loop control. Since instantaneous changes in the input voltage are immediately reflected in the inductor current, current-mode control provides excellent line transient response. There are various techniques to sense the inductor current, among the most used being the sense resistor or the current transformer. The designer has to choose the method that will comply better with the specifications of the project.

Series-Sense Resistor

This technique is the most common way of sensing current in flyback power supplies; it inserts a sense resistor in the path of the inductor current, as depicted in [Figure 19](#). If the value of the resistor is known, the current flowing through the inductor is determined by sensing the voltage across it. The advantage of this method is that it has good accuracy, but it unfortunately reduces the efficiency of the converter as the current flowing through the sense resistor dissipates power. The RC filter is used due to the parasitic capacitance between the gate and the source of the MOSFET. When the gate is pulled high, it generates a glitch on the current sense resistor that can prematurely end the PWM pulse if not filtered off, or blanking if it is not enabled on the falling event trigger.

FIGURE 19: CURRENT SENSING WITH A SERIES-SENSE RESISTOR



RDS Sensing

This technique uses the ON resistance of the MOSFET to calculate the current; assuming small drain-source voltages, the equivalent resistance of the device is calculated using Equation 17.

EQUATION 17: EQUIVALENT RESISTANCE

$$R_{DS} = \frac{L}{W\mu C_{OX}(V_{GS} - V_T)}$$

Here, μ is the mobility, C_{OX} is the oxide capacitance per unit area, and V_T is the threshold voltage. This technique lacks accuracy since the resistance of the MOSFET is nonlinear, has process variations and depends on temperature, but allows for higher efficiency, as series resistance is omitted.

Sensorless Approach

This technique uses the inductor voltage to measure the inductor current using the voltage-current relation of the inductor as shown in Equation 18. Sensorless method is never used in offline flyback design because the voltage across the transformer primary is very large, and jumps even higher during discharge.

EQUATION 18: VOLTAGE-CURRENT IN AN INDUCTOR

$$V = L \frac{di}{dt}$$

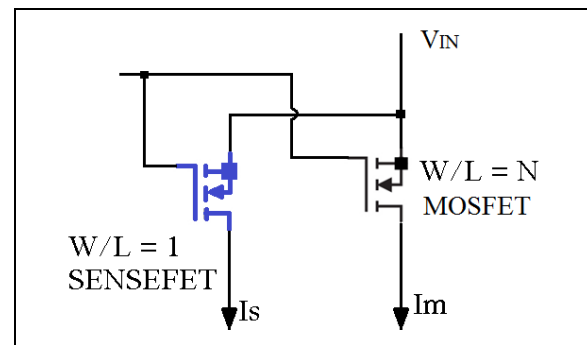
Current Transformers

This technique uses the current-sensing transformers and is very common in high-power designs. The idea is to sense a fraction of the high-inductor current by using the mutual inductance properties of a transformer. The major disadvantage is the increase in cost and size.

SENSEFETs

This technique uses a current-sensing MOSFET in parallel with the power MOSFET as shown in Figure 20, and uses its measuring capabilities to sense the current.

FIGURE 20: USE OF SENSEFET TO MONITOR THE CURRENT



The effective width (W) of the sense MOSFET is significantly smaller (at least 100 times) than the one of the power MOSFET and the voltages of node M and S should be equal.

TABLE 1: ADVANTAGES AND DISADVANTAGES OF CURRENT-SENSING TECHNIQUES

Method	Advantages	Disadvantages
Series Resistor	Good Accuracy	High-Power Dissipation
RDS	Lossless	Low Accuracy
Observer	Lossless	Knowledge of L
Current Transformer	Lossless, isolation	Cost, Size
SenseFET	Lossless, moderate accuracy	Special MOSFETs, matching issues, Low bandwidth (not available for high voltages)

Table 1 summarizes the methods briefly discussed.

When selecting a sensing method for the project, the designer must take into consideration the priorities like cost, size, efficiency, accuracy and the type of control.

In this design the series-sensing resistor method is selected, and taking into account that the current flowing in the inductor will vary from 0.9A at full load to 0.1A at low load, a 1Ω, 1.5Ω or 2Ω resistor will provide a triangular waveform voltage signal from 0.1V to 2V t, equivalent to the current waveform in the inductor. The RC filter has R = 510Ω and C = 470 pF components, this combination attenuating the signal enough to stop the switching peak to trigger a false turn-off, and it is fast enough not to introduce a delay and a larger minimum duty cycle.

TRANSFORMER DESIGN

The design guidelines that help achieve a better transformer are summarized below:

1. Minimize the leakage inductance from the primary winding to the main secondary winding. This can be achieved by minimizing the separation, interleaving or even using a core with long and narrow window that allows minimum number of layers.
2. Minimize the leakage between the main secondary and the auxiliary.
3. Consider using Multifilar® or Litz wires for better efficiency.
4. The turn ratio has an impact on duty cycle and efficiency.
5. Always test the transformer in a real test circuit to validate and optimize the design.

If the designer has the opportunity to build a transformer, that will leave room for improvements and adaptations.

When designing the transformer using the equations or the tools, the first step is to determine the turns-ratio required at low-input voltage that will give a proper output voltage without having a too big duty cycle. If the turns-ratio is too small, there is the possibility to have a close-to-zero duty cycle or pulse skipping when the circuit is in low load.

When designing a project for a low-power flyback converter, it is common to operate with a low maximum duty cycle in order to have a smaller stress on the power switcher, but when designing projects for higher powers some may allow the duty cycle to go over 50% to reduce the stress on the secondary parts.

For this design, the maximum duty cycle is allowed to go close to 47%, and with minimum input voltage of 85V, a turns-ratio bigger than five will provide sufficient voltage to operate over the specified range.

Equation 19 and Equation 20 will show these calculations:

EQUATION 19: TURNS-RATIO EQUATION

$$n = \frac{V_{IN}}{V_O} \cdot \frac{D}{(1-D)}$$

EQUATION 20: DUTY CYCLE EQUATION

$$D = \frac{nV_O'}{V_{IN} + nV_O'}$$

The freedom of choosing the primary inductance value is even bigger, and for many flyback converters that operate at 10W or less, the designer will choose a value to force the converter to operate in Discontinuous Conduction mode. At all load conditions, but with higher power levels this will cause high-primary currents, while a larger inductance value will reduce the peak current stress. All equations give a starting point to the design and some testing with different transformers will be beneficial.

The turns-ratio determines the trade-off between primary and secondary peak voltages and peak currents.

Equation 21, Equation 22 and Equation 23 will help calculate the values of the current waveforms. Equation 22 uses $I_{MIN} = 0$ in CrCM and DCM.

EQUATION 21: DC CURRENT

$$I_{dc} = D \frac{(I_{pk} + I_{min})}{2} = DI_{AV}$$

EQUATION 22: RMS CURRENT

$$I_{rms} = \sqrt{D \left[(I_{pk} \cdot I_{min}) + \frac{1}{3} (I_{pk} - I_{min})^2 \right]}$$

EQUATION 23: AC CURRENT

$$I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

For this design the following considerations are taken to calculate the transformer values:

- Input Voltage (85V-265V)
- Output Voltage (12)
- Full-load Current (1.8A)
- Circuit Topology (Flyback, CCM)
- Switching Frequency (125 kHz)
- Desired Duty Cycle (0.47 @ 110V input)
- Maximum Ripple Current in the Secondary (4.2A @ 12V)
- Peak Short-circuit Current in the Secondary (14A)

The turns-ratio are defined using Equation 24.

EQUATION 24: TURNS-RATIO CALCULATION

$$n = \frac{V_{IN}}{V_O} \cdot \frac{D}{(1-D)} = \frac{85}{12.5} \cdot \frac{0.47}{1-0.47} \approx 6$$

Then, a core material has to be selected using guidance from the manufacturer's data sheet *Core*. The maximum flux density and maximum flux swing are determined afterwards for the operation of the core. It is recommended to use a saturation-limited B_{MAX} of 0.3T; B will reach its maximum when peak currents reach the short-circuit limit. The gapped core is assumed to have reasonable linearity of the B-H characteristic so B_{MAX} can be calculated with maximum current ripple, as seen in Equation 25.

EQUATION 25: MAXIMUM MAGNETIC FIELD VARIATION

$$\Delta B_{MAX} = B_{MAX} \frac{\Delta I_{pk-pk}}{I_{SC}} = 0.3 \frac{4.2}{14} = 0.09 \text{ Tesla}$$

Select the core shape and size using guidance from manufacturers or using the area product formula: Core type, Family: E-E core – EFD Series.

An approximate core area of 0.499 cm² is needed and the core EFD30 offers a minimum area of 0.66 cm², which will provide enough space for this project.

EQUATION 26: FERRITE CORE VOLUME AND NUMBER OF TURNS CALCULATIONS

$$\mu_0 = 4 \cdot \pi \cdot 10^{-7} \frac{H}{m}; \mu_e = 125 \quad V_e = \mu_0 \cdot \mu_e \cdot \frac{I^2 L_{max} \cdot L_{Smin}}{B_{max}^2} = 4 \cdot \pi \cdot 10^{-7} \left(\frac{H}{m} \cdot 125 \cdot \frac{(14A)^2 \cdot 4.3 \mu H}{(0.3T)^2} \right) = 1470 \text{ mm}^3$$

FERRITE CORE, EFD30, EC90 with the $AL = 160 \text{ nh/sp}^2$ and $A_e = 69 \text{ mm}^2$

$$\text{Number of turns in the secondary coil: } N_s \quad N_s = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{4.3 \mu H}{0.16 \mu H/sp^2}} \sim 5$$

$$\text{Number of turns in the primary coil: } N_p \quad N_p = N_s \cdot n = 5 \cdot 5.6 = 28$$

Wire conditions and considerations: Current density: $J_{Cu} = 3 \text{ A/mm}^2$; Resistivity: $\rho_{Cu} = 1.7 \times 10^{-8} \Omega m$;

$$I_{SRMS} = \sqrt{D \left[(I_{pk} \cdot I_{min}) + \frac{1}{3} (I_{pk} - I_{min})^2 \right]} = \sqrt{0.47 \left[(4.2 \cdot 1.5) + \frac{1}{3} \cdot 7.29 \right]} = 2.02A$$

$$I_{PRMS} = \sqrt{0.47 \left[(0.9 \cdot 0.3) + \frac{1}{3} \cdot 0.36 \right]} = 0.42A$$

Wires from the primary:

$$\text{Selectional area of the wire: } A_{Wp} = \frac{I_{PRMS}}{J_{Cu}} = \frac{0.42A}{3 \text{ A/mm}^2} = 0.14 \text{ mm}^2$$

$$\text{Diameter of the wire: } d_p = \sqrt{\frac{4 \cdot A_{Wp}}{\pi}} = 0.422 \text{ mm} \quad \text{or} \quad \cong 25 \text{ AWG}$$

$$\text{Length of the wire: } l_{Wp} = N_p \cdot \pi \cdot \sqrt{\frac{4 \cdot A_e}{\pi}} = 824 \text{ mm}$$

$$\text{Resistance of the wire: } R_{WpDC} = \rho_{Cu} \cdot \frac{l_{Wp}}{A_{Wp}} = 100 \text{ m}\Omega$$

EQUATION 27: WIRE DIMENSIONS CALCULATIONS

Wires from the secondary:

Selectional area of the wire:
$$A_{Ws} = \frac{I_{SRMS}}{J_{Cu}} = \frac{2.02A}{3 A/mm^2} = 0.67 mm^2$$

Diameter of the wire:
$$d_s = \sqrt{\frac{4 \cdot A_{Ws}}{\pi}} = 0.92 mm \quad or \quad \approx 20 AWG$$

We have to use 4 AWG24 in parallel with the diameter of a single wire $d_{parallel} = 0.511 mm$ and external equivalent diameter of $\sim 0.92 mm$

Length of the wire:
$$l_{Ws} = N_s \cdot \pi \cdot \sqrt{\frac{4 \cdot A_e}{\pi}} = 147 mm$$
 Resistance of the wire:
$$R_{WsDC} = \rho_{Cu} \cdot \frac{l_{Ws}}{A_{Wparallel}} = 8 m\Omega$$

R_{AC} is approximatively three times greater than R_{DC} : $R_{WpAC} = 300 m\Omega$; $R_{WsAC} = 24 m\Omega$

Power loss in wire:
$$P_{CuP} = I_{PRMS}^2 \cdot R_{WpAC} = 52 mW ; P_{CuS} = I_{SRMS}^2 \cdot R_{WsAC} = 96 mW$$

Power loss in magnetic core $PV = 375 kW/m^3$
$$P_{core} = P_V \cdot V_e = 0.45 W$$

Total losses in the transformer
$$P_{Traf} = P_{CuTOT} + P_{core} = 0.6 W$$

Using the Power 4-5-6 tool to characterize the transformer is simpler, as all the mathematical equations are embedded. It also holds records of manufacturer values of different core types and materials, so the designer can verify all the changes just with a click, omitting all the complex equations. If choosing different core materials and bobbin, the mathematical equations and the tool will provide other values for the turns and wire thickness as depicted in [Figure 21](#), but that does not mean the transformer is not good; for the same application multiple configurations of transformer can do the job, so experimenting is encouraged.

FIGURE 21: TURNS AND CORE WINDOW IN POWER 4-5-6

Flyback Transformer Design

FLYBACK TRANSFORMER CORE SELECTION

Approximate Core Area: 0.437 sq. cm

☐ Generic Core ☒ Use Selected Core

CORE TYPE AND AREA

Core Type: coilcraft EFD25 Primary Inductance: 466.52 μ H

Minimum Area: 0.55 sq. cm

MAXIMUM FLUX LEVEL SETTING

0.3 T This value impacts the number of turns needed
0.3 T rugged commercial supply with ferrite
0.25 T aerospace supply with ferrite

FLYBACK TRANSFORMER TURNS

Primary Turns: 56 43

Secondary Turns: 13 13.00208 Maximum Flux Density: 0.227 T

CORE PHYSICAL DETAILS

Core Volume	3.3	cu. cm
Window Width	1.4	1.64 cm
Window Build	0.4	0.245 cm
Inner Turn Length	3	4.64 cm
Outer Turn	4.5	6.17 cm

CORE GAPPING

0.46 mm 18.4 mils

Note that gap length is a rough guide only. Manufacturing design is specified by AI, and the core is gapped to achieve the correct value

AI value: 148.76 nH/n2

Once you select OK, values appearing on this form will be used in the converter simulation.

The tool also provides the ability to control the dimension of the winding window; margins and insulation can be added in order to be compliant with the standards imposed by the project. The tool allows the designer to choose the winding structure, among magnet wire, insulated wire or copper foil, if available. It will show the maximum wire size that will fit perfectly on the bobbin, based on the selected number of layers or number of parallel wires, and also makes the calculation in case the interleaved secondary and primary winding strategy is chosen. All of this can be done on paper, it is just more time consuming.

Again, these parameters are the starting point of the transformer design, as with the use of the equations, some personal experimentation and tests are needed in order to adapt the design to better work in the project. Later on, the designer may choose to contact a transformer designing company to improve the design.

Figure 22 shows the difference in size between two transformers that work approximately the same in this design; the one on the left is designed in Microchip's laboratory, and the one on the right was designed with the help from Coilcraft and matches the needs of this project. The transformer built by Coilcraft can be ordered with the following code: UA8233-AL.

FIGURE 22: TWO FLYBACK TRANSFORMERS THAT WORK SIMILARLY: LEFT- BUILT IN MICROCHIP'S LAB; RIGHT- BUILT BY COILCRAFT

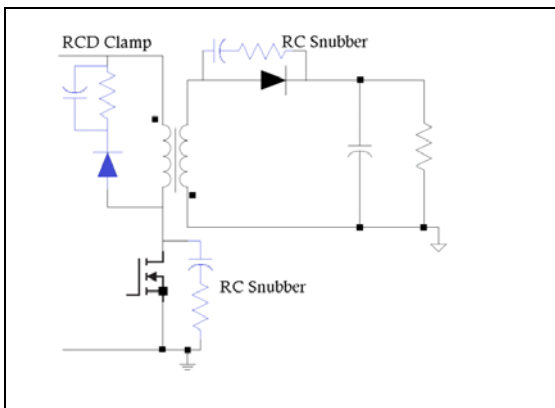


SNUBBER DESIGN

Switching mode power supplies have non-ideal parasitics, which must be suppressed, this being the main cause for ringing waveforms. Semiconductors can fail if not used properly and noise levels might be higher than required. Some design techniques for the most commonly used snubber and clamp circuits for the flyback converter will be discussed.

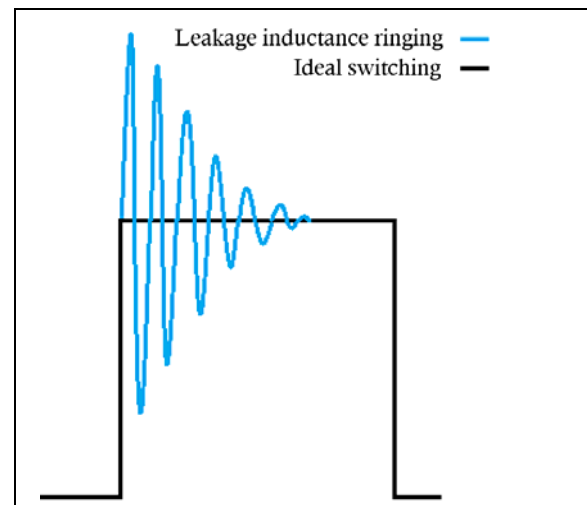
Figure 23 shows the basic flyback circuit with RCD Clamp and Snubbers in place, marked in blue. Ideally, without snubbers and clamps, the circuit has square-wave characteristics when turning on and off. In practice, the turn-off of the power switch stops the current flow through the leakage inductance and this causes voltage spikes on the drain of the MOSFET.

FIGURE 23: FLYBACK CONVERTER WITH RCD CLAMP AND SNUBBERS



The inductance will then ring with stray capacitances in the circuit, producing high-frequency waveforms of large amplitude, as shown in Figure 24.

FIGURE 24: FLYBACK CONVERTER DRAIN VOLTAGE WITH NO SNUBBER



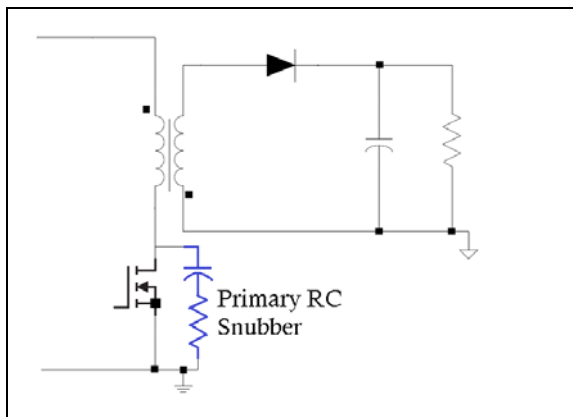
On the flyback primary, the leakage inductance will ring with primary capacitances. The problem here is the excessive voltage on the drain of the MOSFET, which can cause avalanche breakdown and failure of the device. Another problem is the ringing energy which will be radiated and conducted in the power supply, load, and creates noise issues and logic errors. This ringing will cause a peak in the EMI spectrum, in both radiated and conducted measurements. Thus, in such designs it is necessary to add a clamp, a snubber or both.

Primary RC Snubber

Figure 25 shows an RC snubber circuit, used to damp the ringing on the drain of the MOSFET. The resistor is used to damp the LC resonance of the power circuit. A capacitor is added in series to the resistance with the role of protecting the resistor from high voltages. The capacitor value is calculated to maximize the effectiveness of the resistor at the switching frequency.

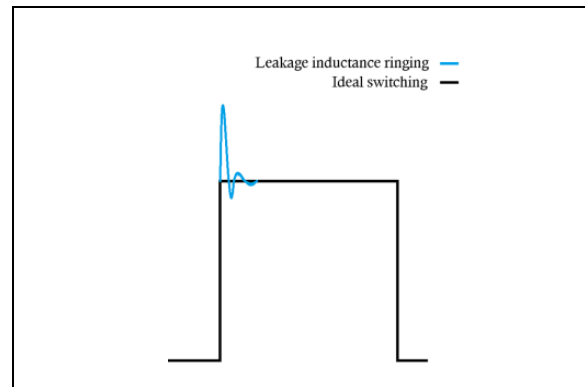
The main function of this type of RC snubber is to protect the switcher and must be placed as close as possible across the device. If the designer uses a sense resistor for peak current-mode control, to avoid the detection of the current spike from the discharging capacitor at the turn-on, the snubber must be placed from the drain of the MOSFET to the top of the sense resistor. The designer has to choose a resistor that will damp ringing, then choose a capacitor and ensure that the dissipation is not excessive.

FIGURE 25: FLYBACK CONVERTER WITH PRIMARY RC SNUBBER



Knowing the leakage inductance, the designer must measure the ringing frequency, as displayed in Figure 24. From the waveform, the designer must estimate the ringing frequency (f_r), which should be two orders of magnitude higher than the switching frequency, so that dissipation does not become excessive. If the ringing frequency is not as high as the switching frequency, the leakage inductance of the transformer is too big and must be reduced, or if possible, try to reduce the circuit capacitance.

FIGURE 26: DRAIN WAVEFORM WITH PRIMARY RC SNUBBER



Once the ringing frequency and the leakage inductance are determined, the designer has to use Equation 28 and Equation 29 to calculate the capacitance and resistance of the snubber.

EQUATION 28: SNUBBER RESISTANCE

$$R = 2\pi f_r L$$

EQUATION 29: SNUBBER CAPACITANCE

$$C = \frac{1}{2\pi f_r R}$$

The dissipation of the snubber can be calculated knowing the capacitor and using Equation 30, where V is the voltage on the input plus the reflected output voltage.

EQUATION 30: SNUBBER POWER DISSIPATION

$$P_{snubber} = CV^2 f_s$$

The practical results should now be verified, and should be close to what is depicted in Figure 26. The ringing is very well-damped and the peak of the waveform is reduced, reducing significantly the EMI noises.

Primary RCD Clamp

Figure 28 shows a RCD clamp circuit, used to limit the peak voltage on the drain of the MOSFET when an RC snubber is insufficient to prevent switch overvoltage. Once the drain voltage exceeds the clamp capacitor voltage, the current is absorbed from the leakage inductance. The MOSFET is thus protected from the voltage peaks and a larger capacitor will keep the voltage constant over a switching cycle. The resistor always dissipates power, even with very little load. The capacitor will always be charged to the voltage reflected (v_f) from the secondary. With full load, there is more energy into the capacitor, and the voltage is higher (by a certain amount v_x), above the ideal square wave, these voltages being depicted in Figure 28.

FIGURE 27: FLYBACK CONVERTER WITH PRIMARY RCD CLAMP

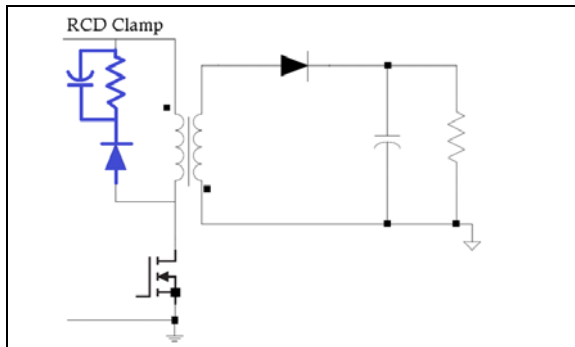
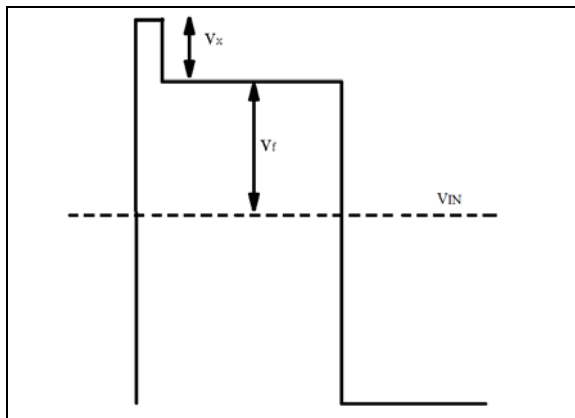


FIGURE 28: VOLTAGES AFFECTING THE MOSFET



When designing a RCD clamp, the designer has to measure the leakage inductance, but in this case, the quantity of energy stored is more important than the incremental value at the ringing. So, it is better to use the value measured at the switching frequency. After determining how much voltage can be tolerated by the switcher, calculate the amount of power that will be dissipated in the clamp. The energy stored in the leakage inductance ($L_{leakage}$) with a current I_p at turn-off can be calculated using Equation 31.

EQUATION 31: LEAKAGE POWER

$$P_l = \frac{1}{2} L_{leakage} I_p^2 f_s$$

All the leakage energy is assumed to be conducted into the snubber capacitor from the leakage inductance and the capacitor to be large enough that its value does not change significantly during one switching cycle, so the higher the clamp voltage rise on the switch, the lower the overall dissipation becomes. The power dissipated by the RCD clamp is calculated using Equation 32.

EQUATION 32: SNUBBER POWER DISSIPATION

$$P_{snubber}^{max} = P_l \left(1 + \frac{V_f}{V_x^{max}} \right)$$

This must be balanced against the total voltage seen across the switcher.

A typical design is for the voltage V_x to be equal to $\frac{1}{2}$ the flyback voltage. This is just an estimate because it does not account for lossy discharge of the inductor and stray capacitance, so the design will have less loss in the clamp than anticipated, due to these effects. For high-voltage offline designs which are constrained to use a MOSFET with a maximum voltage of 600V or 650V, the voltage V_x will have a hard limit set by the maximum input line, a maximum current, and a switcher breakdown voltage. V_{DS} must not be exceeded and the designer must take into consideration that breakdown degrades with temperature.

The capacitor is large enough to keep a constant voltage while absorbing the leakage energy, but the value is not critical for the peak voltage. The important component for determining V_x is the resistance. If the value is too large, the discharge will be too slow, and increasing the voltage, in contrast with a too small value, will lower the clamp voltage by higher dissipation. Use Equation 33 to calculate the resistance. The diode must be selected to be as fast as possible with the correct voltage rating.

EQUATION 33: RDC CLAMP RESISTANCE CALCULATION

$$R = \frac{2 v_x T_s (v_f + v_x^{max})}{L_p^2}$$

Figure 29 depicts how a switching voltage will look with a RCD clamp in the primary. After the clamping is done, there is still a ringing effect. The RDC clamp solves the peak voltage problem, though it does not solve the EMI problem, in which case the primary RC snubber helps, as seen in Figure 30. This solution solves the voltage stress and EMI problem, with higher dissipation.

FIGURE 29: DRAIN VOLTAGE WITH PRIMARY RCD CLAMP

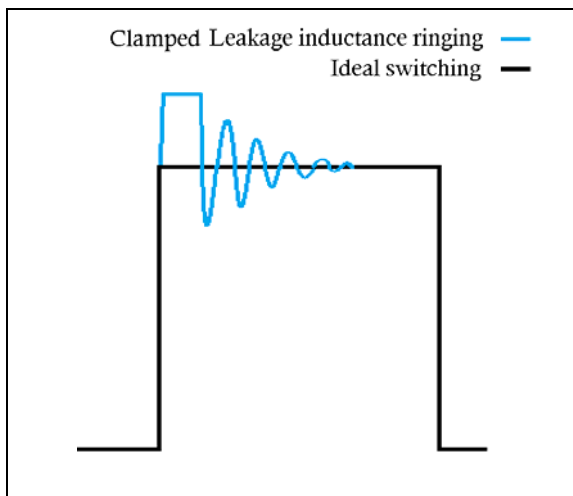
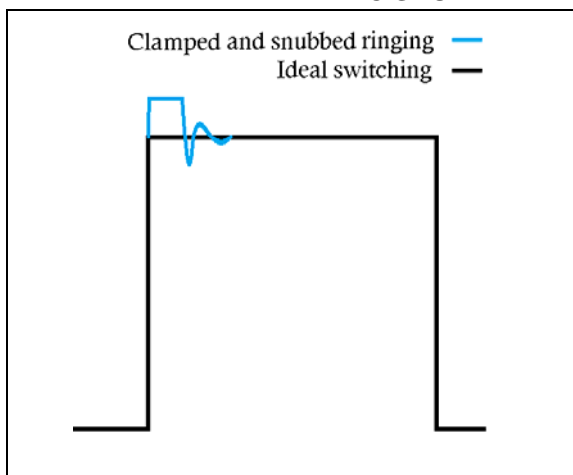
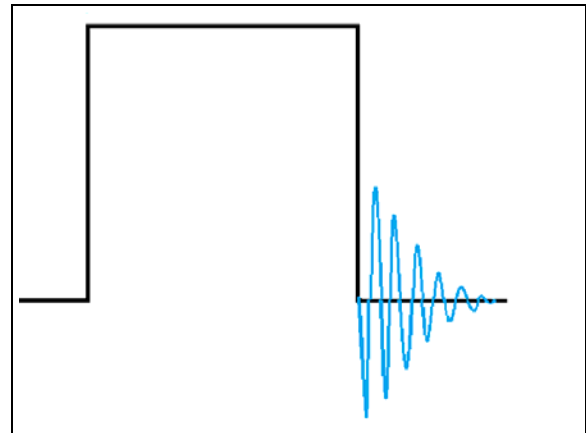


FIGURE 30: DRAIN VOLTAGE WITH PRIMARY RCD CLAMP AND PRIMARY RC SNUBBER



The last problem to be solved is the secondary ringing caused by the output diode turn-off. Figure 31 depicts this ringing. These excessive peaks can be more dangerous than the ones on the primary and they must be suppressed with a RC snubber.

FIGURE 31: SECONDARY DIODE WAVEFORM WITHOUT SNUBBER



The secondary snubber is best placed directly across the diode, as seen in Figure 32. The design procedure for the secondary snubber is almost identical to the primary snubber but the leakage inductance is the measured one from the primary, divided by the squared turn ratio. The secondary ringing will more likely have a higher frequency and so will be easier to deal with.

FIGURE 32: SECONDARY RC SNUBBER

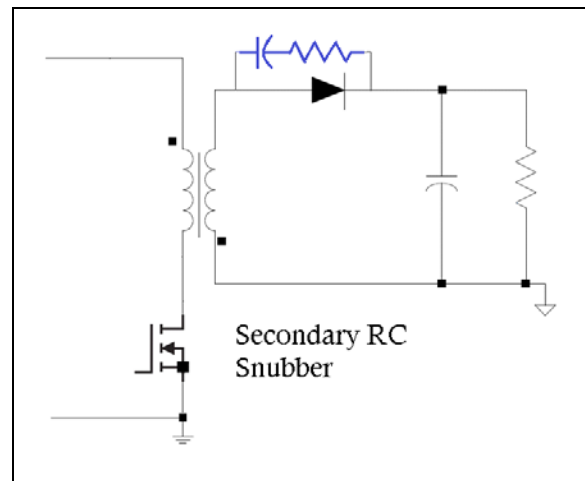


Figure 33 shows what the result of adding a secondary RC snubber looks like. The designer must also take into consideration the auxiliary outputs of the converter. Figure 34 shows the suggestions given by POWER 4-5-6.

FIGURE 33: SECONDARY DIODE WAVEFORM WITH SNUBBER

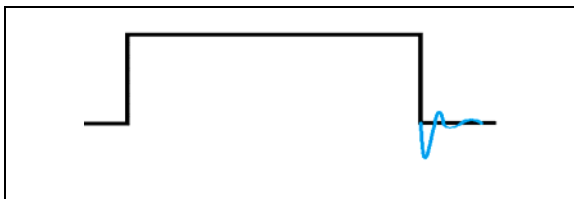
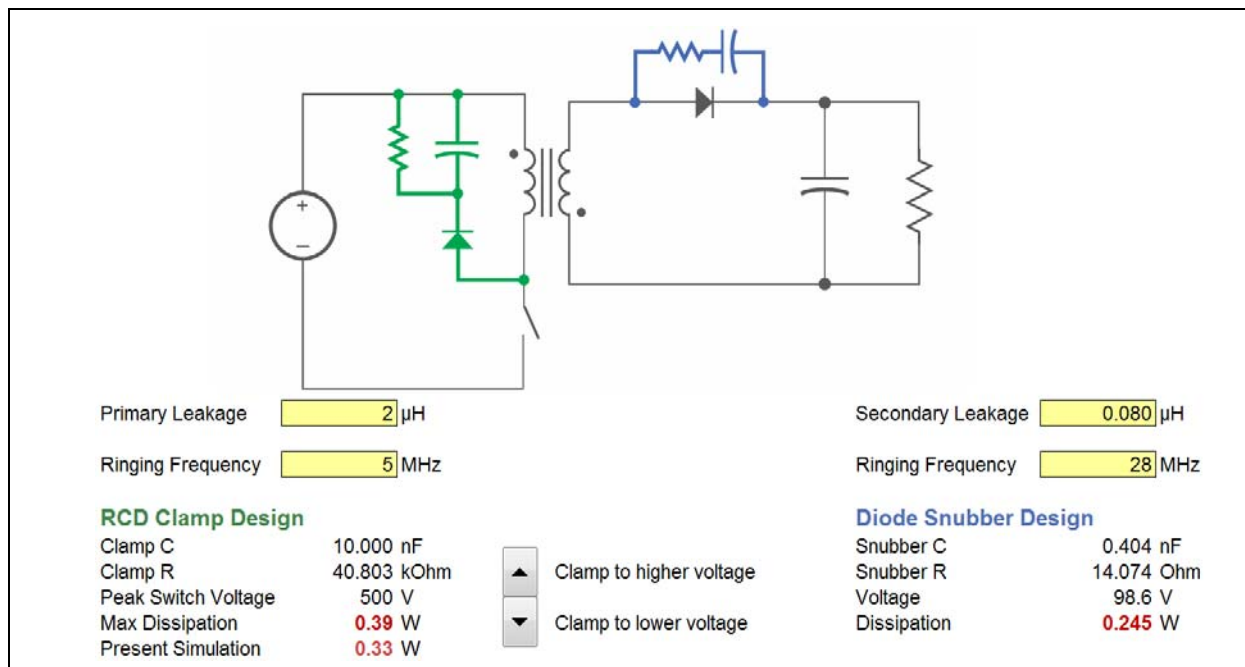


FIGURE 34: SNUBBER DESIGN WINDOW IN POWER4-5-6



FEEDBACK AND COMPENSATION CIRCUIT

This chapter will look at the problems that can appear from not compensating the feedback control loop, the type of compensation, how to calculate the values and how to use the optocoupler when isolation is needed.

When designing the SMPS, there are other instability sources besides the compensation loop that can appear, but may be prevented in the design phase. One such instability source is the control chip component placement or layout, where the clock signal is the most sensitive area and the capacitors have to be placed as close to the pins as possible.

Another instability source is the amplifier noise pickup through active devices, and even the operational amplifier and optocoupler, which can cause pulse skipping and sub-harmonic oscillations. This can be fixed with a small RC filter with the time constant of half the switching frequency placed at the output of the error amplifier.

The current waveform can cause premature turn-off because of the turn-on spike. This can be fixed either by using a filter and/or by using the leading-edge blanking function of the control device.

Operation close to the maximum duty cycle can also cause instability by prematurely ending the clock timing signal. Operation close to the minimum duty cycle or in light-load high input can also create instability problems by experiencing pulse skipping. The current loop should also be considered; when the duty cycle approaches 50%, the SMPS can experience sub-harmonic oscillation. This source of instability can be fixed by adding a comparator ramp.

As for the voltage loop instability, there are three types of compensating circuits used: Type I, Type II and Type III, with Type II having a Type 2a and 2b variation. For more detailed information, see [3] in the [Section "References"](#).

A loop analysis may be conducted to decide upon the type of compensation circuit to be used. The loop analysis consists in studying the open-loop/phase response of the SMPS, through a BODE plot, and shaping it via the compensation network to stabilize the power supply over the various input/output conditions the converter may encounter.

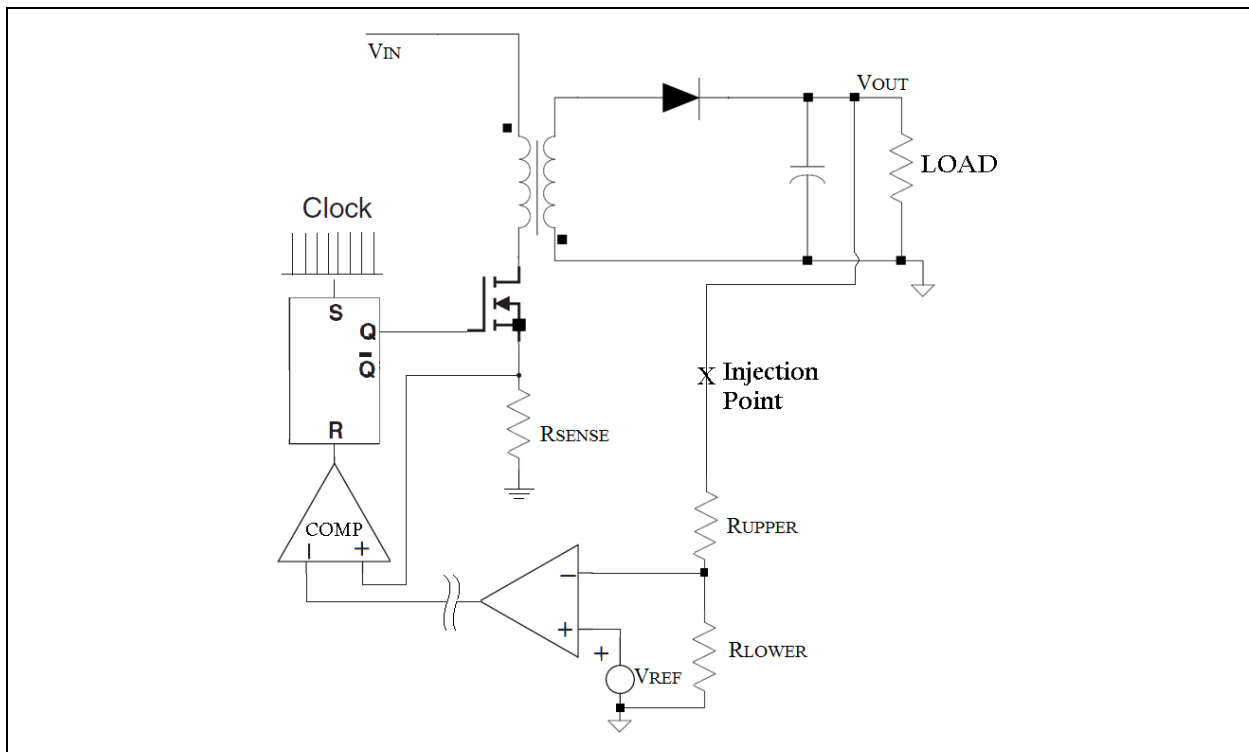
Observation Points

The simplest method to reveal the transfer function of a converter is by breaking the loop and injecting an input signal to observe what is obtained on the other side of the opened path. This is performed through the Frequency Response Network Analyzer. The disturbance signal will be distributed around the loop, and depending on the loop gain, the signal will be amplified or attenuated and shifted in phase. The

output will provide the disturbance signal, whereas the inputs will measure the transfer function of the loop. To ensure that the measured loop gain equals the real loop gain, there must be a point where the loop is restricted to a single path and where the impedance looking in the direction of the loop is much higher than the impedance looking backwards.

Figure 35 shows the feedback loop of the circuit and indicates the suitable injection point. The injection point is across a 10-22 ohm resistor in series with the feedback and sensing present on both sides to get a measurement of the signal value difference. The impedance, looking backwards, equals the output impedance of the converter which is very low, and the impedance looking in the direction of the loop is formed by the compensator and the voltage divider and it is in the range of several kilo-ohms.

FIGURE 35: INJECTION POINT IN THE FEEDBACK LOOP



The converter has a negative feedback loop when the divided output voltage is higher than the reference voltage. The error voltage will become smaller and this will make the pulse width smaller, thus reducing the output voltage and vice versa when the output is lower. As frequency increases, the converter output stage introduces further delay and its gain drops. Combined with the correction loop, a case might quickly appear where the total phase difference between the control signal and the output signal vanishes to 0 degrees. Theory shows that if, for any reason, both output and error signals arrive in phase while the gain loop reaches unity (or 0 dB in a log scale), a *positive feedback* oscillator has just been built, delivering a sinusoidal signal at a frequency fixed by the 0 dB crossover point.

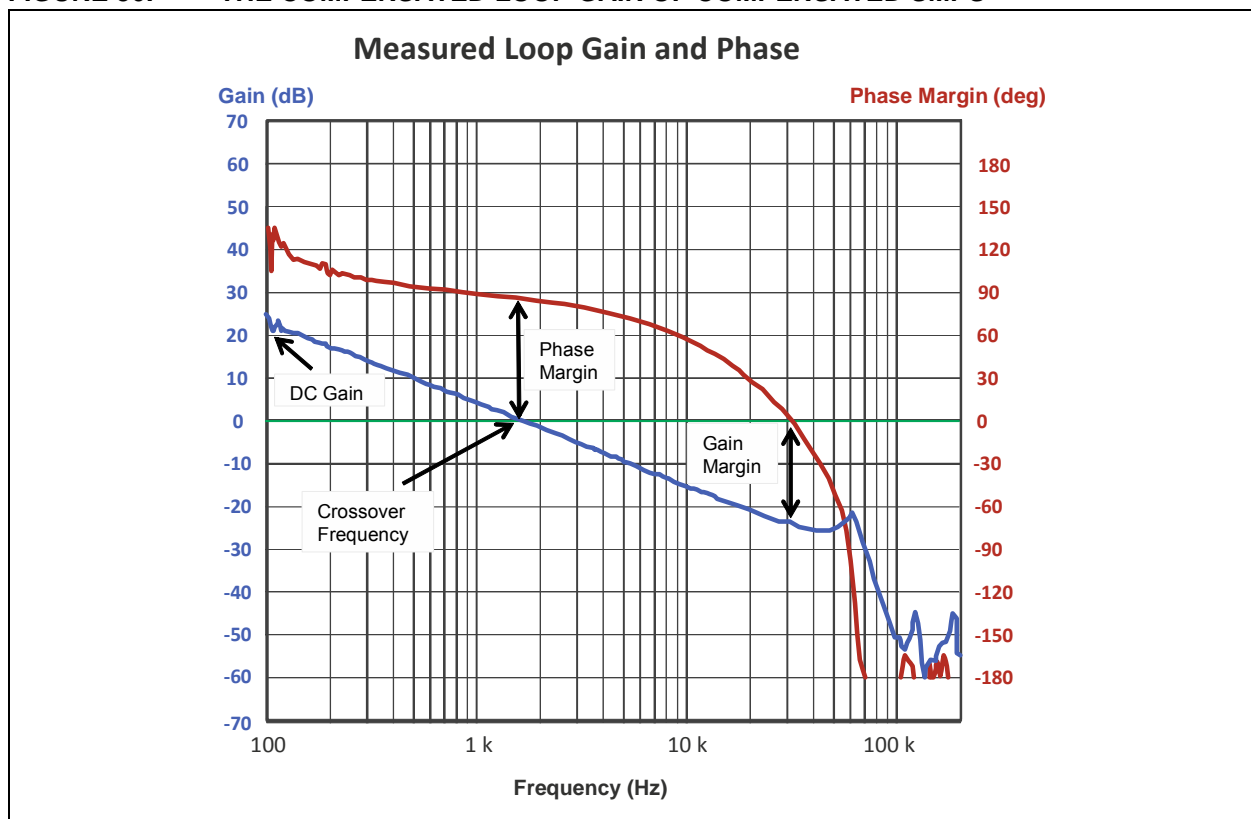
When a power supply is compensated, the idea is not to build an oscillator; the design work will consist of shaping the correction circuit to make sure that:

- When the loop gain crosses the 0 dB axis, there exists sufficient phase difference between the error and the output signal.
- The correction circuit offers a high-gain value in the DC portion to reduce the static error and the output impedance and to improve the input line rejection.

This phase difference is called the Phase Margin (PM) and generally must be over 45 degrees.

Figure 36 presents the loop gain of a compensated SMPS and highlights the DC gain, the phase margin, the gain margin and the crossover frequency. The gain increase necessary to reach the 0 dB axis can be noticed and called *Gain Margin* (GM). Good designs ensure at least 10-15 dB margins to cope with any gain variations, due to loading conditions, component dispersions, ambient temperature and so on.

FIGURE 36: THE COMPENSATED LOOP GAIN OF COMPENSATED SMPS



If the phase margin is too small, the peaking induces high-output ringing, exactly as in a RLC circuit. On the contrary, if the phase margin becomes too large, it slows down the system: the overshoot goes away to the detriment of response and of recovery speed. Solid designs aim to around 70 to 80 degrees phase margin, offering good stability and a fast non-ringing transient response.

A stable voltage loop requires shaping the compensation circuit in order to provide adequate phase margin at the selected crossover point, together with a high gain in DC. To do so, several compensation circuits can be used, assembling poles and zeros.

Type 1 Amplifier – Active Integrator

Implementing the largest DC gain naturally pushes the usage of an op amp as part of the corrective loop. Rather than cascading the passive networks followed by the high-gain op amp, designers often combine them to form active filters. This is the case for the pure integrator shown in [Figure 37](#). The ramp on the right of the image is on a gain vs. frequency plot axis.

The transfer function of this integral compensator is shown in [Equation 34](#), which features an origin pole, given by R_1 and C_1 , as shown in [Equation 35](#).

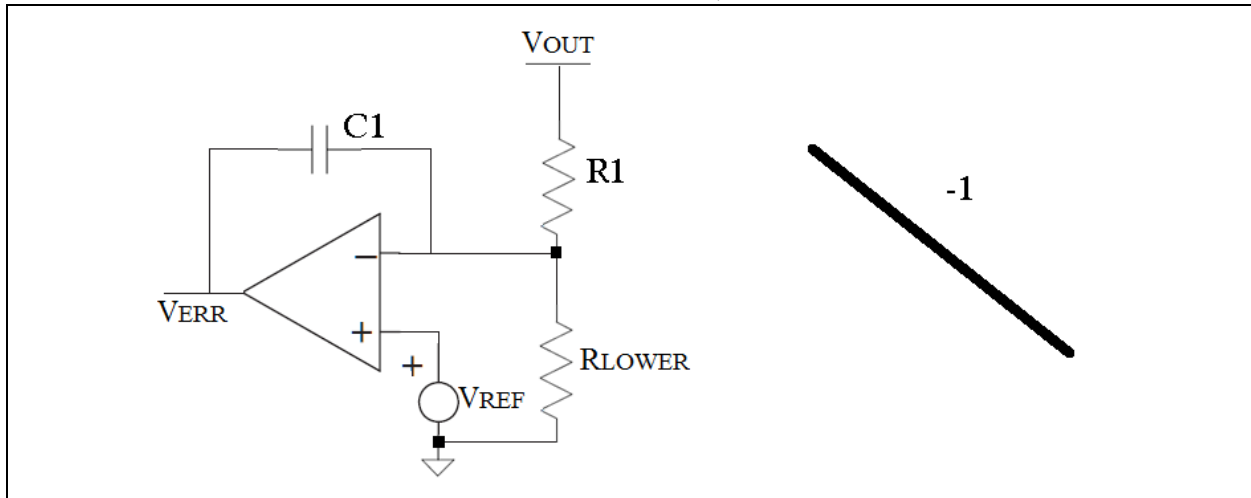
EQUATION 34: TRANSFER FUNCTION OF INTEGRAL COMPENSATOR

$$G(s) = \frac{1}{sR_1C_1}$$

EQUATION 35: ORIGIN POLE

$$\omega_{p1} = \frac{1}{R_1C_1}$$

FIGURE 37: TYPE 1 AMPLIFIER: NO PHASE BOOST, JUST DC GAIN



Type 2 – Zero – Pole Pair

The previous amplifier type did not provide any phase boost, which is needed if the phase margin is too low at the desired crossover frequency. [Figure 38](#) depicts such a compensator, referenced as a type-2 amplifier. It produces an integrator together with a zero-pole pair. Its transfer function is shown in [Equation 36](#).

EQUATION 36: TYPE 2 AMPLIFIER TRANSFER FUNCTION

$$G(s) = \frac{1 + sR_2C_1}{sR_1(C_1 + C_2) \left(1 + sR_2 \frac{C_1C_2}{C_1 + C_2} \right)}$$

A zero, an origin pole and a high-frequency pole are shown in [Equation 37](#), [Equation 38](#) and [Equation 39](#).

EQUATION 37: ZERO POLE

$$\omega_z = \frac{1}{R_2C_1}$$

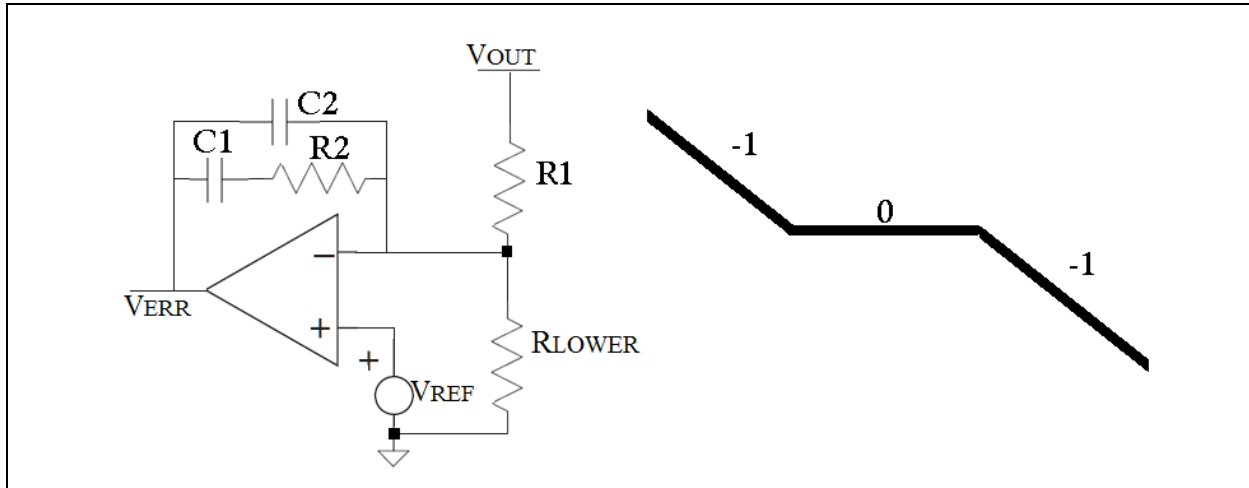
EQUATION 38: FIRST POLE

$$\omega_{p1} = \frac{1}{R_1(C_1 + C_2)}$$

EQUATION 39: SECOND POLE

$$\omega_{p2} = \frac{1}{R_2 \left(\frac{C_1C_2}{C_1 + C_2} \right)}$$

If: $C_2 \ll C_1 \Rightarrow \omega_{p2} = \frac{1}{R_2C_2}$

FIGURE 38: TYPE 2 AMPLIFIER CAN BOOST THE PHASE**TYPE 2a – ORIGIN POLE PLUS A ZERO**

By suppressing a capacitor C2, the high-frequency pole can get dismissed and the frequency response of the compensation network be changed. [Figure 39](#) shows how the type-2 amplifier changed.

The transfer function changes as depicted in [Equation 40](#). [Equation 41](#) and [Equation 42](#) calculate the zero and the origin pole.

EQUATION 40: TRANSFER FUNCTION

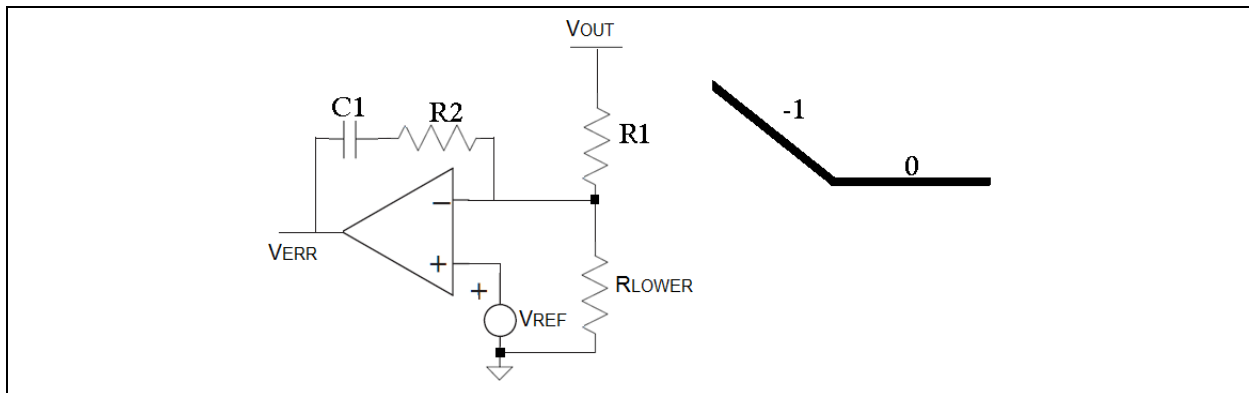
$$G(s) = \frac{I + R_2 C_I}{s R_I C_I}$$

EQUATION 41: ZERO POLE

$$\omega_z = \frac{I}{R_2 C_I}$$

EQUATION 42: ORIGIN POLE

$$\omega_{pI} = \frac{I}{R_I C_I}$$

FIGURE 39: TYPE 2a COMPENSATOR**TYPE 2b – PROPORTIONAL PLUS A POLE**

Another variation of the type-2 amplifier consists of adding a resistor to make a proportional amplifier and removing the integral term present with the two previous configurations. [Figure 40](#) displays such an arrangement where a capacitor C1 placed in parallel with the resistor R1 introduces a high-frequency gain, necessary to roll off the gain. This type of amplifier offers a flat gain imposed by R2 and R1, until the pole imposed by C1 starts to act.

The transfer function is given by [Equation 43](#) and the pole by [Equation 44](#).

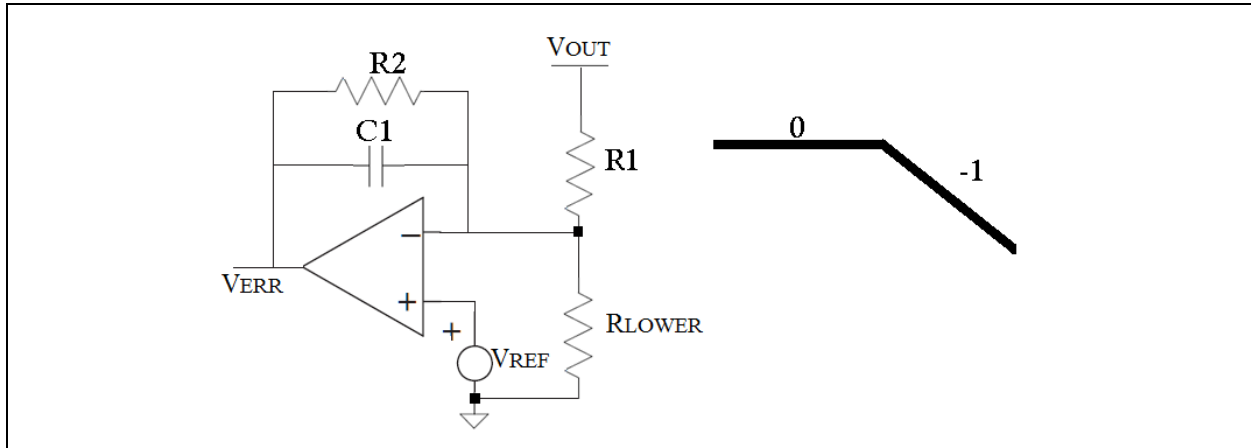
EQUATION 43: TRANSFER FUNCTION

$$G(s) = \frac{R_2}{R_1} \frac{I}{I + sR_2C_1}$$

EQUATION 44: POLE

$$\omega_{p1} = \frac{1}{R_2C_1}$$

FIGURE 40: TYPE 2b AMPLIFIER WHERE PROPORTIONAL CONTROL IS NEEDED



Type 3 – Origin Pole Plus Two Coincident Zero-Pole Pairs

The type-3 amplifier is used where a large phase boost is necessary, for instance, for the operation of converters which feature a second-order response, or in CCM Voltage mode, as depicted in [Figure 41](#). Its transfer function is given by [Equation 45](#).

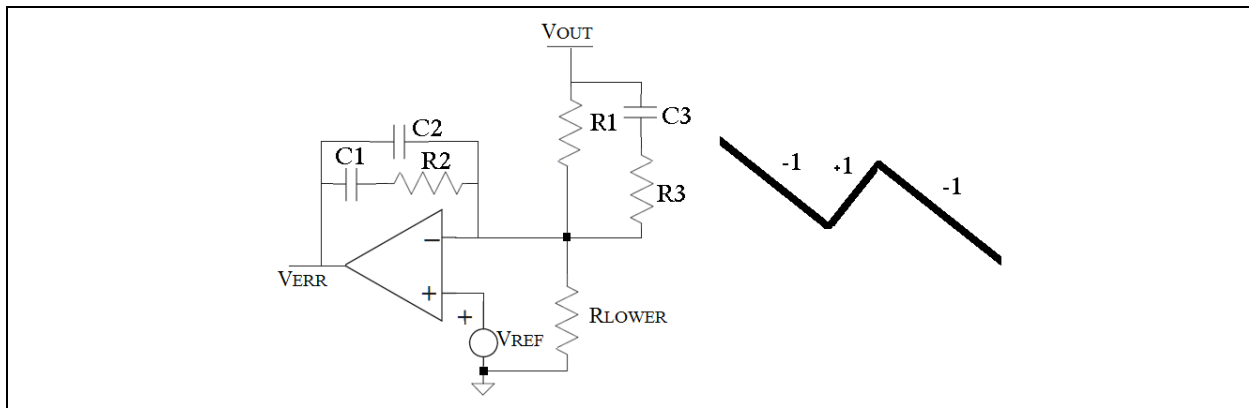
EQUATION 45: POLES AND ZEROES FOR TYPE 3 COMPENSATOR

$$G(s) = \frac{I + sR_2C_1}{sR_1(C_1 + C_2) \left(I + sR_2 \frac{C_1C_2}{C_1 + C_2} \right)} \cdot \frac{sC_3(R_1 + R_3) + I}{sC_3R_3 + I}$$

If $C_2 \ll C_1$ and $R_3 \ll R_1$ are selected, the following poles and zeros result, as it follows:

$$\omega_{z1} = \frac{1}{R_2C_1} \quad \omega_{z2} = \frac{1}{R_1C_3} \quad \omega_{p1} = \frac{1}{R_1C_1} \quad \omega_{p2} = \frac{1}{R_3C_3} \quad \omega_{p3} = \frac{1}{R_2C_2}$$

FIGURE 41: TYPE 3 COMPENSATION CIRCUIT, TWO COINCIDENT POLE – ZERO PAIRS AND AN INTEGRATOR



A small characterization of where the above amplifiers are used, according to the converter type and transient response are listed below.

Type 1

The type-1 amplifier can be used in converters where the power stage phase shift is small. As in any integral type compensation, it brings the largest overshoot in the presence of a sudden load change. This type is widely used in Power Factor Correction (PFC) applications via a transconductance amplifier.

Type 2

This amplifier is the most widely used and works fine for power stages lagging down to -90 degrees, where the boost brought by the output capacitor ESR must be canceled. This is the case for current-mode CCM and Voltage mode converters operating in DCM.

TYPE 2a

Same as the above application field, except the boost brought by the output capacitor ESR can be neglected.

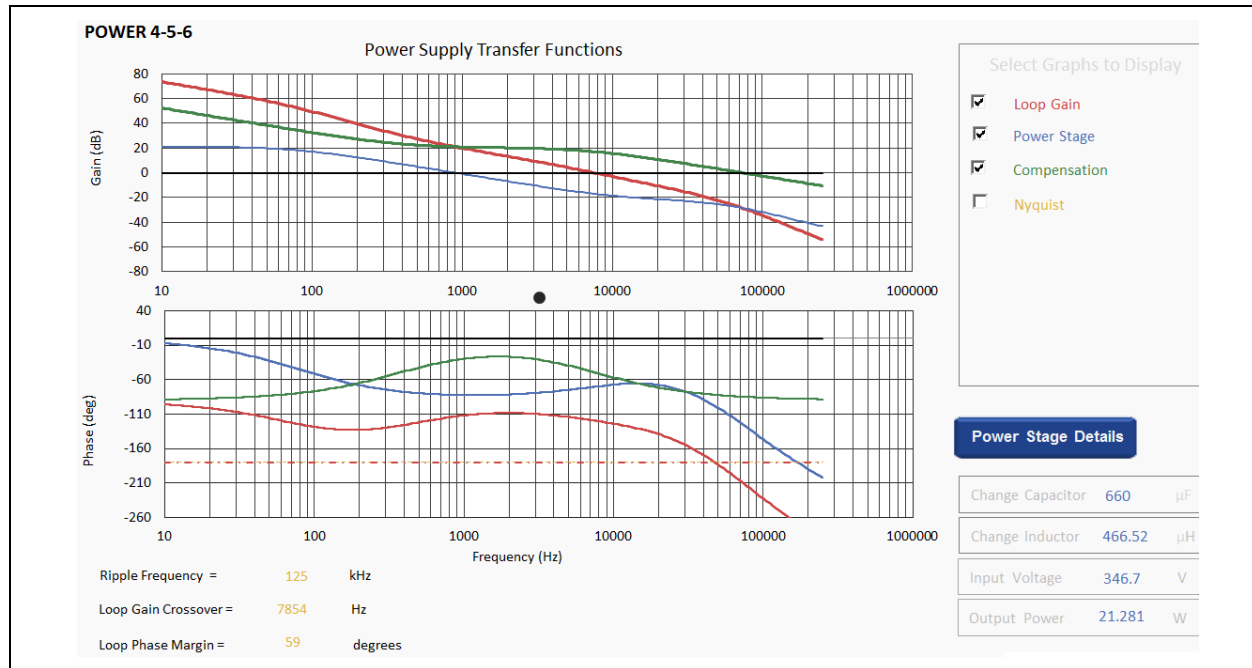
TYPE 2b

By adding the proportional term, it can help reduce the under or overshoots in severe design conditions. It prevents the output impedance from being too inductive, therefore offering superior transient response, for the cost of DC gain reduction, which gives a larger static error.

Type 3

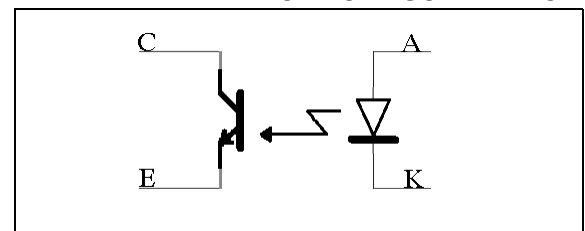
This configuration is used when the phase shift brought by the power stage can reach -180 degrees. This is the case for CCM Voltage mode buck or boost-derived types of converters.

Figure 42 depicts the transfer functions calculated in Power 4-5-6. It shows the Power Stage transfer function without compensation, the compensation transfer function and the loop gain transfer function with compensation.

FIGURE 42: POWER SUPPLY TRANSFER FUNCTIONS IN POWER 4-5-6

The optocoupler provides an optical link between a primary side and a secondary side, isolated from the primary. The link is made via the light emitted by a LED (photons), pointing to a base of bipolar transistor, that will collect the photons. This gives rise to a collector current whose intensity depends on the injected current in the LED and thus, on the luminous flux intensity it emits.

The amount of current flow in the collector links to the current flowing in the LED via the current transfer ratio (CTR), which depends on the LED current, the optocoupler age, and the junction temperature. The optocoupler is depicted in [Figure 43](#).

FIGURE 43: OPTOCOUPLER ELECTRICAL SCHEMATIC

The error signal can be obtained using the KA431 precision-programmable shunt reference integrated or separate.

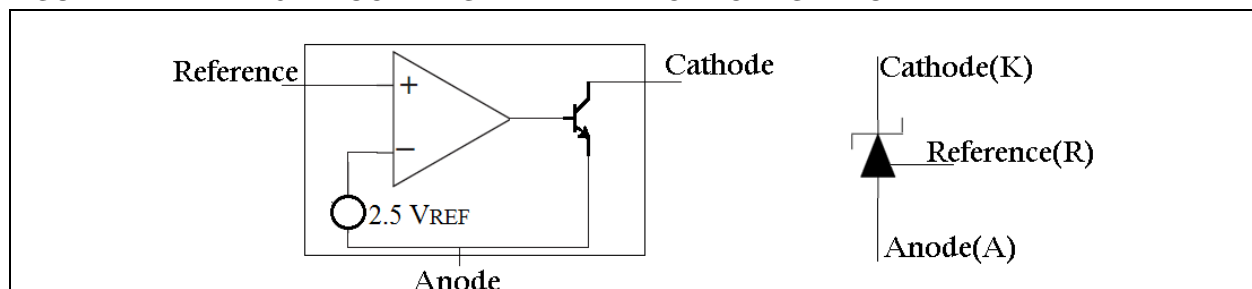
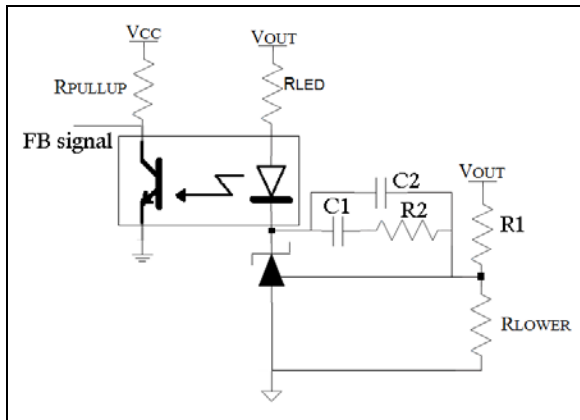
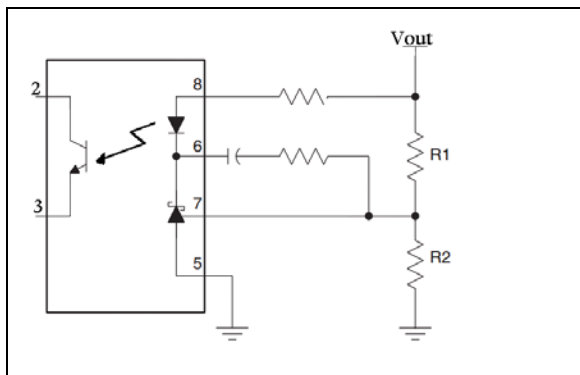
FIGURE 44: KA431 BLOCK DIAGRAM AND ELECTRICAL SYMBOL

FIGURE 45: A TYPE-2 ISOLATED COMPENSATION CIRCUIT USING THE KA431 AND THE OPTOCOUPLER



Optocouplers used in power supplies are designed for a very linear response from LED in to transistor out, so they are more expensive than regular optocouplers. For this design, an integrated circuit that consists of optocoupler, precision reference and error amplifier in a single package was chosen. It has a 2.5V reference, CTR from 100% to 200%, 5 kV RMS isolation, comes in tolerances from 0.5% to 2% and has the block diagram with typical connection depicted in Figure 46.

FIGURE 46: INTEGRATED OPTICALLY ISOLATED ERROR AMPLIFIER BLOCK AND TYPICAL CONNECTIONS



A type-2 compensator with opto-isolated IC was used in this case, with the following calculated values for the compensation components:

- $R_{PULLUP}(R_1) = 5.6 \text{ k}\Omega$
- $R_{LOWER} = 1.47 \text{ k}\Omega$
- $R_2 = 20 \text{ k}\Omega$
- $R_{LED} = 2.4 \text{ k}\Omega$
- $C_1 = 27 \text{ nF}$
- $R_{PULLUP} = 5.1 \text{ k}\Omega$

BOOTSTRAP DESIGN

In some power-supply applications, the Pulse-Width Modulator (PWM) controller is powered from an auxiliary winding, tapped off the power stage's transformer. This technique is used to reduce power loss. The only drawback is at start-up as the capacitor needs to be trickle charged from the rectified voltage, as shown in Figure 47. Another discrete technique to start-up the circuit is depicted in Figure 48. These techniques work well but they have the following disadvantages:

- Inefficiency – Draws current continuously from the high-voltage source
- Poor dynamic range – bias must be set for the minimum input voltage (at high-input voltage, the current drawn is higher)
- Poor regulation
- No current limit
- No overtemperature protection
- Requires large power resistor and Zener diode

FIGURE 47: ZENER IMPLEMENTATION BOOTSTRAPPING CIRCUIT

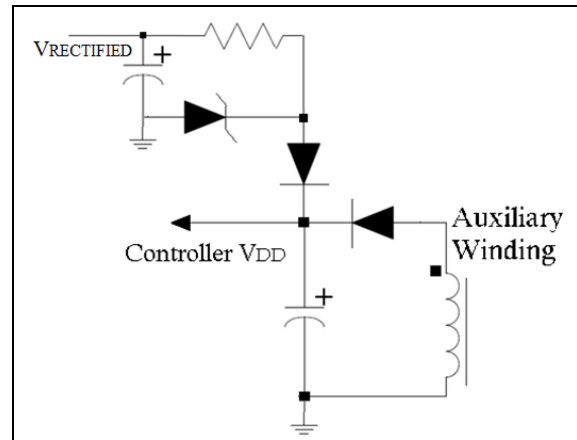
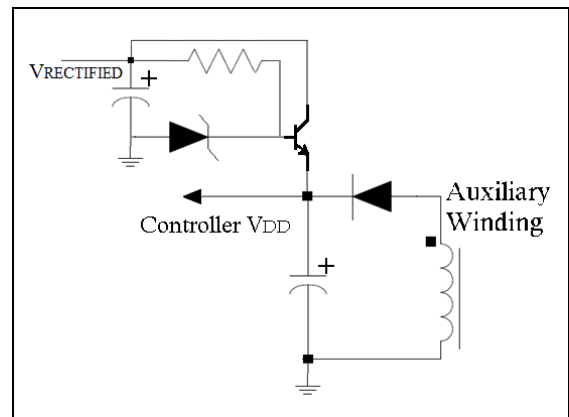


FIGURE 48: TRANSISTOR IMPLEMENTATION BOOTSTRAPPING CIRCUIT



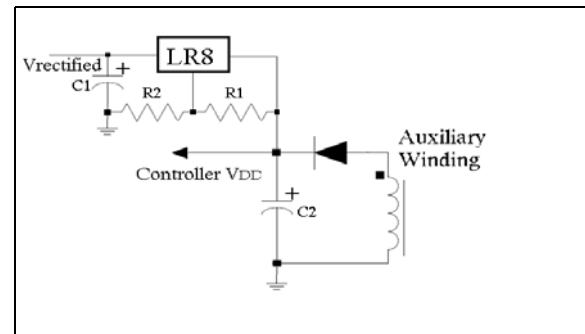
The schematic in [Figure 49](#) depicts a simplified offline switching power supply's auxiliary using the LR8 for start-up. This IC solves the problem of continuous current draw by entering in a Standby mode after the auxiliary voltage rises higher than the set output voltage. All current is then supplied from the bootstrap circuit rather than from the high-voltage source, increasing overall efficiency. The output voltage of the LR8 should be set high enough above the minimum operating voltage of the PWM controller; yet, low enough to ensure the bootstrap circuit takes over after start-up. If boot time is short, die temperatures will not reach the overtemperature protection trip point.

For more information on this device please visit [4] in [Section "References"](#).

The advantages of using this technique are the following:

- LR8 goes in to Standby mode after supply has bootstrapped, drawing no current from high-voltage input
- Good regulation
- Built-in current-limiting
- Overtemperature protection

FIGURE 49: START-UP IMPLEMENTATION USING THE LR8



[Table 2](#) shows the relevant specifications of the LR8.

TABLE 2: LR8 SPECIFICATIONS

Parameter	LR8
Input Voltage Range	(V _{OUT} + 12V) to 450V
Output Voltage Range	1.2V to (V _{IN} - 12V)
Power Dissipation Capabilities	TO-92: 0.6W
	TO-243AA: 1.3W
	TO-252: 2W
Output Current	0.5 to 10 mA
Output Voltage Accuracy	5%
Minimum C _{OUT}	1 uF

EQUATION 46: LR8 OUTPUT VOLTAGE

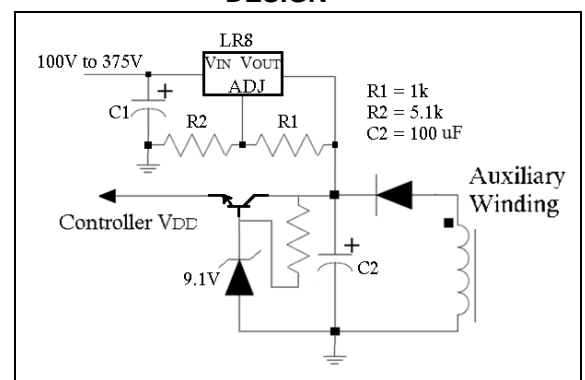
$$V_{OUT} = 1.2V \cdot \left(1 + \frac{R_2}{R_1}\right)$$

The output voltage of the LR8 can be calculated as shown in [Equation 46](#). [Figure 50](#) depicts the selected bootstrap design for the project. R₁ of 1 kΩ and R₂ of 5.1 kΩ are selected, thus [Equation 47](#) results from [Equation 46](#):

EQUATION 47: CALCULATED OUTPUT VOLTAGE

$$V_{OUT} = 1.2V \cdot \left(1 + \frac{5.1}{1}\right) = 7.3V$$

FIGURE 50: OFFLINE BOOTSTRAP DESIGN



Most PWM controllers have an undervoltage lockout (UVL) circuit or programmable start-stop voltages so that when the supplied voltage reaches the turn-on threshold, the device will start consuming current. Thus, if the consumed current is greater than the current delivered by the LR8, the output voltage will fall. If a large enough capacitor (C_2) is added, the auxiliary will start to supply current before the reach of the turn-off voltage.

INPUT FILTER DESIGN

Switch mode power supply energy conversion process produces powerful EMI in broad radio frequency range, which is considered a serious and increasing form of environmental pollution. This problem can be controlled by adopting the practices of electromagnetic compatibility (EMC), which have two complementary aspects:

- Describe the ability of electrical and electronic systems to operate without interfering with other systems
- Describe the ability to operate as intended within a specified electromagnetic environment (see [5] in [Section "References"](#)).

Interference can propagate and affect other devices connected to the same AC line distribution networks. The conducted EMI noise consists of two modes:

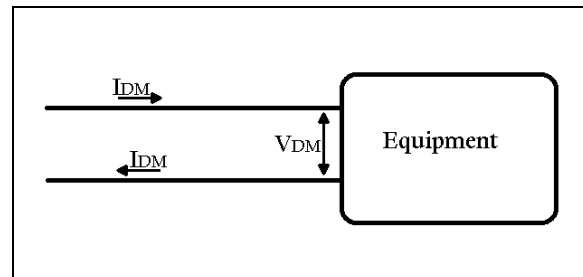
- Common-Mode (CM) interference – the EMI noise present on the line and neutrally referenced to the safety ground
- Differential-Mode (DM) interference – the EMI noise present on the phase line referenced to the neutral line.

Switched mode power supplies are the strong noise generators because of the high dV/dt and di/dt switching slopes generated by the power switches. So, the source of differential-mode interference is the current switched by a MOSFET or a diode, while the high rates of dv/dt and parasitic capacitors to the ground are the sources of common-mode interference.

Differential-Mode Noise (DM)

This is measured between each power line and neutral line and is present in a SMPS because of the magnetic coupling. [Figure 51](#) depicts the current path of DM which attempts to dissipate its energy along any path from line to neutral.

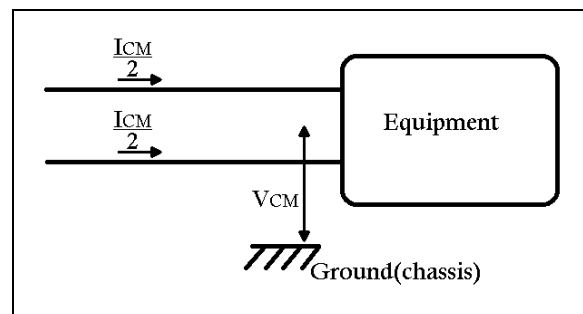
FIGURE 51: DIFFERENTIAL-MODE CURRENT PATH



Common-Mode Noise (CM)

Common-Mode (CM) Noise is measured between line and ground; the major contributor to common-mode emission in the SMPS is the primary side parasitic capacitance to ground, comprised from a switching transistor to heat sink capacitance, a transformer inter-winding capacitance, and a stray primary side wiring capacitance. Stray capacitor paths may exist within SMPS because they are smaller in size and more densely packaged as compared to other types of power supplies. Common-mode noise is present on both input and output lines; its current path is shown in [Figure 52](#).

FIGURE 52: COMMON-MODE CURRENT PATH



The transmission of CM noise is entirely through parasitic or stray capacitors, stray electric and magnetic fields, which exist between various system components and between components and ground. A typical EMI filter topology to suppress common-mode (CM) and differential-mode (DM) noises in switching mode power supplies is shown in [Figure 53](#). LCM is a common-mode choke and LDM is a differential-mode choke, C_{X1} and C_{X2} are DM capacitors (called "X" capacitors) and C_Y is a CM capacitor (called "Y" capacitor).

FIGURE 53: A TYPICAL Π EMI FILTER CONFIGURATION

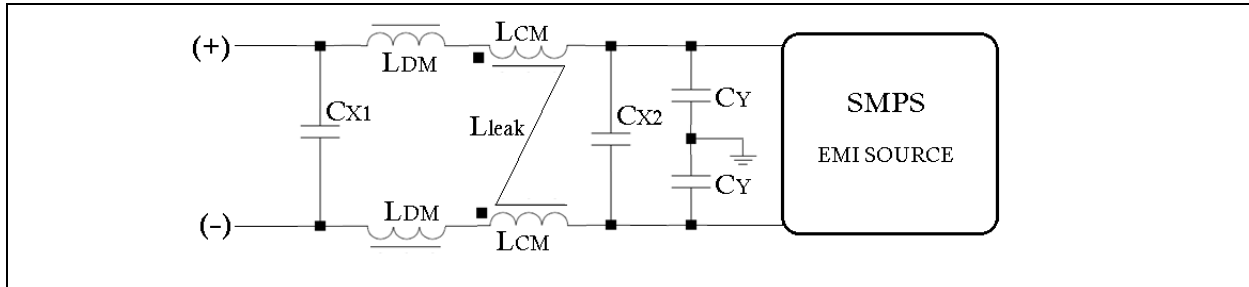


FIGURE 54: EQUIVALENT CIRCUIT FOR CM COMPONENTS

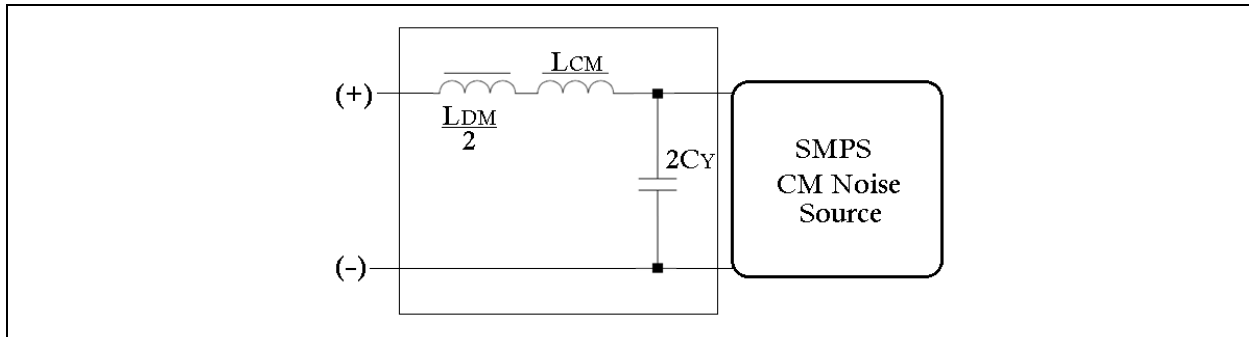
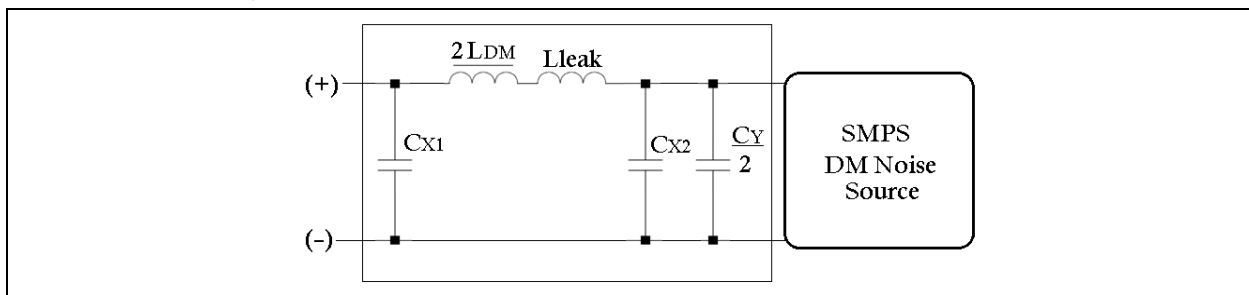


FIGURE 55: EQUIVALENT CIRCUIT FOR DM COMPONENTS



Because of the ground leakage current-limits set by the safety regulations in different countries, the Y capacitor cannot surpass a maximum value. A limit of maximum 3.2 nF ($C_Y < 3.2 \text{ nF}$) will satisfy all the regulations around the world. The common-mode inductor is designed to have a high-enough leakage inductance, in order to use it as a differential-mode inductance.

The first step is to accurately measure the common-mode and differential-mode noise spectrum of the SMPS (without the EMI Filter). This can be achieved by connecting a Line Impedance Stabilization Network (LISN) between the line and the input of the SMPS, and by measuring the noise with a spectrum analyzer. The required attenuation is calculated using [Equation 48](#) and [Equation 49](#).

EQUATION 48: COMMON-MODE ATTENUATION

$$(V_{req, CM}) \text{ dB} = (V_{CM, measured}) \text{ dB} - (V_{limit}) \text{ dB} + 6 \text{ dB}$$

EQUATION 49: DIFFERENTIAL-MODE ATTENUATION

$$(V_{req, DM}) \text{ dB} = (V_{DM, measured}) \text{ dB} - (V_{limit}) \text{ dB} + 6 \text{ dB}$$

Here (V_{CM,measured}) dB and (V_{DM,measured}) dB are the baseline noise voltage measured with the spectrum analyzer and (V_{limit}) dB is the required EMI limit (60 uV dB average in class B standard) and the last “+6dB” is intended to be a correction factor in order to avoid errors.

The third step is to determine the minimum corner frequency of second order L-C filter for CM and DM according to the attenuation requirement. [Figure 54](#) and [Figure 55](#) depict the EMI equivalent circuits for CM and DM noise. The CM noise is affected only by the parallel effects of both Y capacitors and the two CM inductors; the DM noise can be attenuated by both the inductance L_{DM} and the leakage inductance of the CM choke; the two Y capacitors also affect the DM noise but their DM noise attenuation is small in comparison with that of the two X capacitors with large capacitance. As previously mentioned, the DM inductance can be replaced by the leakage inductance of the CM choke, thus cost and size are reduced. In order to adopt a simple model for designing a conducted EMI filter that can ignore the effect of noise source impedance, the choice of the component value in the EMI filter must satisfy the following conditions: the CM filter equivalent $1/(2\omega C_Y) \ll Z_{PC}$, $\omega(L_{CM} + L_{DM}/2) \gg 25\Omega$ and the DM filter equivalent $C_{X1} = C_{X2} = C_X$:

a) if the rectifier diodes are OFF: $100\Omega \gg (1/\omega C_X) \gg Z_{SD}$ and

b) if the rectifier diodes are ON: $\omega L_{DM} \gg 100\Omega$, $Z_{pd} \gg (1/\omega C_X) \gg 100\Omega$.

Here, ω is the angular frequency of the CM or DM noise, Z_{PC} is the high-impedance of the CM noise source, Z_{PD} is the high-impedance of the DM noise source when the diodes are ON and Z_{SD} the low-impedance when the diodes are OFF.

For high-frequency conducted noise with frequency $f \gg f_c$, where:

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

the required attenuation of CM and DM can be expressed by [Equation 50](#) and [Equation 51](#).

EQUATION 50: COMMON-MODE ATTENUATION

$$(V_{req, CM}) \text{ dB} = 40 \log_{10}(f/f_{R, CM})$$

EQUATION 51: DIFFERENTIAL-MODE ATTENUATION

$$(V_{req, DM}) \text{ dB} = 40 \log_{10}(f/f_{R, DM})$$

The two corner frequency $f_{R, CM}$ and $f_{R, DM}$ correspond to the minimum intersection of the 40 dB/decade slope along the frequency axis.

The last part consists in finding the component values from the corner frequencies using [Equation 52](#) and [Equation 53](#).

EQUATION 52: COMMON-MODE CORNER FREQUENCY

$$f_{R, CM} = \frac{1}{2\pi\sqrt{(L_{CM} + 0.5L_{DM}) \cdot 2C_Y}} = \frac{1}{2\pi\sqrt{L_{CM} \cdot 2C_Y}} \text{ if } L_{CM} \gg 0.5L_{DM}$$

EQUATION 53: DIFFERENTIAL-MODE CORNER FREQUENCY

$$f_{R, DM} = \frac{1}{2\pi\sqrt{(L_{DM} + 0.5L_{leakage}) \cdot C_X}}$$

Because C_Y has to be lower than 3.2 nF, it can be chosen first and calculate LCM by using [Equation 54](#).

EQUATION 54: COMMON-MODE INDUCTANCE

$$L_{CM} = \left(\frac{1}{2\pi f_{R, CM}} \right)^2 \cdot \frac{1}{2C_Y}$$

For DM components, the differential-mode inductor can be at designer's choice, so the capacitor value is calculated using [Equation 55](#).

EQUATION 55: DIFFERENTIAL-MODE CAPACITANCE

$$C_{XI} = C_{XI} = \left(\frac{1}{2\pi f_{R, DM}} \right)^2 \cdot \frac{1}{L_{DM}} = \left(\frac{1}{2\pi f_{R, DM}} \right)^2 \cdot \frac{1}{L_{leakage}}$$

LOGIC AND CONTROL WITH CIPS**CIPs Application in a MCU**

Using an 8-bit microcontroller to control the behavior and operation of a SMPS is not a common solution yet, and that is because a microcontroller is not usually equipped with all the control logic needed, and even if it has the capability to do so, it needs programming knowledge. The problem arises when the core is busy implementing one operation and the SMPS needs assistance; if the MCU is not ready to immediately respond to that need, the whole board may fail.

This does not happen with microcontrollers equipped with CIPs, which have analog and digital peripherals that can operate independently from the core. The CIPs are especially advantageous for applications like a SMPS, where a sudden change needs to be processed immediately to ensure correct functioning and protect against hazardous situations. Having a microcontroller with analog and digital peripherals independent of the core, helps in achieving more functionality with less coding space used. After the configuration phase has ended, the peripherals can work without being bothered, and, if needed, they can be reconfigured at any time during run time, which gives high flexibility to the circuit.

Some designers may not consider using a microcontroller because of the lack of programming knowledge, but that is not an issue anymore, as the configuration can be done in minutes using the Microchip Code Configurator (MCC) plug-in from MPLAB® X. The MCC is a user-friendly and easy to use plug-in, and it generates all the code needed to start the project. The latest version of the MCC allows the user to add libraries, solving the designer's trouble with just a few clicks, an online server-based version being available in the same time. This gives the CIPs an advantage, and using them properly may result in having a project that can do multiple tasks simultaneously, with minor software involved, less stand-alone peripherals on the board and less components. These can be reconfigured anytime using the communication capabilities, which translates into smaller costs and less time needed to implement an application.

Suppose a designer can build a board that has three main functions instead of three different boards. Each function uses a set or combination of CIPs, and by means of communication the designer can change functions, without changing hardware components, but just the internal peripheral connections. As such, the cost of one board will obviously be smaller than the cost of three boards with three ICs. Also, the time to build the board will be significantly reduced.

To access the CIPs the user needs to configure them according to the data sheet and to the specific function that needs to be used. For example, if a comparator is needed, the user has to configure a register to enable the comparator, select the polarity, use the zero latency filter and/or the hysteresis capability of the comparator, and even has the possibility to synchronize it to a timer. Another register allows to enable or disable the Interrupts and two more registers are allocated to select the positive and negative inputs. That will result in a configured and ready-to-go comparator that can be disabled or changed in any configuration during run time.

The CIPs that are typically used in a SMPS application are the Complementary Output Generator (COG), Comparator, Operational Amplifier (op amp), Digital-to-Analog Converter (DAC), and the Capture Compare PWM modules (CCP), since they form the usual control configuration.

Capture Compare PWM (CCP)

The CCP is used to generate the clock for the COG in Current mode (fixed-frequency) topologies, but can also be used to limit the duty cycle in topologies where needed.

Digital-to-Analog Converter (DAC)

The DAC can be used to create a reference voltage that can be changed in software; this can be used as the reference voltage for the op amp and will control the value of the output voltage. It is useful if compared to a Fixed Voltage Reference (FVR), when the output voltage needs to be changed (i.e. in battery charging applications). The DAC can also be used together with the comparator to set limits or to trigger protection protocols.

Operational Amplifier (Op Amp)

The op amp is usually mandatory in a SMPS that uses the error of the output voltage compared to a fixed voltage, but can also be used as an amplifier to sense the inductor current.

Comparators

The comparators can be used by the topology to compare the received current with the output feedback. They can also be used to detect hazardous events, such as overvoltage, short-circuit and others.

Complementary Output Generator (COG)

The COG is the one that will interpret all the events and generate the control waveform for the driver or the MOSFET itself in some applications. The COG can convert two or more separate input events into a single or complementary PWM output, where the falling and rising events control the frequency and duty cycle. The rising and falling events may have the same source, different sources, synchronous or asynchronous to the COG clock. The selectable COG clock input is used to generate the phase delay, blanking and dead-band times.

The COG module has an array of features, such as selectable clock sources, independently selectable rising/falling sources, independently selectable edge or level event sensitivity, independent output polarity selection, phase delay with independent rising/falling delay times, dead-band control with independent rising/falling events or synchronous/asynchronous timing, independent event blanking control, auto-shutdown control with independent sources and auto-restart function. The COG can also work in six modes: Steered PWM, Synchronous Steered PWM, Forward Full-Bridge, Reverse Full-Bridge, Half-Bridge and Push-Pull.

Programmable Ramp Generator (PRG)

Even though these CIPs are typically the ones used in SMPS, there are others that can be of use to designers. The Programmable Ramp Generator (PRG) can be used to generate the ramp for a Voltage Mode Control topology, and can also work as a slope compensator to fight the sub-harmonic oscillations in a current-mode control topology.

Zero-Cross Detection (ZCD)

The Zero-Cross Detection (ZCD) can be used to trigger the rising event in a Boundary Conduction mode topology.

Fixed Voltage Reference (FVR)

The Fixed Voltage Reference (FVR) can be compared to the output voltage to obtain the error voltage, or it can be connected with the DAC and obtain a more accurate programmable voltage reference than the DAC alone.

Configurable Logic Cell (CLC)

The Configurable Logic Cell (CLC) can be used to detect a hazardous event and interrupt the operation. It is useful when connected as an individual falling event or shutdown event for the COG, as it does not need an interrupt event to handle the problem and can work independently of the core.

Other CIPs

Other peripherals can also be used in a SMPS application, depending on the needed result. Some may add communication and control to the device in the application, some may use other combinations to obtain more features.

Peripheral Pin Select Module

A new feature recently added to microcontrollers, that is very useful in SMPS applications is the Peripheral Pin Select (PPS) module. The PPS module connects the CIPs inputs and outputs to the device I/O pins, but works only for the digital signals; all analog inputs and outputs remain fixed to their assigned pins. The designer can move the inputs of the Timer clocks and gates, CCP inputs, COG inputs pin, CLC inputs, the PRG rising and falling event input and even the serial communication pins, and in this way the noisier pins can be separated from the sensible ones. The outputs can also be moved to different pins, the comparators outputs, CCP, PWM, COG, CLC and even the communication pins.

This feature proved its utility when designing the layout, especially in PCBs with one or two layers. It made the hardware debugging easy by enabling the designer to do step-by-step validation, a feature that is not possible with other SMPS controllers (an example will be provided during the COG analysis).

Advantages of Using CIPs

The MCU with CIPs is very useful when the designer needs more than just a brick SMPS such as something that allows control, monitoring, communications and automated functions. The control capabilities allow the user to:

- Change the interconnections between internal CIPs
- Add and control limits
- Change the frequency
- Change maximum duty cycle allowed
- Change the slope compensation starting points or slope ramp
- Change which pin is connected to which CIP

There are many more control capabilities, some will be presented in this application note, others in future application notes.

Monitoring is possible thanks to the many ADCs available on the MCU such as the possibility to store the collected data on the internal memory and transform that data with equations the core can solve without compromising the SMPS correct functioning. When monitoring is used with control, the user can implement adaptive limits to ensure the safety of the SMPS.

The communication capability is an important advantage, as it allows the user to know at any moment what is happening in the SMPS in terms of efficiency of information, status, changes occurred from last check, error logs or fault logs. It also offers the possibility to change any designed function or feature without interrupting the supply to the load. The communication capabilities are not presented in this application note as it is reserved for a future design and application note.

The use of automated functions allows making any changes or updates to the SMPS without changing the hardware. For example, if a NiMH battery charging function is implemented on the microcontroller of a SMPS, with few lines of updated code, the same SMPS can assume the function of charging any new type of battery added. The battery charging possibilities will be presented in a future application note. Automated functions such as short circuit retries limit and soft-start function will be presented. Many more such functions can be achieved as there is still many unused CIPs and ample coding space.

For more information on CIPs, see [6] in the [Section "References"](#).

Flyback Logic with CIPs

To implement the logic combination needed to a SMPS using CIPs is easy once the topology and the Control mode is selected. For this project, there is an offline flyback topology, which means isolation is needed for the feedback signal. This means that instead of using the internal op amp of the MCU, an external one is needed that is either incorporated in the opto-isolator or in a separate combination with an optocoupler. The current-mode control technique is used, which means that a clock signal is needed to set the rising moment of the PWM, which will also set the switching frequency. The clock can be changed anytime during runtime so frequency dithering can be achieved to spread the noise and lower EMI noise. A comparator is needed to reset the PWM, which will determine the duty cycle. The slope compensation is also very important as it prevents subharmonic oscillations in CMC and can be obtained internally with the PRG. The PRG will also provide smooth entering in regulation at start-up if the duty cycle limit is set as far as 80% on a flyback without allowing any instability.

The COG can generate a waveform based on the rising and falling events on its input, and it will serve as a SR latch. The rising event can be generated by the CCP and configured with the needed frequency. Since it has to be similar to a small pulse, the rising event has to have the minimum duty cycle possible. For falling events, it is possible to add a second CCP to determine the maximum duty cycle of the driving waveform. Another falling event has to be the output of the comparator that has the feedback signal and the sensed current on the primary as inputs.

The Complementary Output Generator (COG)

The primary purpose of the Complementary Output Generator (COG) is to convert a single-output PWM signal into a two-output complementary PWM signal. Due to the available modes, a single-steered PWM signal can be obtained at one or more of the outputs available. The COG can have three possible clock sources, multiple rising and falling event sources, or multiple shutdown sources, etc. It is capable of adding dead band, blanking and phase delay to all the events, and since it is equipped with four outputs, it can use multiple control modes that can be chosen by the user.

The COG is the one that will interpret all the events and generate the control waveform for the driver or, in some applications, for the MOSFET itself. The rising and falling events may have the same source, different sources, synchronous or asynchronous sources to the COG clock, and the detection can be selected to be either edge or level-sensed, which can be favorable for some events. The selectable COG clock input is used to generate the phase delay, blanking and dead-band times, which are useful in Complementary output modes, as well as in a Single Output Steered mode, due to the high-powered switching transients that may trigger a false falling event which needs to be blanked out. All the details needed to better understand the COG can be found in [7] in the [Section “References”](#).

Going through the data sheet to configure all the registers may be time consuming, so the easy solution is to use the MPLAB Code Configurator plug-in. The user has to enable it and set the following parameters: operating mode, clock frequency, output, the rising and falling events, the type of trigger sensing (edge or level), and the pin for the COG waveform. The MCC also offers the option to see the registers and modify them entirely, if needed, and to notify the user if some other CIPs (CCP1, CCP2, Comparator 1 and Comparator 2) must be configured to comply with the configuration of the COG.

Peripheral Pin Select Module (PPS)

The PPS helps during the PCB design, as it gives the possibility to change the output of the CIPs to other I/O pins than the default ones. This translates into a better layout component placement, shorter copper lines and protection against noisier lines. Another valuable use of the PPS is during the laboratory test procedure, as it can take the internal signals that usually are not accessible in other controllers, and set them on an I/O pin. This gives the user the possibility to implement a step-by-step test and validation and to verify the comparators output, the PRG output, the CCP output, the DAC output, and other CIPs, while the devices are working or prior to connecting them to the COG; [Figure 64](#) shows this implementation.

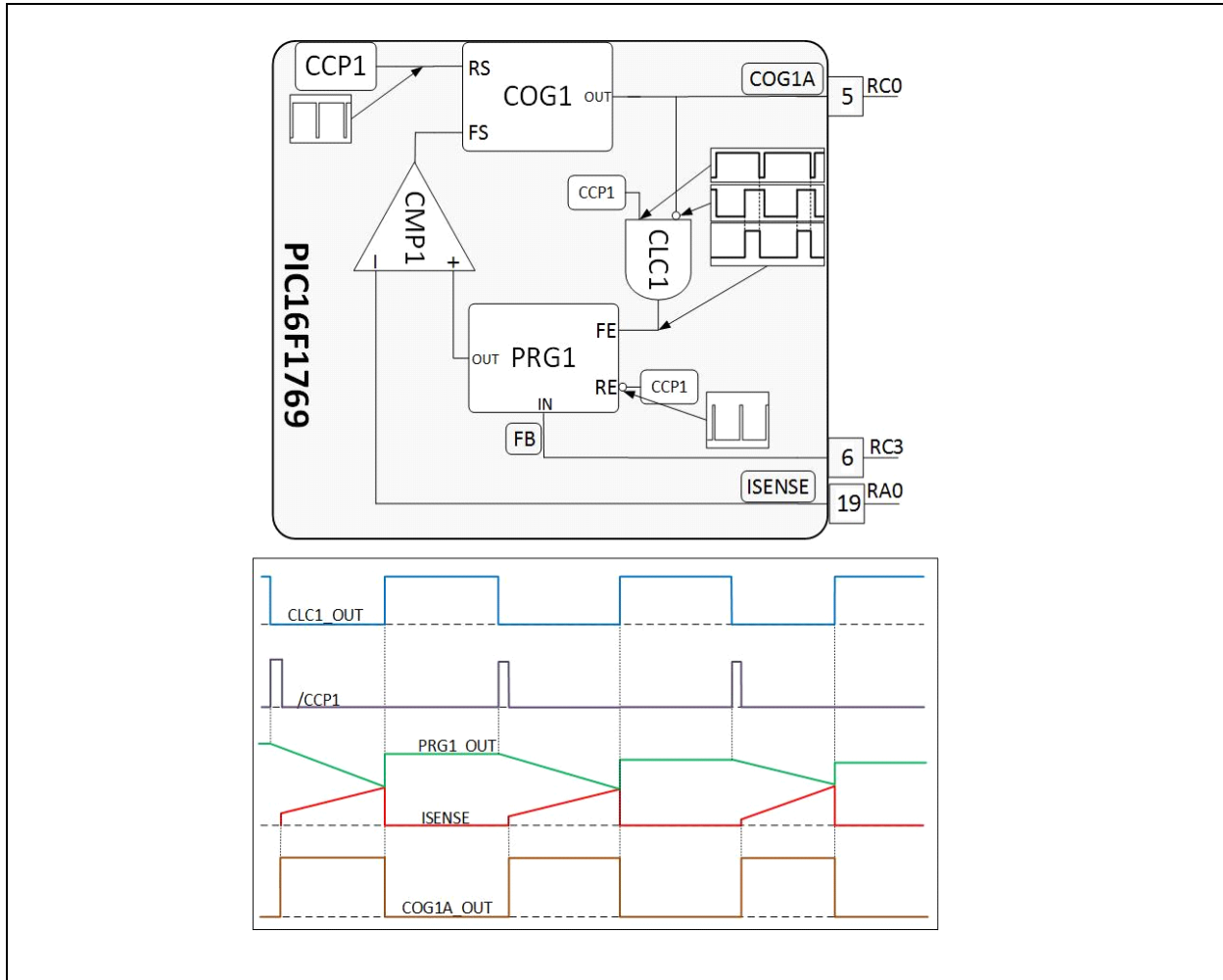
Slope Compensation

The slope compensation is an important part of the control circuit for many current-mode controlled (CMC) switching mode power supplies (SMPS). Many SMPS controllers do not have the slope compensation integrated in the chip and are implemented with external components and do not provide customization opportunities once the components are soldered.

The PIC16F176X family microcontrollers are built with internal Core Independent Peripherals (CIPs) that can be configured to control a CMC SMPS and permits different customizations and functions that can be helpful in many situations. The Programmable Ramp Generator (PRG) Core independent peripheral is used to generate the needed slope compensation signal. This CIP can be configured in multiple ways with a vast variety of slope values, but other internal CIPs can be connected to the PRG to generate a custom ramp that provides higher accuracy to the duty cycle control and eliminates instabilities.

The example below shows a way to interconnect internal CIPs to the PRG and obtain a ramp that provides high accuracy at low and high duty cycle values, which creates instabilities in classic implementations.

This is an example of one of many implementations that can achieve this result.

FIGURE 57: PRG CONFIGURED TO IMPLEMENT SLOPE COMPENSATION

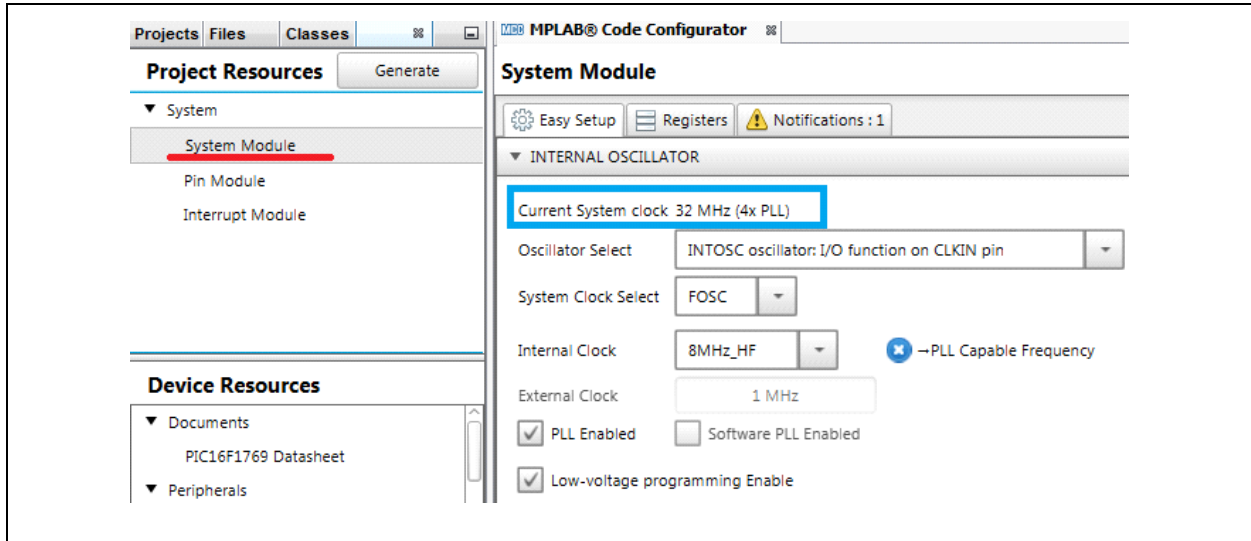
MCC Configuration

Microchip Code Configurator is the tool used to configure the PIC16F1769 and make all the CIP internal links needed to obtain the CMC for the Flyback. How to install and use the tool can be found at [14] in [Section "References"](#). Instructions to start and set-up a new project are given on page 25.

To configure the CIPs and MCU for this project, follow these steps:

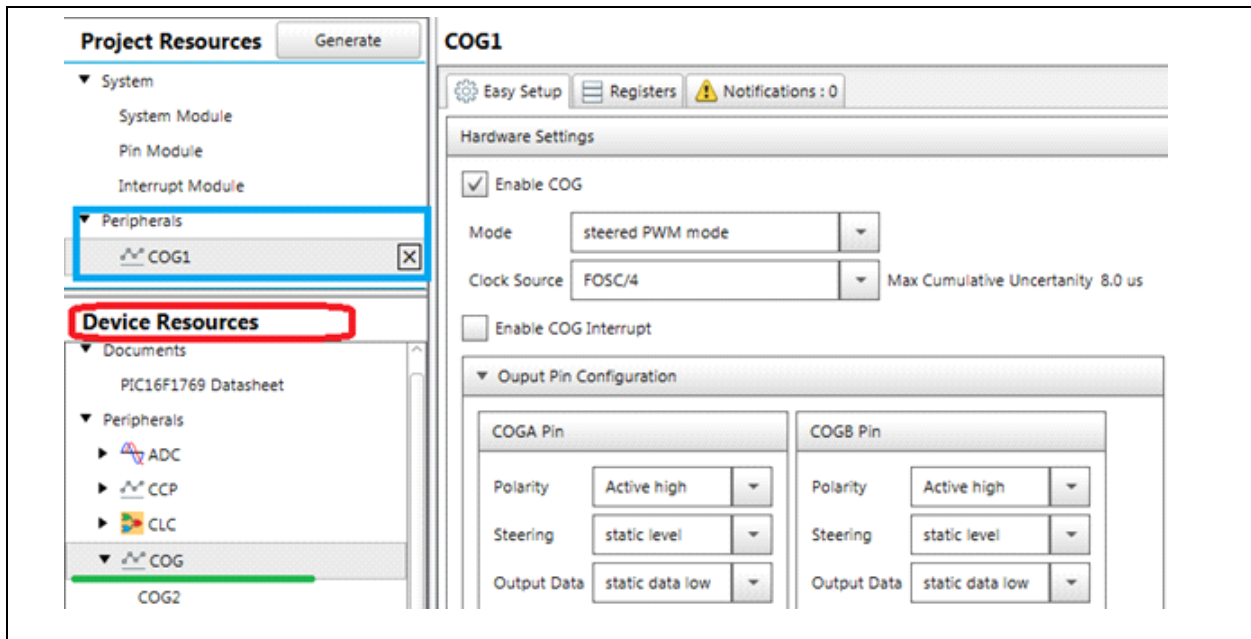
1. Start a new MPLAB® X project
2. Open MCC plugin in the MPLAB X
3. Set-up the clock frequency

FIGURE 58: CLOCK SELECTION IN MCC

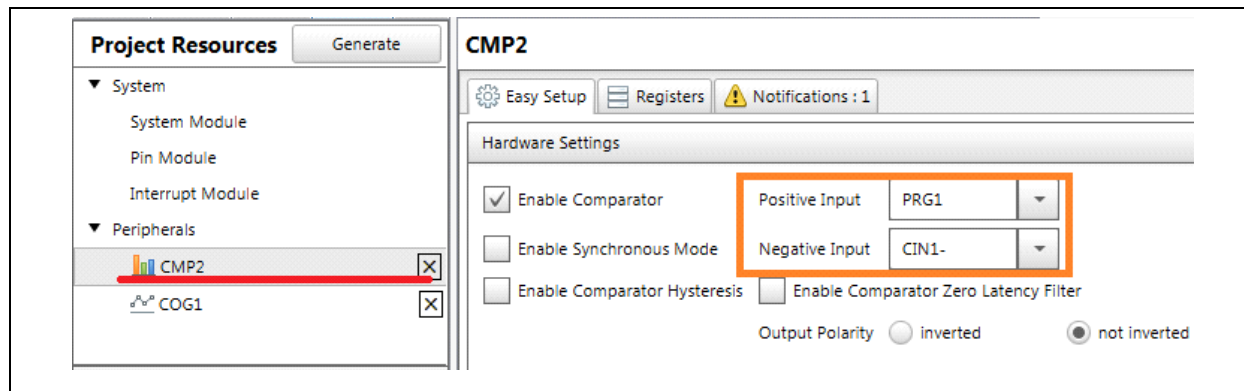


4. All the needed device resources are included in the project by double clicking on them.

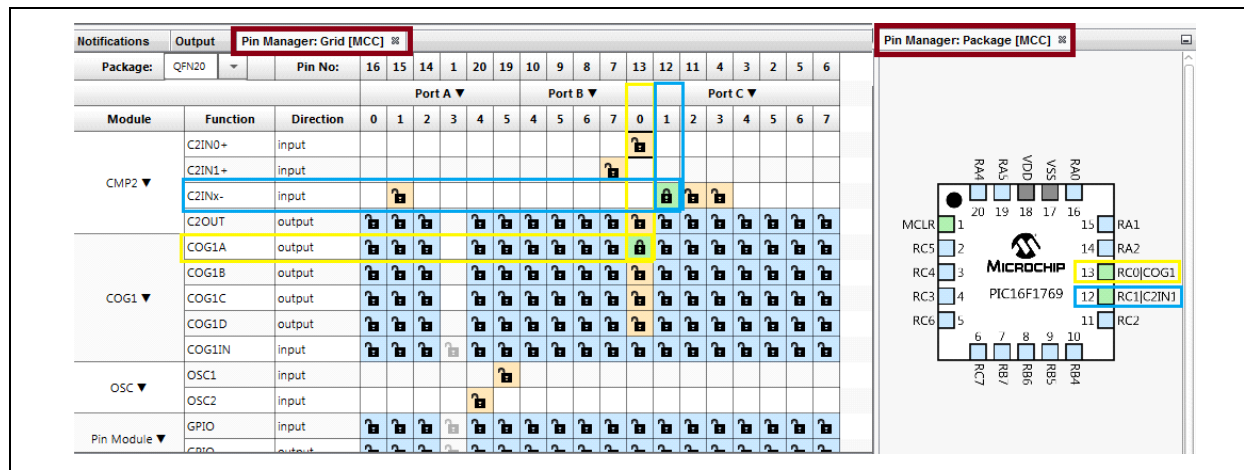
FIGURE 59: CIP ADDITION TO THE PROJECT WITH MCC



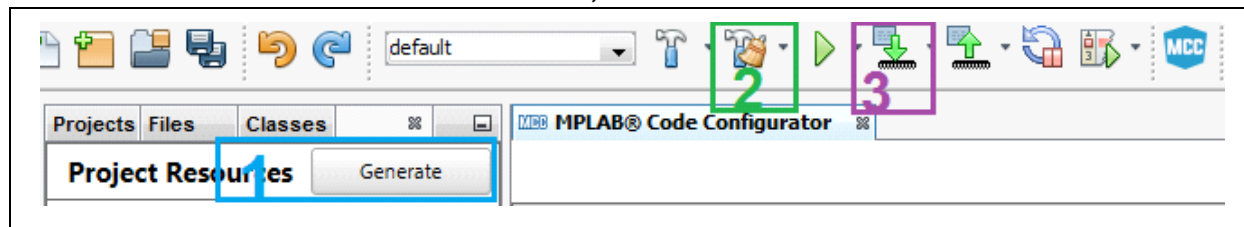
5. The CIP configuration are intuitive once the function is decided (Ex: For the peak current comparator the pin Isense connected on the negative input and the output of the PRG1 on the positive input).

FIGURE 60: SETTING THE COMPARATOR 2 FOR CMC

6. The Pin Manager: Grid view and Pin Manager Package view helps the user to see where the CIP connections will be available and where it is already busy by another CIP.

FIGURE 61: PIN FUNCTION SELECTION IN MCC GRID VIEW

7. After configuring all the CIPs step by step and verifying the logic, the user generates the code and programs it in the MCU. 1: Generate code; 2: Clean and build; 3: Program device.

FIGURE 62: STEPS TO GENERATE CODE, MAKE AND PROGRAM THE DEVICE WITH MCC

8. Test the board and enjoy.

By following these easy steps the designer will be able to configure the part without writing a single line of code. For more advanced automated functions, then the code can be written directly on the files generated by MCC, thus not altering the configuration and allowing the user to modify any configurations later on without damaging the code of the function.

The code for the current flyback project is available on the Microchip website, both written in MPLAB X and generated in MCC. The user can import the generated MCC project, adapt it or change it to the needed logic and values.

The logic implementation for this design should look like [Figure 63](#).

FIGURE 63: CIP INTERNAL BLOCK DIAGRAM

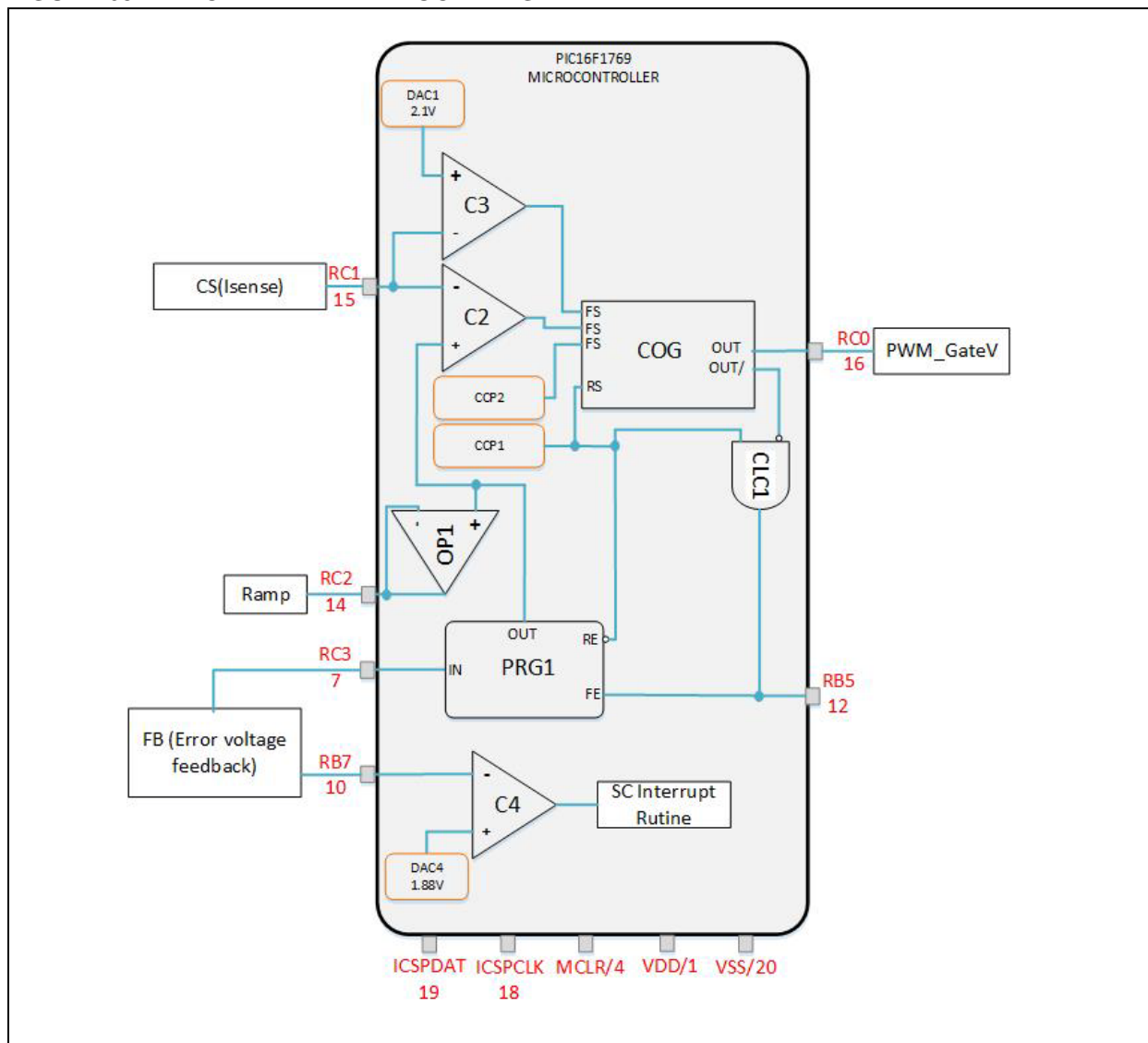
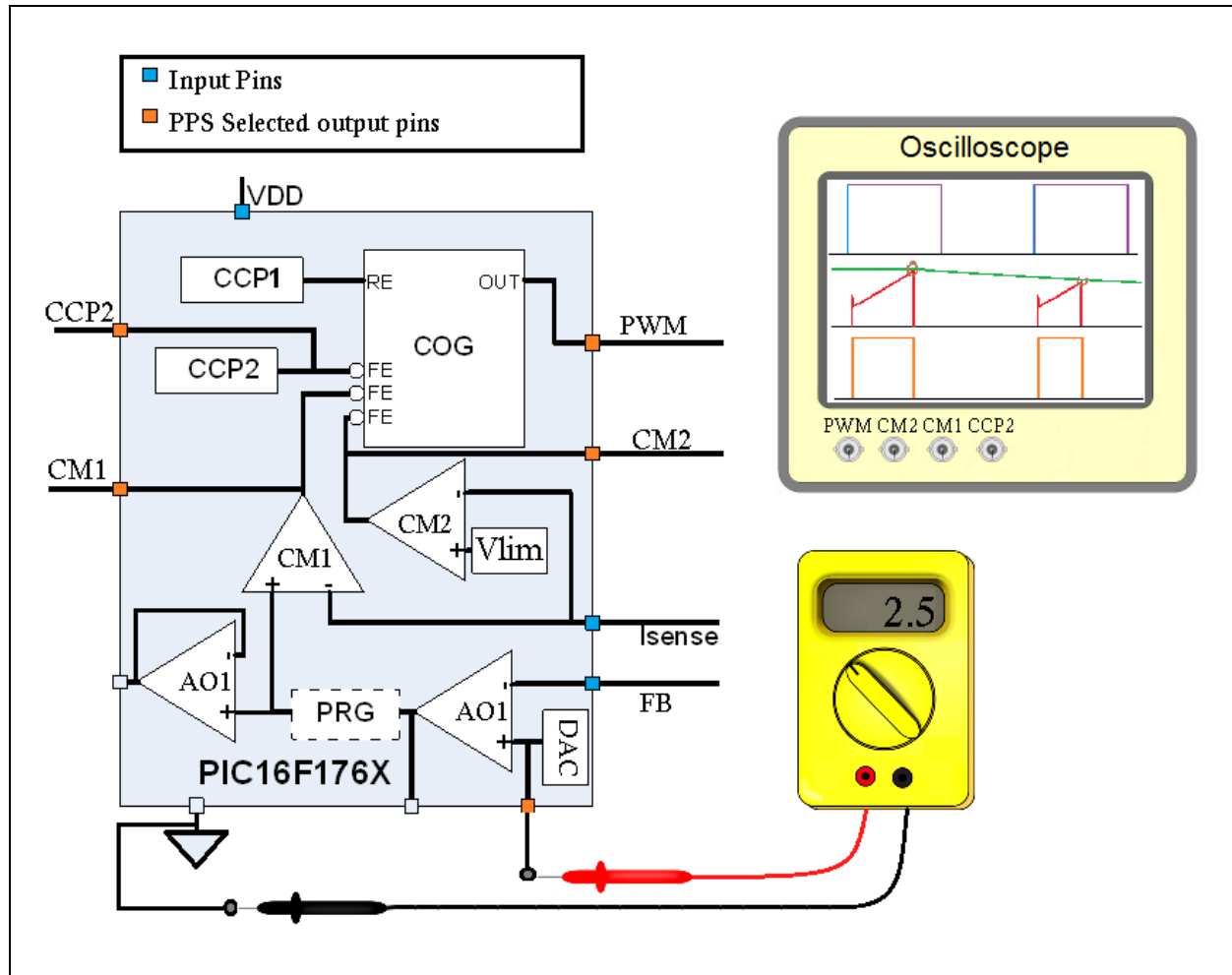


FIGURE 64: CONNECT THE INTERNAL SIGNALS TO I/O PINS USING PPS



For more detailed information on the COG and PPS, refer to [8] and [9] in [Section “References”](#).

MOSFET Drive

After the power stage is designed and the power components are selected, the next step is to select a proper gate driver. The PIC16F176X is equipped with two I/O pins that can deliver 100 mA each, and if connected in parallel with the same control signal (using PPS), they can achieve a 5V @ 200 mA drive. This can work with smaller power designs and must be taken into consideration by the designer from cost reducing reasons. For this design, the MOSFET needs are bigger than this device can support, so a gate driver must be taken into account.

The selected MOSFET has a collection of relevant operating parameters that will help to decide the drive design. Matching the MOSFET driver to the MOSFET in the application will primarily be based on how fast the application requires to turn the MOSFET on and off (rise and fall time of the gate voltage). The optimum rise/fall time in any application is based on many requirements, such as EMI (conducted and radiated), switching losses, lead/circuit inductance, switching frequency, etc.

The speed at which a MOSFET can be turned on and off is related to how fast the gate capacitance of the MOSFET can be charged and discharged. The relationship between the gate capacitance, the turn-on/turn-off time and the MOSFET driver current rating is shown by [Equation 56](#).

EQUATION 56: MOSFET TURN-ON/OFF TIME

$$dT = \frac{[dV \cdot C]}{I}$$

Where,

dT = turn-on/turn-off time of 28 ns

dV = the gate voltage of 9.1V or 10V (depending on the selected Zener diode and output of the bootstrap)

C = the gate capacitance (from gate charge value)

I = the peak drive current (for the given voltage value)

Considering that $Q = C \cdot V$, where Q is the total gate charge, Equation 56 can be rewritten as Equation 57.

EQUATION 57: MOSFET TURN-ON/OFF TIME (REWRITTEN)

$$dT = \frac{Q}{I}$$

The relationship shown in the equations above assumes that a constant current source is being used for the current I. By using the peak drive current of the MOSFET driver, some error may occur.

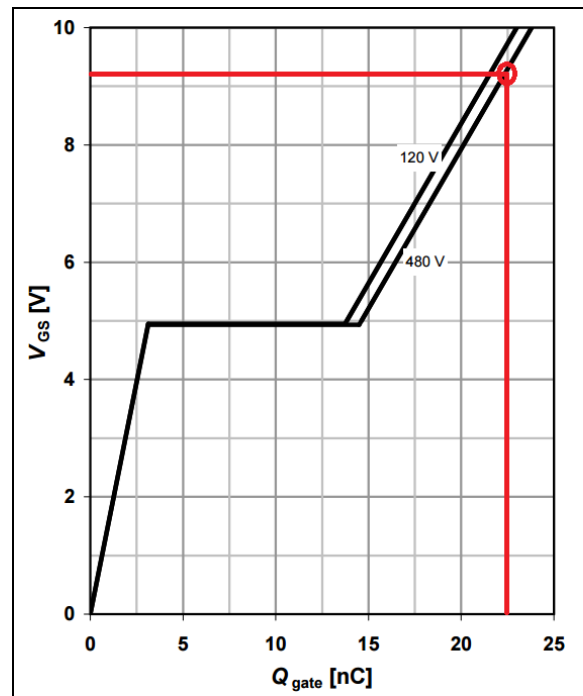
The amount of charge required for changing the gate voltage between 0V and the actual gate drive voltage is characterized by the typical gate charge vs. gate-to source voltage curve, found in the MOSFET data sheet (Figure 65). The red lines show the amount of gate charge needed for a 9.1V V_{GS} , approximately of $Q = 23$ nC. The turn-on/turn-off time in the data sheet equals 28 ns. So, by applying the Equation 57, the peak drive current can be calculated as shown in Equation 58:

EQUATION 58: MOSFET PEAK DRIVE CURRENT

$$I = \frac{Q}{dT} = \frac{23nC}{28ns} = 0.82A$$

The equation has produced a peak-drive current requirement of 0.82A. However, the gate-drive voltage in the design parameters is 9.1V, and this must be taken into account when selecting the appropriate driver. For instance, if the driver selected is rated for 0.8A at 18V, the peak output current at 9.1V will be lower than 0.8A. Because of this, a driver with a 1.5A peak output current at 18V is chosen for this particular application; MCP1416 MOSFET driver was considered in this case.

FIGURE 65: THE GATE CHARGE VS. GATE-TO-SOURCE VOLTAGE FROM THE SELECTED MOSFET DATA SHEET



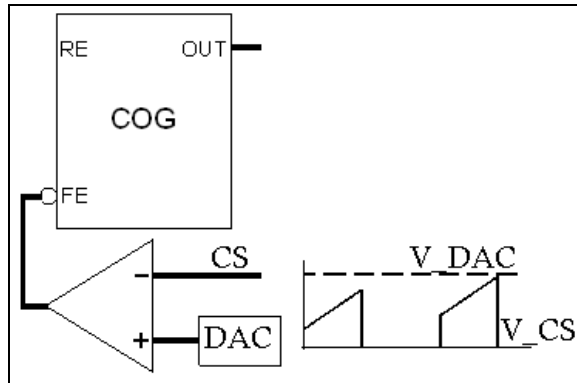
In many gate drive applications, it may be necessary to limit the peak gate drive current in order to slow down the rise of the gate voltage. This is usually done to lower the EMI noise generated by fast slew rates of the MOSFET drain voltage. Slowing the rise and fall time of the MOSFET gate voltage can be accomplished by either switching to a MOSFET driver that has a lower peak current rating, or by adding a series gate drive resistor.

For more information about gate drive design, refer to [10] and [11] in the Section "References".

Primary Peak Current Limit

Sometimes the designer may need to limit the primary current peak or even the power peak, to protect more sensitive components from being destroyed. This can be achieved by using one of the extra comparators in the microcontroller, and one of the DACs, as shown in Figure 66.

FIGURE 66: LIMITING THE PRIMARY PEAK CURRENT USING A DAC AND COMPARATOR



This can be used to configure a set primary current peak limit; when the current reaches the limit, a falling event trigger will set the switch to an OFF state, thus stopping the current from rising further. The limiting value is obtained from the DAC, allowing the user to change the limit, based on the project specification or component limits.

A primary power peak limit can be implemented using this configuration, by connecting the input voltage to the ADC, and setting a defined primary power peak value, so that the DAC value meets the limit. By knowing the primary voltage and the needed power peak, the current peak limit can be calculated as $I_{PEAK} = P_{PEAK}/V_{IN}$; knowing the value of the sense resistor, the voltage on the DAC needed to maintain the peak power can be calculated as formulated in Equation 59.

EQUATION 59: DAC VOLTAGE

$$V_{DAC} = \frac{R_{Sense} \times P_{Peak}}{V_{IN}}$$

The DAC value in decimal can be calculated using Equation 60.

EQUATION 60: DAC VALUE

$$DAC_{Decimal} Value = \frac{V_{DAC} \times Resolution}{V_{Supply}}$$

Using this configuration and a software calculation, the peak power (not the average power) in the primary of the converter can be controlled. This limiter is based on internal connections of CIPs: DAC, comparator, COG and PPS. It is considered one of the control capabilities that a MCU with CIPs can provide. The user has full control over the limit value and PIN connections for the comparator sources. This control capability can be merged with the automated function capability and the monitoring capability. The user can obtain an adapting limit based on observation interpretations, this is more advanced than an ASIC can provide.

EXAMPLE 1: DAC LIMIT CALCULATION

Suppose, a 10-bit resolution DAC powered from $V_{DD} = 5V$.

$P_{PEAK} = 30W$; $V_{IN} = 90V$; $R_{SENSE} = 2\Omega$.

Using Equation 59: $V_{DAC} = (2\Omega \times 30W)/90V = 0.66V$

Using Equation 60: $DAC_{decimal} Value = (0.66 \times 1024)/5V = 135 \Rightarrow DAC = 0d135 = 0x87 = 0b10000111$

The Soft-Start Software

At start-up, the converter may encounter some problems, as the output is not yet powered and the control circuitry tends to deliver a high duty cycle to the switching device. This may induce component stress due to the sudden current flow and it can cause inrush currents and acoustic noise, and even a high-output voltage overshoot. This condition continues until the output voltage of the power supply approaches its nominal value. There is a problem when the load is capacitive, because of the large transient currents required to charge it. The repeated high stress of the start-up can result in failures of the power MOSFET transistors or the power rectifiers.

Soft-start circuits fix this problem by slowly increasing the output of the power supply. The reduced rate limits the initial error and the overall drive of the system is reduced.

This can be achieved either by using a hardware solution that will add to the BOM cost or by a software solution presented here (an automated function).

Another interesting solution of Soft-Start is presented in [12] in Section "References".

The solution used for this project is based on the CCP2 peripheral, which is enabled as a falling event to the COG, and it basically limits the allowed maximum duty cycle within a time limit, enough to allow the output voltage to increase slowly. As shown in Figure 67, the signal will drive the switching device, while the CCP2 signal implements a soft-start function by inducing a falling event to the COG. The duty cycle of the CCP2 is controlled by the software and thus, the soft-start timing can be changed according to user's preferences. The feedback signal is shown as a green line and it starts at the highest position due to the lack of output voltage. As the output voltage closes to the desired value, the feedback gets closer to the sensed current signal (purple line) and the loop starts to take control over the soft-start procedure. The gray lines show which signal gives the falling event that determines the COG duty cycle. The soft-start software does not add to the BOM price and can be configured without any hardware changes, due to the CIPs automated and control functions that the CIPs bring to a SMPS.

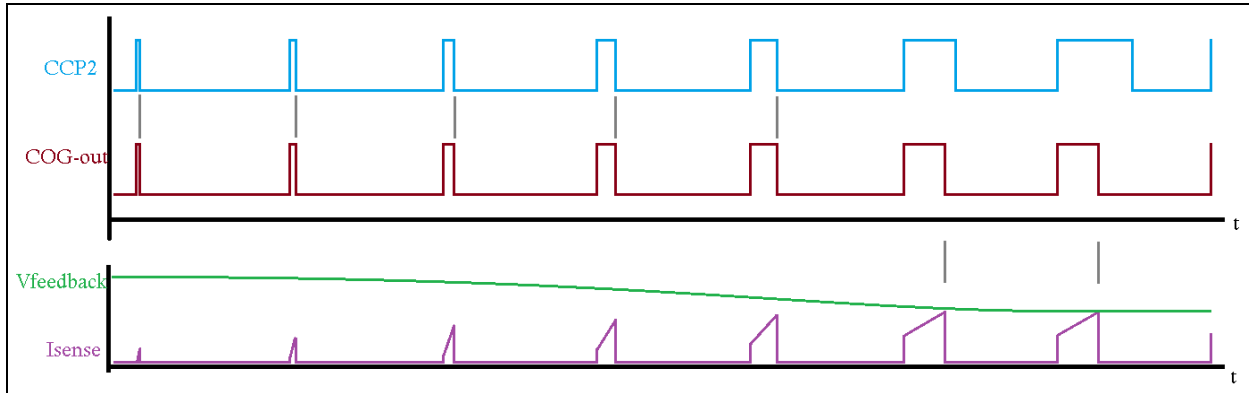
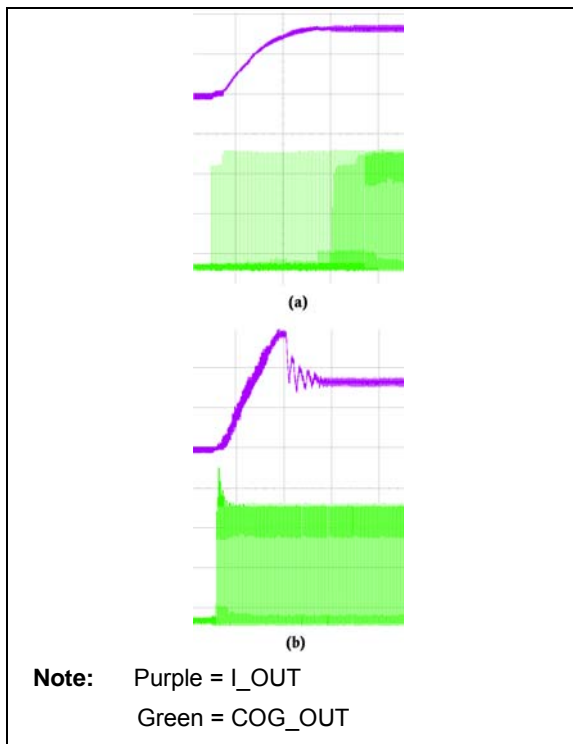
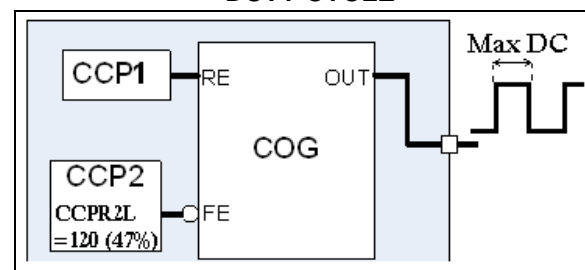
FIGURE 67: SOFTWARE SOFT-START IMPLEMENTATION USING CCP2

Figure 68 shows the output current of the converter (a) with the Soft-start and (b) without the Soft-start procedure.

FIGURE 68: START-UP (A) WITH SOFT-START (B) WITHOUT SOFT-START

Minimum and Maximum Duty Cycle

In a flyback SMPS topology, the energy transfer from the primary to the secondary happens during the OFF time of the switcher, which means that the energy is stored in the primary of the transformer when the MOSFET is ON, while during the OFF time, the energy is transferred to the secondary of the transformer. For other converters, there is the possibility to have a close to 100% duty cycle, but if this is done for the flyback topology, there will not be enough time for the energy to be transferred in the secondary, and the converter will not work as desired. To make sure this does not happen, the user can implement a duty cycle limiting circuit that will not allow the MOSFET to stay ON more than a selected percentage of the switching period. This method is part of the control capabilities that the CIPs can provide. It uses one of the CCPs with the pulse width defined in software; it is connected to the falling event of the COG. Figure 69 shows the maximum allowed duty cycle can be modified at any time in software offering great flexibility to the user.

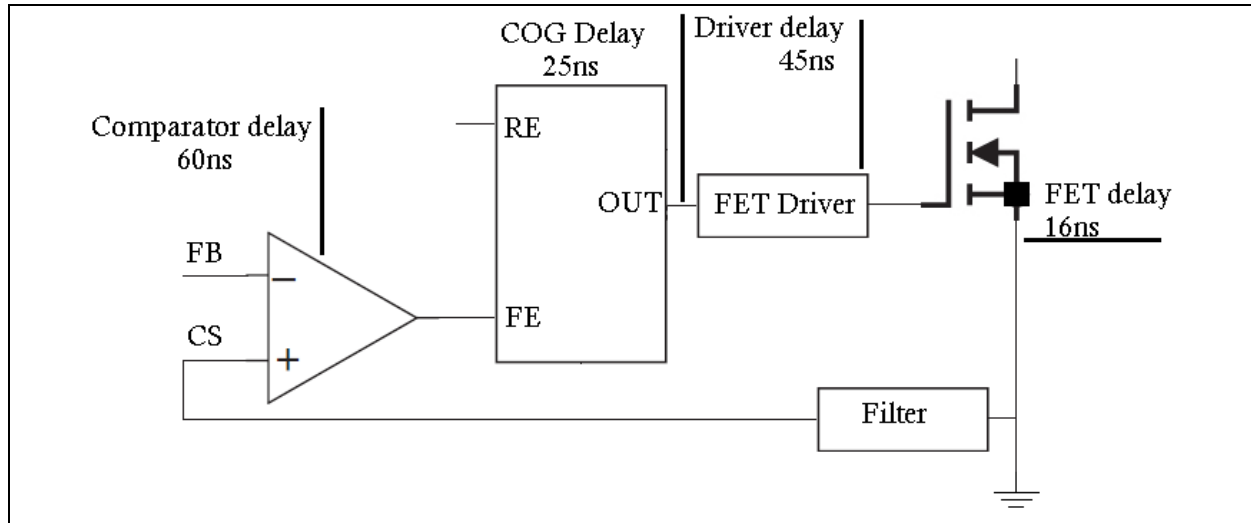
FIGURE 69: SETTING CCP2 TO LIMIT THE MAXIMUM ALLOWED DUTY CYCLE

On the other hand, the minimum duty cycle the control circuitry can have is something that can either be controlled when a higher minimum duty cycle is needed, caused by the delays that happen in the device, or in other electronic components that carry the control signals.

To generate a minimum set duty cycle, the COG can be used. The blanking function will allow masking an input event for a period of time set by the user. This is usually done to prevent electrical transients, caused by the turn-on/off of the power components, from generating a false input event. If the user needs a higher minimum duty cycle, the above method is to be used without any external components. Most of the time, a minimum duty cycle is unwanted, as it limits the loop control during low loads with high input. [Figure 70](#) shows the most

important delays in the current control loop; those that cannot be changed are the following: Comparator, COG, MOSFET, driver, and the microcontroller PAD delay, unless the components themselves are changed. But the delay caused by the filter can be carefully calculated, so that it does not add too much to the chain, and still helps filter the signal.

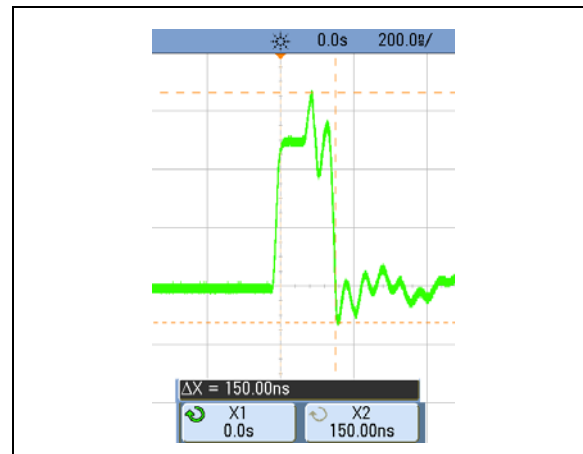
FIGURE 70: CURRENT LOOP DELAY SOURCES



When this problem was first encountered in the project, the total delay was of 270 ns, which meant a 3.3% minimum duty cycle. After the filter was redesigned, the total delay went down to 150 ns, which is 1.8% minimum duty cycle. In [Figure 71](#), the total measured delay of the current control loop can be seen after the corrected filter design.

Note: This is the minimum possible duty cycle achievable with this configuration at this frequency.

FIGURE 71: FALLING EVENT DELAY



Short-Circuit Protection

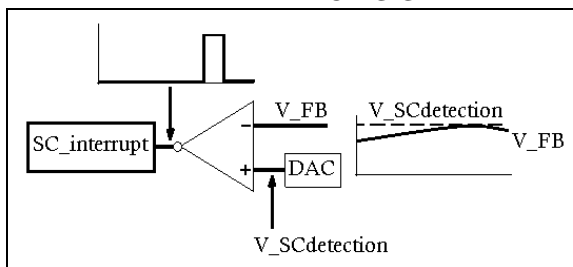
A short circuit occurs when an electric current flows along a path different from the intended one in the electric circuit. When this happens, there is an excessive electric current that may lead to circuit damage, fire, or explosion. This can happen when the insulation of the wiring used breaks down, also due to the presence of an external conducting material (such as water) introduced accidentally into the circuit.

When using an offline topology with the controller on the primary side, it is challenging to monitor the output current at all times. It is recommended to identify the symptoms that can be seen in the primary when a short circuit is happening, and use them to notify the MCU to start the short-circuit fault procedure.

The identified symptoms that can be used are the rising of the auxiliary voltage, the rising of primary peak current, and the feedback error voltage. A detection method can be used to monitor either of the signals separately, or use them together.

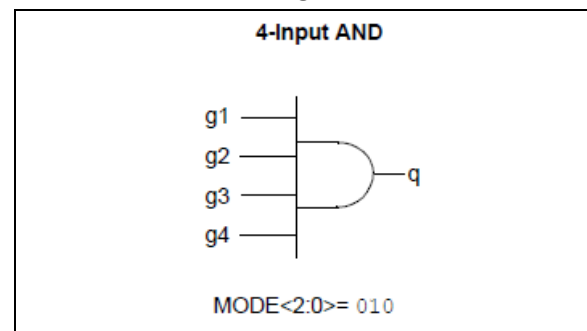
Separate detection can be achieved by using one of the comparators and by setting a voltage threshold. If the limit is passed, then the comparator will change the output state, thus, notifying the device that a short circuit has happened, as shown in Figure 72.

FIGURE 72: SHORT-CIRCUIT DETECTION USING A FEEDBACK SIGNAL



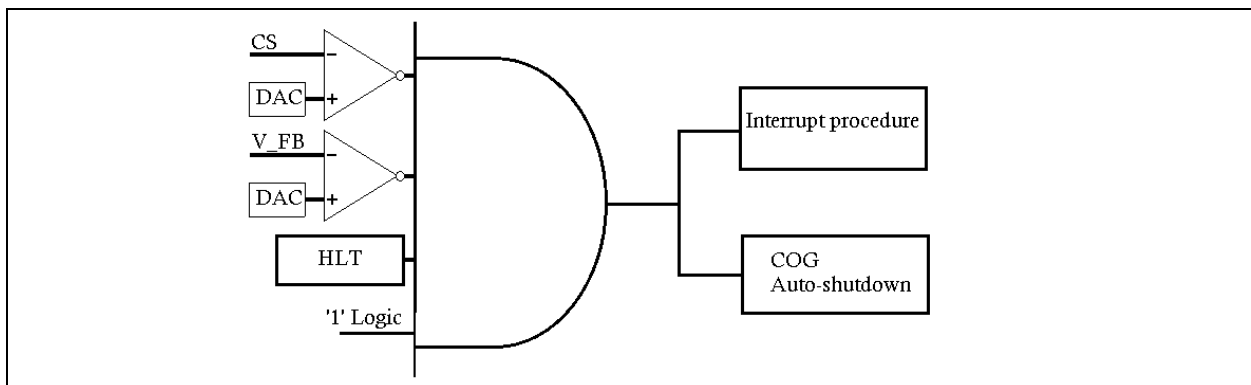
There is also the possibility to have multiple signals to detect a short circuit using the CLC. This can be configured as a 4-input AND, as shown in Figure 73. Two comparators can be connected as an input source: one comparator can monitor the peak current and the other the feedback voltage. When both conditions are met, a short-circuit interrupt can be activated, which allows the user to take into account the errors that can occur and activate the SC-interrupt protocol (only in case of definite short circuit).

FIGURE 73: CLC CONFIGURED AS A 4-INPUT AND



This configuration allows adding two more decision inputs. One of them can be a hardware-limit timer that can take into account the start-up procedure, and be taken off the circuit once a stable condition is achieved. This configuration is shown in Figure 74.

FIGURE 74: SHORT-CIRCUIT PROTECTION CIRCUIT USING THE CLC



The problem of detecting a short circuit can be solved, but if the problem causing the short circuit persists, another procedure must be applied in order to retry to deliver power and to decide how many times to do so. If the SMPS is placed where assistance can be provided to fix the problem causing the short circuit, then a procedure that retries a limited amount of times to restart the power delivery can be implemented. After the number of retries is exceeded, a notification can be sent to the user.

Using software during this procedure allows the user to select the number of retries, the delay between each retry, and the way to configure the retry duration, based on the specifications.

For this project, a feedback signal was taken into account for identifying the short circuit, and a limited number of retries, as shown in [Figure 72](#). A 10-bit DAC is used to set the SC threshold, and the interrupt routine includes only few lines of code. This allows the user to detect the short circuit during normal functioning and to continue the conversion when the problem is eliminated. It even detects the problem when the circuit is first started and a SC is present, as it will be explained further on in this application note.

If the user is not careful, this may lead to issues with the primary IC power. Setting the operating frequency high during the OFF time will take up a lot of energy, but this can be solved by lowering the frequency without impacting the efficiency of the circuit. This SC protection is a perfect example of the control, monitoring and automated function that the MCU with CIPs is capable.

Open Circuit

The SMPS design will not always have a load connected to the output. When there is a small load or no load at all, the duty cycle of the control circuit will reach its minimum, so the control loop will not have any influence and the circuit will work as an open loop. This can cause the output voltage to rise to the point of damaging the load.

ADDING A RESISTOR TO THE OUTPUT

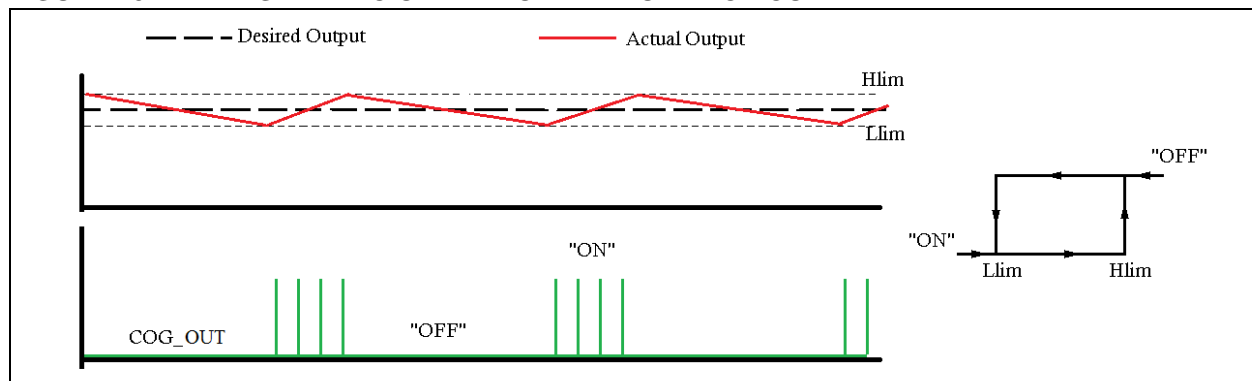
There are multiple ways to ensure the output voltage does not surpass the limit, and the most used one was to add a resistor to the output of the converter that will ensure a minimum load presence. This method will not allow the control circuit to reach an open-loop condition, but it drops the efficiency of the converter, as the resistor will always take up power that will be converted into heat and, therefore, not used by the load.

USING HYSTERESIS

Another way to solve this problem is to use two limits on the output voltage that will form a hysteresis. When the output voltage goes above the set limit (i.e., 14V on a 12V output SMPS), then the converter will be stopped, as the output voltage drops lower than another set limit (i.e., 9V on a 12V output SMPS). The converter is restarted with the same minimum duty cycle for a short period, enough to reach the desired output level in an open-circuit condition. After the time limit, if the voltage limit was not reached, it means that a load was connected and the converter will be allowed to re-enter soft-start and its closed-loop control. This method will allow the converter to consume very little power when a load is not present, and still maintain the desired output voltage.

This method is shown in [Figure 75](#).

FIGURE 75: HYSTERETIC OPERATION WITH OPEN CIRCUIT

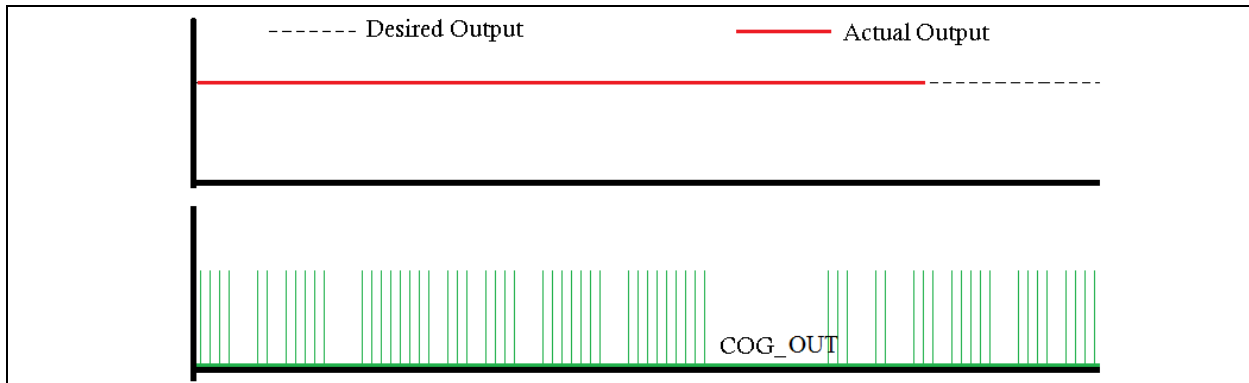


THE PULSE SKIPPING METHOD

Another method that can be used to maintain the output voltage at the desired value, without additional power losses, is to replicate what the Voltage Mode Control does: by having the falling event active when the rising event becomes active, the rising event will be overwritten immediately and the control signal will not rise.

This method reminds of a pulse skipping, and has an advantage over the hysteresis, as it adapts faster to load changes and the COG is never in Shutdown mode. Also, it maintains the output voltage constant and at the desired value. [Figure 76](#) shows the implementation of this method: the pulse skipping is not at equal distances, as it shows the adaptation with input voltage changes.

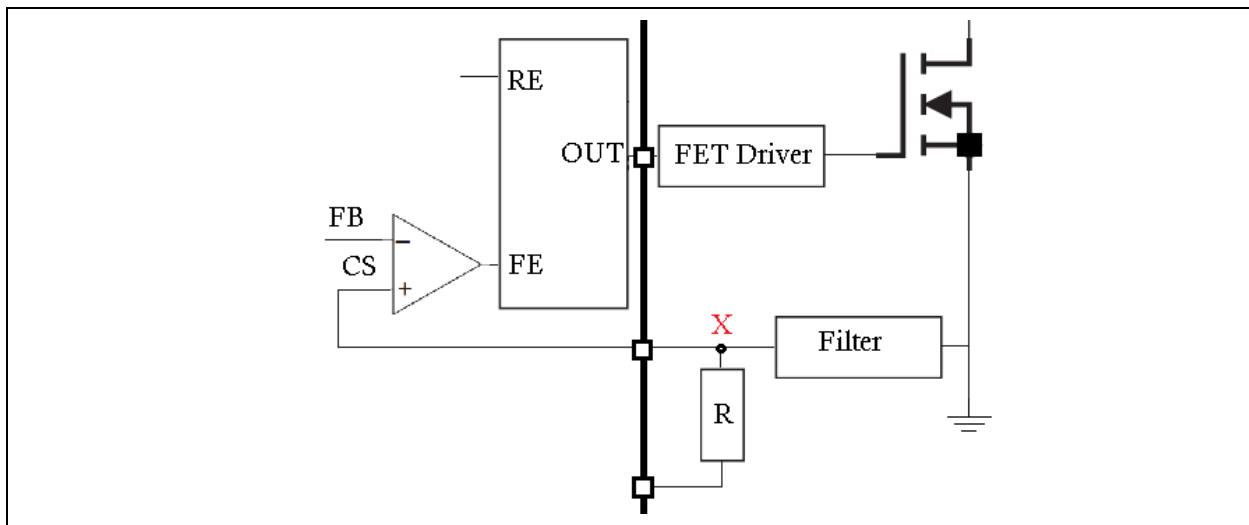
FIGURE 76: PULSE-SKIPPING OPERATION FOR OPEN-CIRCUIT CONDITION



For this project, the pulse skipping method was chosen, as it can be done only by adding a resistor to the circuit without using internal components, and save them for other purposes. The resistor is used to add a fixed value to the DC voltage component over the current sensing waveform. This gives the comparator the possibility to activate the falling event for a longer time, as the comparison is not near the zero voltage level, but it will be raised by a certain value.

The DC voltage component can be added even without using the external resistor, by connecting the FVR output to the pin or even control the DC voltage by connecting the DAC instead of the FVR (if they are not needed elsewhere). [Figure 77](#) shows the implementation and [Section "Light Load or Open-Circuit Operation"](#) can be consulted to verify if it works as expected.

FIGURE 77: HARDWARE IMPLEMENTATION FOR PULSE-SKIPPING OPERATION



The needed DC value can be calculated by using Ohm's law, along with the installed resistor and the filter's resistor, as indicated in [Example 2](#).

EXAMPLE 2: VOLTAGE RISE CALCULATION

Suppose,
 $R = 1.8 \text{ k}\Omega$
 Voltage on the pin = 5V
 filter's resistance is $R_f = 512\Omega$
 To calculate the DC Voltage value:
 $X = 5V * (512\Omega / 2312\Omega) = 1.1V$.
 If the current sense waveform is raised by 1.1V, the pulse skipping is possible when the load is missing.

MCU Consumption During Idle Mode

The bootstrap will provide enough energy to start the converter. After the conversion is started, the energy necessary to drive the converter is taken from the auxiliary winding. This method is widely used and highly efficient when the converter delivers power.

If the MCU is working at a high frequency, it will consume the power stored in the capacitor before the time comes to retry and receive more power from the auxiliary winding. The bootstrap circuit will supply only enough power to maintain the MCU running, but the MOSFET will never be switched as the driver will be depleted of power.

A solution to this issue is to deliver more power from the bootstrap, but this can affect the efficiency, as more power will be used than is actually needed.

A better solution is to use the MCU to either decrease the working frequency, so that the energy consumption during the OFF time is less than the energy stored in the capacitor, or even disable some of the CIPs that do not have any purpose during the OFF time, and put the MCU in Sleep. This way, the eXtreme Low-Power (XLP) features ensure a reduced energy consumption.

To set this up, it takes only a few lines of code and some lab time to test everything. It can be reconfigured and changed every time with minimum effort, with no hardware changes and without affecting the overall efficiency of the converter.

This feature may be useful for the converters that must be compliant to more strict energy consumption regulations, as the MCU can be configured to go to Sleep when the load is not present, and re-test for load presence after a specified time, making the overall consumption of the converter during Idle lower than 0.02% of the normal operating energy consumption from the network.

LAYOUT TIPS

Once the schematic is ready and the components are selected, the PCB has to be designed. In this chapter, some simple tips will be discussed, helping the designer to avoid the total redesign of the PCB.

Component Placement

The component placement is as important as any layout rule, and in many cases can make the difference between a working board and a faulty board, even though the components used are the same and they connect to each other in the same way.

The parts that cause the biggest trouble have to be placed separately from the sensible components that can change functionality, if influenced. Such an example is the usual separation of the analog and digital components on the same board.

In a SMPS, the component placement plays an important role as the nature of the switching imply high-frequency noises, the presence of magnetic and inductive parts and sensible triggering control ICs.

The tip will be to place the components that are responsible to implement a specific function together, in close proximity to the ones that implement a function related or linked to theirs and separate from the ones that are not related and may influence the correct functionality.

In the case of the offline flyback circuit, the components that have the function to transform the AC voltage into a rectified AC voltage are placed together in a group and separated from the DC part of the circuit, as it can harm and destroy the components rated for DC voltages.

The high-voltage switching components are also bound to be placed in close proximity to each other, and other more sensible components must be either shielded from them or placed where the influence is smallest.

If the components responsible for the high-voltage and high-frequency switching function are placed far from each other, the long lines connecting them will most likely work as antennas and the noise will disrupt the correct functionality. The layout software allows the user to place the components anywhere on the PCB, which sometimes allows for smaller designs, but it is better to keep the components designed for a specific functionality together to eliminate delays and influences.

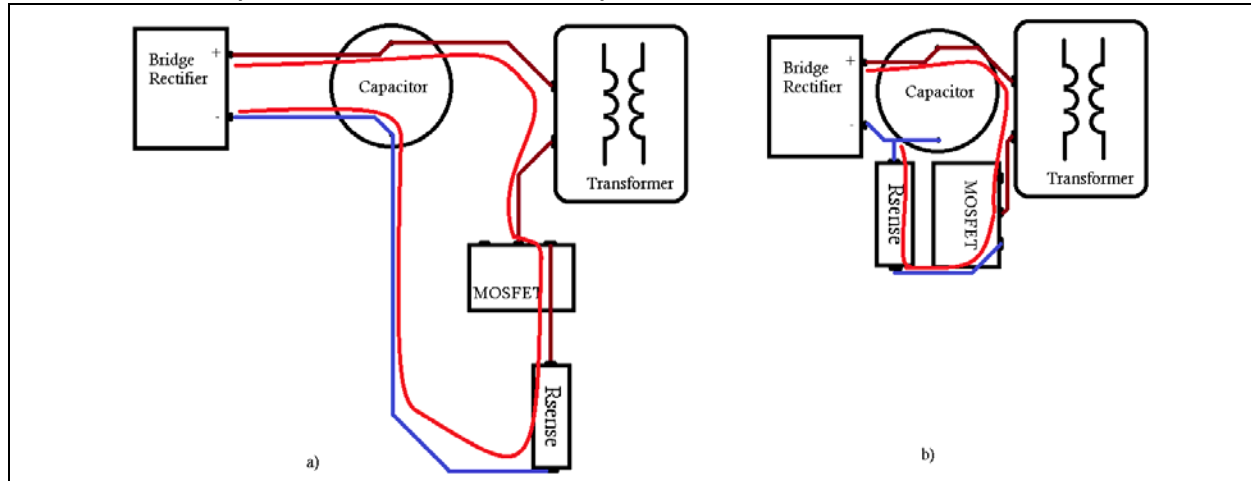
In order to maintain the isolation status of the output, the designers use the isolated transformer to transmit the energy, optocouplers to send back the output information and separate ground planes so no current passes directly from one side to another. The correct component placement also takes part as one of the measures to stop the current from having a direct connection. In this case, if the output components and lines are placed close to the components directly connected to the primary side, then depending on the ambient conditions on the board, arks of current can be produced and destroy the intended isolation.

Short “High dV/dt ” Lines

Another useful tip is to keep all the lines that have high-frequency and high-voltage switching as short as possible; sudden changes can cause electromagnetic emission in the cables and affect the nearby sensitive components.

As depicted in Figure 78, the components can be placed at different distances in the same circuit and the lines connecting them will vary in length.

FIGURE 78: A) LONG HIGH dV/dt LINES; B) SHORT HIGH dV/dt LINES IN THE SAME DESIGN



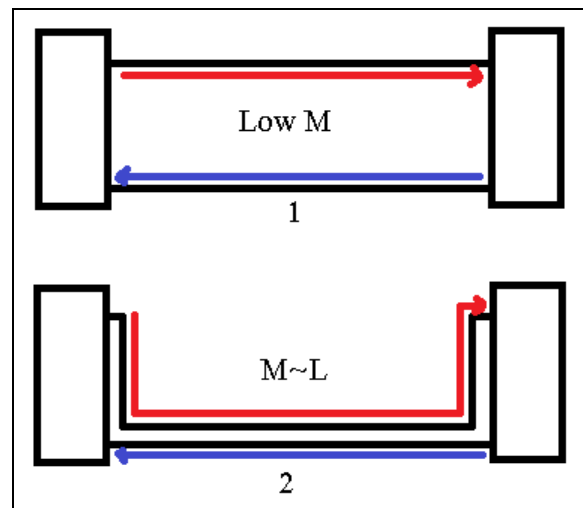
Return Paths and Ground Plane Cuts Problems

Each signal or power line that delivers energy or information to one point on the board has to have a return path so that current flow can take place, usually this return path is called ground or 0V. The ground lines provide a low-impedance path for the current, but depending on the geometry and position of this path, the designer can use it in an advantageous or disadvantageous way.

With high-frequency signals (> 10 s to 100 s kHz), when the signal line and its return path are placed close to each other, the neighboring currents will flow in opposite directions. This reduces the inductive impedance of the total path because the mutual inductance of the loop will rise (this can be seen in Figure 79, where the effective inductance of a signal loop is $2*(L-M)$, L being the self-inductance of each half of the loop and M the mutual inductance between the halves). The current will always choose the path with the least inductance, while forcing a path with higher inductance will cause some problems that will disturb or limit the functionality of the application, but will not necessarily stop the board from running. Any high-frequency current that will flow through a high-inductance path will cause a voltage to appear on

the surface and, thanks to the capacitive coupling forms, a radiating dipole that can be enhanced by nearby cables. The present inductance also represents a way for magnetic coupling with the environment, which causes the board to be susceptible to external noise.

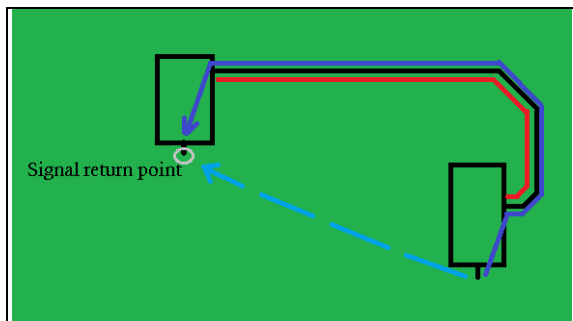
FIGURE 79: SEPARATION OF SIGNAL AND RETURN



A solution to this problem may be the implementation of a ground plane or a 0V plane. The ground plane will offer the return signal the possibility to choose the path with the least inductance. It is easier to implement the layout, provide shielding to some susceptible tracks and if correctly used, allow better EMC performance.

As depicted in [Figure 80](#), thanks to the ground plane, the current will now be able to choose the path best suited even if that is not the shortest geometrical path. (The dotted line shows the shortest path, while the blue line shows the path chosen by the current).

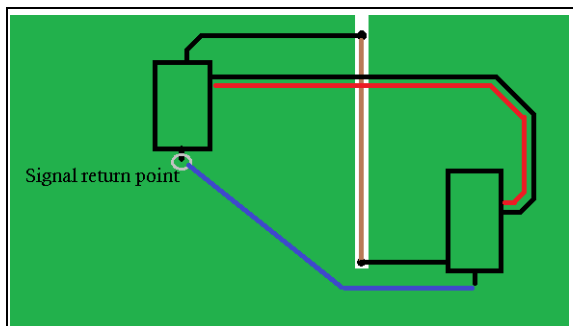
FIGURE 80: RETURN CURRENTS ON A PCB GROUND PLANE



Sometimes, the ground plane cannot be without cuts as some tracks must be placed on the same side. This can change the return path to critical signals and generate a radiating dipole, as depicted in [Figure 81](#). Now, in some designs it is not a problem if the ground plane has some breaks, the important thing to do is to identify the critical tracks that carry signals with higher frequencies (> 100s kHz) and with high di/dt and make sure not to have any cuts on their optimal return path.

So, the effect of the ground plane is to reduce the ground inductance, to minimize self-generated ground noise and differential ground noises generated by incoming interference, hence, providing a better EMC performance of the board.

FIGURE 81: GROUND PLANE CUT



Thermal Considerations

Thermal considerations must be taken when designing a SMPS that can be used in many thermally uncontrolled situations and this problem has been seen in solutions that worked fine on the bench but failed due to thermal failure on the field. The thermal calculations are not easy to understand and a solution for electrical engineers is to compare it to an electrical problem instead of a thermal problem, or maybe make an equivalent to the problem.

As in an electrical circuit, the voltage difference will induce a current flow, in this case, a thermal difference will induce a power flow, a thermal resistance will resist the flow of power and a thermal capacitance will store heat that can be later dissipated just with the analogical electrical capacitor. [Table 3](#) explains this analogy.

For electrical circuits, Ohm's law states that the voltage rise across a resistive device is equal to the current passing through it, multiplied by the resistance. Using the thermal analogies, Ohm's law in thermal equivalent will look as shown in [Equation 61](#).

EQUATION 61: THERMAL EQUIVALENT OF OHM'S LAW

$$\Delta T = P(\text{watts}) \cdot \theta (\text{°C/watt})$$

Where:

ΔT is the rise in degrees Celsius

P is the power in Watts

θ is the thermal resistance in °C/W

In order to model a thermal problem to look like a solvable electrical problem, the following steps need to be taken:

- Model a source of heat with an electrical current source where the value of the current represents the power of the source in Watts.
- Model anything that resists the flow of heat with an electrical resistor where the value of resistance is equal to the thermal resistance.
- Model ambient thermal nodes where the temperature remains the same when heat flows in or out of them, with an electrical voltage source. The voltage is equal to the temperature in degrees Celsius (the surrounding can be used as an ambient node).
- Model a hot object with an electrical capacitor where the value of the capacitor is equal to the heat capacitance of the object.

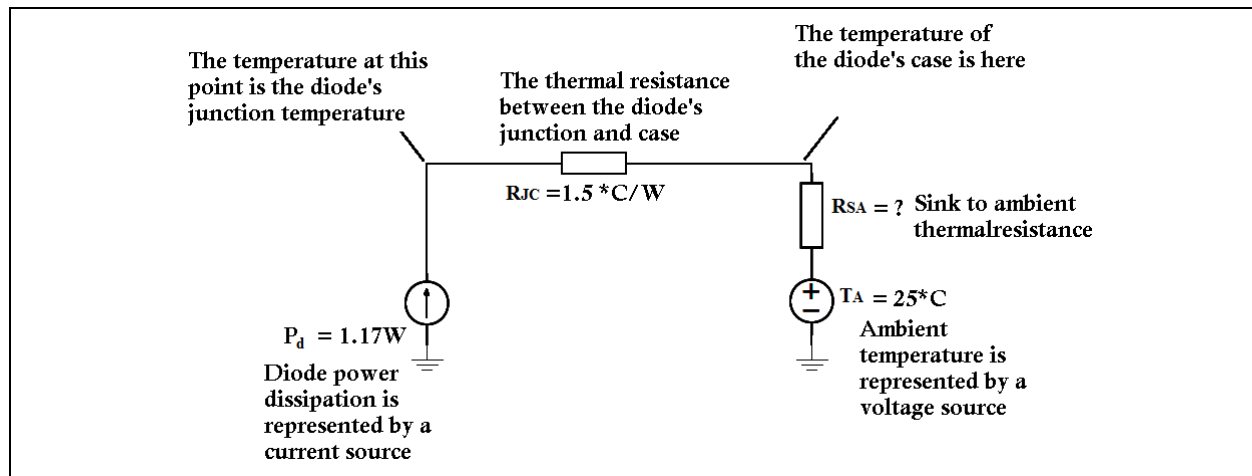
With this analogy used to the output diode, as an example, calculate what heat sink is needed to ensure the junction of the diode does not overheat. The ambient temperature used as example is 25°C, and the maximum T_j allowed is 150°C, while the junction per case thermal resistance is of 1.5°C/W.

The forward drop of this diode is 0.65V and the average current flowing of 1.8A, which gives an average power dissipation of 1.17W. [Figure 82](#) helps depict the analogical circuit.

TABLE 3: ELECTRICAL AND THERMAL ANALOGY

	Basic Element	Flow of Element	What Pushes the Element	What Resists the Flow	Storage of the Element
Electrical	Charge (Coulombs)	Current (Coulombs/second)	Voltage Difference (Joules/Coulomb)	Resistance (Ohm)	Capacitance (Farads or Coulombs/V)
Thermal	Thermal Energy or Heat (Joules)	Power (Joules/second or Watts)	Temperature Difference (°C)	Thermal Resistance (°C/W)	Heat Capacity (Joules/°C)

FIGURE 82: THERMAL CIRCUIT OF THE OUTPUT DIODE



The diode junction temperature is computed and using Ohm's law (see [Equation 62](#)).

EQUATION 62: DIODE JUNCTION TEMPERATURE EQUATION

$$T_J = T_A + P_D(R_{SA} + R_{JC})$$

$$R_{SA} = \left[\frac{(T_J - T_A)}{P_D} \right] - R_{JC} = \left[\frac{(150 - 25)}{1.17} \right] - 1.5 = 105 \text{ } ^\circ\text{C/W}$$

With this analogy, the maximum ambient temperature that the diode can function with can be calculated for a given sink thermal resistance and so on, if one centimeter square of one ounce copper ($R_{SA} = 71^\circ\text{C/W}$) is used as example while the case temperature can be calculated, as shown in [Equation 63](#).

EQUATION 63: CASE TEMPERATURE EQUATION

$$T_{CASE} = T_A + P_D R_{SA} = 25 + 1.17 \cdot 71 = 105 \text{ } ^\circ\text{C/W}$$

The useful thing to know is to use the manufacturer's data sheet in order to implement the analogical thermal circuit and calculate the needed heat sink or the maximum ambient temperature that the system will work without thermal failure.

Since a sink of 105°C/W thermal resistance on the diode has been previously decided, so that the diode will not fail, and since one centimeter square of one ounce copper has the thermal resistance of $R_{SA} = 71^\circ\text{C/W}$, the PCB contains 1.7 cm^2 of copper and resulted in $R_{SA} = 42^\circ\text{C/W}$, enabling thus the diode to work to a maximum ambient temperature calculated using [Equation 64](#).

EQUATION 64: AMBIENT TEMPERATURE EQUATION

$$T_A = T_J - P_D(R_{SA} + R_{JC}) = 150 - 1.17(42 + 1.5) = 99 \text{ } ^\circ\text{C}$$

Using this method, the dimensions of the sinks for all the endangered components can be established.

For non-PCB sinks, off-the-shelf heat sinks can be used since they have their resistance provided by the manufacturer or use online sink calculators that are provided by manufacturers such as Aavid Thermalloy. The manufacturers will also provide information as to how low the thermal resistance can go if a certain air flow is applied on the heat sink. For more information, see [13] in [Section “References”](#).

RESULTS

Stability Bode Plots

To test the stability of the build SMPS, a Frequency Response Network Analyzer is used as described in the [Section “Feedback and Compensation Circuit”](#).

[Figure 83](#) depicts the stability test results when the circuit is at 120% load with the input 110 VDC. The resulting gain margin is 60 degrees and gain margin 12 dB. This result follows the established goal of gain margin >10 dB and Phase margin >45 degrees with just the components values calculated at the beginning, but more tweaks can be made to the compensation values to improve the stability of the system.

These results prove the system is stable, at full load and under various input conditions.

[Table 4](#) shows the results for other Input-Output conditions, which reinforce the argument that the system is stable.

FIGURE 83: MEASURED LOOP GAIN AND PHASE OF 110 VOLTS

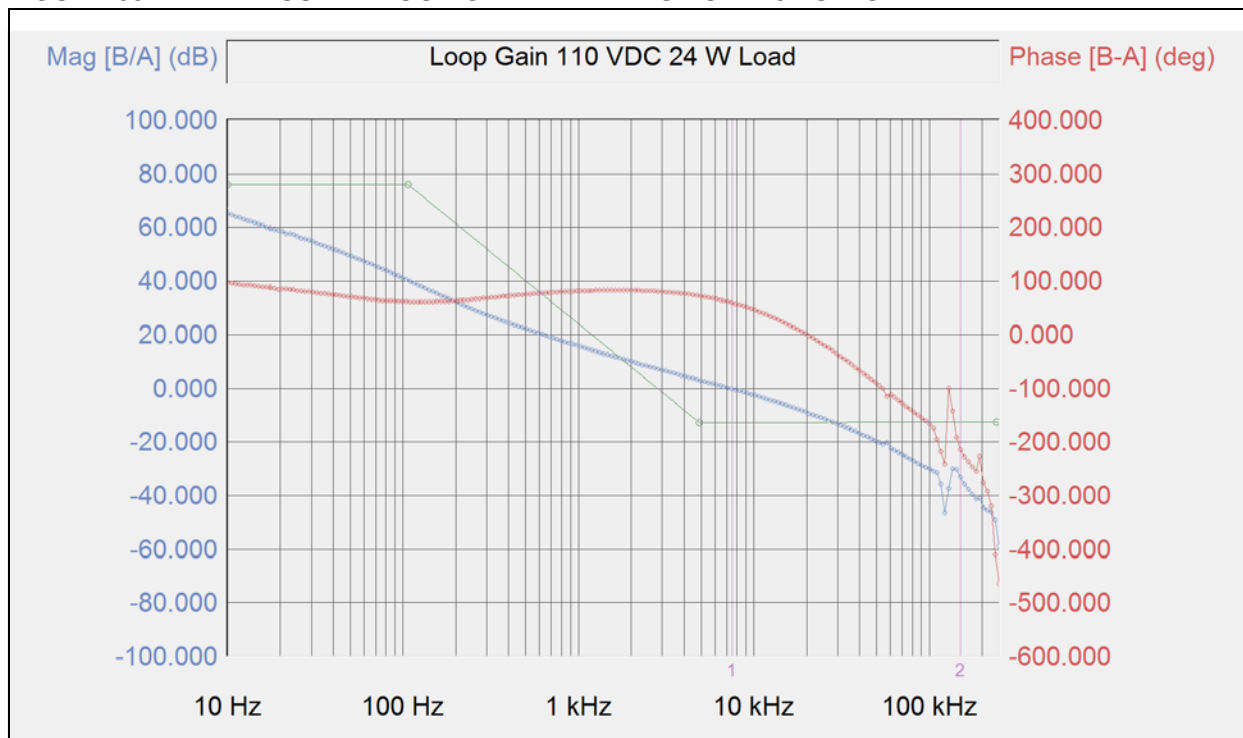


TABLE 4: MEASURED LOOP GAIN AND PHASE

P _{OUT}	2W	20W
V _{IN} = 90 VAC	$\Phi_M = 58^\circ$; $f_X = 5$ kHz; $G_M = 17$ dB	$\Phi_M = 59^\circ$; $f_X = 7.3$ kHz; $G_M = 12$ dB
V _{IN} = 120 VAC	$\Phi_M = 58^\circ$; $f_X = 5.5$ kHz; $G_M = 18$ dB	$\Phi_M = 60^\circ$; $f_X = 7.5$ kHz; $G_M = 12.5$ dB
V _{IN} = 185 VAC	$\Phi_M = 57^\circ$; $f_X = 5.4$ kHz; $G_M = 17$ dB	$\Phi_M = 60^\circ$; $f_X = 7.5$ kHz; $G_M = 13$ dB
V _{IN} = 210 VAC	$\Phi_M = 60^\circ$; $f_X = 5.7$ kHz; $G_M = 18$ dB	$\Phi_M = 61^\circ$; $f_X = 7.6$ kHz; $G_M = 13$ dB

Transient Operation

To make sure the design works correctly even when the load or input voltage is suddenly changed, a transient test has to be performed. The test setup is depicted by [Figure 84](#). Switch no.1 is positioned at the output and will change the current drawn by changing the load value. The result of the low load to high load can be seen in [Figure 85](#). The output voltage does not suffer of high spikes during this transition but remains stable, considering the current difference of 1.3A.

In [Figure 86](#), the output current is suddenly changed from 1.45A to 0.18A, and as a result, the output voltage is not affected by spikes or abrupt changes. [Figure 87](#) depicts the output voltage during an input voltage change, and only the noise created by the switching device can be noticed. The voltage remains constant during that period.

FIGURE 84: TRANSIENT TEST SETUP TO CHANGE INPUT VOLTAGE AND OUTPUT LOAD

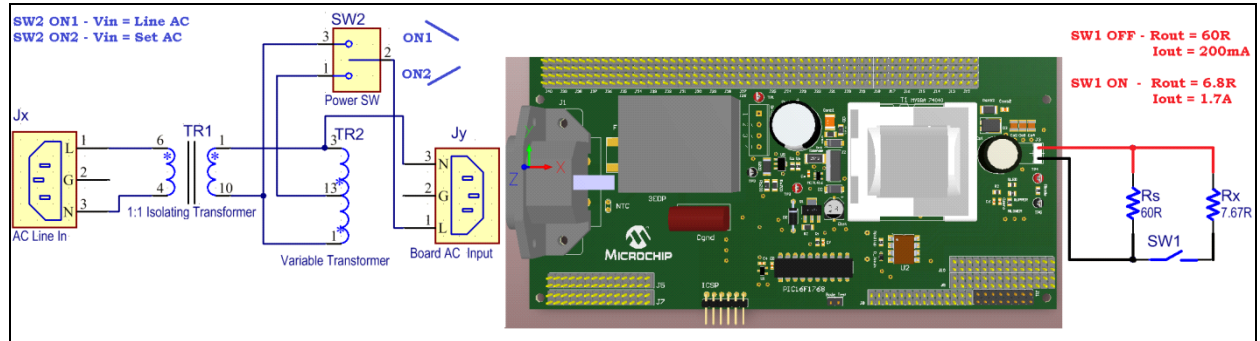


FIGURE 85: LOAD RISE

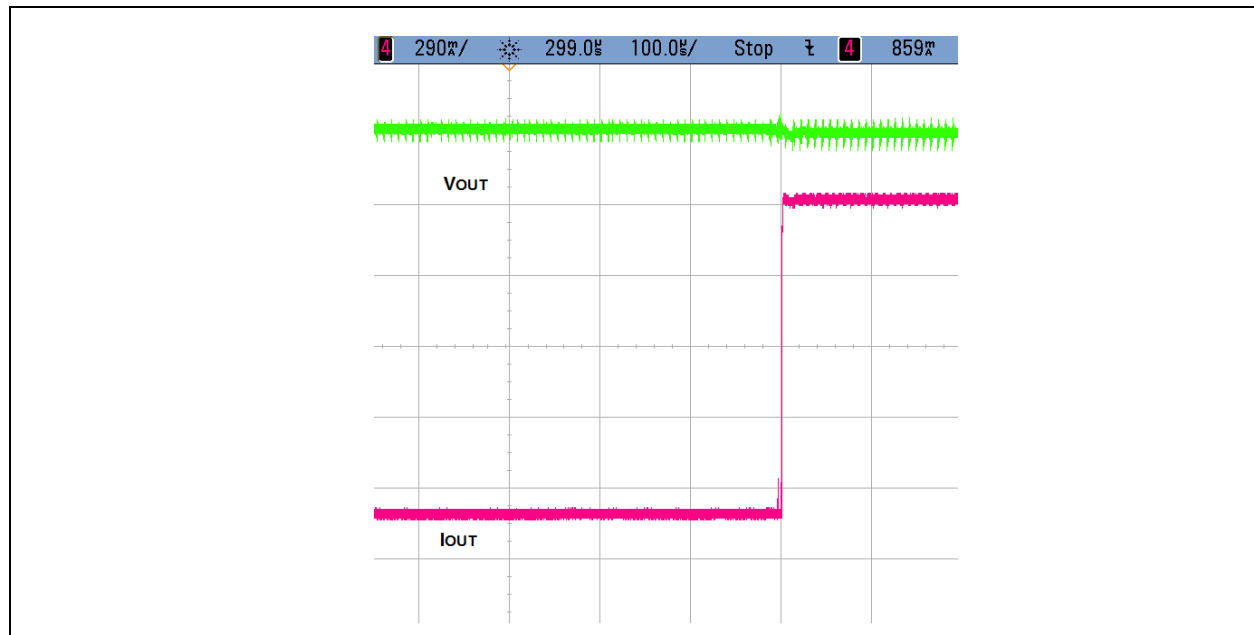


FIGURE 86: LOAD DUMP

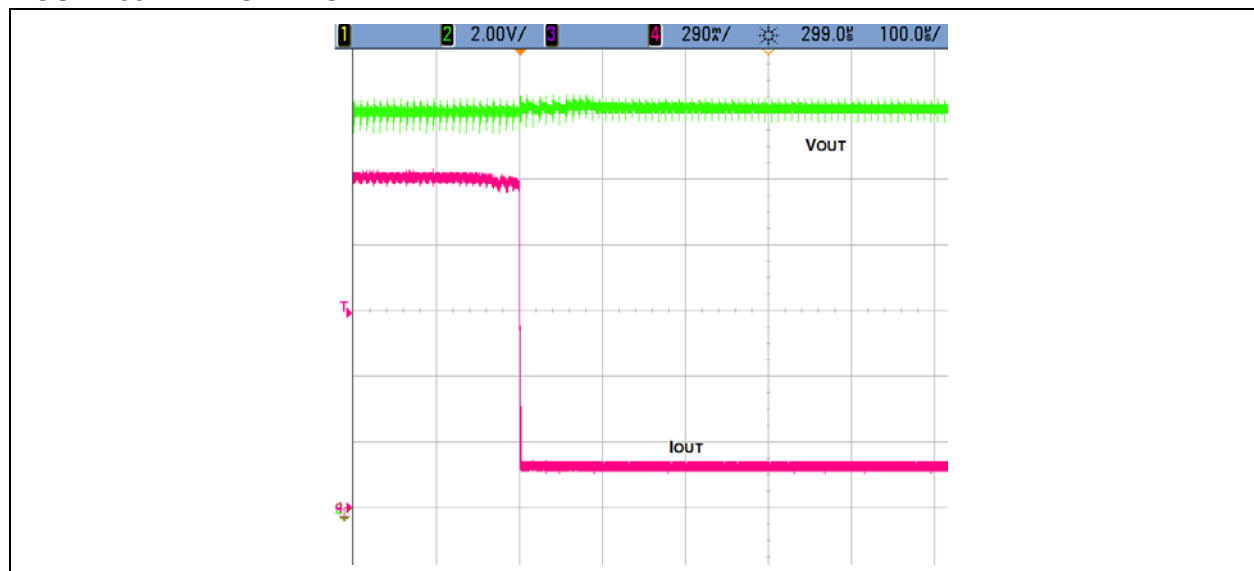
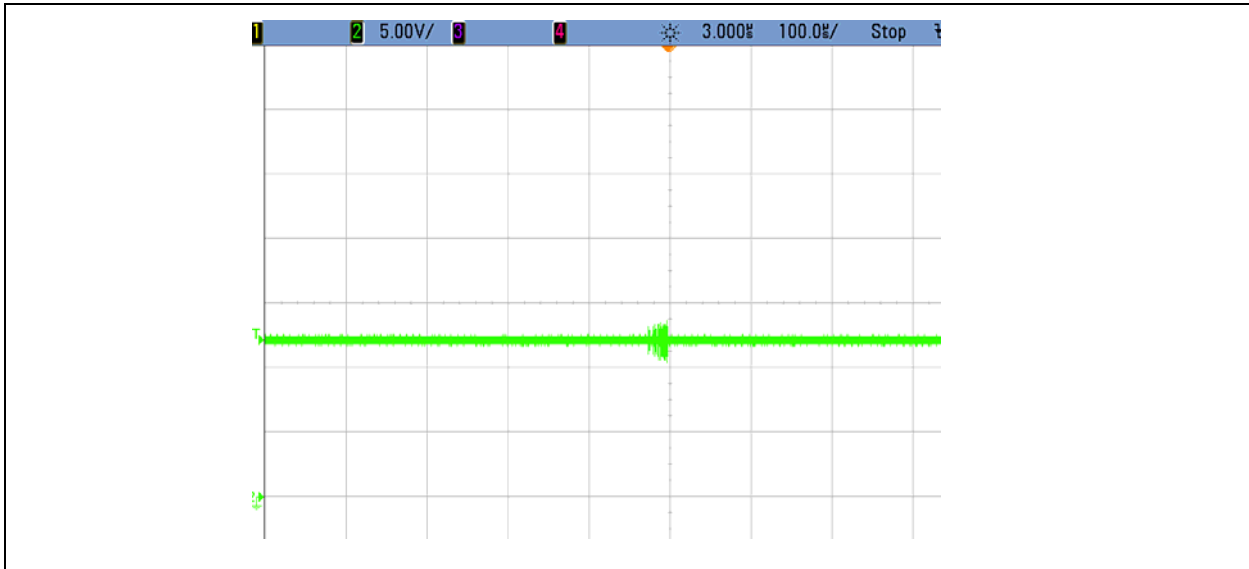
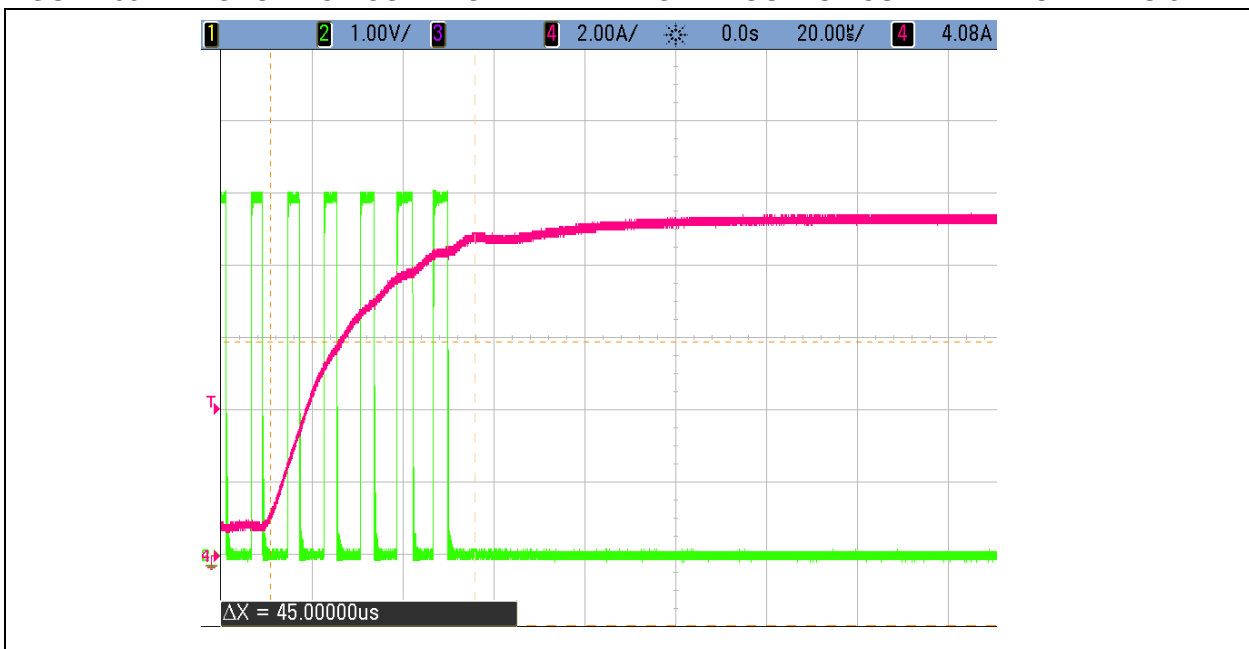


FIGURE 87: V_{out} DURING INPUT VOLTAGE SWITCH

Short-Circuit Operation

The short circuit tests were made using an electronic load and a high-power resistor, as depicted in Figure 88. The period of time from the beginning of the short circuit until its detection by the circuit and cease is of approximately 45 μ s. The load current was suddenly changed from 1A to 9A and the control output was monitored in the same time. Taking into account that the detection is made from the primary isolated side of the flyback, the response is quite fast. The response is almost the same in all input conditions, meaning that if the input voltages change, the short-circuit detection time is the same.

FIGURE 88: SHORT-CIRCUIT TEST THAT TAKES THE OUTPUT CURRENT FROM 1A TO 9A

The implementation of the limited three retries is depicted in [Figure 89](#), while [Figure 90](#) displays the plot of the unlimited retries working. These pictures show how the control PWM signal is stopped during a short-circuit condition, and as the short is still present, the control tries to restart in order to verify if the short-circuit condition is any longer valid.

[Figure 91](#) evinces a short-circuit condition that appears for a limited period of time. At the third retry, the circuit starts to work normally again.

FIGURE 89: COG_OUT PLOT DURING SHORT CIRCUIT WITH THE LIMITED RETRIES OPTION ACTIVATED

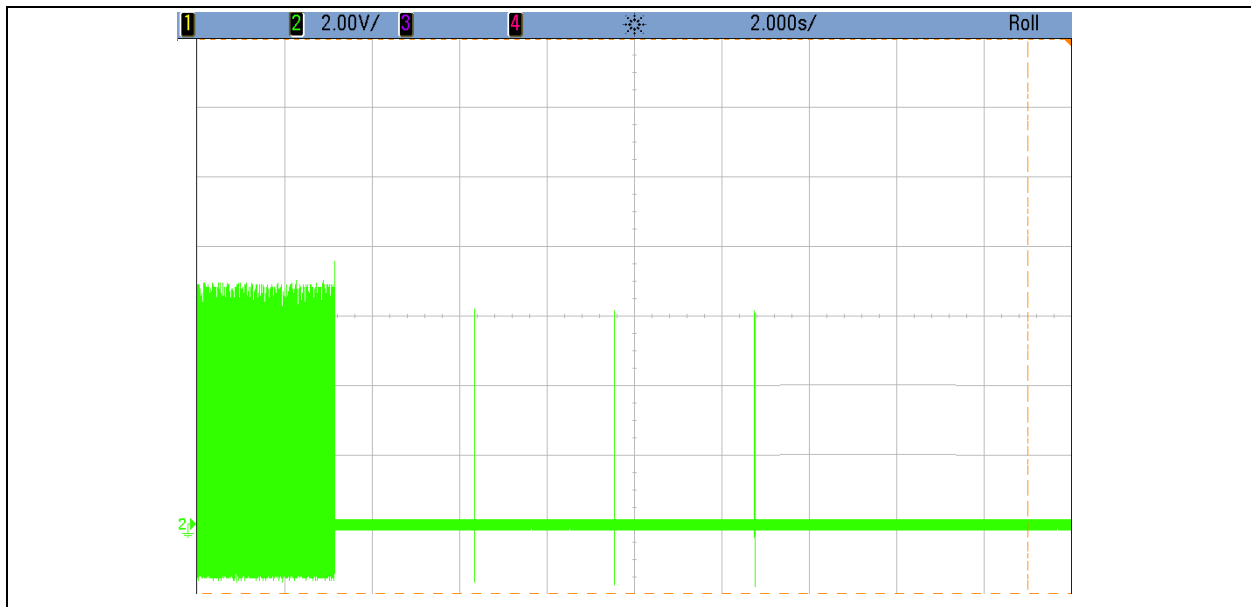


FIGURE 90: COG_OUT PLOT DURING SHORT CIRCUIT WITH THE UNLIMITED RETRIES OPTION ACTIVATED

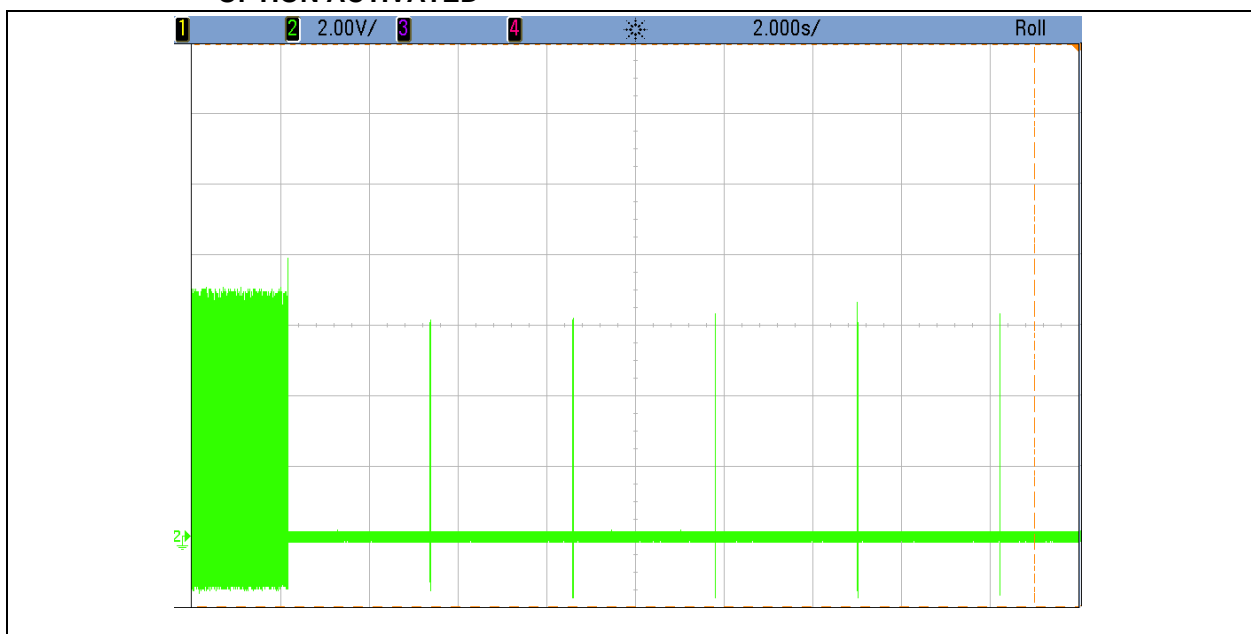
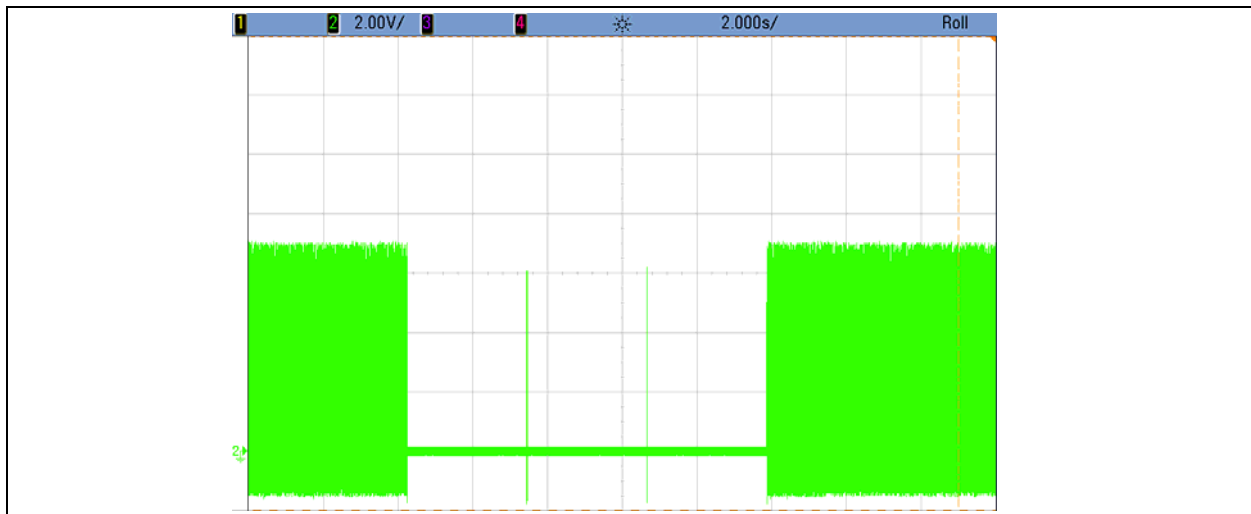


FIGURE 91: COG_OUT PLOT DURING A LIMITED SHORT CIRCUIT WITH THE UNLIMITED RETRIES OPTION ACTIVATED



Light Load or Open-Circuit Operation

As described in the previous chapters, the circuit is designed so when no power is drawn from the output or when there is an open-circuit condition, the 12V level will still be maintained at the output. [Figure 92](#) shows the switching-control signal or the output of the COG when the input of the SMPS is of 90V, and there is no load present (open circuit), and as it can be seen, the duty cycle is at minimum possible limitation and some pulses are skipped in order to maintain the output stable.

This happens because in an open-circuit condition, the system works as a Voltage mode controlled system instead of current-mode controlled, but as soon as the load starts to draw power, the current-mode will start to work again. [Figure 93](#) depicts the same circuit without the load present, but this time the input voltage is of 210V, and more pulses are skipped to ensure a constant 12V output.

FIGURE 92: COG_OUT SIGNAL AT 90V AND OPEN-CIRCUIT CONDITION

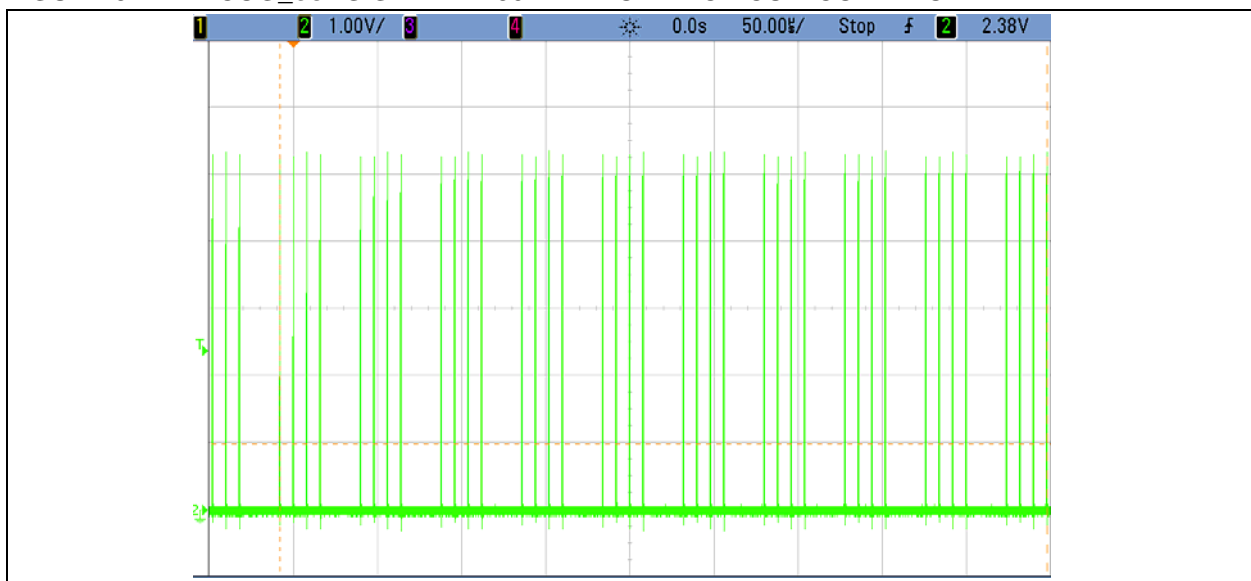
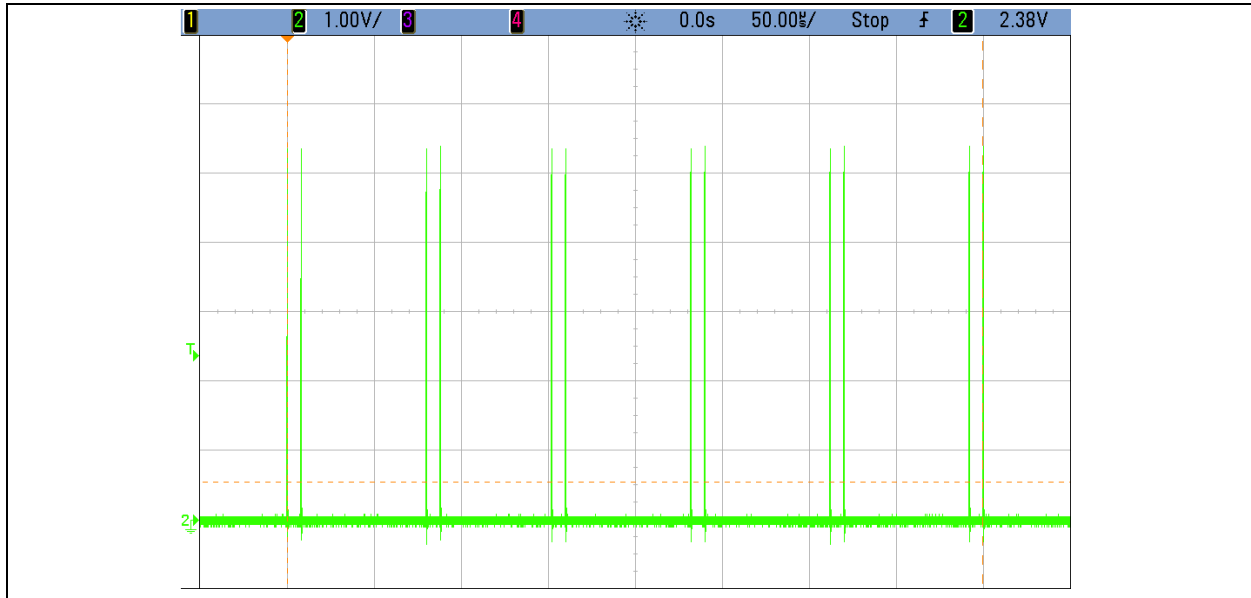


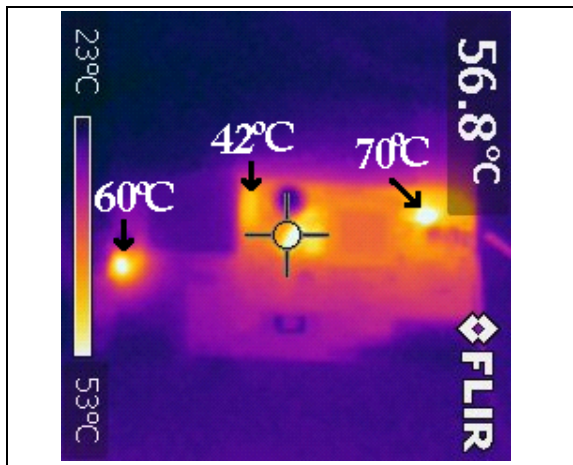
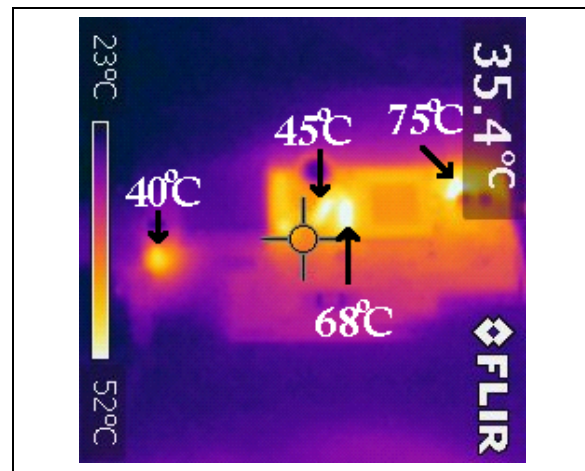
FIGURE 93: COG_OUT SIGNAL AT 210V INPUT AND OPEN-CIRCUIT CONDITION

Temperature Captures

The board temperature was measured during full-load conditions with different input levels, as depicted in [Figure 94](#) (90 VAC input voltage) and in [Figure 95](#) (265 VAC input voltage).

In [Figure 94](#), the NTC:60°C, Bridge:42°C, Sense Resistor:57°C, MOSFET 50°C and Output diode:70°C are distinguished.

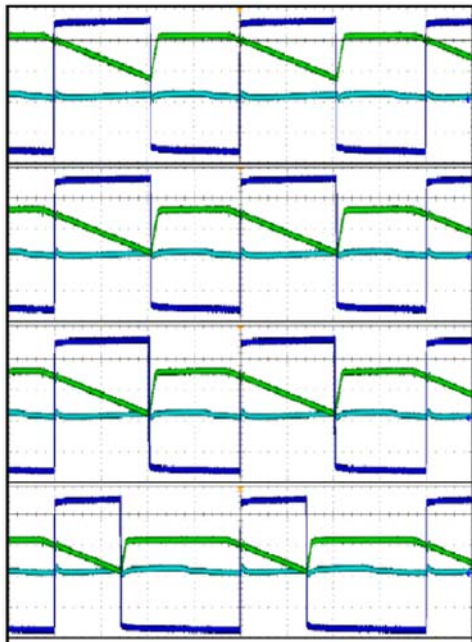
These results suggest that the NTC and Sense Resistor do not need a cooling system if the resistor value is lowered, but the MOSFET and Output Diode need a cooling system if the board is to work at ambient temperatures higher than 75°C.

FIGURE 94: TEMPERATURE MEASUREMENT OF THE BOARD VIN:90 VAC Pout 21W**FIGURE 95: TEMPERATURE MEASUREMENT OF THE BOARD VIN:265 VAC Pout 21W**

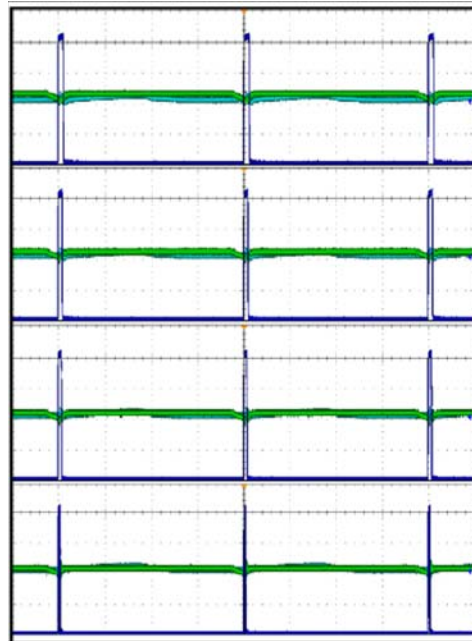
Slope Compensation Influence on Duty Cycle Accuracy Results

Experimental results may vary depending if the Blanking is activated, or the current-sensed signal is filtered or not.

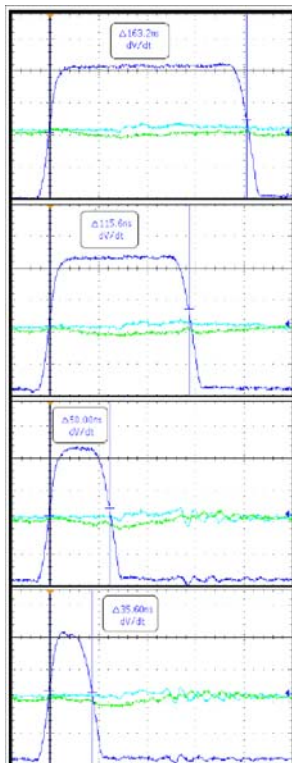
FIGURE 96: HIGH – LOW DUTY CYCLE



High Duty Cycle: Clean entering into regulation.



Low Duty Cycle: Clean regulation into pulse skipping



Low Duty Cycle: Resolution

Efficiency Calculations

FIGURE 97: EFFICIENCY CHART

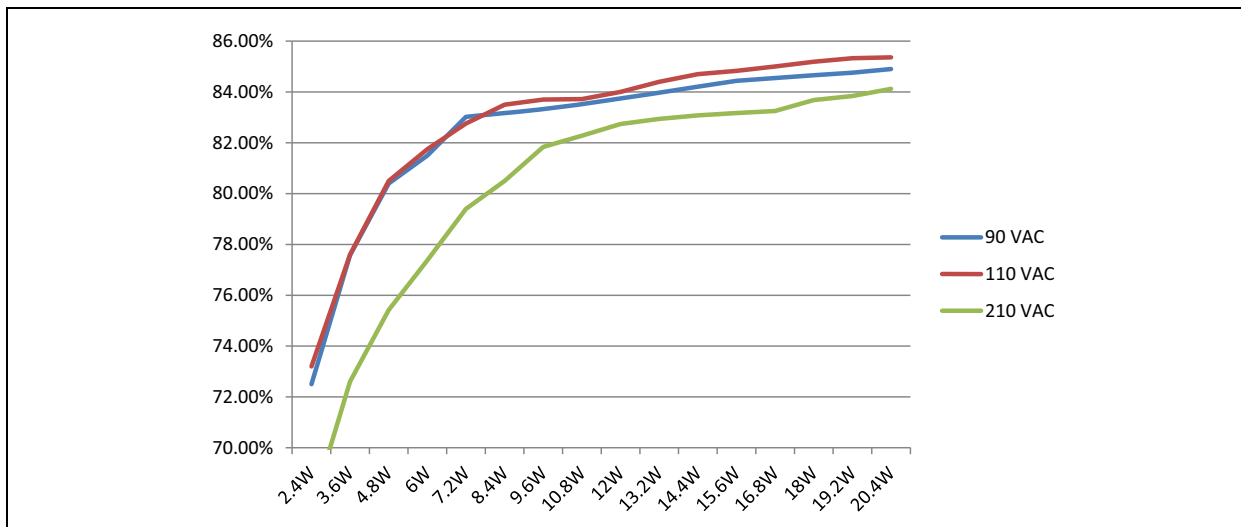


Figure 97 depicts the efficiency measurements of the system for different input conditions.

CONCLUSIONS

This application note familiarizes the reader with the Core Independent Peripherals capable of implementing the logic necessary for a SMPS. It shows some of the control capabilities that they provide over the SMPS behavior and the advantages of having monitoring capabilities in such an application. This document demonstrates that the use of automated functions can make the SMPS safer, smarter and more versatile.

This application note offers details regarding the implementation of a 20W flyback SMPS using the PIC16F1769 as a logic controller.

Enough information is provided for readers unfamiliar with the procedures of flyback topology, transformer, snubber and compensation design, to start a SMPS project and explore the CIPs' capabilities.

The second part provides basic information about what CIPs are and how to use them to implement the current-mode control logic for the flyback, or for any other logic; how to use MCC to configure the part without writing actual code and how to define and use the capabilities of the CIPs for control, monitoring and automated functions to implement a SMPS controller with smart adaptable features. The application note shows that the intended use of the MCU with CIPs in a SMPS application is to add more features, control and adaptability. These features were previously available only with a full digital controller that was limited to designers with skills in code programming; but also providing the advantages of pure analog components. The communications capabilities and more advanced automated functions such as battery charging are not covered in this document. The correct functionality is explained in the [Section "Results"](#) so the reader can understand the use of CIPs in SMPS applications without the fear of failure of the MCU that controls the converter.

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