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Thursday, May 5, 2016

DRV2700 Piezo Driver

DRV2700 is a single chip Piezo driver which is 4 mm x 4 mm x 0.9 mm in size. It can be used in 100 V boost or 1 kV flyback configuration. Supply voltage is 3 V - 5.5 V. In this article, evaluation of DRV2700EVM module is discussed.

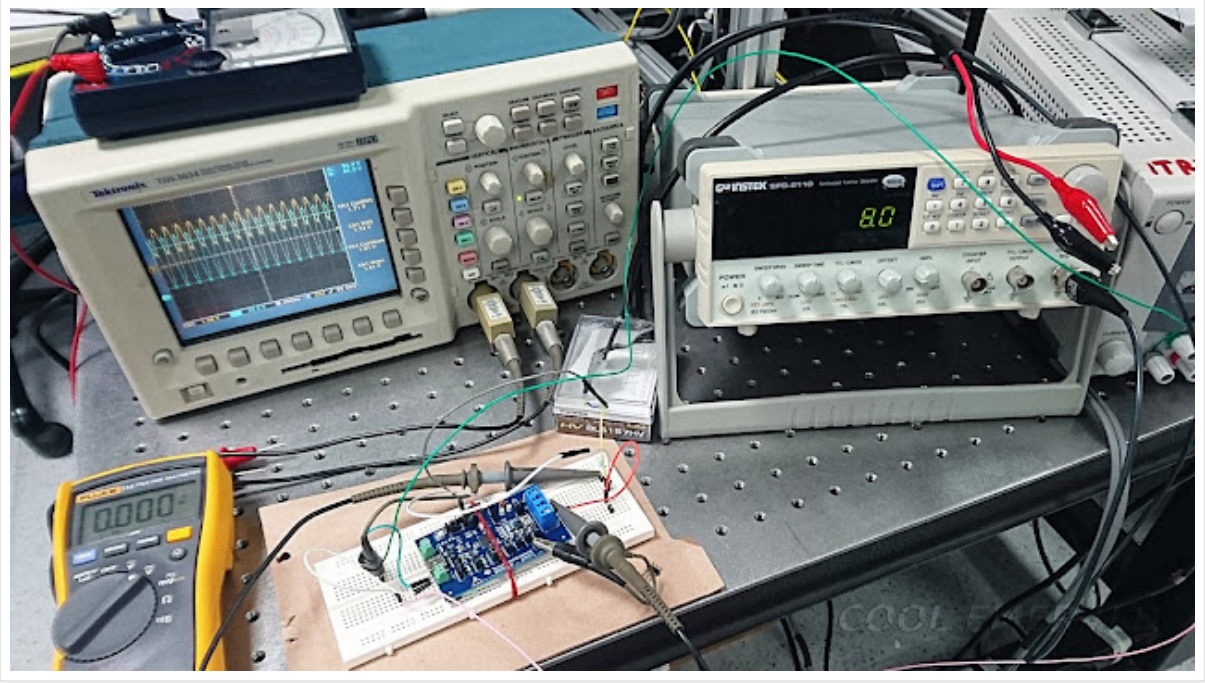


Figure. Testing DRV2700.

The following figure illustrate boost + amplifier configuration of DRV2700.

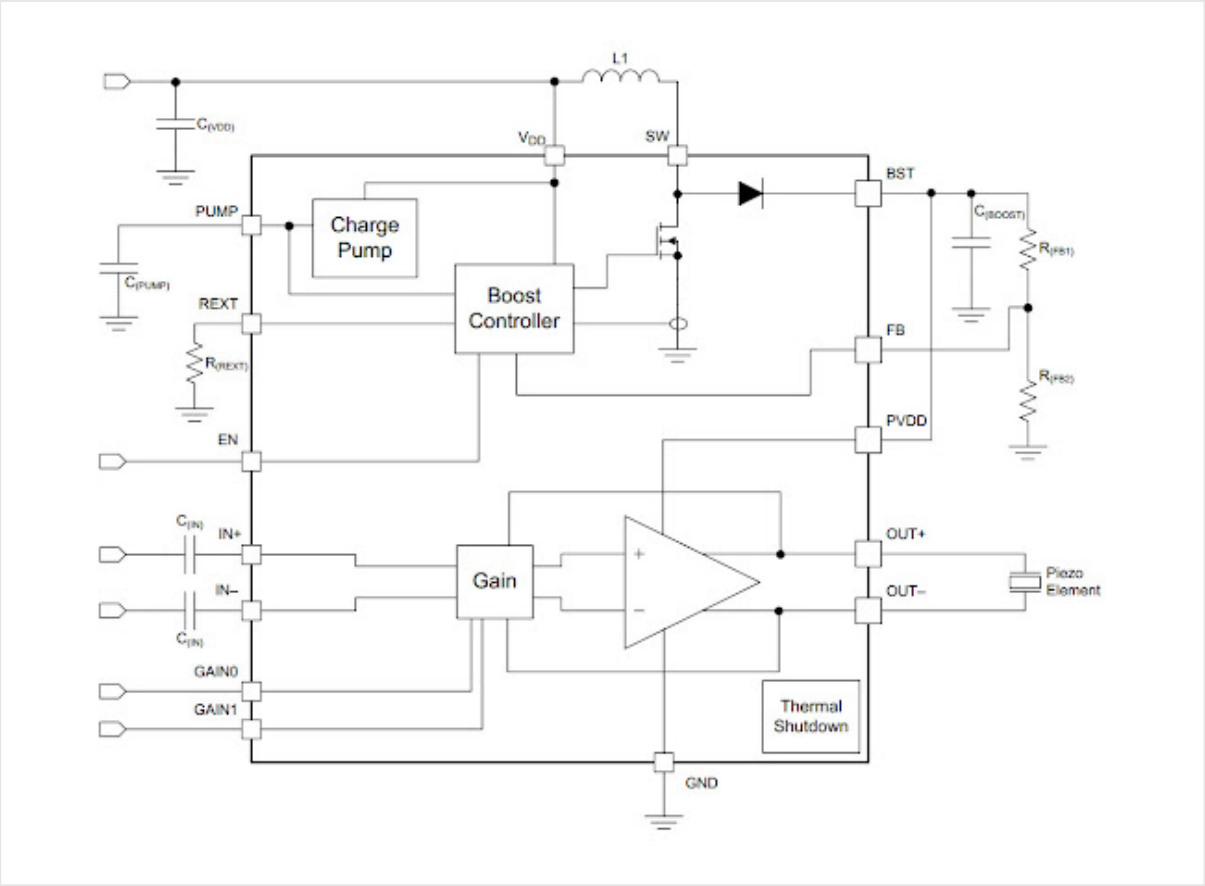


Figure. DRV2700 boost + amplifier configuration.

Where BST is boost output voltage. BST is used as supply voltage (PVDD) for the amplifier. EN is chip enable. FB is boost feedback used together with R_{FB1} and R_{FB2} to produce required boost voltage. V_{FB} = 1.3 V and,the relation between R_{FB1}, R_{FB2}, and V_{BST} in boost + amplifier configuration is as follow.

$$V_{BST} = V_{FB}\left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

For example, if we want V_{BST} of 105 V, we can use R_{FB1} = 806 kΩ and R_{FB2} = 10.1 kΩ. When R_{FB1} = 806 kΩ and R_{FB2} = 16.45 kΩ, V_{BST} will be 65 V. Jumper settings and V_{BST} table for Evaluation module DRV2700EVM is shown below.

BST	R_{EQ}	JP2	JP3	JP4
23 V	50 kΩ	Open	Open	Open
37 V	30.8 kΩ	Open	Open	Closed
45 V	25 kΩ	Open	Closed	Open
58 V	19.0 kΩ	Open	Closed	Closed
70 V	15.7 kΩ	Closed	Open	Open
83 V	13.2 kΩ	Closed	Open	Closed
91 V	12 kΩ	Closed	Closed	Open
105 V	10.4 kΩ	Closed	Closed	Closed

Figure. BST Setting Based on the Jumper Configuration.

GAIN0 and GAIN1 pins define the gain of amplifier which is ($\frac{OUT^+ - OUT^-}{IN^+ - IN^-}$).

Table. Amplifier gain

GAIN[1:0]	G_{dB}	G_{AMP}
00	28.8	27.54
01	34.8	54.95
10	38.4	83.18
11	40.7	108.4

The performance of DRV2700 largely depends on the choice of inductor also. The recommended values for the inductor is between 3.3 µH and 22 µH. In general, the smaller the inductance, the higher the saturation current limit. When a large inductance value is used, DRV2700 will automatically switch to lower switching frequency which gives smaller switching losses. On the other hand, it will has higher parasitic inductor losses. Typically, smaller inductance values are used to obtain higher current limit. In this evaluation module, 4.7 µH, 2.7 A inductor is used.

REXT is used to limit boost current by connecting a resistor to ground. The value of resistor should be between 6 kΩ and 35 kΩ. The relationship between Current limit (I_{LIM}) and resistor (R_{EXT}) is shown below, where K=10500, V_{REF}=1.35 V, and R_{INT}=60 Ω.

$$R_{EXT} = K.\frac{V_{REF}}{I_{LIM}} - R_{INT}$$

For example, when R_{EXT}=6.04 kΩ, I_{LIM} wil be 2.32 A. To obtain I_{LIM} = 1 A, the value of R_{EXT} should be 14 kΩ.

The minimum value of boost capacitor should be 50 nf. X7R type 100 nF capacitor is recommended. It is found that the lower the boost voltage, the better the efficiency. The efficiency at 80 V is around 50 % as shown in the following charts.

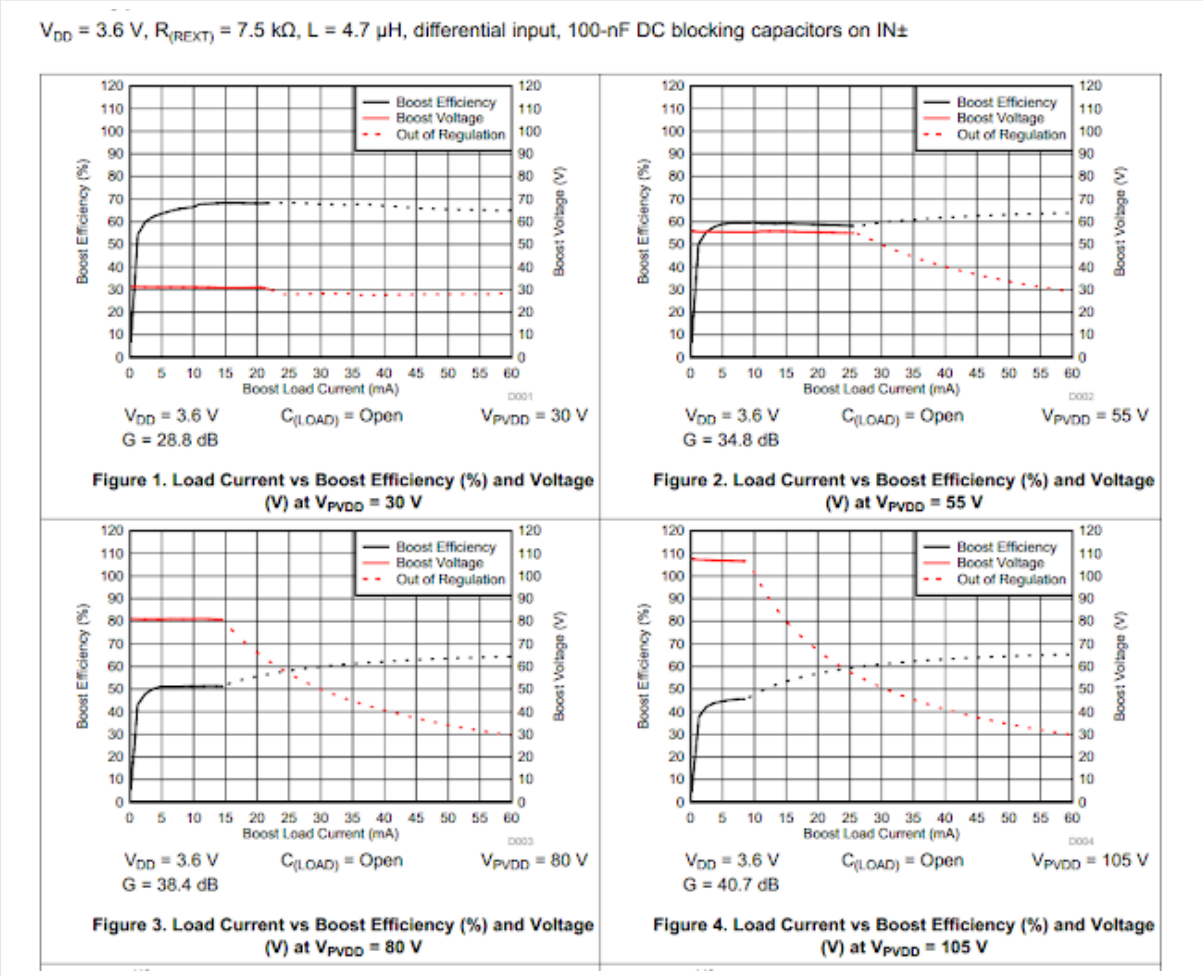


Figure 1. Load Current vs Boost Efficiency (%) and Voltage (V) at V_{PVDD} = 30 V

Figure 2. Load Current vs Boost Efficiency (%) and Voltage (V) at V_{PVDD} = 55 V

Figure 3. Load Current vs Boost Efficiency (%) and Voltage (V) at V_{PVDD} = 80 V

Figure 4. Load Current vs Boost Efficiency (%) and Voltage (V) at V_{PVDD} = 105 V

Figure. Typical characteristics.

A system example which uses DC coupled input is shown below.

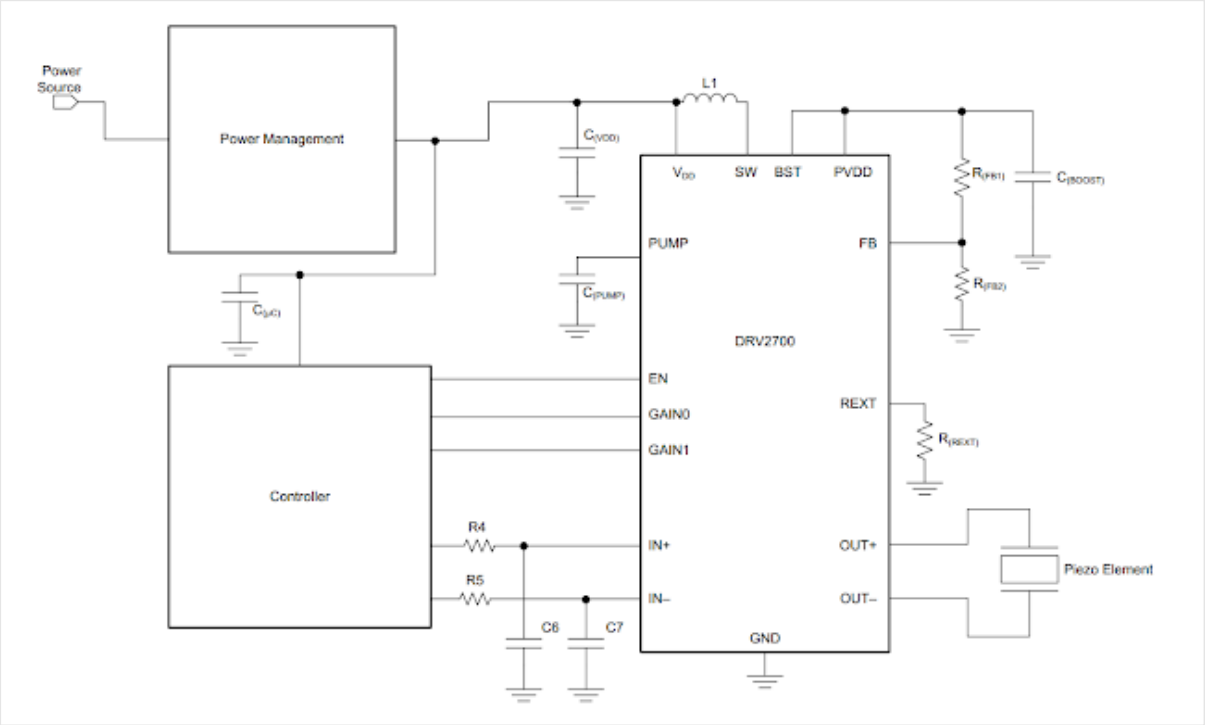


Figure. DC coupled DAC input configuration.

A piezo element can be modeled as a capacitor. Then, the peak value for its load current - I_{peak} can be calculated as follow.

$$I_p = 2.\pi.f.C.V_p$$

If you want the value of peak supply current for DRV2700, I_{DD}, the voltage ratio, and efficiency - μ can be used to calculate as follow.

$$I_{DD} = 2.\pi.f.C.V_p.\frac{V_{BST}}{V_{DD}.\mu}$$

For example, Stack Multilayer Piezo Actuator, PICMA P-885.91 (Physik Instrumente, Karlsruhe, Germany) has capacitance 3.1 μF and travel range 32 μm. For V_p= 50 V and frequency 10 Hz, I_{peak} is 9.7 mA. Using V_{BST}= 105 V, V_{DD}= 3.3 V, and efficiency μ=45%, peak I_{DD} is obtained as 689 mA.

As an another example, Noliac plate stack actuator NAC2003-H50-A01 has capacitance 24620 nF and travel range 72 μm. For V_p= 30 V and frequency 10 Hz, I_{peak} is 46.4 mA. Using V_{BST}= 65 V, V_{DD}= 3.3 V, and efficiency μ=55%, peak I_{DD} will be 1.66 A.

DRV2700 is compared against DRV8662 which is used in PDu100D. For Piezo actuator with large capacitive load, DRV2700 is said to be more suitable.

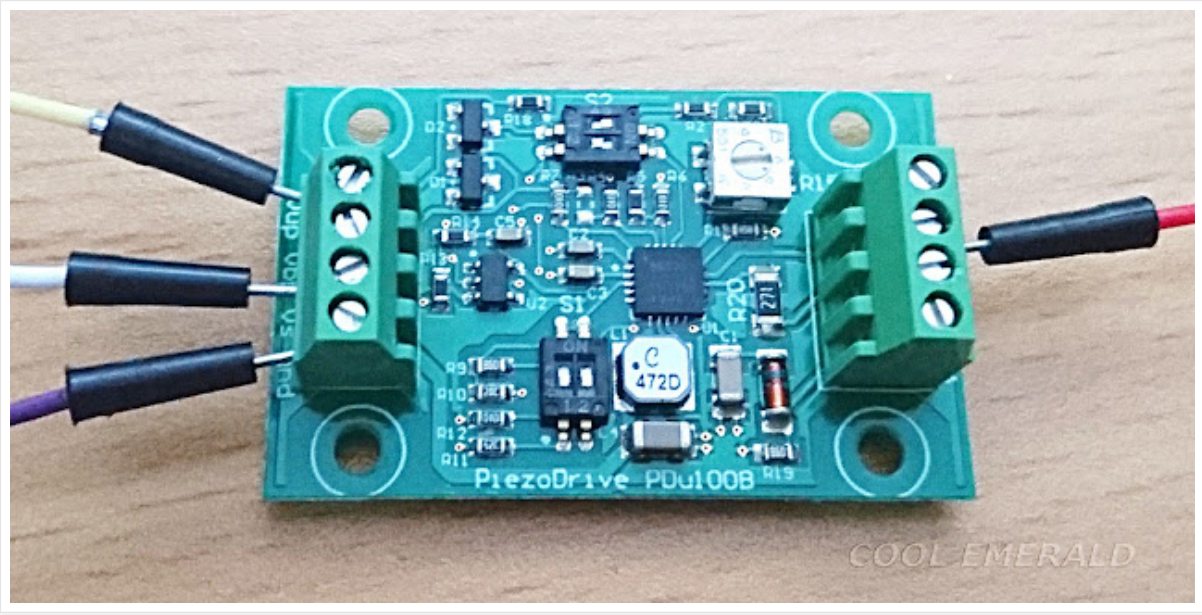


Figure. pDu100B

To reduce noise at output voltage, output resistor R_o is normally used to connect piezo element in series. Bandwidth is same as that of first order RC low pass filter.

$$f_c = \frac{1}{2.\pi.R_o.C}$$

The result of comparison between these two piezo drivers is shown below.

Table. Driving NAC2003-H50-A01, 25 µF with 60V peak to peak sinusoidal @ V_{BST}= 60 V, V_{DD}= 5 V, R_o= 1 kΩ

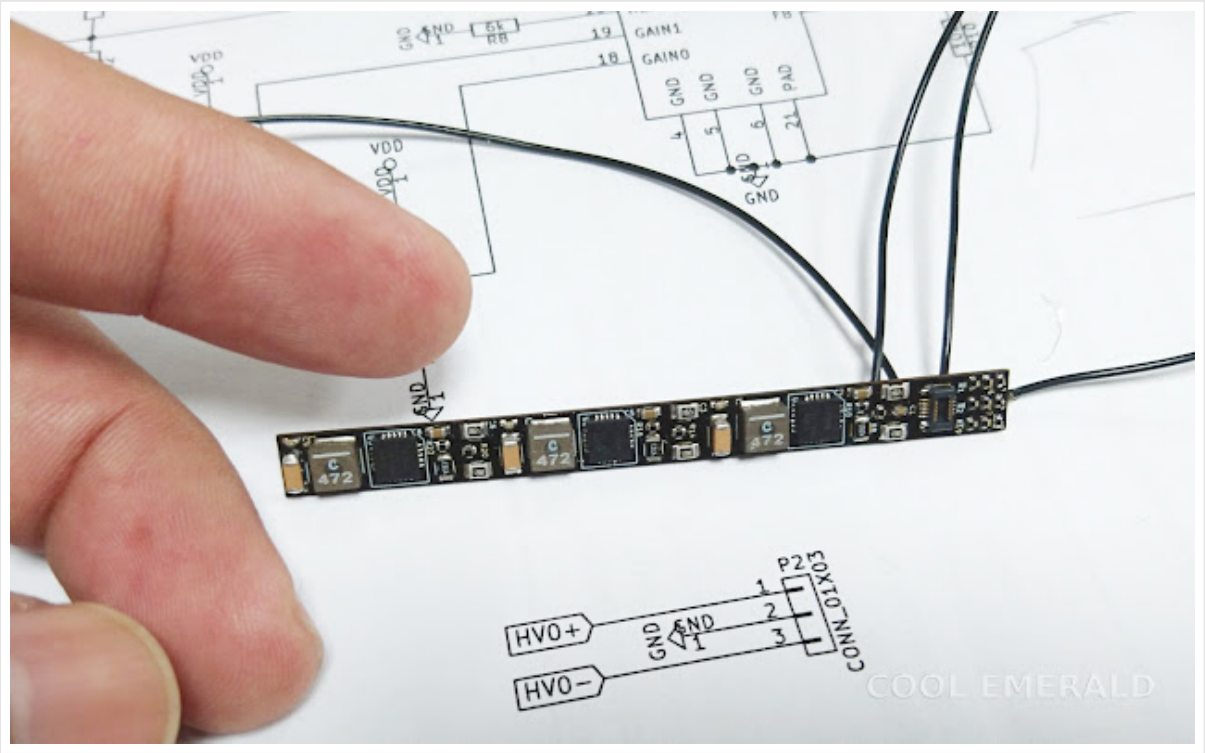
Driver	DC	1 Hz	10 Hz
DRV2700	13.5 mA	10 ~ 110 mA	170 ~ 250 mA
pDu100B	33 mA	30 ~ 130 mA	200 ~ 300 mA

Table. Driving PICMA P-885.91, 3 µF with 60V peak to peak sinusoidal @ V_{BST}= 100 V, V_{DD}= 5 V, R_o= 1 kΩ

Driver	DC	1 Hz	10 Hz
DRV2700	34 mA	32 ~ 57 mA	120 ~ 167 mA
pDu100B	73 mA	80 ~ 125 mA	160 ~ 220 mA

I have designed a 3 channel piezo driver which is shown in the following figure. It uses three

DRV2700. It is 4 layered PCB with only 6 mm x 69 mm in size.



Posted by Yan Naing Aye at Thursday, May 05, 2016

Labels: Amplifier, Driver, DRV2700, Electronics, Piezoelectric

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