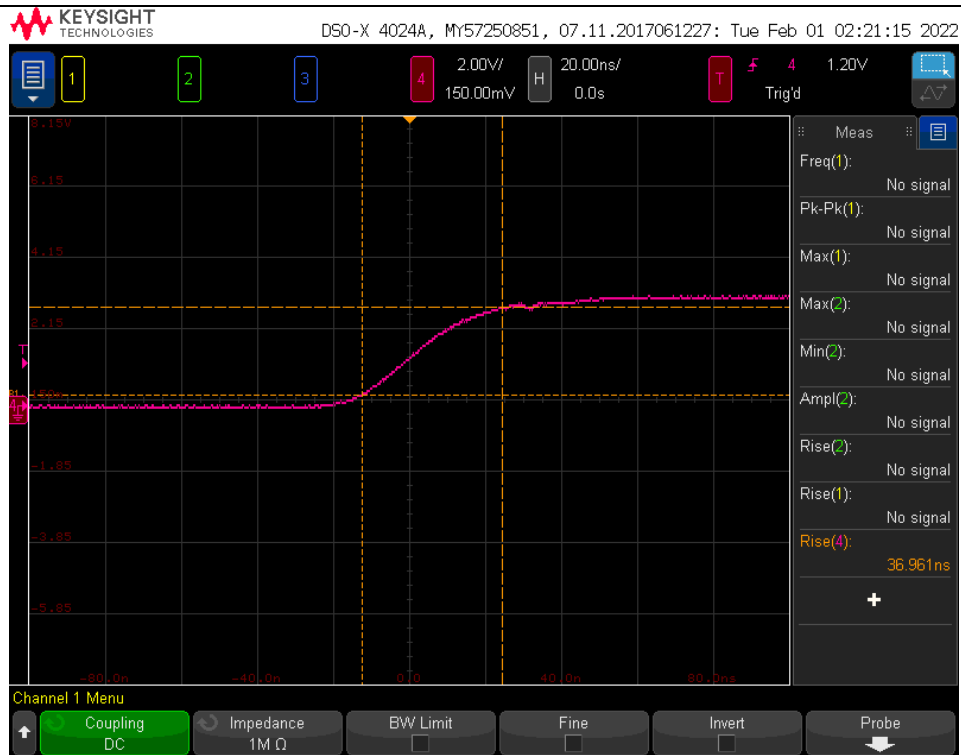


## Lab 6: Benefits of a continuous Ground plane, Pull-up resistors and proximity of Decoupling capacitor

- Rishab Shah

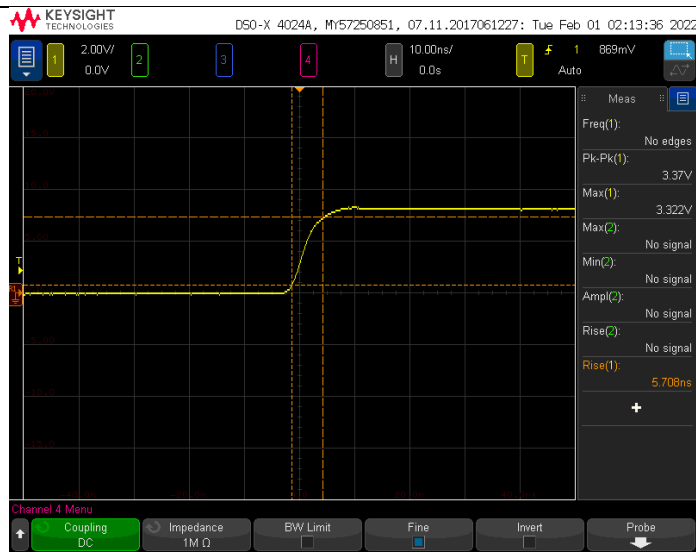
Q1) a) Rise time of the hex scope trigger output and the 555-timer output

### 555 Timer Rise time:

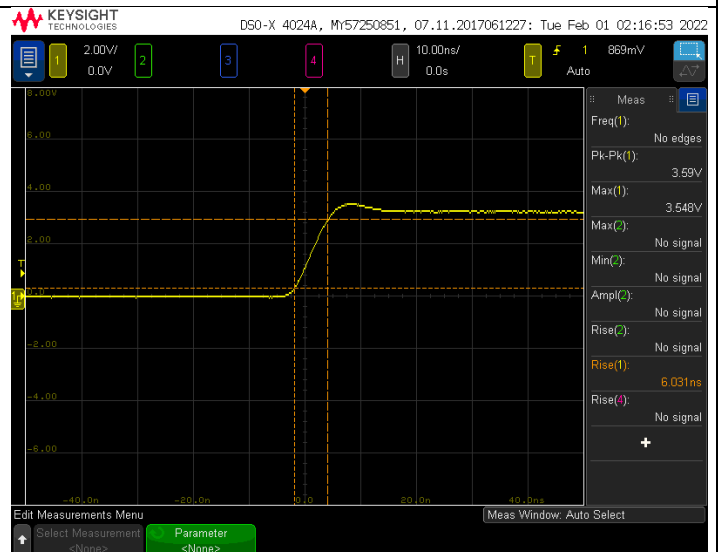


Rise Time = 36.961 nsec

### Hex Inverter Rise time:



Good Layout : Rise Time = 5.708 nsec

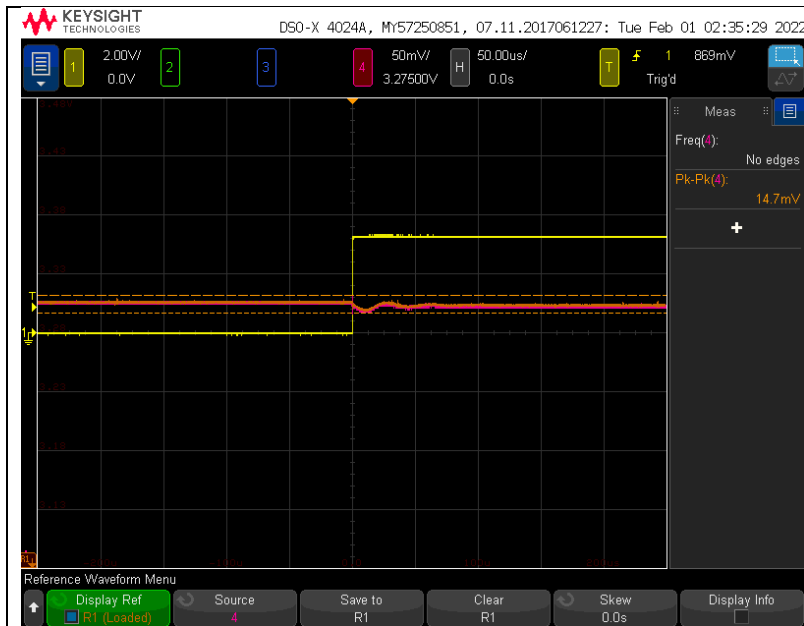


Bad Layout : Rise Time = 6.031 nsec

The rise time is negatively affected by 5.6% for Hex inverter

*From the images, it is found that a poor layout of Hex inverter negatively affects the rise time of the signal which has a negative impact for high-speed electronics as the rise time is more.*

Q1) b) *Q-hi outputs on good and bad layouts, and why they are different?*

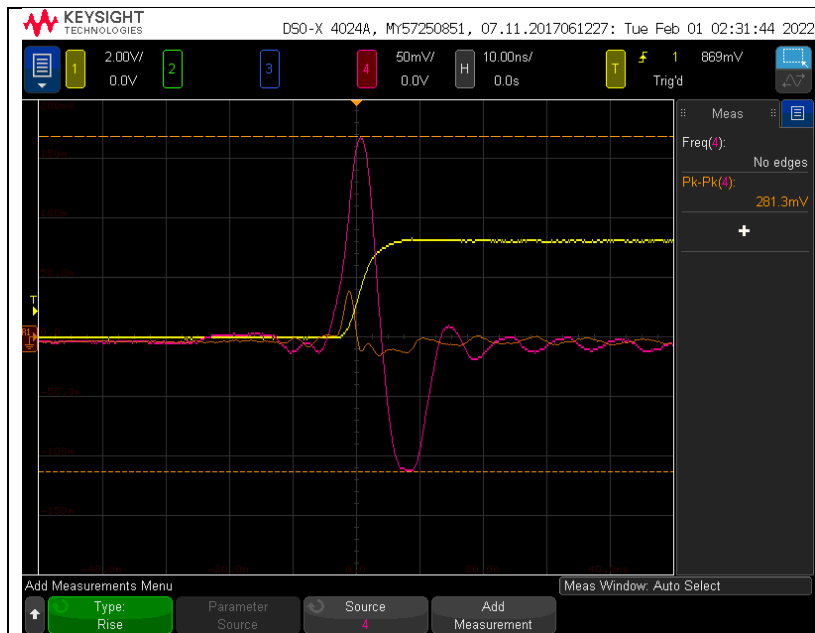


*Yellow = Output of the hex inverter circuit  
Orange = Reference s/w noise for GL = 10.5 mVpp  
Pink = s/w noise for BL = 14.7 mVpp*

*The noise contributed due to a Bad layout (BL) is more compared to good layout. It is due to the lack of common ground plane causing noise in the victim trace.*

This is used for measurement of switching noise on the power rail when the other I/O's switch.

Q1) c) *Q-low outputs on good and bad layouts, and why they are different?*



*Yellow = Output of the hex inverter circuit  
Orange = Reference s/w noise for GL = 53 mVpp  
Pink = s/w noise for BL = 281.3 mVpp*

*The noise contributed due to a Bad layout (BL) is more compared to good layout. It is due to the lack of common ground plane causing noise in the victim trace*

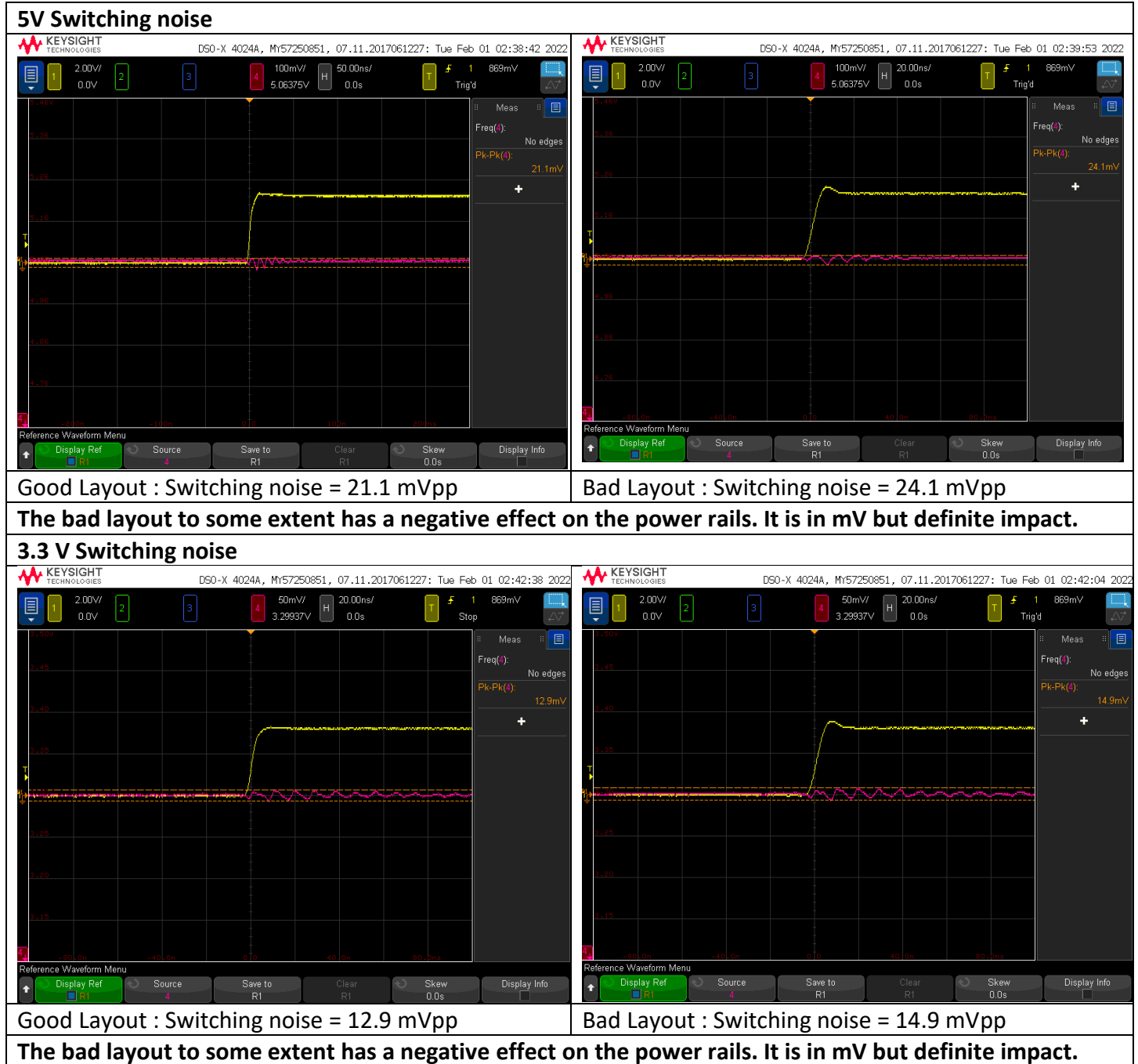
This is used for measurement between quiet output signal-return loop that is not switching and the other signal-return loops that switch and is used to measure ground noise/crosstalk.

These two pins are called quiet HIGH and quiet LOW because nominally, these pins are not switching, and they should have no changing voltage on them. Any voltage we measure must be switching noise.

2) What features on this board contributed to the reduced noise in the good layout section?

In the good layout section, a common ground plane, proximity of decoupling capacitor to the IC's Vcc and usage of a continuous ground plane helped to reduce the noise.

3) Switching noise on the 5 V and 3.3 V rails (zoom in to see any synchronous noise)



4) *Based on what you measured, what do you recommend as best design guidelines in your next design to reduce switching noise?*

***Conclusion/ Learnings:***

1. One should make of a proper continuous common ground plane to minimize the signal return path. This minimizes the current loops that help lower the radiation, while reducing the parasitic inductance in the absence of a continuous path, all the signals would require travelling through a common path which can cause a significant noise in the victim.
2. I should make use of a decoupling capacitor and keep it close to the power supply as much as possible to remove the impact of the inductance to the maximum extent possible. The decoupling capacitor provides a low-impedance path from the power supply to ground to shunt the unwanted RF energy.
3. The capacitor to be chosen should be small in package as this would have a lower parasitic and/or lead inductance.
4. The output of the LED was fluctuating because a pull-up resistor was missing. It is necessary to have a pull-up resistor to tie the input either to high or low and not keep it floating.

***Oscilloscope learnings:***

1. The significance of selecting the signal to be **centered** for comparative analysis using Utility-> preferences
2. The average option from acquire is very useful as it eliminates stray noises and makes the signal cleaner to view.