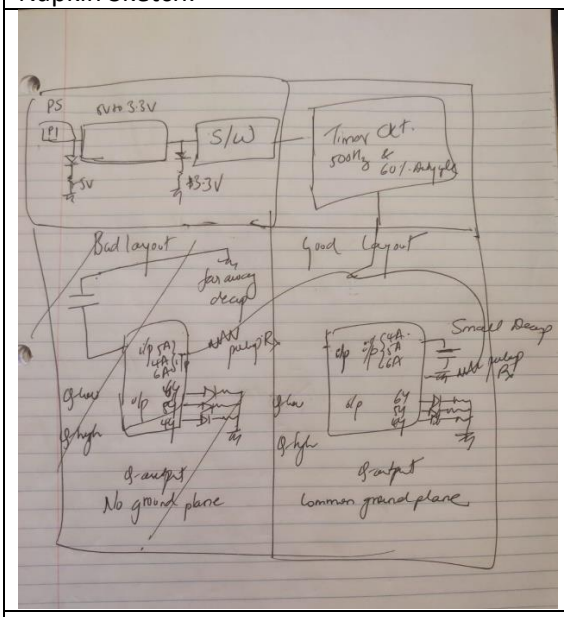
Good Layout Bad Layout Board 1 Report (03/05/2022) Rishab Shah

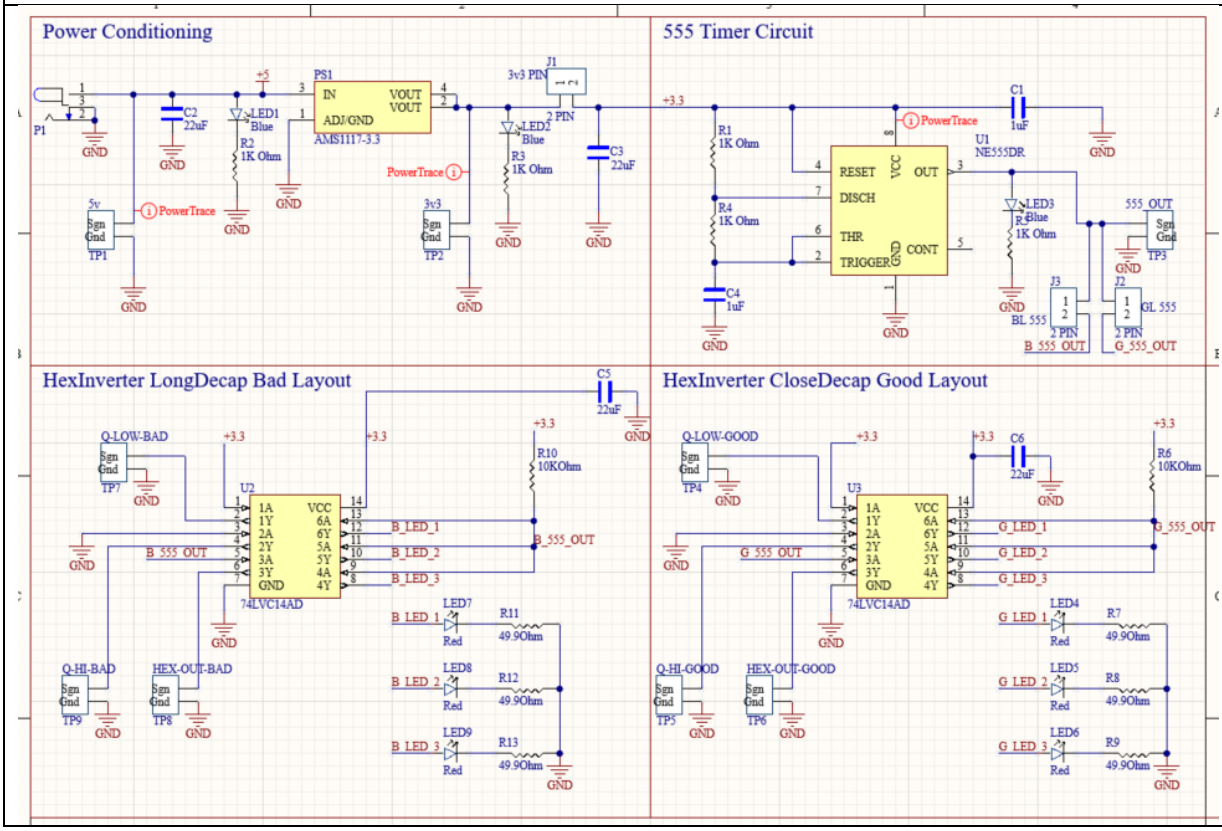
Project Overview/Definition of work:

There will be two designs integrated in one – Good Layout and Bad Layout for Hex-inverter driven by a 555 timer. The good layout would have a decoupling capacitor in proximity and a contiguous ground plane whereas a Bad layout would have decoupling capacitor placed far away as well only one via to the ground plane (no common ground place). Significant parts are AMS1117 (5v to 3.3V regulator), 555 timer IC – Asynchronous mode (input clock source) and Hex-inverter (7414)) to act as buffered system for output and addition of pull-up resistors so that pins do not float. The output of hex-inverter should be a opposite logic level of the input fed with a frequency of about 500 Hz and duty cycle of 60%.

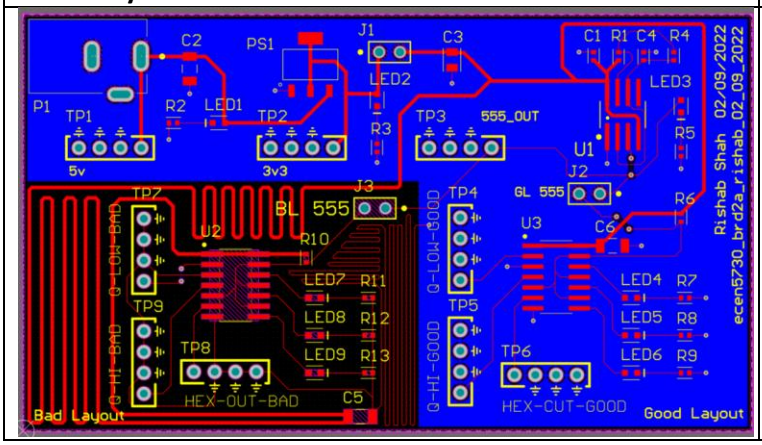
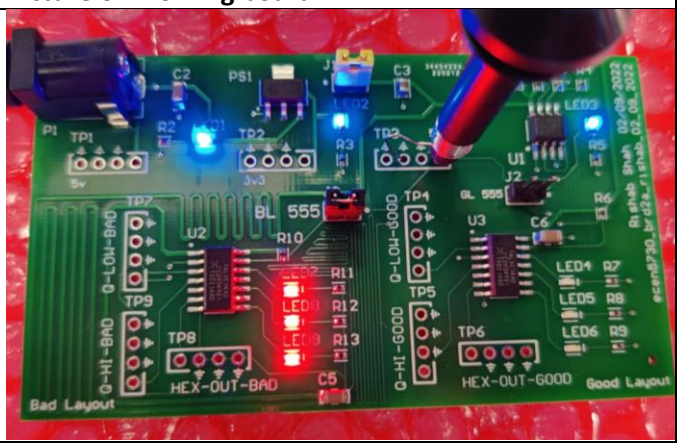
Napkin Sketch:



Schematic

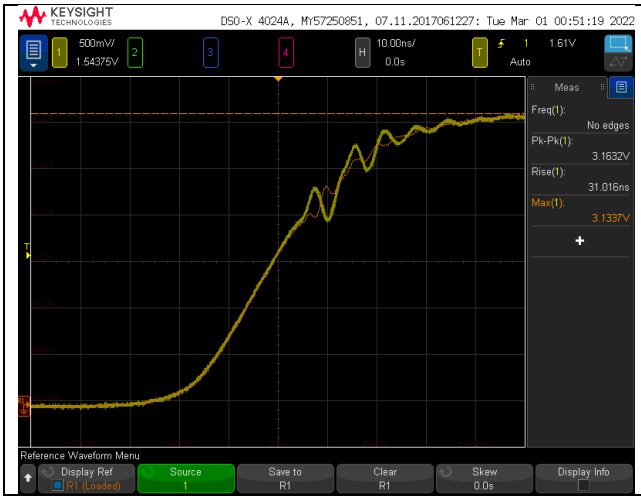


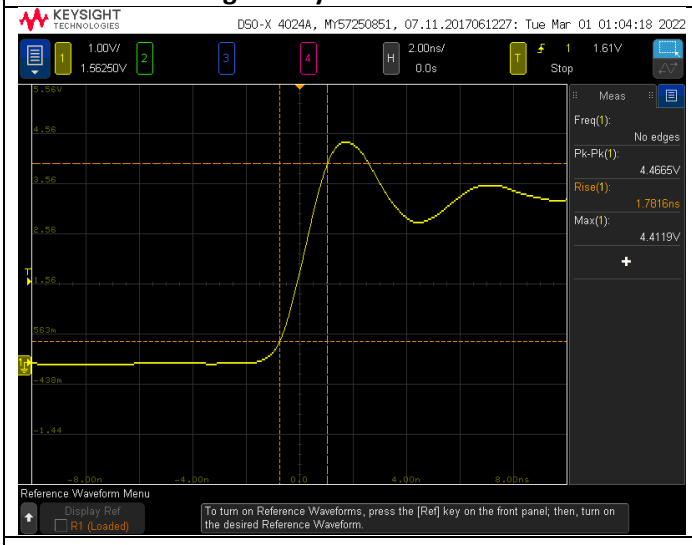
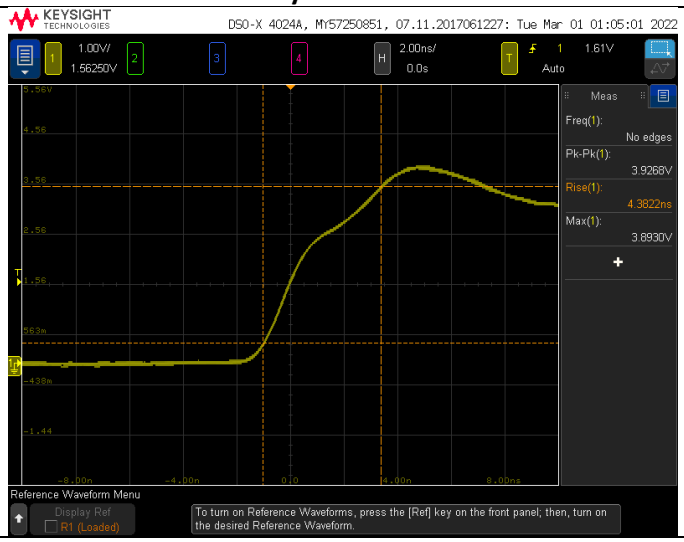
Sketch of schematic:

Board Layout	Picture of Working board
	

Measurements:

a) Impact of load on 555 timer (input source) due to Bad and Good Layout:

	**The orange represents the impact of load on 555 due to good layout whereas to allow represents the impact due to bad layout.**

Rise time due to good layout of 555 timer: 1.78nsec	Rise time due to bad layout of 555 timer: 4.38 nsec
	

Rise time is negatively imapcted due to bad layout

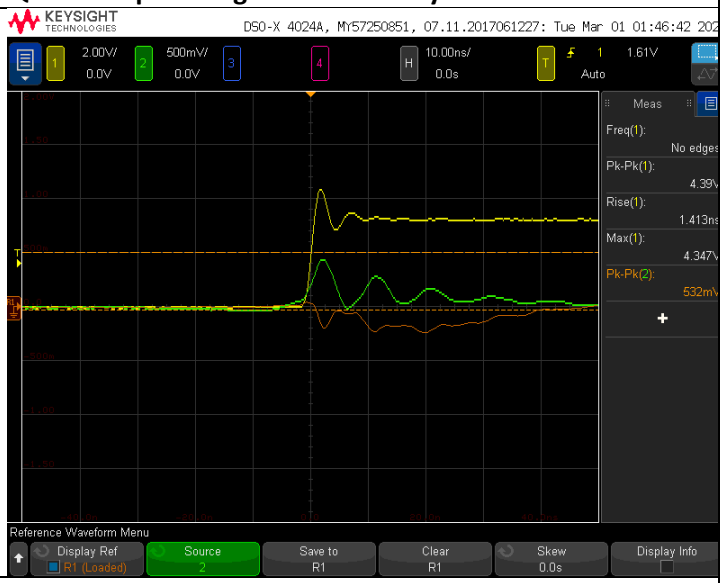
From the images, it is found that a poor layout of Hex inverter negatively affects the rise time of the signal which has a negative impact for high-speed electronics as the rise time is more.

Q-High and Q-Low significance for measurement of ground bounce:

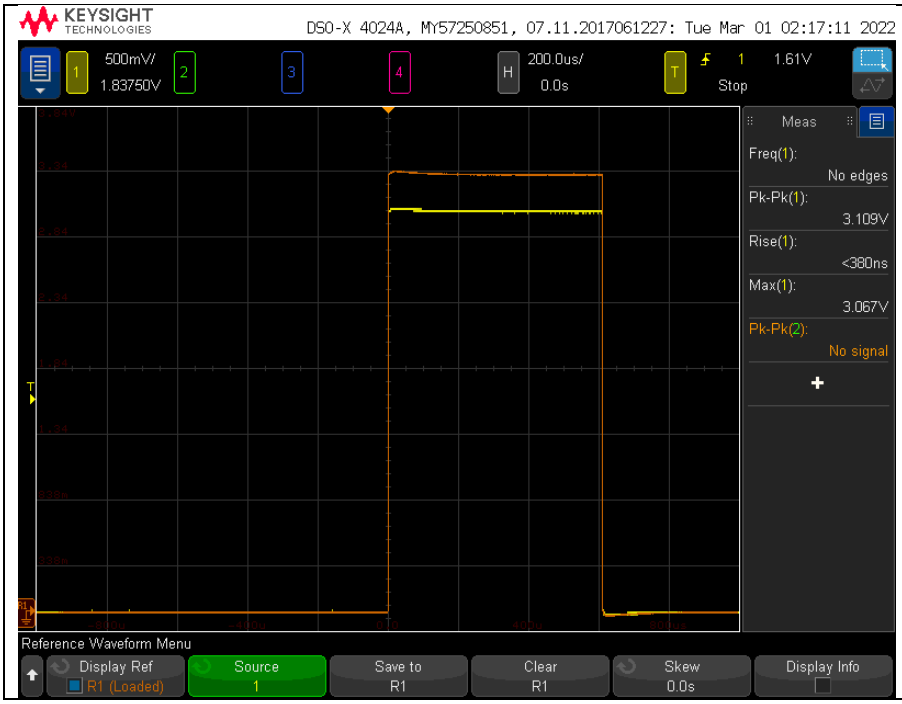
This is used for measurement between quiet output signal-return loop that is not switching and the other signal-return loops that switch and is used to measure ground noise/crosstalk.

These two pins are called quiet HIGH and quiet LOW because nominally, these pins are not switching, and they should have no changing voltage on them. Any voltage we measure must be switching noise.

b) Q outputs on good and bad layouts:

Q-High outputs on good and bad layouts	**Q-Low outputs on good and bad layouts**
	
Yellow = Output of the hex inverter circuit *Orange = Reference s/w noise for GL = 439mVpp* *Green = s/w noise for BL = 1.605V* *The noise contributed due to a Bad layout (BL) is more compared to good layout.* *It is due to the lack of common ground plane causing noise in the victim trace.*	*Yellow = Output of the hex inverter circuit* *Orange = Reference s/w noise for GL = 267mVpp* *Green = s/w noise for BL = 532 mVpp* *The noise contributed due to a Bad layout (BL) is more compared to good layout.* *It is due to the lack of common ground plane causing noise in the victim trace*

C) Thevenin output resistance of the Hex inverter I/O: (Extra-Credit)



Thevenin Output Resistance of the Hex-inverter (good Layout):

Vth = 3.23V

Vl= 3.067

Rl = LED + Resistor= 50 Ohm (approx..)

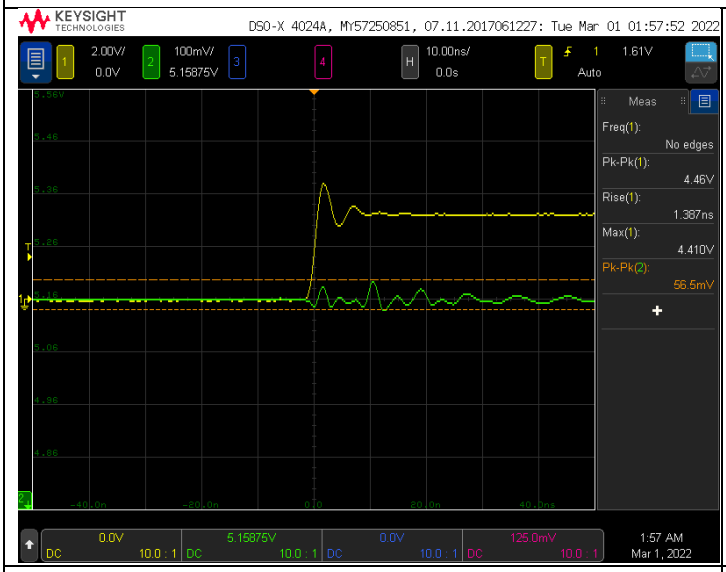
Rth = Rl*(Vth-Vl/Vl)

= 50*(3.23-3.067/3.067)

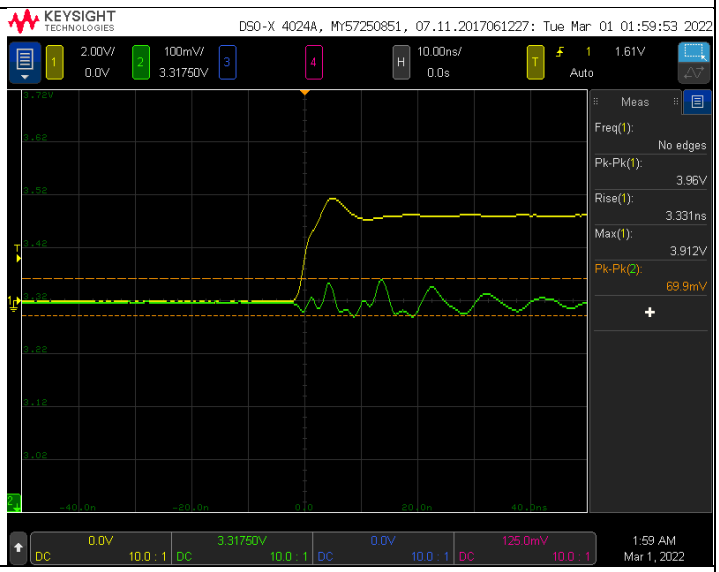
= 2.657 Ohm

d) Switching noise on the 5 V and 3.3 V rails

5V Rail



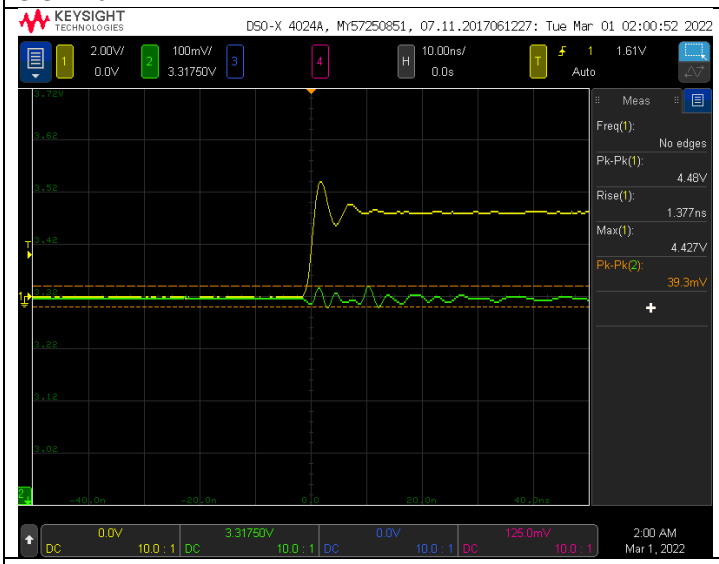
Good Layout: Switching noise = 56.5 mVpp



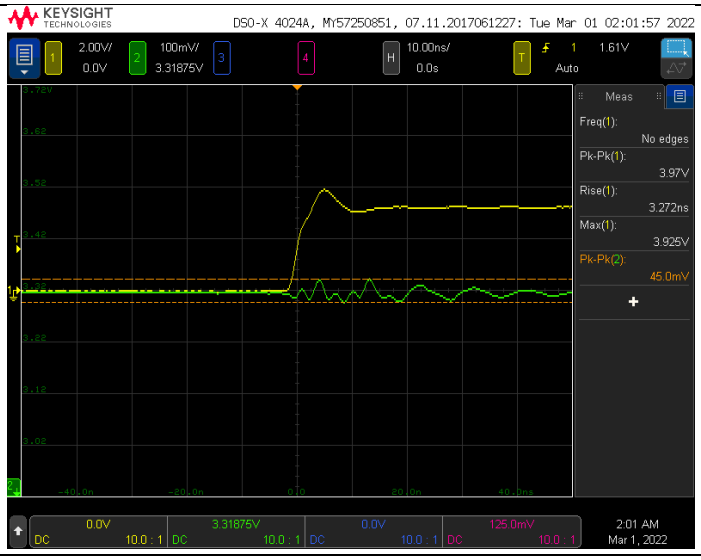
Bad Layout: Switching noise = 69.9 mVpp

The bad layout to some extent has a negative effect on the power rails. It is in mV but definite impact.

3.3V Rail



Good Layout: Switching noise = 39.3 mVpp



Bad Layout: Switching noise = 45 mVpp

The bad layout to some extent has a negative effect on the power rails. It is in mV but definite impact.

The noise on a 3.3 v rail is less compared to a 5v rail comparatively.

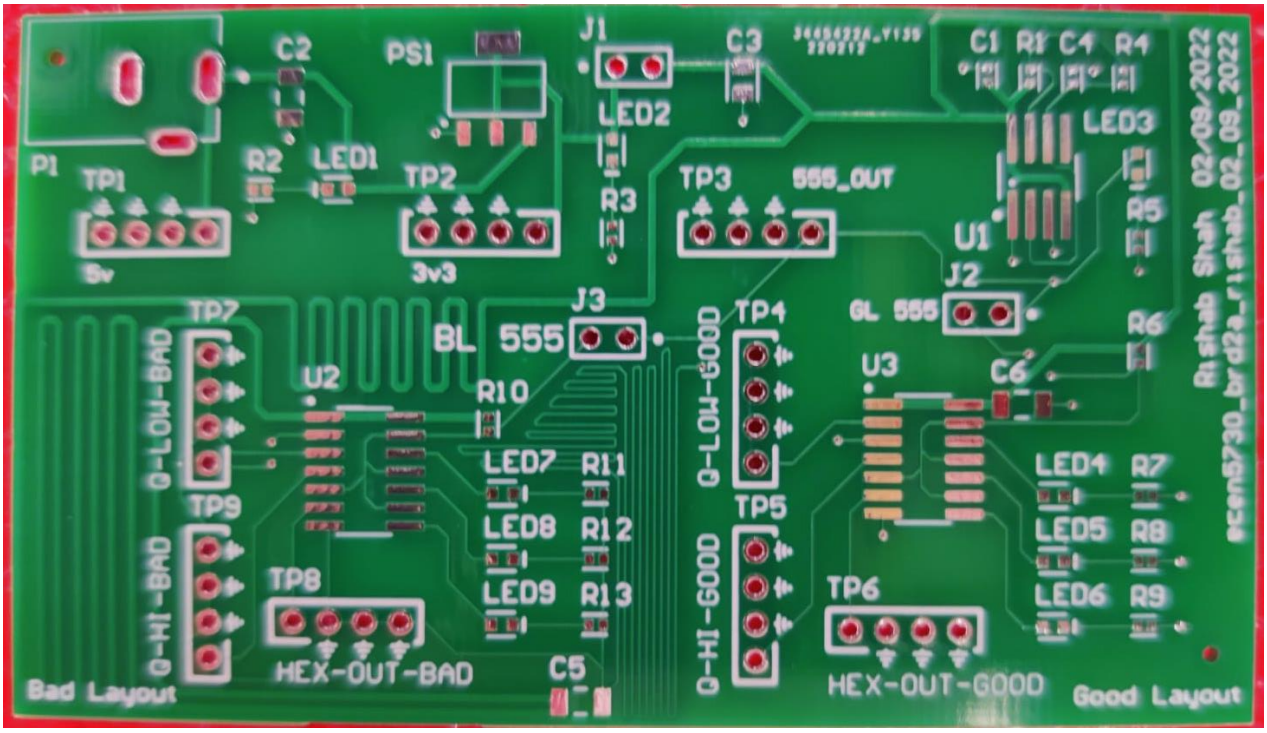
Demonstration of best design practices and best measurement practices:

Spring tips were used for measurement using CRO to reduce the inductance and decoupling capacitor was placed close to the power of the 555 IC.
The significance of selecting the signal to be **centered** for comparative analysis using Utility-> preferences
The average option from acquire is very useful as it eliminates stray noises and makes the signal cleaner to view.

Improvement/Care for next time:

To make use of common ground plane in future layouts as well as placement of the capacitor close to the controller.
Make use of 36mm as height and 6mm as width of stroke for all the silkscreen as they are readable and consume less space.

Picture of Board:



Analysis of your project:

Q. What worked and you did well and want to do in future design

- Labelling every component and division of the blocks beforehand helped to visualize and breakdown tasks.

Q. What did not work, and you will want to do differently in future designs.

- The noise contribution on good layout was more compared to the board which was analyzed in Lab 6.

Q. Were there any hard errors- why did they go wrong

- No hard errors

Q. Were there any soft errors that you would like to do differently next time?

- Continue using common ground plane and