# Design & implementaion of a 1-Bit Full Adder using 28 nm CMOS technology

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***Abstract*—This paper presents the design and implementation of a 1-Bit Full Adder circuit using 28 CMOS technology. All the Simulations are done on Synopsis tool. For the representation of inputs and outputs, we have taken voltage range 0v to 1.8v. The truth table of the 1- Bit Full Adder is verified by the waveform obtained from the simulation. Full adder can be designed using two Half adders but this design is a little modified version with less no of MOSFETs.**

***Keywords— Half Adder, Full Adder, 28nm CMOS, VLSI.***

## REFRENCE CIRCUIT DETAILS

Addition is one of the fundamental arithmetic operations. Adder is the core element of complex arithmetic circuits like addition, multiplication, subtraction, division, exponentiation address calculation and generation in case of cache memory etc. Adders are classified as Half Adder and Full Adder. The Half adder takes two inputs A and B and generates two outputs such as Sum and Carry, no previous carry is taken in account. But in case of a Full Adder, it takes three inputs like A, B and Cin (previous carry), and generated two outputs such as Sum and Carry. Now, here we are focusing on 1-bit full Adder, then in this case inputs and outputs will be of single bit only.

The output expressions for the 1- bit half adder is given by,

$$SUM=A \otimes B \quad (1)$$

$$Cout= AB \quad (2)$$

So we need one XOR gate and one AND gate to implement the Half Adder Circuit.

Also, we know the circuit of Full Adder using Half Adder can be implemented as follows,

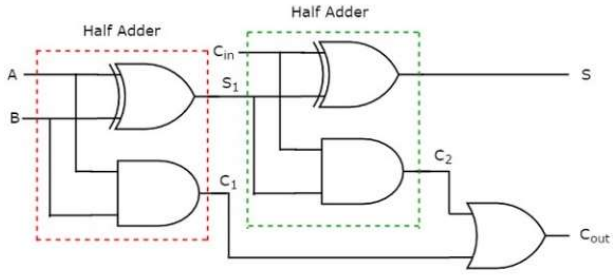


Fig.1 Conventional Circuit of Full Adder using two Half Adders

Input and output relations of 1-bit Full Adder can be seen from its truth table. The output expression for the sum is given by

$$SUM=A \otimes B \otimes C \quad (3)$$

$$Cout= AB + Cin\ (A \otimes B) \quad (4)$$

Here, '⊗', represents XOR operation.

As the basic building blocks of digital are NAND and NOR gates. A little modification can be done in the design in following manner by replacing the "AND-AND-OR" logic with its r=equivalent "NAND-NAND-NAND" logic.

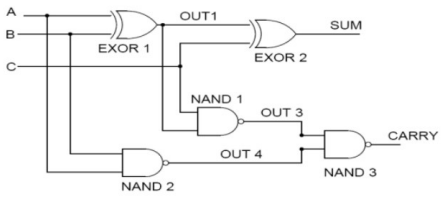


Fig.2 Modified Circuit of 1-Bit Full Adder[2]

## REFRENCE CIRCUIT

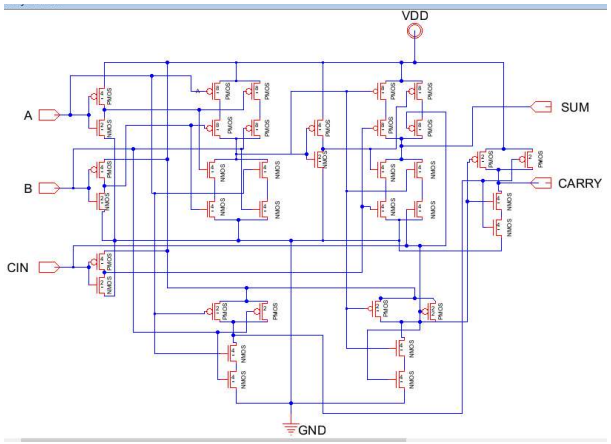


Fig.3 Reference Circuit of 1-Bit Full Adder

## REFRENCE CIRCUIT WAVEFORM

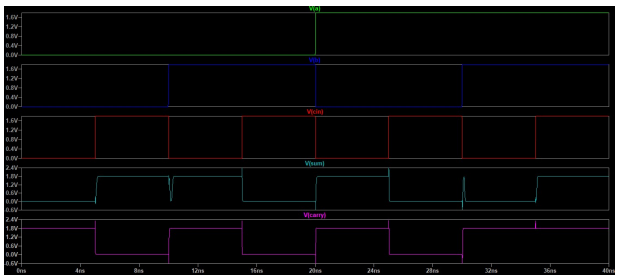

Fig.4 Reference waveform of inputs and outputs of 1-Bit Full Adder

## REFRENCES

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